Future Architectural/Compiler Research Directions

David Bernstein
Bilha Mendelson
Compiler/Optimization activities in IBM Research Lab in Haifa

- Group of 15 researchers with high academic degrees (PhD, MSc)
- 15 years of research and development activities:
  - Instruction scheduling
  - Register allocation
  - Data prefetching
  - Feedback directed optimization
  - Post-link optimization
  - Whole compiler back-ends
- Architectures:
  - PowerPC microprocessor (for IBM Unix WS and Apple Desktops)
  - Experimental signal processors
  - IBM Network processor
- Compilers:
  - IBM (proprietary) XL compiler
  - Experimental “home-grown” compiler back-ends
  - GCC compiler
Architectural Aspects

- SoC family of architectures
- Based on a general purpose core (PowerPC, ARM, etc.)
- Hardware acceleration units
  - Signal processing cores
  - Network processing engines
  - Graphics acceleration units
- Power/Space/Performance/Cost tradeoffs
Performance and Tools Aspects

- Simulation of a parameterized system
- Performance analysis and prediction modeling
- Compiler optimization for specific engines (e.g. SIMD)
- Optimization for new criteria (e.g. power, space)
- Hardware/Software tradeoffs
Backup
Compiler Research Publications

• "MisSPECulation: Partial and Misleading Use of SPEC CPU2000 in Computer Architecture Conferences", D. Citron, ISCA 2003
• "Optimization Opportunities Created by Global Data Reordering", G. Haber, M. Klausner, V. Eisenberg, B. Mendelson, M. Gurevich, CGO'2003
• "Revisiting Instruction Level Reuse", D. Citron, and D. G. Feitelson, WDDD 2002
• "Light Weight Optimization for Reducing Hot Saves and Restores of Callee-Saved Registers", G. Haber, M. Klausner, B. Mendelson and V. Eisenberg, FDDO 2001
• "Reliable Post-link Optimizations Based on Partial Information", G. Haber, E. A. Henis and V. Eisenberg, FDDO 2000
• "FDPR - A post-link optimization tool for large subsystems", E. A. Henis, G. Haber, M. Klausner and A. Warshawsky, FDDP 1999
• "Sharpening Global Static Analysis to Cope with Java", S. Porat, B. Mendelson, and I. Shapira, CASCON 1998
• "Compiler Optimization of C++ Virtual Function Calls", S. Porat, D. Bernstein, Y. Fedorov, J. Rodrigue and E. Yahav, COOTS 1996
• "Adding class assertions to C++", S. Porat and P. Fertig, 1993
• "Performance Evaluation of Instruction Scheduling on the IBM RISC System/6000", D. Bernstein, D. Cohen, Y. Lavon and V. Rainish, Micro 1992
**Post Link Tool:**
FDPR (Feedback Directed Program Restructuring)

- **Properties**
  - Using a global view of the entire program (global view)
  - Operating on the executable file after linkage
- These properties enable FDPR to do:
  - Global Code Reordering
  - Inter Procedure Boundaries Optimizations
  - Static Data Rearrangement
  - Constant Area Rearrangement
- Examples of FDPR additional optimizations:
  - Usage of Branch Tables
  - Usage of TOC load instructions
- The idea is to complement compiler optimization

- **Method**
  - Code instrumentation
  - Profile information gathering
  - Global Code & Data Optimizations
Performance Improvement

FDPR-Pro Improvements on Power4
SPECINT2000 Compiled with Xlc (-O3 -qpdf)

FDPR-Pro Improvements (%)