3D modelling of the performance and variability of high electron mobility transistors for future digital applications

Results in Brief

FinFETs' potential realised

The semiconductor industry is looking for ways to exploit the high electron mobility of III-V materials like InGaAs using silicon (Si) substrates for the next generations of complementary metal-oxide semiconductor (CMOS) technology.

In the design of integrated circuits, there are three types of transistors to choose from: traditional bulk planar field-effect transistors (FETs), fully depleted silicon-on-insulator (FD-SOI) transistors and FinFETs. Only FinFETs offer the possibility to extend CMOS technology to sub-10 nanometre dimensions.
Within the EU-funded project PERSEUS (3D modelling of the performance and variability of high electron mobility transistors for future digital applications), researchers sat down to investigate the scalability of Si and InGaAs FinFETs.

In this multi-gate structure, the semiconductor body is turned on its side to form a 'fin' of material standing perpendicular to the wafer plane. A gate electrode is formed along the fin.

Using state-of-the-art 3D simulation tools, the PERSEUS team investigated the performance of different FinFETs with dimensions selected to meet the targets set in the 2012 International technology roadmap for semiconductors.

For a silicon-on-insulator (SOI) FinFET, scaling down the gate length from 12.8 to 8.1 nanometres increased the on-current by 64 %. For the InGaAs-on-insulator (InGaAs-OI) FinFET, the increase was 44 % when the gate length was scaled down from 14.0 to 10.4 nanometres.

In addition, PERSEUS researchers studied the impact of three different microscopic sources of fluctuations affecting the performance of SOI and InGaAs-OI FinFETs. The presence of random dopants, line-edge roughness and metal-gate function variations was simulated in 300 microscopically different transistors.

The random dopants induced voltage variations in both SOI and InGaAs-OI FinFETs. The line-edge roughness also resulted in voltage variations similar to the random dopant ones. However, the metal gate function variations were the dominant source of disturbances.

Project outcomes on FinFETs are invaluable to academia and industry to meet stringent circuit and system requirements in the future. The findings of the PERSEUS project are expected to provide designers with clues for which is the best choice for future digital applications. The benefit brought to the European semiconductor industry is a lower production cost and improved efficiency for devices with greater resistance to variability.

Keywords

FinFETs, semiconductor industry, complementary metal-oxide semiconductor, field-effect transistors, 3D simulation
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