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MEEP Project: A Flexible System Supporting Next Generation European Open Source Software and Hardware

The European funded project MEEP brings together three European Union (EU) partners: as coordinator, BSC (Spain) will provide software and hardware, UNIZG-FER (Croatia) will contribute with its significant expertise in architecture and building and deploying FPGA-based systems, and TÜBİTAK BILGEM (Turkey) will contribute offering deep expertise in verification, architecture and advanced logic design.



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Launched on 1 January and coordinated by the Barcelona Supercomputing Center (BSC), the European project “MareNostrum Experimental Exascale Platform” (MEEP) supports the goal of the European Union program EuroHPC to create competitive European technology integrated into future exascale supercomputers.

Specifically, it aims to develop an exploratory supercomputing infrastructure for the development, integration, testing and co-design of a wide range of European technologies which could form part of future European exascale systems, based on European-developed intellectual property (IP). The ultimate goal is to create an open full-stack (software and hardware) ecosystem that could form the foundation for many other European systems, both in high-performance computing (HPC) and embedded computing, with benefits for numerous stakeholders within academia and industry.

“The MareNostrum Experimental Exascale Platform (MEEP), as a performance

evaluation and software development vehicle for future chip designs, will provide European technology that will set a foundation for many systems, both in HPC and beyond,” says John Davis, MEEP coordinator at BSC. “By championing the open-source RISC-V instruction set architecture, MEEP will help ensure European technological sovereignty by avoiding the export restrictions associated with proprietary models, while building the software ecosystem necessary to make RISC-V viable for a wider range of applications.”


Using an innovative emulation platform based on field-programmable gate arrays (FPGAs), MEEP will provide a testbed for RISC-V-based infrastructure, as well as building the initial software ecosystem to support this. MEEP’s software development will translate into a proof-of-concept for industrial usage, enabling next-generation exploration of computer architecture as well as software development of existing and future HPC applications, including emerging artificial intelligence workloads, across sectors from pharmaceutical to automotive.

“By experimenting with RISC-V-based hardware designs through FPGA emulation, we can fine-tune the right architectures before committing to silicon,” adds Peter Hsu, MEEP director at BSC. “The emulation platform will also allow us to test the full stack, from applications to hardware.”

The European funded project MEEP will run for three years with a budget of €10.3 million, of which €5.15 million is directly funded by the European Union. In order to reach its goals, MEEP brings together three European Union (EU) partners: as coordinator, BSC (Spain) will provide software and hardware as well as expertise to create infrastructure for European chip developing targeting exascale machines, UNIZG-FER (Croatia) will contribute with its significant expertise in architecture and building and deploying FPGA-based systems, and TÜBİTAK BILGEM (Turkey) will contribute offering deep expertise in verification, architecture and advanced logic design.

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