Catching up with MEEP: Bringing forward the development of tomorrow’s European exascale supercomputing

When the MEEP project ended in mid-2023, it had developed an exploratory supercomputing infrastructure. In 2024, we examine to what extent capabilities have been expanded to ultimately create a state-of-the-art platform for exascale systems based on European technology.

The EU-funded MEEP project introduced a large-scale field programmable gate array (FPGA) system involving a complete collection of hardware intellectual properties (IPs) and software components. These were seamlessly integrated into the FPGA-based system.

“MEEP isn’t just an infrastructure, it’s more than that,” states project coordinator Vanessa Fernandez, senior research project manager at the Barcelona Supercomputing Center (BSC). “It’s about the contributions to the RISC-V ecosystem in many of the layers of the open stack (software and hardware). It’s also about contributing to European chip sovereignty, to society and to economic growth by offering a set of reusable RISC-V-based IPs, tools and infrastructure.”

The RISC-V-based IPs, tools and infrastructure make it possible to improve system design exploration flow by offering a mechanism that quickly and easily evaluates new ideas. They also offer an educational vehicle for people interested in RISC-V in high-performance computing (HPC) but who have no previous experience.
Furthermore, they provide a mechanism to save costs when designing and developing processors, accelerators or other complex systems.

**Two in one: Evaluation platform and software development tool**

From a technical perspective, research activities begun during MEEP continue to evolve under new projects. One noteworthy example is adapting the tools and environments. Specifically, project partners have worked on the stabilisation and maintenance of the Linux kernel, the verification of all the Linux distributions available for the Lagarto cores, and the general services that the operating system offers to the environment and applications.

Another notable example is increasing the set of functionalities and tools for exploiting the platform. This is being done by adding design verification capabilities on an FPGA and by allowing the partitioning of one large design into multiple FPGAs and then connecting those through Aurora.

By organising and participating in events such as the RISC-V Summit Europe 2023 and RISC-V for HPC workshops, MEEP is contributing to the growth of the RISC-V ecosystem, and consequently to the success of the adoption to RISC-V instruction set architecture as a dominant architecture in Europe.

Lastly, project partners are improving the information delivered to end users, including the documentation found on the GitHub repositories, and offering more detailed information about the infrastructure to users.

“Thanks to EU funding, we have an FPGA-based infrastructure for researchers that’s up and running,” concludes Fernandez. “This platform isn’t only the physical infrastructure, but the tools and support surrounding it that make it attractive for use in different activities related to the analysis and evaluation of new hardware and software IPs and ideas.”

**Keywords**

MEEP, exascale, supercomputing, supercomputer, field programmable gate array, FPGA, RISC-V, high-performance computing, hardware, software

**Related projects**