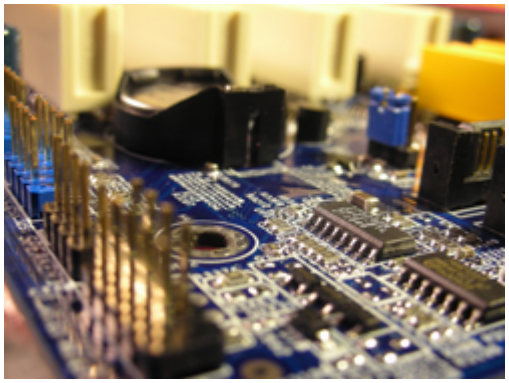
Advanced techniques for high temperature system-on-chip

Results in Brief

High temperature testing of microelectronic circuits

With the continual improvements in semiconductor fabrication technologies, microelectronics circuits can now be integrated into critical systems used within the automotive and avionics industries. To ensure their integrity and reliability, the ATHIS project partners undertook the challenge of testing them under their real operating conditions.

INDUSTRIAL TECHNOLOGIES



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Silicon on insulator (SOI) technology has been widely recognised as a viable choice for the replacement of conventional bulk silicon (Si) substrates in manufacturing complementary metal-oxide semiconductors (CMOSs). Moreover, SOI technology providing dielectric isolation as well as a significant reduction of the leakage current has been established as the preferred choice in designing heterogeneous electronic systems.

The ultimate aim of the ATHIS project was to ensure the reliability of CMOS transistors built on this technology under operating conditions that exclude the use of conventional semiconductor technologies. Project partners at the Université catholique de Louvain in Belgium tested laterally diffused metal-oxide semiconductor (LDMOS) transistors in high temperature environments such as those found in a

modern engine.

To support results of numerical device simulations, a LDMOS transistor structure was fabricated on extremely thin SOI films whose thickness did not exceed 80nm. This is the first qualitative study of the physical phenomena deteriorating the output characteristics of LDMOS transistors in ultra-thin SOI films. In fact, different parasitic effects could be observed at low and high front gate voltages, the kink effect and quasi-saturation respectively.

The results of two-dimensional (2D) numerical simulations performed on Silvaco's ATLAS platform clearly showed that both these effects should be taken into account in order to improve the breakdown voltage. On the basis of available simulation and experimental results, the optimum value for geometrical parameters such as length and doping of the drift region and the field plate length were determined. Additional trade-offs between the characteristics of LDMOS transistors are subject of research in order to further improve their performance.

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ATHIS

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