Extended Large (3-D) Integration TEchnology

Seventh Framework Programme
FP7-ICT-2007-1
Project Number: FP7-ICT-215030

Deliverable 3.6

Final report incl. test and characterization of demonstrator

Version 1

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Project Name	Extended Large (3-D) Integration Technology
Project Number	ELITE-215030
Document Title	Final report incl. test and characterization of demonstrator
Deliverable Number	D3.6
Work Package	WP3
Dissemination Level	Confidential (consortium members and commission)
Lead Beneficiary	CEA-Leti Minatec
Document Editor	Jean-Charles Souriau
Delivery Date	July 2011
Version	1

Abstract

The final objective of the ELITE project was to answer major technological issues and enable the fabrication of a 3-D circuit with multiple chips levels including multiple memory chips and a control logic chip inside the same package. However, the ELITE project has encountered some unexpected technical challenges that have lead to cancel the delivery of demonstrator. The consortium wished nevertheless to deliver technology demonstrators and have continued their efforts on test vehicle. This deliverable is mainly focused on 3-D integration technology which allows an indefinitely repeatable chip to chip interconnection 3D module. The electrical tests and the characterization of the test vehicle achieved in the project are presented and commented.

Keywords

3D Stacking, chip on wafer, copper pillar technology

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1. Introduction

The key challenge in the ELITE Project was to minimise the additional area required by the intra-silicon connections. On the other hand, the feasibility of etch and fill of these vias give a limitation on the aspect ratio of the holes, hence a minimum wafer thinning. The final silicon thickness chosen for Elite is in the range of 50µm. Since the handling of thinner wafers is very problematic below 100µm, the use of an additional substrate (named here a handle) bonded on top of the wafer is mandatory. To allow thin die pick and place, the wafer is sawed with handle and this one is removed after the hybridation process. Regarding the dies interconnection the solution chosen in the ELITE project was based on copper pillars.
The process for multi-level stacking was developed on test vehicle and electrical testing were performed in order to characterize in detail the parameters of the through chip connections.

2. Test vehicle description

Dies size is 6.2x11mm² and silicon interconnection network is 8.2x13mm². The test vehicle is designed in order to give the possibility to stack as many bottom die as wanted between the top die and the silicon substrate. The electrical continuity through the stacking could be tested from the substrate thanks to "Kelvin" or "Daisy Chain" patterns.

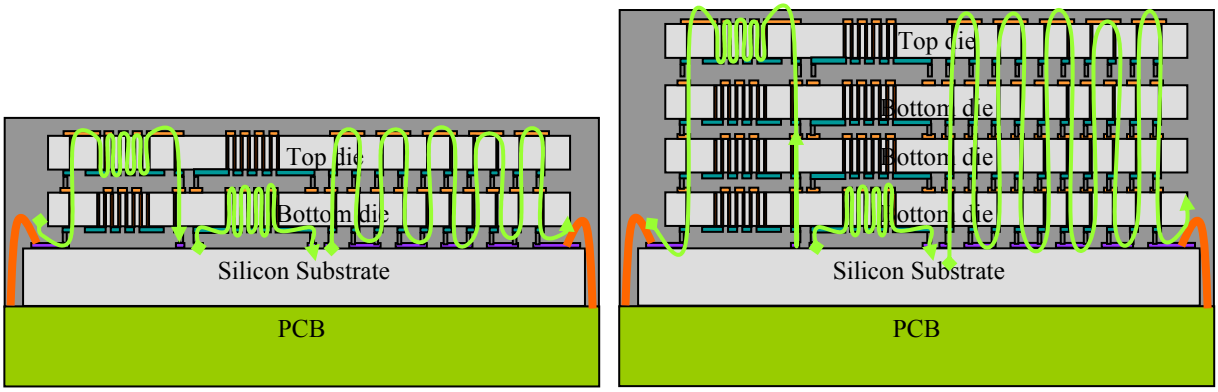


Fig. 1: Daisy chain electrical continuity through the stacking dies

The test vehicle consists of both dense and isolated die, simultaneously printed on silicon, to permit direct comparisons between different patterns. Dense layout is aimed to study a wide range of electrical structures covering the whole die area, while isolated layout was drawn with vias only at die periphery, in order to simulate a possible pad configuration of memory devices and to validate the stacking technology with reliability tests.

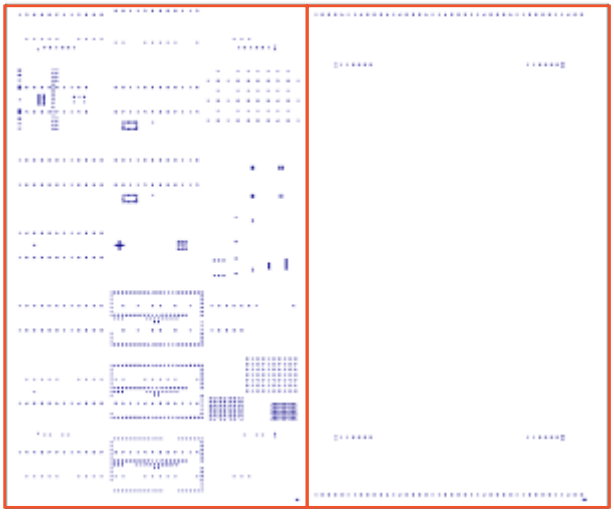


Fig. 2: Frame 1x2 dice: TSV level with dense pattern on the left and isolated pattern on the right.

The test vehicle includes in dense die "Kelvin" and "Daisy Chain" patterns that could be used after stacking to validate interconnection from each die to the substrate.

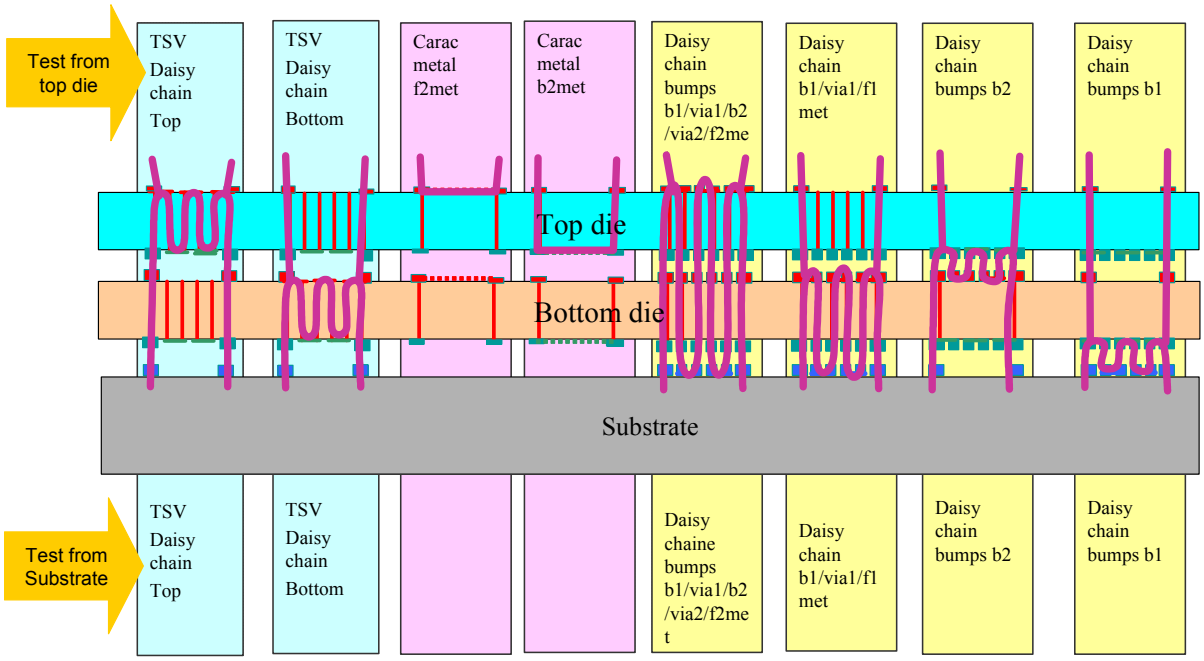


Fig. 3: Test after Stacking

To facilitate the electrical test, die has been divided in 21 identical size blocks. The associated test of each block is summarized in the table 1.

N°	**Name block**	**Test side** **Front side** **Back side** **Substrat**	**Type of test**			
1	CBsac f2met	Fs + Bs	kelvin TSV-f2met	Deltacote f2met	Vanderpaw f2met	Serpentin f2met

2	CBsac f1pad	Fs + Bs	kelvin f2met-f1pad	Deltacote f1pad	Vanderpaw f1pad	Serpentin f1pad
3	CBsac b1met	Fs + Bs	kelvin TSV-b1met	Deltacote b1met	Vanderpaw b1met	Serpentin b1met
4	CBsac b1pad	Fs + Bs	kelvin b2met-b1pad	Deltacote b1pad	Vanderpaw b1pad	Serpentin b1pad
5	Vias chain top CHVTOP	Fs+Bs +Sub	2 vias	n vias		
6	Vias chain bottomCHVBOT	Fs+ Bs +Sub	2 vias	n vias		
7	Bumps chain b1CHBU1	Sub+Fs	Bumps chain	kelvin		
8	Bumps chain b2CHBU2	Sub+Fs	Bumps chain	kelvin		
9	Chain of b1+via1+f1metCHBVF	Sub+Fs	Bumps chain	kelvin		
10	Chain of b1+via1+f1+TSV ds bump CHBVFB	Sub+Fs	Bumps chain	kelvin		
11	Chain of b1+via1+b2 +via2+f2met	Sub+Fs	Al + bumps	Al + bumps	Chaine de bumps	kelvin
12	Breakdown voltage CLAQ	Fs+Bs	1 bumps	Sans bumps Sauf 1		
13	Capas de chaines CACH		Without bumps	Sans bumps		
14	Capas max CBSEF	Fs+Bs				
15	Capas rob FsCAFS	Fs+Bs				
16	Capas rob BsCABS	Fs+Bs				
17	Tips +croixPOCR					
18	Tests RF	Bs				
19	Tests RF	Bs				
20	Tests F	Fs				
21	Tests R	Fs				

Table1.

The layout including the 21 tests blocks is presented in the figure 4 and 5.

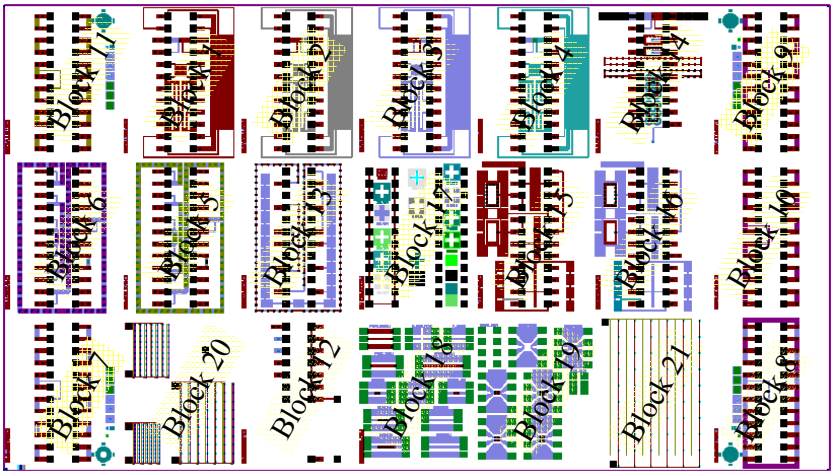


Fig. 4: Layout on dies

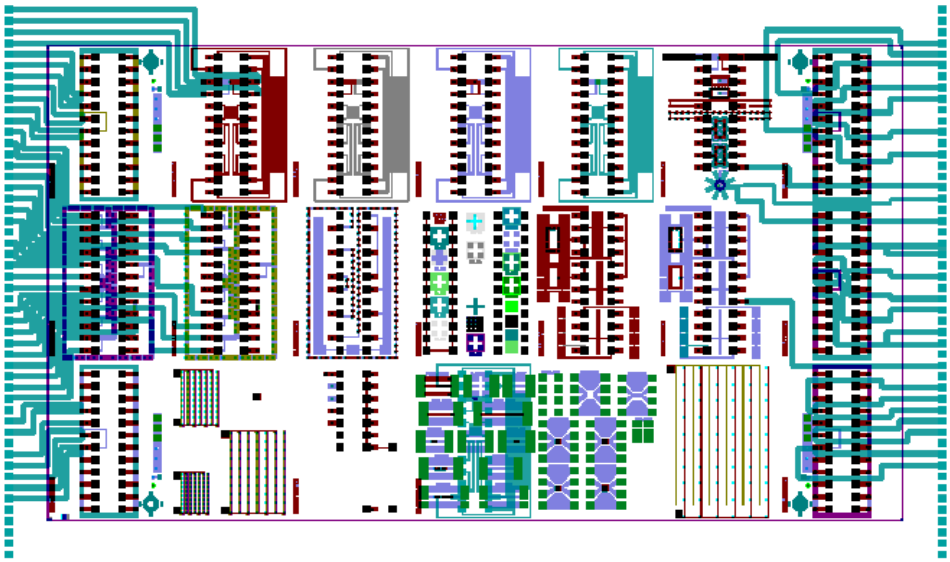


Fig. 5: Layout on die and substrate

For the isolated die, electrical rerouting from the top die to the substrate can be checked only through "daisy chain" patterns.

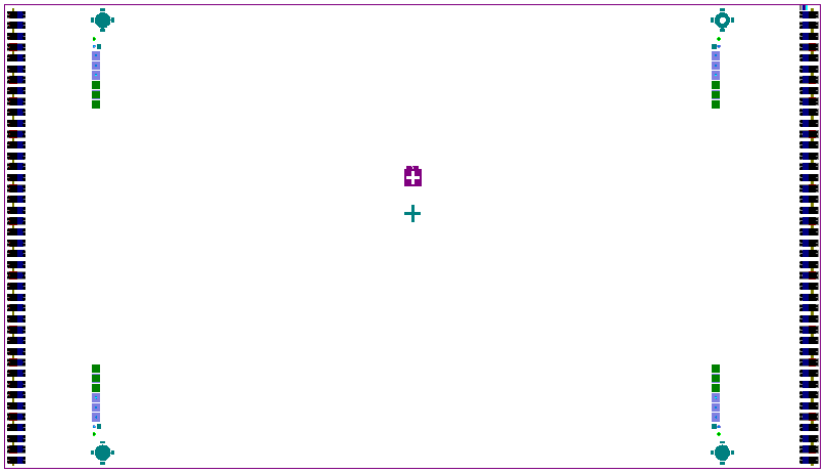


Fig. 6: Layout on dies

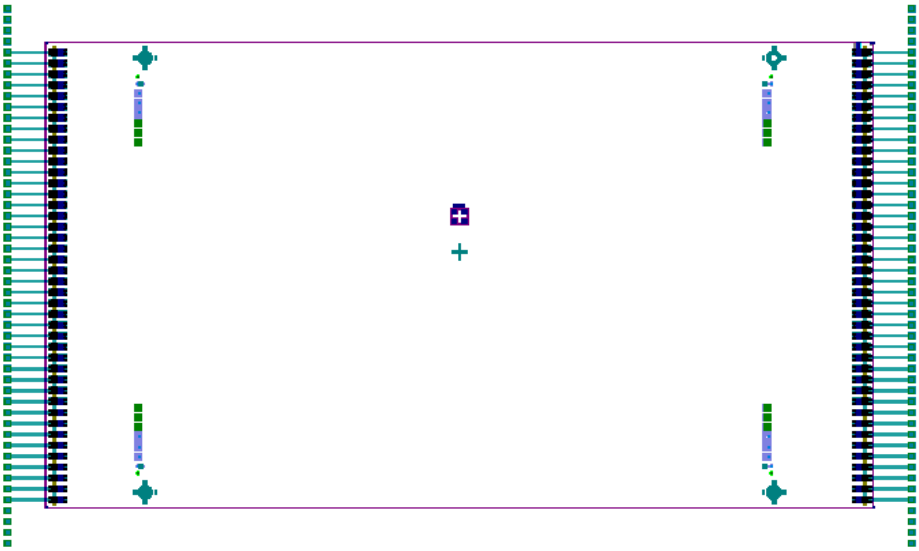


Fig. 7: Layout on die and substrate

3. Stacking technology

For 3D interconnections, the solution chosen in the ELITE project was based on pillars, formed by a copper post on the bottom wafer (only Cu) and a copper pillar (Cu and lead free alloy) on the top die. This technology has been developed at CEA-LETI few years ago and the process was implemented on ELITE test vehicle wafer.

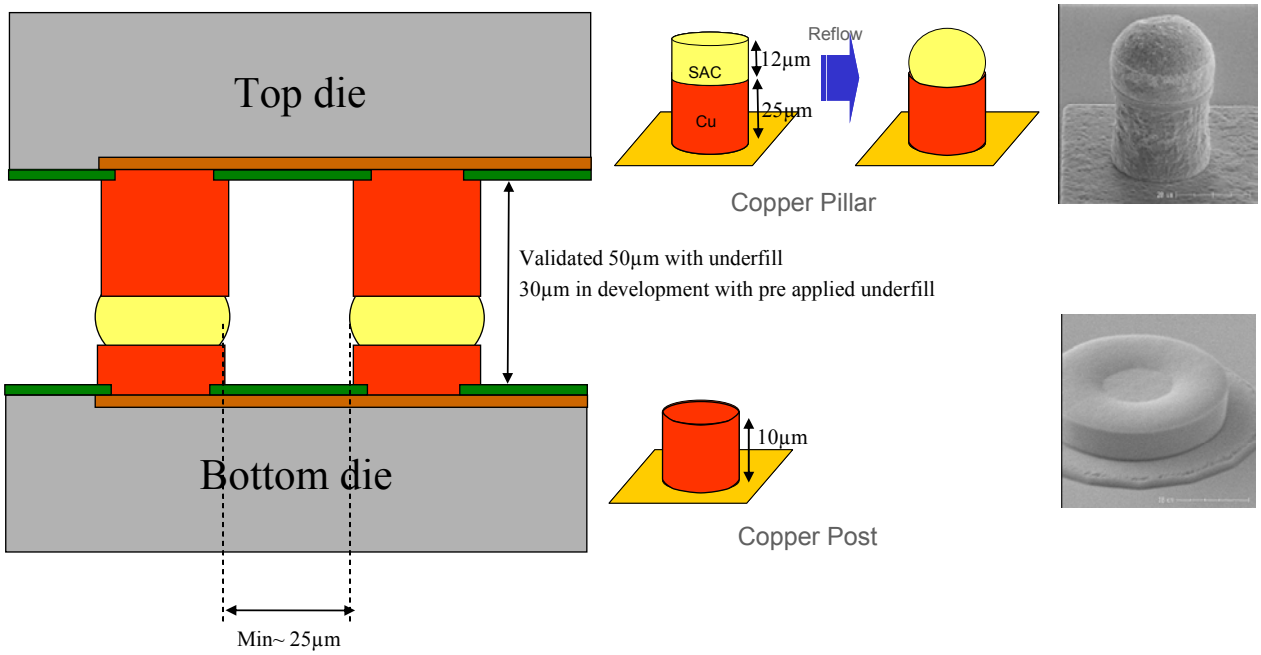


Fig. 8: Copper pillar interconnection

Due to the specific design of ELITE device (low copper-pillar count) the bath chemistry was not adapted and electroplating process was not performed in the best conditions. More investigations to reach adequate yield are needed. However some nice copper pillars have been obtained and pictures are presented below.

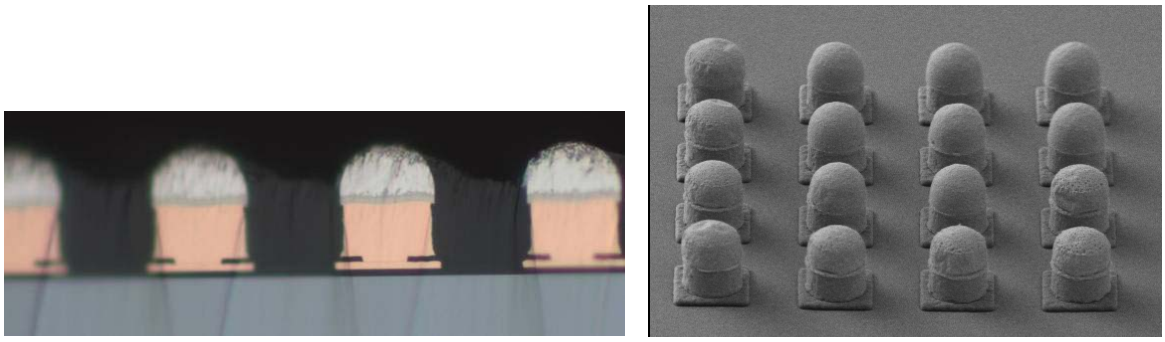


Fig. 9: Pictures of Copper pillar (Cu and reflowed lead-free) on the top chip

In the ELITE project it has been ruled out the possibility to slide off 60 µm thick wafer because of its fragility. The strategy proposed is to release handle after dicing and stacking by chemical etching.

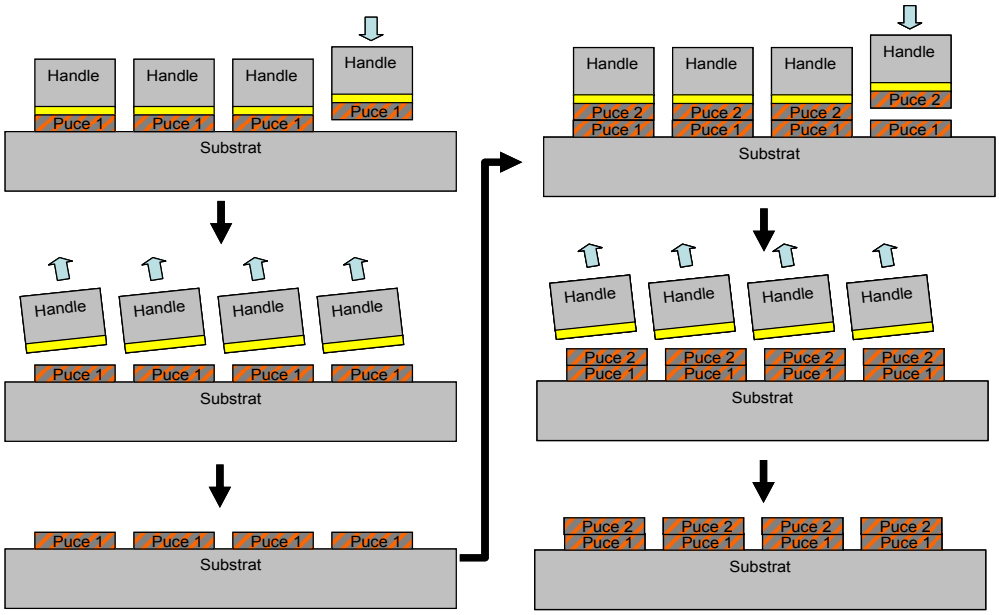
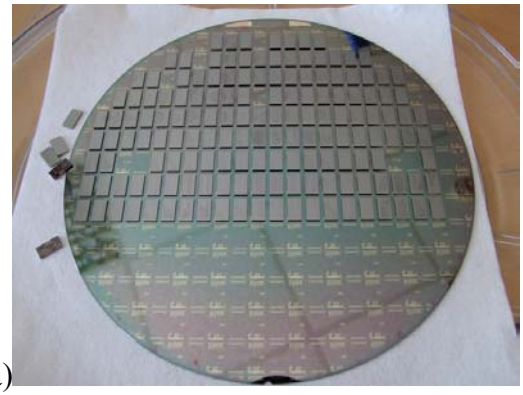


Fig. 10: Strategy proposed in ELITE

Two wafers with bottom and top dies were fully treated with copper pillar.

Both top and bottom dice (44 and 43 respectively) were stacked on a portion of the substrate wafer and a collective chemical process using the HT1010 solvent "WaferBOND Remover" was used to remove the silicon handle. Results are presented following figures.

a) 

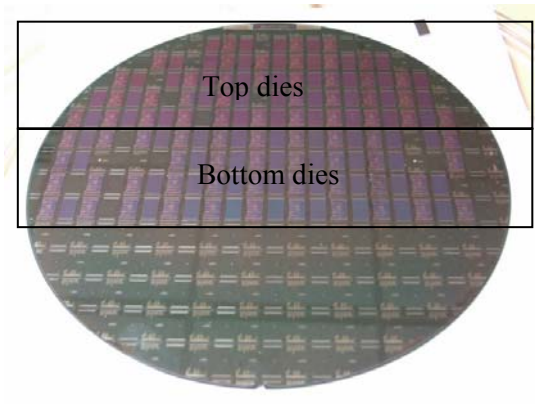
b) 

Fig. 11: Wafer substrate a) after the first stacking and b) after handle removing

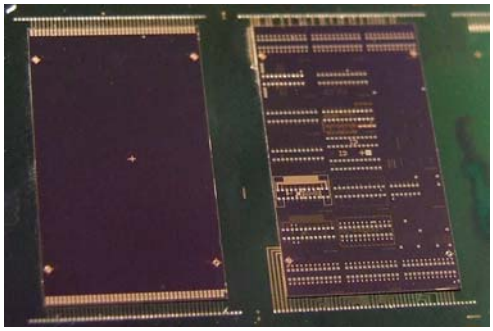
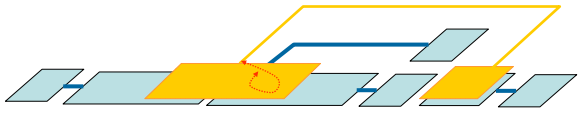
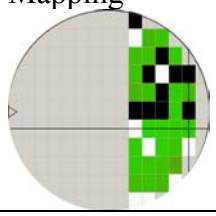
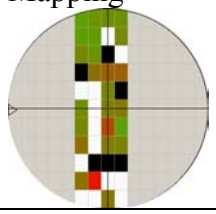
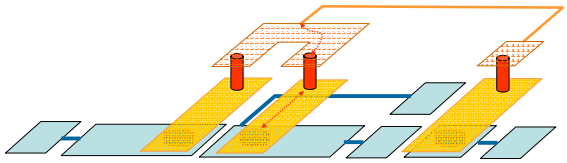
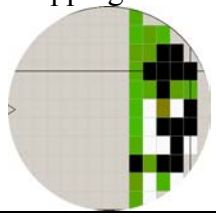


Fig. 12: Test vehicle (dense die and isolated) after staking and handle removing

Kelvin measurements

Several electrical Kelvin structures were measured from the substrate to estimate the contact resistance through copper pillar bump and TSV and results are summarized in the following table 2.

Resistance of bump + RDL 	**Top die** Yield: 58% Ravg= 31mΩ σ=4mΩ	Mapping 
	Bottom die Yield: 57% Ravg= 30mΩ σ=5mΩ	Mapping 
Resistance of bump + RDL +TSV 	**Top die** Yield: 49% Ravg= 0.22Ω σ=0.03Ω	Mapping 
	Bottom die Yield: 54%	Mapping

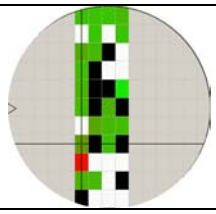
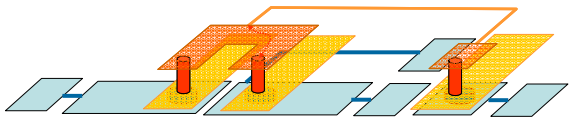
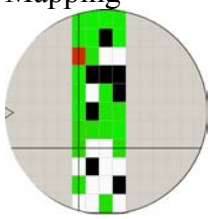
	Ravg= 0.21Ω σ=0.02Ω	
Resistance of bump + RDL +TSV (TSV self aligned to Cu pillar) 	**Bottom die** Yield: 62% Ravg= 0.12Ω σ=0.02Ω	Mapping 

Table 2.

Whatever the type of die (top or bottom) the contact output through copper pillar bump and TSV is between 50 to 60%. This result is very encouraging for a first stacking. Taking into account the results on resistance of (bump + RDL) and knowing the characteristics of RDL in front side and back side it was possible to estimate the copper pillar resistance around 9mΩ. This value was considered to calculate resistance of all test structures and to allow verifying the coherence with measurements.

	R calculated Ω	R measured Ω
Resistance of bump + RDL +TSV	0.193	0.21 ± 0.03
Resistance of bump + RDL +TSV (with TSV self aligned to Cu pillar)	0.108	0.12 ± 0.02

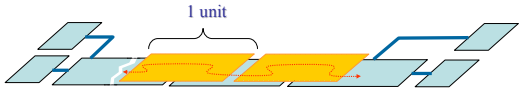
Table 3.

The average measured values are in good agreement with the calculations.

An important result is that there is no negative effect to build the copper pillar directly aligned to the TSV. So, it may be investigated the possibility to omit the step of back side RDL.

Daisy chain characterization

According to the low stacking yield observed on the Kelvin structures, daisy chain made of 22 copper pillars proved to be very defective. Nevertheless, some functional structures have shown good results, in agreement with calculation.

	R calculated Ω	R measured Ω
Daisy chain of (Bump +RDL) 	2.489	2.8 ± 0.1

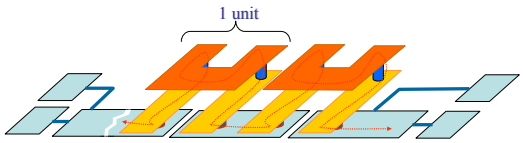
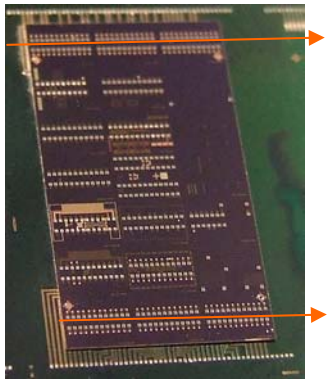
Daisy chain of (Bump +TSV +RDL) 	6.740	6.9 ± 0.1

Table 4.

To understand the low yield, profile measurements were performed on several chips stacked and it was found that they were warped (see figure 9).



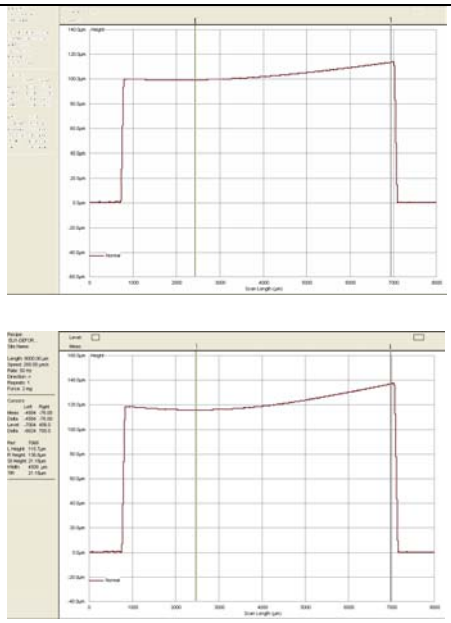


Table 5.

This warpage could be attributed to some residual stress inside the die and its flexibility due to thin thickness. More investigations are necessary to understand this phenomenon. However, several directions were identified to improve the yield:

- To perform underfilling before to remove the handle
  It was planned in the ELITE project to evaluate Wafer Level UnderFill (WLUF). Wafer-Level Underfilling is an emerging technology that consists of pre-applying the underfill material on wafer during the wafer fabrication process. WLUF is very attractive technology and is on development in major 3D research labs. Several material suppliers have been identified and tested by the CEA-LETI. But none of them could be used in the project on time. As a consequence, reliability tests after packaging were not possible.
- To increase the number of bump by using dummies
  Bumps redundancy should improved die adhesion on substrate and moreover facilitate conventional underfill.
- To optimize copper pillar bath chemistry taking into account design of ELITE.

Despite issues described in this section a tentative of multi-stacking was carry out and a photo is presented in the following figure. T*his work is in progress. The results will be presented during the finale meeting and add to the final version*

Fig. 13:

4. Conclusion

In the frame of this work, technological elementary bricks for 3D integration have been developed such as thin die handling and stacking on wafer interconnections based on Cu pillars technology. Solving the technical hurdles and focusing on the test vehicles have impacted the realization of the final packaging, not achieved. Nevertheless, the electrical results obtained on the test vehicle are positive and very encouraging

The feasibility of 3D integration technologies has been demonstrated thanks to this project and pathways for improvement were identified.