Extended Large (3-D) Integration TEchnology

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D2.2: 3-D IC Analysis

Version 1.04
**Extended Large (3-D) Integration Technology**

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Abstract

This document describes compact models for the electrical representation of through-silicon-vias (TSV) to be used in delay, signal and power integrity, and power and energy dissipation calculations. The parasitic parameters in the equivalent electrical circuit are predicated on physical details such as dimensions of the individual via structures, their relative positioning and material constants. This report proposes novel closed-form equations for TSV parasitics in terms of physical dimensions and material properties using a general methodology based on dimensional analysis. The proposed equations are compared with field solver derived parasitic values to check for variations in relevant metrics such as delay and coupled noise amplitude, in order to investigate their suitability for pre-fabrication analysis of signal propagation through TSVs in a 3-D stack. It is shown that these equations allow electrical modelling of TSV bundles within an error margin that is less than the errors in the parasitics themselves. Recommendations are also made with respect to the electrical model to be used for TSVs in a stand-alone structure and in a bundle. The relative importance of the parasitic capacitive and inductive coupling terms as well as the nature of their variation with changing dimensions is discussed.

Keywords

3-D Integration, Through-Silicon Via (TSV), Parasitic parameter extraction, Flash memory, Integrated Circuit (IC) design.

NB:

This deliverable was due according to the initial project plan in Month 15, and hence reflects the technology initially envisaged in the project with QFL as a partner.

With the reorganisation of the project, the technology shifted to encompass different TSV dimensions and materials such as TSV shape, cross-sectional dimensions, height, barrier materials and thicknesses, and substrate properties.

Due to the structured way in which the work was carried out and the generality of the topology considered in order to aid design space explorations, all of the work carried out thus far remains relevant. The dimension and material property space that has become relevant due to the technology shift with Numonyx replacing QFL as a partner is being researched since the redefinition of the technology in Month 24.

The updated models for a wider range of dimensions and electrical properties will be reported in a new internal report to be distributed among the partners as well as in the final Modelling and Simulation Conclusion Report, D2.5 due in Month 28 + 6.

The specific range of dimensions and parameters to be included in the models due to the technology shift are discussed on pg 7 of this document.
# Table of Contents

1. **INTRODUCTION** ........................................................................................................................................... 5

2. **ELECTRICAL MODELLING OF TSVS** ........................................................................................................ 6
   2.1. TSV SPECIFICATION ................................................................................................................................. 6
   2.2. COMPACT MODELLING OF TSV PARASITIC PARAMETERS ................................................................. 8
      2.2.A Related Work ......................................................................................................................................... 8
      2.2.B Isolated TSV ........................................................................................................................................ 8
          Resistance .............................................................................................................................................. 8
          Capacitance .......................................................................................................................................... 9
          Inductance .......................................................................................................................................... 10
      2.2.C RLC Extraction of a TSV Bundle ......................................................................................................... 11
          Capacitance .......................................................................................................................................... 11
          Inductance .......................................................................................................................................... 14
      2.2.D Fidelity of Electrical Models ............................................................................................................. 17

3. **DELAY AND SIGNAL INTEGRITY ANALYSIS** ............................................................................................ 18
   3.1. EQUIVALENT CIRCUIT STRUCTURES .................................................................................................... 18
      3.1.A Simulation Setup .................................................................................................................................. 19
      3.1.B Isolated TSV ...................................................................................................................................... 19
      3.1.C Coupled TSVs .................................................................................................................................... 21
          Inductive Contribution ............................................................................................................................ 22
          Capacitive Contribution .......................................................................................................................... 22
      3.1.D Distributed vs. Lumped Modelling .................................................................................................... 23
   3.2. SIGNAL INTEGRITY (SI) SIMULATIONS IN TSV STRUCTURES ............................................................. 24
      3.2.A Cascaded Effects of Isolated TSVs ..................................................................................................... 25
      3.2.B Crosstalk in a 3×3 Bundle of TSVs ..................................................................................................... 26
      3.2.C Delay Contribution for Various Switching Events .............................................................................. 28
      3.2.D Cascaded 3×3 TSV Bundle ................................................................................................................ 31
      3.2.E Eye Diagrams for Signal Integrity in a 3×3 Bundle .......................................................................... 31
      3.2.F Incorporation of IBIS model of DRAM Driver .................................................................................... 34

4. **DISSEMINATION** ........................................................................................................................................ 35

5. **ON-GOING WORK** .................................................................................................................................... 35

6. **CONCLUSIONS** ......................................................................................................................................... 35

7. **REFERENCES** .......................................................................................................................................... 36
1. Introduction

A major goal in WP2 is the construction of compact models for performance, signal integrity (SI), power integrity (PI), power and energy consumption, thermal stress, and cost analysis of 3-D ICs. The first step in building models for latency, SI, PI and power and energy consumption is the development of electrical models for the through-silicon vias (TSV). These electrical models are predicated on physical level details such as geometries of interconnect and via structures and material constants. Mirroring well established practice in conventional IC design, this report proposes equivalent circuits for the TSVs, as well compact models for the parasitic elements in the equivalent circuits. Preliminary versions of separate parts of this report were circulated within the consortium as internal reports for alignment of work with CEA-LETI and KTH [1],[2].

The extraction of electrical parameters of structures is usually carried out by using a field solver which uses numerical techniques to solve Maxwell’s Equations. However, the use of field solvers for parasitic extraction restricts design space exploration due to the length of time required for simulation. Examination of different physical architectures for various performance metrics requires efficient models that trade-off accuracy for computational complexity, where the inaccuracy in the parameter calculation does not result in a significant enough error in the relevant performance metric to warrant the extra time spent in simulating with a field-solver (See Figure 1).

The electrical modelling of TSVs is not well documented in the literature. Therefore, this report firstly outlines a methodology for generating appropriate electrical level models for TSV structures, based on field solver simulations and analytical insight. These models enable the behaviour of different topologies to be investigated and optimized as planned in WP1, as well as provide initial approximations for design tasks of the demonstrator to be constructed within ELITE. Secondly, the derived models have been used in circuit simulations to estimate delay and SI analysis within a TSV bundle, as would typically be used in a 3-D IC. Based on these simulations, reduced order models for the TSV to be used in delay and signal integrity are also proposed. Shown in Figure 2 is the analysis methodology and flow of tasks from TSV specifications to parasitic extraction to delay and SI analysis.

Figure 1: Tradeoff between accuracy and speed in parasitic extraction.

Figure 2: Signal integrity simulation flow for stacked chips.
The rest of this document is organised as follows. Section 3 deals with the electrical modelling of the TSVs as relevant for the ELITE project, the compact modelling methodology, and the resulting closed-form equations. The delay and SI analysis of vertical bus structure is thoroughly discussed in Section 4. Finally, we draw our conclusions and outline future work to be presented in deliverables D2.3, D2.4, and D2.5.

2. Electrical Modelling of TSVs

TSV electrical parameters consist of resistive \( R \), inductive \( L \), conductive \( G \), and capacitive \( C \) terms including self and mutual (i.e. coupling) terms when nearby structures are present. An equivalent electrical model for two TSVs including self and mutual components is shown in Figure 3 (a). However, in a 3-D chip stack the likely configuration for TSVs is in a regular matrix, for which a representative unit is a 3×3 bundle (see Figure 3(b)). Within such a bundle, the capacitive and inductive terms include self terms to ground and mutual terms to surrounding structures. In this section, the methodology for deriving closed form equations for the relevant parasitic terms is discussed.

A 3×3 bundle structure has been simulated in Ansoft Q3D, a commercial 3-D/2-D quasi-static electromagnetic field solver specifically used for parasitic extraction of electronic components [3]. This tool utilizes the Finite Element Method (FEM) and the Method of Moments (MoM) to solve Maxwell’s equations and estimate RLGC parameters of a structure. These extracted values are functions of the structure’s geometry and the material constants. These variables have been combined into dimensionless quantities according to the principles of dimensional analysis [4][5] in order to reduce the number of independent variables where possible, and joined in functional forms suggested by insight into field theory and empirical validation.

![Figure 3: (a) Equivalent electrical circuit model for two TSVs and (b) coupling terms in a TSV bundle.](image)

2.1. TSV Specification

The general structure of a TSV and its specifications as relevant for ELITE are discussed in this section. TSVs are assumed to have a uniform circular cross-section. The material used for TSVs is copper (Cu), with an annular dielectric barrier (Silicon dioxide SiO\(_2\) or Silicon Nitride Si\(_3\)N\(_4\)) surrounding the Cu cylinder. Further, a thin annular Titanium Nitride (TiN) layer is usually deposited between the Cu and SiO\(_2\) layers, which acts as an adhesion layer [6]. Also, the high resistivity in the TiN region concentrates the current in the copper bar. This TiN barrier layer has been neglected for the sake of simplicity and to reduce computational time in the field solver, since its inclusion has an apparently negligible effect on the parasitic parameters. Further, the TSV structure and silicon substrate is assumed to be floating as layout level information describing adjacent ground layers as defined by nearby metal lines distributing power and ground is not present early in the design flow. Also, it is assumed that the substrate is highly resistive [7] as is typical for low noise applications; therefore, the conductance term \( G \) is not present in the model. This assumption will be revisited in future work in order to expand the validity of the models.

The notation used to represent the TSV physical dimensions, as well as their simulated ranges where relevant is shown in Table 1. The geometrical quantities referred in Table 1 are defined in Figure 4.
### Table 1: Notation used in the document

<table>
<thead>
<tr>
<th>Notation</th>
<th>Description</th>
<th>Simulated Range</th>
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<tbody>
<tr>
<td>$r_v$</td>
<td>TSV radius</td>
<td>10 µm – 40 µm</td>
</tr>
<tr>
<td>$l_v$</td>
<td>TSV length or height</td>
<td>20 µm – 140 µm</td>
</tr>
<tr>
<td>$d_b$</td>
<td>SiO2 dielectric barrier thickness</td>
<td>0.2 µm</td>
</tr>
<tr>
<td>$s_v$</td>
<td>Separation of two TSVs</td>
<td>40 µm – 200 µm</td>
</tr>
<tr>
<td>$\sigma$</td>
<td>Conductivity of Copper</td>
<td>$58 \times 10^6$ S/m</td>
</tr>
<tr>
<td>$\varepsilon_{\text{SiO2}}$</td>
<td>Relative permittivity of SiO2</td>
<td>3.9</td>
</tr>
<tr>
<td>$\varepsilon_{\text{Si}}$</td>
<td>Relative permittivity of Si</td>
<td>11.9</td>
</tr>
<tr>
<td>$\varepsilon_{0}$</td>
<td>Permittivity of air</td>
<td>$\frac{1}{36\pi} \times 10^{-9}$ F/m</td>
</tr>
<tr>
<td>$\mu_{0}$</td>
<td>Permeability of air</td>
<td>$4\pi \times 10^{-9}$ H/m</td>
</tr>
</tbody>
</table>

#### Figure 4: Geometry of a TSV bundle.

As per the new shift in the technology to match the requirements of Numonyx the prototype within ELITE is expected to utilise a tapered TSV structure with top and bottom diameters being 15 µm and 12 µm respectively and a pitch within a range of 50-80 µm. The height of the TSV is expected to be 50 µm. This copper pillar is going to be surrounded by a 60 nm thick SiN layer and a 300 nm SiO2 dielectric layers to electrically isolate the substrate which typically has a resistivity of around 10 Ω-cm for memory applications.

The simulations carried out in this report include a wide range for the intended system architectural explorations and to be useful within the wider research and design community. However, the existing compact models are for uniform diameter TSVs in highly resistive substrates (conductivity less than 0.4 S/m).

In order to accommodate the new technology, the effect of different substrate types such as EPI and CZ together with new TSV configurations is currently being investigated. However the electrical properties of the substrate affect mainly capacitance and conductance components, whereas resistance and inductance remain unaffected. The closed-form models for capacitance estimation for different configurations presented in this paper will be updated considering the effect of changed substrate properties where necessary, as well as with an additional variable representing substrate conductivity in order to aid design space explorations.

These updates will be shared between the partners within the newly defined project timelines and included in the final *Modelling and Simulation Conclusion Report* of WP2.
2.2. Compact Modelling of TSV Parasitic Parameters

Compact models are necessary for obtaining TSV parasitics more efficiently than with the use of a computationally expensive field solver. Such models are essential in simulation-based explorations at the system-conceptual level in 3-D IC design.

The parasitic parameters of TSVs in a bundle have complex field dependence predicated on the physical geometry, and the material constants. Identifying these dependencies and creating a simple compact model is a challenging task. The data to be matched consists of electrical quantities extracted from a field solver for a range of physical dimensions.

Two methods can be identified for derivation of formulae for the prediction of these TSV parasitics. One method is the response surface method [9], where a least-squares approach is used to estimate formulae in terms of linear, square, and product terms of all independent variables. Though it is quite simple to come up with an equation using this method, the outcome is a long and unwieldy set of equations, providing no physical insight, or portability for different boundary conditions.

The second method, which is used in this work, is to use dimensional analysis [4][5]. Dimensional analysis enables the number of independent variables in a function to be reduced, through the combination of 2 or more variables into a single variable, such that the resulting variable is dimension neutral. The combination of the variables has to be carried out in such a way that the resultant variable has a meaningful interpretation. Also some combinations of variables are not possible, due to the possibility of two data points being available for the same set of coordinates, and the success of the approach depends on minimising the error in such cases.

2.2.A Related Work

Parasitic modelling of TSVs and investigation of signal transmission characteristics in a TSV has received some attention in the literature, but to the authors’ best knowledge a comprehensive set of self-consistent compact models for capacitance and inductance extraction in a TSV bundle does not exist. Alam et.al. in [10] have used closed-form equations to estimate TSV resistance and capacitance values as functions of their geometric parameters. These models have not been validated thorough field-solver based simulation or experimental results. There are a few works which provide high frequency parasitic models for TSVs [11]-[13], but these do not report any DC parameter models, nor do they model structures of varying geometry. The model proposed in [13], decomposes the coupling and self capacitance terms into two components: that representing the capacitance to the SiO$_2$ annular layer ($C_{ox}$), and to the silicon substrate ($C_{si_sub}$). The equivalent circuit model presented in this work combines these two terms and presents an effective value. A recent work [7] proposed an empirical delay model for a TSV in terms of its geometry, but no explicit formulae are given for parasitic parameter estimation. Although the propagation delay of a TSV is a function of its physical dimensions, the more useful formulation would be to describe the TSV using its equivalent circuit. This provides circuit intuition that allows not only propagation delay calculation, but also power and energy calculations and signal integrity analyses. Another work [14], published very recently, discusses trends in TSV parasitics for a specific structure in the MIT Lincoln Labs 3-D integration process. It presents a thorough study, articulating capacitive and inductive time constants and loop inductance behaviour, but does not in general give a clear methodology to estimate parasitics without the help of a field solver.

2.2.B Isolated TSV Resistance

Resistance can be described accurately as a function of its conductivity and cross sectional area. For a TSV with radius $r_v$, conductivity of material (copper in this case) $\sigma$, and length $l_v$, the resistance is:

$$ R = f(l_v, r_v, \sigma) = \frac{l_v}{\sigma \pi r_v^2} $$

The simulated values are accurate to within 98% of those found from the analytical equation given in Equation (1); see Figure 5.
Capacitance

The capacitance $C_{TSV}$ of an isolated TSV is a function of its geometry, i.e. radius $r_v$, length $l_v$, and thickness of SiO$_2$ barrier $d_b$, as well as the effective permittivity of the surrounding dielectrics, $\varepsilon$. Using the principles of dimensional analysis, $C_{TSV}$ may be expressed as a function of dimensionless variables as follows:

$$C_{TSV} = \frac{l_v}{ \varepsilon_0 r_v}$$

Note that the independent dimensionless variables have been selected so that they represent a meaningful physical quantity, such as aspect ratio (i.e. height to diameter ratio). The success of the model and modelling approach, as explained earlier, is subject to the combination of variables not resulting in overlapping values of capacitance for the same independent coordinates after combination.

For a given technology, since the dielectric barrier thickness is a constant, the capacitance model is characterised under the assumption that its dielectric thickness is held constant at 0.2µm. This assumption is logical given that $d_b$ is a constant related to the technology, as well as the considerable reduction in complexity afforded by not treating this parameter as an independent variable. It is possible to recalibrate the equation constants for different $d_b$ values. Should there be a compelling need to treat $d_b$ as an independent variable the model will be revisited.

Therefore, $C_{TSV}$ is now reduced to a function of one independent variable. For various combinations of $l_v$ and $r_v$, the plot of $\frac{C_{TSV}}{\varepsilon_0 l_v}$ against the aspect ratio, $\frac{l_v}{r_v}$, is shown in Figure 6.
The relationship between \( \frac{C_{TSV}}{\varepsilon_0 l_v} \) and \( \frac{l_v}{r_v} \) can be expressed in the form of a compact model as:

\[
\frac{C_{TSV}}{\varepsilon_0 l_v} = \frac{63.34}{\ln \left(1 + 5.26 \frac{l_v}{r_v} \right)}
\]

(3)

Even though Equation (3) does not contain a term that represents dielectric barrier thickness \( d_b \), since the variation of capacitance with \( d_b \) is not significant for typical ranges, the proposed empirical self-capacitance formula has a maximum error contained to within 8% for the simulated range of \( 0<d_b<1 \mu m \). The form of the equation is derived from analytical insight given by field theory.

**Inductance**

The inductance of an isolated TSV is a function of the geometrical parameters of radius \( r_v \) and length \( l_v \) and effective permeability \( \mu \) of the surrounding medium. Due to the nature of the electromagnetic field, the dependence of inductance on \( d_b \) is negligible. Again using dimensional analysis, the TSV inductance can be expressed as:

\[
\frac{L_{TSV}}{\mu l_v} = f \left( \frac{l_v}{r_v} \right)
\]

(4)

The variation of \( L/(\mu l_v) \) versus \( l_v/r_v \) is depicted in Figure 7. The empirical formula in Equation (5) can be formulated for the self-inductance of an isolated TSV. The maximum error in this model is contained to within 3%. As with the capacitance, the form of the function is suggested by field theory.

\[
\frac{L_{TSV}}{\mu l_v} = 0.16 \ln \left(1 + 0.9 \frac{l_v}{r_v} \right)
\]

(5)
Figure 7: (a) Variation of $\frac{L_{\text{exc}}}{\mu_0 l_c}$ vs $\frac{I_v}{r_v}$ ratio and (b) percentage error in predicted and extracted values.

2.2.C RLC Extraction of a TSV Bundle

Capacitance
In a TSV bundle that comprises an $m \times m$ matrix, all the self and coupling capacitance terms are defined by:

$$C = \begin{bmatrix}
C_{1,1} & -C_{1,2} & \cdots & -C_{1,n} \\
-C_{2,1} & C_{2,2} & \cdots & -C_{2,n} \\
\vdots & \vdots & \ddots & \vdots \\
-C_{n,1} & -C_{n,2} & \cdots & C_{n,n}
\end{bmatrix}, \quad (6)$$

where $n = m^2$.

In the capacitance matrix (6), the diagonal element $C_{i,i}$ represents the sum of inter-via coupling capacitances ($C_{i,j}$) and self capacitance ($C_{i,0}$) as given in:

$$C_{i,i} = C_{i,0} + \sum_{j=1}^{n} C_{i,j}. \quad (7)$$
Figure 8: Coupling capacitance terms of the centre TSV in a 7X7 bundle normalized to total capacitance of the centre TSV.

The capacitance matrix is sparse; the main diagonal and adjacent diagonals representing terms to nearest neighbours are populated while the other entries are vanishingly small in comparison (see Figure 8). Further the symmetry in the structure is exploited to reduce the number of terms to be investigated. With reference to the naming convention given in Figure 9 the distances from M TSV to N, E, S and W TSVs are the same, while the distances to NE, NW, SE and SW TSVs are also equal. Therefore, the capacitance formulae for the total capacitance of M, N, and NE TSVs \( C_{i,0} \), and the coupling terms to their nearest neighbours \( C_{i,j} \) as defined in Figure 9 are a representative unit for a TSV bundle of any size.

Figure 9: Electrical model of a TSV bundle.

The well established practice in parasitic modelling is to distribute the total capacitance of a wire into its self \( C_{i,0} \) and coupled components \( C_{i,j} \) such that switching pattern dependent cross-talk effects on delay and SI can be examined in a circuit simulator. Therefore, we present two self-consistent equations for self and coupling capacitances in (8) and (9) from which the total capacitance \( C_t = C_{i,0} \) can also be estimated as their sum.

The self capacitance \( C_t = C_{i,0} \) formula is of the form:
where $C_{\text{tsv}}$ is the capacitance of an isolated TSV given in (3) and the constants in (8) are defined in the first three rows of Table 2. In (8) the constants $k_2$ and $k_3$ are negative, and therefore as $p_v$ approaches infinity, $C_z$ approaches $C_{\text{tsv}}$, the capacitance of an isolated TSV given in (3), with a maximum error contained to 6% for the simulated range.

The formula for the coupling capacitance ($C_z = C_{i,j}$) terms of (6) for $i \neq j$ is of the form:

$$C_z = \frac{k_i \epsilon_0 l_v}{\ln \left( k_2 \frac{p_v}{r_v} \right)} \left[ 1 + k_3 \left( \frac{p_v}{l_v} \right)^{k_4} + k_5 \left( \frac{l_v}{r_v} \right)^{k_5} + k_7 \left( \frac{p_v}{l_v} \right)^{k_7} \right] \tag{9}$$

with constants $k_{1, \ldots, 8}$ corresponding to $C_{c_{-l}}, C_{c_{-p}}$ and $C_{c_{-d}}$ defined in the last three rows of Table 2 respectively.

### Table 2: Constants for self and coupling terms of 3×3 TSV bundle (see Figure 9 for capacitance definitions)

<table>
<thead>
<tr>
<th></th>
<th>$k_1$</th>
<th>$k_2$</th>
<th>$k_3$</th>
<th>$k_4$</th>
<th>$k_5$</th>
<th>$k_6$</th>
<th>$k_7$</th>
<th>$k_8$</th>
<th>Maximum % Error</th>
<th>Average % Error</th>
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<tr>
<td>(a)</td>
<td>$C_{s-M}$</td>
<td>0.1505</td>
<td>-0.0071</td>
<td>-0.0291</td>
<td>0.1849</td>
<td>-1.9371</td>
<td>6.9577</td>
<td>-0.0131</td>
<td>-0.0354</td>
<td>13.0</td>
</tr>
<tr>
<td>(b)</td>
<td>$C_{s-N}$</td>
<td>0.6876</td>
<td>-0.0390</td>
<td>-0.0583</td>
<td>1.8076</td>
<td>-0.2229</td>
<td>11.3537</td>
<td>0.0402</td>
<td>-13.1813</td>
<td>10.2</td>
</tr>
<tr>
<td>(c)</td>
<td>$C_{s-NE}$</td>
<td>0.3406</td>
<td>-0.0345</td>
<td>-0.0586</td>
<td>5.0708</td>
<td>-0.1530</td>
<td>-5.6346</td>
<td>-0.1530</td>
<td>-0.7643</td>
<td>13.3</td>
</tr>
<tr>
<td>(d)</td>
<td>$C_{c-l}$</td>
<td>10.191</td>
<td>0.5490</td>
<td>-0.014</td>
<td>0.796</td>
<td>0.054</td>
<td>-1.157</td>
<td>-0.018</td>
<td>-0.600</td>
<td>8.7</td>
</tr>
<tr>
<td>(e)</td>
<td>$C_{c-p}$</td>
<td>3.180</td>
<td>0.5440</td>
<td>-0.199</td>
<td>0.586</td>
<td>0.122</td>
<td>0.540</td>
<td>2.176</td>
<td>0.110</td>
<td>10.9</td>
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<tr>
<td>(f)</td>
<td>$C_{c-d}$</td>
<td>18.117</td>
<td>28.457</td>
<td>-1.734</td>
<td>-2.178</td>
<td>0.600</td>
<td>-0.518</td>
<td>-0.470</td>
<td>0.188</td>
<td>8.0</td>
</tr>
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Also shown in Table 2 are the absolute maximum errors while the full scatter plots are shown in Figure 10. As can be seen, all models have a minimum accuracy over the full simulated range of approximately 90%. It should be noted that the $C_{s-M}$ value is valid only when $C_{s-M} / C_{t-M} \geq 0.09$, where $C_{t-M}$ ($C_{i,l}$) is the total capacitance of the M TSV. Below this range $C_{s-M}$ values are so small that they are negligible for any meaningful delay, SI or PI analysis. For those geometries the self capacitance values are in fact indistinguishable from numerical noise in the field solver. Comparisons between the calculated and extracted $C_{i}$ values for M, N, and NE TSVs for the whole range have maximum absolute errors of 2.3%, 3.6% and 2.9% respectively.
Figure 10: Percentage error in parasitic capacitance estimated from formulae (8) and (9) for the order (a)…(f) given in Table 2.

**Inductance**

The self and mutual inductance terms for a TSV bundle are defined by:

\[
L = \begin{bmatrix}
L_{1,1} & -L_{1,2} & \cdots & -L_{1,n} \\
-L_{2,1} & L_{2,2} & \cdots & -L_{2,n} \\
\vdots & \vdots & \ddots & \vdots \\
-L_{n,1} & -L_{n,2} & \cdots & L_{n,n}
\end{bmatrix}.
\]  

As shown in Figure 11, the inductive coupling is long range and therefore the inductance matrix is well populated, with all elements being of a similar order of magnitude.

Figure 11: Mutual inductance terms of centre TSV in a 7×7 bundle normalized to self inductance of centre TSV.
The self inductance of a wire is not affected due to the presence of neighbouring wires, an observation borne out by simulations of two parallel TSVs. Therefore, the self inductance $L_s$ can be estimated from the equation derived for an isolated conductor in (5). However, mutual inductance between lines is a function of the effective permeability of the material, as well as the geometrical parameters of TSV center-to-center distance $d_v$, length $l_v$ and radius $r_v$.

$$L_m = f(\mu, r_v, l_v, d_v)$$  \hspace{1cm} (11)

Following principles of dimensional analysis, (11) can be expressed as a function of dimensionless quantities:

$$\frac{L_m}{\mu l_v} = f\left(\frac{r_v}{l_v}, \frac{d_v}{l_v}\right)$$  \hspace{1cm} (12)

Figure 12 depicts the variation of mutual inductance between two parallel TSVs with $\frac{d_v}{l_v}$ for various $\frac{r_v}{l_v}$ combinations.

The empirical formula modelling this behaviour is:

$$\frac{L_m}{\mu l_v} = 0.199 \ln \left(1 + 0.438 \frac{l_v}{d_v}\right)$$  \hspace{1cm} (13)

The maximum error in this model is contained to within 8%.
A snapshot of some of the data points illustrating the accuracy of the models is shown in the following tables. The extracted inductance values for a 3x3 TSV bundle for \( l_v=70\mu m, p_v=101\mu m \) and \( r_v=25\mu m \), are shown in Table 3. The values predicted from the proposed models and the error in comparison to the simulated values are shown in Table 4 and Table 5 respectively.

<table>
<thead>
<tr>
<th>Table 3: Extracted inductance values for a TSV bundle ((l_v=70\mu m, p_v=101\mu m, r_v=25\mu m))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance from the field Solver (in pH)</td>
</tr>
<tr>
<td>Centre</td>
</tr>
<tr>
<td>--------</td>
</tr>
<tr>
<td>Center</td>
</tr>
<tr>
<td>E</td>
</tr>
<tr>
<td>NE</td>
</tr>
<tr>
<td>NW</td>
</tr>
<tr>
<td>S</td>
</tr>
<tr>
<td>SE</td>
</tr>
<tr>
<td>SW</td>
</tr>
<tr>
<td>W</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 4: Predicted inductance values for a TSV bundle ((l_v=70\mu m, p_v=101\mu m, r_v=25\mu m)) from Equations (5) and (13)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductance from the proposed models (in pH)</td>
</tr>
<tr>
<td>Centre</td>
</tr>
<tr>
<td>--------</td>
</tr>
<tr>
<td>NE</td>
</tr>
<tr>
<td>NW</td>
</tr>
<tr>
<td>SE</td>
</tr>
<tr>
<td>SW</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 5: Error between predicted and simulated inductance values for a TSV bundle ((l_v=70\mu m, p_v=101\mu m, r_v=25\mu m)) from Equations (5) and (13)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Percentage Error = ( \frac{[1-\text{(model’s predicted value)}/\text{field solver extracted value}]}{100} )</td>
</tr>
<tr>
<td>Centre</td>
</tr>
<tr>
<td>--------</td>
</tr>
<tr>
<td>Center</td>
</tr>
<tr>
<td>E</td>
</tr>
<tr>
<td>N</td>
</tr>
<tr>
<td>NE</td>
</tr>
<tr>
<td>NW</td>
</tr>
<tr>
<td>S</td>
</tr>
<tr>
<td>SE</td>
</tr>
<tr>
<td>SW</td>
</tr>
<tr>
<td>W</td>
</tr>
</tbody>
</table>
2.2.D Fidelity of Electrical Models

As the intended use of the compact models is to calculate circuit related metrics, it is important that any deviations in these from the values when using the nominal parasitic values returned by the field solver, is contained. In order to check the sensitivity of the circuit metrics to errors in the parasitic values, simulations were carried out to estimate the 50% delay and coupled noise amplitude with a worst-case switching pattern in a 3x3 bundle. The absolute error in delay and noise resulting from the recorded maximum errors in each parasitic component when the others are held at their nominal values is reported in Table 6. Inductance is not considered as its effect is negligible, as shown in the next section. It can be seen that in all cases the error is less than the error in the parasitic values predicted by the compact models. Given in the last column are the errors in delay and noise resulting from a worst-case combination of errors in the parasitic values, which is contained to 10% in the case of delay, and 14% in the case of noise. These errors represent the absolute upper bound, and will occur only in the singular case when $R_{tsv}$, $C_s$, $C_l$, and $C_d$ are all individually in error by their maximum values simultaneously, and in a manner that maximises the error in the calculated metric.

Table 6: Variation of delay and coupled noise for the center TSV in a 3x3 bundle with worst-case switching

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max. % error in Model</th>
<th>% in Error in metric</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Delay</td>
</tr>
<tr>
<td>$R_{tsv}$</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>$C_s$</td>
<td>13</td>
<td>3</td>
</tr>
<tr>
<td>$C_l$</td>
<td>8.7</td>
<td>6</td>
</tr>
<tr>
<td>$C_d$</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>$R_{tsv}$, $C_s$, $C_l$, $C_d$</td>
<td>Worst-case combination</td>
<td>10</td>
</tr>
</tbody>
</table>

Shown in Figure 13 are example waveforms corresponding to nominal and worst-case error combinations corresponding to a TSV with radius of 35µm and length of 100µm.

![Waveform Image](image1)

Figure 13: Normalised output signal on the middle conductor in a 3x3 TSV bundle using nominal parasitic values obtained from the field solver, as well as worst-case minimum and maximum error combinations when all adjacent TSVs switch from ‘1’ to ‘0’ for (a) switching victim and (b) silent victim.

In order to verify the accuracy of the models further, Monte Carlo simulations were performed using a 3x3 TSV bundle and the maximum range of errors for all components in the circuit. This represents the maximum errors in the full range of TSV sizing and spacing explored in this study. The simulation results were generated from a Monte Carlo statistical analysis in the Spectre circuit simulator. Figure 14 shows a plot of the distribution in the 50% rise time caused by a uniform variation in error for 500 cases. In this case, the centre line was switched from low to high, and the surrounding 8 aggressors were switched in the opposing direction, to cause the worst case delay scenario on the victim line. It is clear from this figure that the error in rise time is focused around a very narrow margin, despite the probability of error between minimum and maximum values being uniform. This means that the maximum error in the model yields only small variations in rise times.
3. Delay and Signal Integrity Analysis

3.1. Equivalent Circuit Structures

The aim of this section is to determine relevant characteristic properties of the equivalent electrical circuit of a TSV derived in Section 2. The exploration of the properties of this structure within a SPICE simulator provides a clearer picture of the dominant components and also verifies its usefulness in this project for prediction of signal integrity and delay parameters. Since the electrical model is comprised of inductance, resistance and capacitance, these components are scrutinized to determine their individual contribution to delay and noise in the electrical simulations. A reduction in model complexity is always desirable if there is minimal effect on the accuracy.
This equivalent electrical circuit derived for TSVs in Section 3 can be incorporated into a SPICE simulator in a straightforward manner to determine the electrical behaviour of the vias with realistic input and load configurations.

### 3.1.A Simulation Setup

In the simulations, the TSV model is driven by an inverter in an AMS 0.35\(\mu\)m technology. The size of the inverter was adjusted from \(H=1\) to 50, where \(H\) is defined as multiples of a minimum sized inverter, and the effect on delay was observed in a single TSV with worst case parasitic properties (see Table 7). Inverter sizes greater than 10 did not have a significant beneficial effect on the delay, thus a driver size of 10 was found to be adequate in these preliminary investigations. The load for the circuit was chosen as a minimum sized inverter to replicate the effects of an input pin. The driver and load setup used in all of the following simulations is depicted in Figure 16.

![Figure 16: Simulation setup with a driver sized to be 10 times a minimum sized inverter, and a minimum sized inverter as pin load.](image)

The parasitics of the TSV are derived from the tables provided in Section 2 and use worst, typical and best case values for different geometries of a TSV as seen in Table 7. The three cases were chosen based on their parasitic values rather than the geometrical configurations. In later simulations, the simple inverter and load models can be replaced with suitable driver and receiver IBIS models to provide accurate results for a FLASH or DRAM device.

#### Table 7: Minimum, typical and worst-case TSV parasitics

<table>
<thead>
<tr>
<th></th>
<th>R</th>
<th>C</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>Worst-Case</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L=20(\mu)m, (R_v=20\mu)m</td>
<td>207m</td>
<td>14.9fF</td>
<td>92.629pH</td>
</tr>
<tr>
<td>Typical</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L=20(\mu)m, (R_v=60\mu)m</td>
<td>0.69m</td>
<td>11.211fF</td>
<td>18.547pH</td>
</tr>
<tr>
<td>Best</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L=20(\mu)m, (R_v=15\mu)m</td>
<td>2.78m</td>
<td>5.574fF</td>
<td>3.13pH</td>
</tr>
</tbody>
</table>

### 3.1.B Isolated TSV

The first investigations are carried out on a single, isolated TSV. The next three figures show simulation results from a sweep of the resistive, capacitive and inductive parasitics within the entire range of parasitic parameter values of an isolated TSV structure for the considered geometries. The sweeps for each parameter cover the entire range of physical configurations, with a large margin for the upper bound.

In the following cases, the \(R\), \(C\), and \(L\) values are swept independently of each other to demonstrate their individual contribution to the shape of the waveform and integrity of the signal. Figure 17, Figure 18, and Figure 19 show the far-end output when sweeping resistance, inductance and capacitance values with the input waveform as a reference.

Sweeping the resistance from 0.1m\(\Omega\) to 500m\(\Omega\) represents the entire spectrum of parasitic resistance values for the range of TSV sizes considered. As seen in Figure 17, the output curves do not deviate despite a full sweep of the range of values. The reason is that the resistive parasitics for TSVs are very small in comparison with the output impedance of the driver, resulting in no visible difference in the outputs corresponding to each parametric sweep.
Figure 17: Resistance is swept from 0.1mΩ – 500mΩ. The waveforms corresponding to each sweep appear more or less on top of each other, and the TSV parasitic resistance shows an insignificant contribution to delay or SI.

Sweeping the parasitic inductance from 1pH to 500pH covers the entire range of possible values for the TSV but as with resistance there is no significant difference in the individual waveforms corresponding to the different values. There are minor fluctuations between each sweep, but there is no significant deviation.

Figure 18: Inductance is swept from 1pH – 500pH. The individual waveforms do not show any appreciable change over the entire range, and thus do not contribute significantly to delay or SI.
The capacitive parasitics on the other hand, have a significant effect as the waveforms of Figure 19 show.

![Input vs. Capacitive Sweep 0-500fF](image)

Figure 19: Capacitance is swept from 1fF–500fF. The capacitive parasitics corresponding to different geometries clearly have an effect on the output waveform. As the capacitance increases, the signal rise time goes up significantly.

Hence these sweeps demonstrate that the dominant parasitic component of a typical isolated TSV structure as is likely to be used in the ELITE prototype is the self capacitance. The resistive parasitics have no significant effect on delay or SI when the TSV is driven by an on-chip driver, while the inductive parasitics also have no significant effect. This investigation indicates that an isolated TSV structure can be represented as a simple lumped capacitive model. This effectively reduces the complexity of the model derived in Section 2.2.B for an isolated TSV.

3.1.C Coupled TSVs

This section explores the coupling parameters shown in the equivalent circuit in Section 2.2.C. There is a single coupling capacitance term, $C_{C}$, as well as 2 parasitic mutual inductance terms between each adjacent TSV. The individual TSVs are defined in the simulation environment with the same circuit setup as used for an isolated TSV shown in Figure 16. The circuit is arranged in a 3x3 bundle of TSVs as shown in Figure 20.

![Figure 20: TSV bundle.](image)

For worst-case coupling, the central TSV is a silent victim line and the surrounding 8 vias in the bundle are aggressors switching simultaneously. The coupled noise on a silent victim line is observed in order to determine the individual effect of both inductive and capacitive coupling. In these studies, the TSV is given typical parasitics and the coupling terms are altered independent of one another.
Inductive Contribution
The effect of inductive coupling was investigated first with various input signals. The centre structure in the bundle was kept as a silent victim and the remaining 8 surrounding aggressor lines were switched from low to high to observe the coupling effects on the victim line. Coupling factors, K, of 0.391 and 0.280 (the maximum in the extracted range) were used for the lateral and diagonal elements respectively. The results from this simulation are produced in Figure 21.

![Inductive Coupling On a Silent Victim](image)

Figure 21: Inductive coupling on a silent net.

As can be seen, there is minimal disturbance on the victim net from the 8 aggressors switching. With 8 surrounding lines switching simultaneously from 0-3.3V, the coupled noise on the victim line is only approximately 7mV peak to peak. The small values of parasitic inductance inherent in the TSV structures do not produce a significant coupling effect between the TSVs. Sweeping the rise times from 1ps-100ps produces slightly different oscillations on the victim line, but the magnitude of the coupled noise does not increase significantly. The effect on the victim net is not large enough to justify parasitic mutual inductance in a 3x3 bundle at this point in the investigation. It is however possible that the simultaneous switching of many different aggressors, including non-adjacent ones, can produce a more significant effect. This is due to the inductive coupling being long range as shown in Figure 11. When such a switching scenario needs to be modelled, the compact models for inductance can be used to model the mutual inductance in bundles much larger than the 7×7 size they have been verified for as a first approximation, due to the relative non-dependence of inductance on the local geometry.

Capacitive Contribution
The simulations performed to evaluate the significance of capacitive coupling had the mutual inductance terms removed. Values used for lateral and diagonal coupling between adjacent structures in the bundle were swept from 0-40fF, representing the entire range of possible coupling values considered for various TSV sizes and pitches. Figure 22 shows the effect of coupling when the adjacent TSVs switch simultaneously in the same direction, as in the inductive example. Voltage spikes of over 0.5V are observable. The effect of capacitive crosstalk clearly has a large effect on the victim line and must be thoroughly investigated and explored in the 3x3 bundle simulations for signal integrity and noise-on-delay effects.

Thus, at this point in the investigation, the inductive coupling between TSVs can be neglected. However, it may be necessary to reintroduce inductive coupling in simulations when more accurate system information is available in order to verify its contribution to the signalling effects in a 3-D environment.
3.1.D Distributed vs. Lumped Modelling
As simulation efficiency is a principal concern in the full-chip evaluation of a system, especially in a complex 3-D IC consisting of many layers of logic, it is of interest to reduce the complexity of the model as much as possible. Signal lines can be evaluated as distributed or lumped models depending on their parasitic characteristics. Distributed models are more expensive computationally but can provide more accurate results. The next simulations compare distributed and lumped models for the TSVs structures with various parasitic values. The electrical model was segmented into 1, 3, 5, 10 divisions in a distributed “T” model in order to determine an appropriate model for TSV simulations. Figure 23 and Figure 24 show the results.
It is clear from these simulations that the distributed models consisting of 3, 5, and 10 segments produce a waveform which nearly exactly traces the lumped model of the TSV. There are only minor differences between the models, which at this point produce no significant differences in delay or signal integrity. This is expected because of the relatively small values of TSV parasitics. This indicates that a lumped model is sufficiently accurate for the simulation of signal integrity and delay in the TSV structures used in ELITE.

**3.2. Signal Integrity (SI) Simulations in TSV Structures**

This section explores the effects on SI caused by varying the geometrical properties, and thus the parasitic values, of TSVs. As TSVs are a recent concept, this area is not well documented in the literature, despite it being of paramount importance in 3-D IC design. It is the purpose of this section to provide a preliminary examination of delay and SI effects in signals propagating through TSV interconnects. As the project progresses, more system-specific information can be considered in the simulations to provide an increasingly accurate picture of TSV interconnect characteristics in a 3-D memory design.

To demonstrate the effect of an isolated TSV’s parasitic characteristics on delay in a 3-D IC, simulations were performed with various parasitic values and signalling conditions. Figure 25 shows the rising edge of the far-end signal in a TSV with a radius of 20\(\mu\)m and length of 60\(\mu\)m with typical parasitic values, along with the input signal.
In this case the 50% delay in a single TSV is of the order of 25 ps. However, it is more likely that the TSVs will be arranged in a bundle or will span multiple layers, as the next section investigates.

### 3.2.A Cascaded Effects of Isolated TSVs

In this section, the effects of a signal propagating through several layers within a 3-D stack are investigated. The model for the isolated TSV is combined in series with appropriate loads to simulate signals traversing multiple layers (Figure 26). Clearly, as the number of layers in a 3-D IC increases, the parasitic effects, namely load capacitance, increase due to the number of TSVs increasing. By determining the effects cascaded TSVs have on the source signal, driver sizing and repeater insertion requirements can be investigated.

![Figure 26: Representation of cascaded isolated TSVs within a stacked IC.](image)

TSVs with length 20µm and radius 40µm were connected in series to simulate a stack of up to 10 TSVs. Each TSV was loaded with a minimum sized inverter and the rise times were calculated from the far-end waveform. The results from these simulations are shown in Table 8.

<table>
<thead>
<tr>
<th>No. of TSVs</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>6</th>
<th>8</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rise Time (ps)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10%</td>
<td>40.76</td>
<td>53.176</td>
<td>54.949</td>
<td>56.963</td>
<td>58.916</td>
<td>60.829</td>
</tr>
<tr>
<td>50%</td>
<td>62.162</td>
<td>113.78</td>
<td>124.07</td>
<td>134.4</td>
<td>144.68</td>
<td>155.04</td>
</tr>
<tr>
<td>90%</td>
<td>108.71</td>
<td>239.29</td>
<td>265.13</td>
<td>290.94</td>
<td>316.69</td>
<td>342.53</td>
</tr>
</tbody>
</table>
As can be seen in the above figures, multiple stacked layers have a significant effect on delay. Figure 27 shows a plot of the above data.

![Number of Cascaded TSVs vs. Delay](image)

**Figure 27:** Variation of delay (ps) with number of layers.

Clearly, the target system specifications will determine whether repeater insertion is required. Simulations with IBIS drivers and loads for a particular device will substantially increase the accuracy of the simulation and allow for recommendations on driver sizing and repeater insertion to maximize the performance and integrity of the system. Figure 28 shows the input and output waveform after the signal traverses a stack of 10 TSVs.

![Input vs. 10 TSVs Cascaded](image)

**Figure 28:** input and far-end waveform in a stack of 10 dies.

The effects of cascading multiple TSVs are even more apparent when coupling occurs between adjacent TSVs in a bundle, as discussed in section 3.2.B.

### 3.2.B Crosstalk in a 3×3 Bundle of TSVs

This section investigates the effects of crosstalk between TSVs organized in a 3×3 bundle, depicted in Figure 29. By employing the equivalent circuits that were verified earlier, various conditions are simulated to analyze crosstalk effects in this structure.
Figure 29: 3×3 TSV bundle.

In order to maximise the benefit afforded by the shorter global interconnects in 3-D ICs, interlayer communication should take place at the maximum possible speed over individual TSVs and minimum TSV pitch within a bundle to provide the widest possible bus width and highest throughput. However, as with 2-D circuits, capacitive and inductive crosstalk between adjacent lines in the 3-D bus structure need to be managed. It is the goal of this section to determine the effects of crosstalk between TSVs within a bus in a 3-D IC on SI and latency. Spectre simulations were carried out for various scenarios expected to cause the most significant effect in a digital system using the parasitic values determined for a TSV bundle in Section 2.2.

The first experiment examines the noise coupled from the simultaneous switching of the neighbouring TSV aggressors on the silent centre TSV in a 3×3 bundle. This was performed with TSV sizes of lengths and radii of 20µm and 40µm respectively and a pitch of 100µm. This resulted in a voltage spike on the victim line of 500mV on both the rising and falling edge. This is not significant enough to disturb the operation of the receiver at 3.3V, but may be significant in a stack with cascaded TSVs and merely demonstrates a typical coupling scenario. The resulting waveform is seen in Figure 30.

Figure 30: Coupled noise amplitude on silent victim from all aggressors within bundle switching simultaneously.

Figure 31 depicts the worst case switching pattern for delay in a 3×3 TSV bundle. The victim is the central via, and the aggressors are the 8 surrounding TSVs. The aggressors all switch from “1” to “0” and the victim line switches from “0” to “1” simultaneously (the effect of aggressor alignment is neglected, as it is a complex study in its own right, independent of TSV specific effects).
As can be seen in the waveform shown in Figure 32 for a TSV bundle with a pitch of 100µm and length and radii of 20µm and 40µm respectively, there is a significant noise-on-delay effect on the victim net, with a 60% increase (393 ps vs. 157 ps) in the 50% delay in comparison to an isolated TSV.

Different switching patterns within the bundle with various parasitic values and pitches are considered in the following section.

3.2.C Delay Contribution for Various Switching Events
This section analyzes various permutations for the switching of aggressors and their respective effect on the delay of a switching victim net. The symbols used to articulate the switching patterns are defined in Table 9.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Switching Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>→</td>
<td>none</td>
</tr>
<tr>
<td>↑</td>
<td>logical switch from 0 to 1</td>
</tr>
<tr>
<td>↓</td>
<td>logical switch from 1 to 0</td>
</tr>
<tr>
<td>↑↑</td>
<td>2 simultaneous switches</td>
</tr>
<tr>
<td>↑↑↑</td>
<td>3 simultaneous switches</td>
</tr>
<tr>
<td>↑↑↑↑</td>
<td>4 simultaneous switches</td>
</tr>
</tbody>
</table>
Using the symbols of Table 9, switching patterns are described for the lateral and diagonal structures in the bundle that cover all conceivable combinations, in Table 10.

<table>
<thead>
<tr>
<th>State</th>
<th>Victim</th>
<th>Lateral</th>
<th>Diagonal</th>
<th>State</th>
<th>Victim</th>
<th>Lateral</th>
<th>Diagonal</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>↑</td>
<td>→</td>
<td>→</td>
<td>A2</td>
<td>↑</td>
<td>→</td>
<td>→</td>
</tr>
<tr>
<td>B1</td>
<td>↑</td>
<td>→</td>
<td>↓</td>
<td>B2</td>
<td>↑</td>
<td>→</td>
<td>↑</td>
</tr>
<tr>
<td>C1</td>
<td>↑</td>
<td>→</td>
<td>↓↓</td>
<td>C2</td>
<td>↑</td>
<td>→</td>
<td>↑↑</td>
</tr>
<tr>
<td>D1</td>
<td>↑</td>
<td>→</td>
<td>↓↓↓</td>
<td>D2</td>
<td>↑</td>
<td>→</td>
<td>↑↑↑</td>
</tr>
<tr>
<td>E1</td>
<td>↑</td>
<td>→</td>
<td>↓↓↓↓</td>
<td>E2</td>
<td>↑</td>
<td>→</td>
<td>↑↑↑↑</td>
</tr>
<tr>
<td>F1</td>
<td>↑</td>
<td>↓</td>
<td>→</td>
<td>F2</td>
<td>↑</td>
<td>↑</td>
<td>→</td>
</tr>
<tr>
<td>G1</td>
<td>↑</td>
<td>↓</td>
<td>↓</td>
<td>G2</td>
<td>↑</td>
<td>↑</td>
<td>↑</td>
</tr>
<tr>
<td>H1</td>
<td>↑</td>
<td>↓</td>
<td>↓↓</td>
<td>H2</td>
<td>↑</td>
<td>↑</td>
<td>↑↑</td>
</tr>
<tr>
<td>I1</td>
<td>↑</td>
<td>↓</td>
<td>↓↓↓</td>
<td>I2</td>
<td>↑</td>
<td>↑</td>
<td>↑↑↑</td>
</tr>
<tr>
<td>J1</td>
<td>↑</td>
<td>↓</td>
<td>↓↓↓↓</td>
<td>J2</td>
<td>↑</td>
<td>↑</td>
<td>↑↑↑↑</td>
</tr>
<tr>
<td>K1</td>
<td>↑</td>
<td>↓↓</td>
<td>→</td>
<td>K2</td>
<td>↑</td>
<td>↑↑</td>
<td>→</td>
</tr>
<tr>
<td>L1</td>
<td>↑</td>
<td>↓↓</td>
<td>↓</td>
<td>L2</td>
<td>↑</td>
<td>↑↑</td>
<td>→</td>
</tr>
<tr>
<td>M1</td>
<td>↑</td>
<td>↓↓</td>
<td>↓↓</td>
<td>M2</td>
<td>↑</td>
<td>↑↑</td>
<td>↑</td>
</tr>
<tr>
<td>N1</td>
<td>↑</td>
<td>↓↓</td>
<td>↓↓↓</td>
<td>N2</td>
<td>↑</td>
<td>↑↑</td>
<td>↑↑↑</td>
</tr>
<tr>
<td>O1</td>
<td>↑</td>
<td>↓↓</td>
<td>↓↓↓↓</td>
<td>O2</td>
<td>↑</td>
<td>↑↑</td>
<td>↑↑↑</td>
</tr>
<tr>
<td>P1</td>
<td>↑</td>
<td>↓↓↓</td>
<td>→</td>
<td>P2</td>
<td>↑</td>
<td>↑↑↑</td>
<td>→</td>
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<tr>
<td>Q1</td>
<td>↑</td>
<td>↓↓↓</td>
<td>↓</td>
<td>Q2</td>
<td>↑</td>
<td>↑↑↑</td>
<td>↑</td>
</tr>
<tr>
<td>R1</td>
<td>↑</td>
<td>↓↓↓</td>
<td>↓↓</td>
<td>R2</td>
<td>↑</td>
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</tr>
<tr>
<td>S1</td>
<td>↑</td>
<td>↓↓↓</td>
<td>↓↓↓</td>
<td>S2</td>
<td>↑</td>
<td>↑↑↑</td>
<td>↑↑↑</td>
</tr>
<tr>
<td>T1</td>
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<td>↓↓↓</td>
<td>↓↓↓</td>
<td>T2</td>
<td>↑</td>
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<tr>
<td>U1</td>
<td>↑</td>
<td>↓↓↓</td>
<td>→</td>
<td>U2</td>
<td>↑</td>
<td>↑↑↑</td>
<td>→</td>
</tr>
<tr>
<td>V1</td>
<td>↑</td>
<td>↓↓↓</td>
<td>↓</td>
<td>V2</td>
<td>↑</td>
<td>↑↑↑</td>
<td>↑</td>
</tr>
<tr>
<td>W1</td>
<td>↑</td>
<td>↓↓↓</td>
<td>↓</td>
<td>W2</td>
<td>↑</td>
<td>↑↑↑</td>
<td>↑</td>
</tr>
<tr>
<td>X1</td>
<td>↑</td>
<td>↓↓↓</td>
<td>↓↓</td>
<td>X2</td>
<td>↑</td>
<td>↑↑↑</td>
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<tr>
<td>Y1</td>
<td>↑</td>
<td>↓↓↓</td>
<td>↓↓↓</td>
<td>Y2</td>
<td>↑</td>
<td>↑↑↑</td>
<td>↑↑↑</td>
</tr>
</tbody>
</table>

The 50% rise times of the victim net for all these patterns were recorded and plotted in Figure 33 and Figure 34. Three sets of parasitics were modelled for different pitch and TSV sizes which are shown in Table 11.
Table 11: Parasitic Sets Used In Switching Events

<table>
<thead>
<tr>
<th>TSV Structure</th>
<th>C_t</th>
<th>R_s</th>
<th>L_s</th>
<th>C_lat</th>
<th>C_diag</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set 1</td>
<td>P_v=50.4µm</td>
<td>L_s=20µm, R_v=5µm</td>
<td>5.8019fF</td>
<td>4.5054 mΩ</td>
<td>6.1851pH</td>
</tr>
<tr>
<td>Set 2</td>
<td>P_v=70.4µm</td>
<td>L_s=20µm, R_v=15µm</td>
<td>10.167fF</td>
<td>0.4919mΩ</td>
<td>3.138pH</td>
</tr>
<tr>
<td>Set 3</td>
<td>P_v=100.4µm</td>
<td>L_s=20µm, R_v=40µm</td>
<td>27.388fF</td>
<td>0.0688mΩ</td>
<td>1.4479pH</td>
</tr>
</tbody>
</table>

Figure 33: Delay in a 3×3 bundle for switching events A1 through Y1.

Figure 34: Delay in a 3×3 Bundle for switching events A2 through Y2.
It can be seen from these figures that the switching patterns of the aggressors can affect the minimum and maximum delay of the victim significantly. The spread in the 50% delay for one set of parasitic values was from 36 ps to 135 ps, almost a 4 fold deviation over the minimum delay.

### 3.2.D Cascaded 3x3 TSV Bundle

To compare results to the stacked isolated TSVs as seen in Figure 28, simulations have also been conducted for a 10 layer stack of 3x3 TSV bundles. In this case, parasitic set 3 as defined in Table 11 is used in the simulation. As with the previous example, each TSV is loaded with a minimum sized inverter to represent a pin connection for each layer. For this simulation, the stacked TSV bundles are compared with the stacked isolated TSVs. Within the bundle, aggressors are set to switch in the worst-case pattern, as described previously and depicted in Figure 31. The results from this simulation are shown in Figure 35 below.

![Figure 35: Input and far-end waveforms in a stack of 10 dies with and without coupling.](image)

The crosstalk in the stacked bundle clearly causes the rise time to increase significantly over the stacked isolated TSVs. The bundled TSV takes 863.5ps to reach the 50% point, compared to 279.1ps for the isolated TSV stack. As it is more likely for the TSVs to be arranged in a vertical bus, determining maximum delay within a bundle is of great importance in the overall system design task.

### 3.2.E Eye Diagrams for Signal Integrity in a 3x3 Bundle

In order to ensure proper operation, a combination of all events previously considered must be carefully examined. In this section, the simulation setup is changed to incorporate a Pseudo-Random Bit Stream (PRBS) input to the 3x3 TSV bundle. Each TSV is provided with a random bit stream driven by an inverter sized to be 10 times a minimum sized inverter. The parasitics used in the simulations to generate the eye diagrams of Figure 36, Figure 37 and Figure 38 are given in Table 12.

<table>
<thead>
<tr>
<th>Rv (µm)</th>
<th>Lv (µm)</th>
<th>Pv (µm)</th>
<th>Ctotal (fF)</th>
<th>Clat (fF)</th>
<th>Cdiag (fF)</th>
<th>C_isolated (fF)</th>
<th>R (mΩ)</th>
<th>L in pH</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>20</td>
<td>50.4</td>
<td>13.95</td>
<td>2.84</td>
<td>0.58</td>
<td>5.57</td>
<td>0.49</td>
<td>3.14</td>
</tr>
</tbody>
</table>

In these cases eye diagrams are used to depict the quality of the victim line’s bit stream given the random switching patterns on the aggressors. Figure 36 shows the eye diagram at the output of the victim (middle) TSV in a bundle with coupling from 8 aggressors. The bit rate is set to 1GBPS initially.
As can be seen in Figure 36, the eye opening is wide and clearly defined, with some variation in delay as evidenced by the thickness of the rising and falling edges of the waveform.

Figure 37 shows the eye diagram with the same parasitics but with a 2 GBPS bit stream. It is clear that the increase in switching speed decreases the size of the eye and increases the variation in delay.

The eye diagram in Figure 38 shows the response when the PRBS bit rate is set to 10 GBPS. The parasitics are the same as before. It is quite clear that the eye has become very narrow and the variation in delay has widened to an unacceptable level. The driver is struggling to cope with the increased bit rate and capacitive effects of the neighbouring TSVs.
Figure 38: Eye diagram of victim line output signal with 10 GBPS PRBS on all lines.

Since the lateral TSVs in the bundle (TSVs to the North, South, East and West of the victim) contribute the majority of the capacitive coupling present in the bundle, it is possible to use these lines as shields such as is practiced in on-chip interconnects, as shown in Figure 39.

Figure 39: Shielded lateral TSVs in a 3×3 bundle.

This effectively eliminates the majority of the coupling and allows for higher bit rates through the device. The eye diagram in Figure 40 below has the same input pattern, bit rate and parasitics as the 10 GBPS example above but uses the lateral lines as shields. It is clear that that shielding has opened up the eye and reduced the delay variation significantly. The drawback of course is that although higher bit rates can be achieved, significant area loss occurs due to the unusable grounded lines. Investigation into optimal configurations for TSV sizing, spacing and shielding has to be performed to determine the best configuration for the highest bandwidth achievable in a 3-D IC.
3.2.F  Incorporation of IBIS model of DRAM Driver

This section of the report incorporates an IBIS model [15] of a Qimonda 256Mb DDR2 SDRAM HYB18TC256 driver [16] to represent the use of IBIS models in relevant simulations. With an accurate model of the actual drivers and receivers, application specific simulations can be carried out to determine signal integrity, driver sizes and strengths, repeater insertion strategies, and power consumption and delay estimates for various signalling situations.

The I/O_NORMAL_MODE model is used from this DRAM IBIS file to drive the TSVs in the same configuration and parasitic setup as in the cascaded 10 TSV example in Figure 28. The DRAM driver is driven by a 1.8V input and the resulting waveforms are plotted in Figure 41.

As can be seen in this figure, the DRAM I/O buffer has a much easier time coping with the 10 layer TSV load than the 10x inverter used in previous simulations. This simulation was simply carried out to demonstrate the
incorporation of actual devices that can be used in simulations with TSV interconnects. As mentioned previously, by using IBIS models a more accurate analysis of the system can be carried out, such that recommendations can be made concerning driver sizing, repeater insertion, power consumption and delay metrics.

4. Dissemination

The dissemination plan for this work is outlined below:

<table>
<thead>
<tr>
<th>Journal/Conference</th>
<th>Content</th>
<th>Full reference</th>
</tr>
</thead>
</table>

5. On-going Work

As outlined in the ELITE Description of Work, the modelling and simulation methodology should incorporate estimation of signal integrity, performance, power and thermal behaviour of 3-D ICs. Power and Thermal analysis, Power and clock Network design and analysis, and substrate noise coupling is currently under investigation by LU and KTH, in collaboration with other ELITE partners. Additionally, circuit level signalling conventions suitable for TSVs will also be examined, following on from the preliminary analysis based on full-swing voltage-model signalling carried out in Section 3. The outcome of these works will be delivered in future deliverables namely D2.3, D2.4, and D2.5.

6. Conclusions

This document details a methodology using dimensional analysis for the generation of compact closed-form equations for modelling resistive (R), inductive (L) and capacitive (C) parasitic parameters of TSVs in 3-D integrated circuits, starting from an isolated TSV and proceeding to a 3×3 bundle. Compact models are useful in system-conceptual level explorations of 3-D ICs. Specifically, the models proposed in this report can be used for prediction of parasitic parameters for comparison of performance and signal integrity related metrics at the system level. In particular, the ability to predict parasitic parameters including all coupling components for a bundle is of great benefit, and a contribution to the state of the art in this field.

The proposed electrical circuit of the TSV with parasitic parameters estimated by the compact models have been used in circuit level simulations to determine their effect on signalling over TSV interconnects in various likely configurations from an isolated via to a 10 layer stack of a 3×3 bundle. Inductance and resistance were shown to be less significant in the considered switching patterns and waveforms, while the capacitance was shown to be very significant. The conclusion drawn from these simulations was that a TSV could be modelled by its parasitic capacitance for signalling down to rise times of tens of ps. Tests were then carried out to determine if the via should be treated as a lumped or distributed model. The simulations performed led the authors to believe there is no significant advantage in segmenting the model.

Further, crosstalk effects between TSV structures in a 3×3 bundle were examined. The contribution from capacitive coupling is greater than that from inductive coupling to the extent that inductance can be ignored in some cases. Crosstalk effects were shown to be significant in a 3×3 TSV bundle, and thus must be included in
any 3-D interconnect simulations. Various simulations were carried out, showing the effects of most relative bit patterns of interest in a TSV bundle. Shielding the adjacent TSVs in a bundle can significantly aid signal integrity and allow faster signalling speeds. The methodology and test bench used in the experiments described in this report will be augmented with system specific information, such as IBIS drivers and receivers, desired bit rates, and other signalling conditions in generating the pre-fabrication behaviour model of the prototype. When such information is available a more accurate and coherent analysis will be performed.

This document also serves to record what has been carried out by LU and KTH, in order that this work may be aligned with the work that has been carried out by other partners. It is a goal to compare the simulated and predicted values against measured values for the actual technology at the end of the project.

7. References

[16] Qimonda DRAM driver IBIS model. [Online.] Available:
http://www.qimonda.com/download.jsp?ref=qis_docs/Simulation%20Models/IBS_HYB18TC256xx0BF_rev110.zip