Extended Large (3-D) Integration TEchnology

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Abstract

Final report of the ELITE project.

Keywords

3-D Integration, flash memory, Integrated Circuit (IC) design, microcontroller, trough silicon via (TSV)

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Publishable Summary Report

Executive summary

The principal goal of the **E**xtended **L**arge (3-D) **I**ntegration **Te**chnology (ELITE) project is to explore 3-D integration by means of vertical integration of a multitude of dies. From a fabrication point of view, this requires investigation of a variety of concepts for implementation of vertical interconnects as well as assembly of the composite structure with controlled stress on the components. The main objective is to identify the strengths and weaknesses of the different approaches and make a prognosis for the future, by providing an integrated technology solution. A further goal is to evaluate different physical topologies and system architectures for the combination of processors and memory to develop an overall architectural solution which ensures that applications get the true benefit of the physical technology. Finally, it is also an objective to explore means of bringing more processing power into memory systems by evaluating related concepts and architectures. This will enable higher storage density and higher storage reliability as well as intelligent power management. This will enable advanced forms of data management and data retrieval for future applications, where processing massive amounts of data at a high speed and with high reliability is essential.

Project Context and Objectives

Introduction

The semiconductor industry has been sustained over the past four decades by the step change in functionality and performance from one technology generation to another, afforded by the shrinking of device dimensions that simultaneously increases the speed and reduces the energy and footprint of a binary switching transfer, the canonical digital computing operation. A hierarchy of reasons related to fabrication and device operation impose fundamental physical limits on how small a transistor can be made and still operate as a transistor. Additionally, the fact that communication across a die consumes an increasing number of clock cycles – up to 40 or more in high performance microprocessors – and increasing design complexity have posed severe challenges in maintaining the exponential increase in performance and functionality seen over the previous two decades.

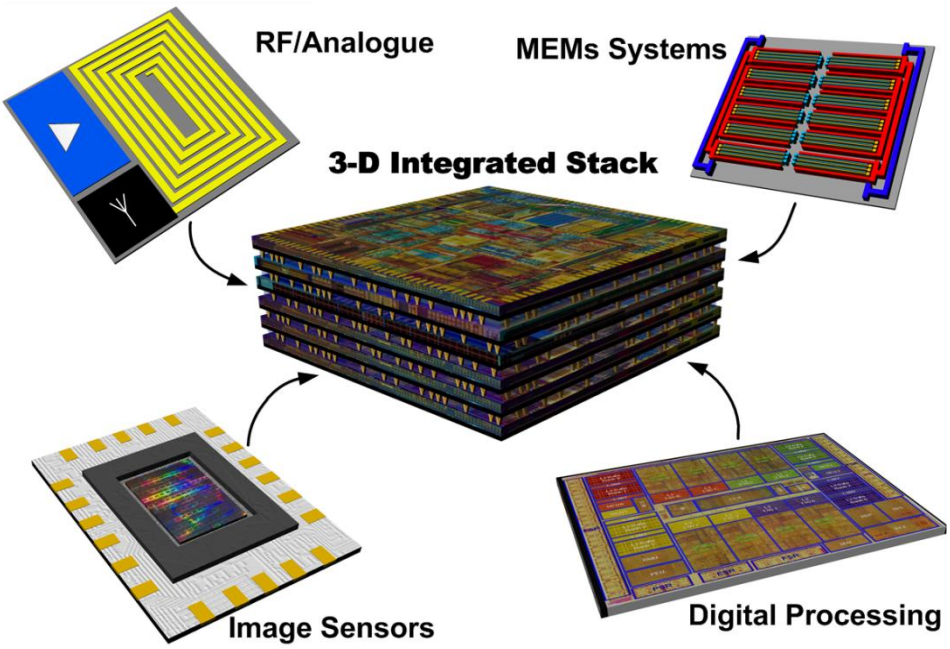


Figure 1 - Stacking dies allows a single package to integrate a heterogeneous mix of functional elements. The electrical characteristics of the TSVs and reduced form-factor of a 3-D package enables scalable performance for the future.

The end of Moore law scaling however does not necessarily spell an end to the era of a big jump ever so often, due to a new design paradigm in digital electronics, 3-D integration. While 3-D integration has been used in the MEMS industry for 20 years or more, the possibility of utilizing the third dimension for massively integrated digital and mixed-signal systems by wafer- and die-stacking is very new, and a very important technology for the future of the semiconductor industry. Our focus here is the potential of 3-D integration in high performance digital systems incorporating low-cost high-density memory. In this context, in addition to the obvious advantages in terms of the available die real estate, key to the performance and energy benefits promised by 3-D integration is the communication over the vertical interconnections, called through-silicon-vias or TSV for short.

ELITE Project Objectives

The principal objective of the ELITE project is to develop die stacking technology and concretely analyze the behaviour and performance of future 3-D die stacking architectures. The performance gap between logic and memory is exacerbated by unfavourable on-chip wire delays and “out-of-package” interconnect transactions. The parasitics of TSV interconnects are much less than the longer 2-D global wires and off-chip traces, acting more like the local interconnect where resistive and inductive parasitics are virtually negligible and the capacitance is minimal. These properties make the TSV electrically fast and attractive to designers, which is what will enable greater signalling performance in 3-D TSV-based technologies and drive further improvements in future integrated circuits.

The principle objectives of the ELITE project are summarised as follows:

- Develop die stacking technology based on through silicon vias.
- Create the technology and controller required of a commercial multi-die flash memory stack.
- Model and characterize the behaviour of the TSV interconnect for low-frequency and RF applications under numerous technological and geometrical constraints
- Define signalling behaviour and develop conventions for signalling over through silicon vias.
- Develop thermal models for 3-D die stacked packages.
- Evaluate the communication infrastructure for 3-D ICs.
- Model the impact of 3-D architectures on the efficiency and capabilities of high-performance computational systems.

Technology and Results

This section discusses the technology developed in the ELITE project and the modelling and analysis methodology for the design of 3-D ICs. The TSV fabrication process and die stacking technology was developed in parallel with models for electrical parasitics from the conceptual design of a 3-D flash memory stack (see Figure 2). The electrical models were used to develop signalling conventions for TSVs and assess the performance limitations and efficiency of package technology for multi-die computational systems under numerous physical constraints. Test structures were created to measure the RF and low-frequency behaviour of the TSVs to compare to the models. To control a multi-tier flash system, a memory controller was also developed. Finally, a powerful toolset was created which incorporates all of the models developed in the ELITE project for the thermal, electrical and system-level performance of TSV integrated die stacks.

This section is organised as follows. First we discuss the TSV technology developed in ELITE and the related fabrication steps. We follow by discussing the modelling and analysis of 3-D die stacks and the memory controller. We end with some brief conclusions.

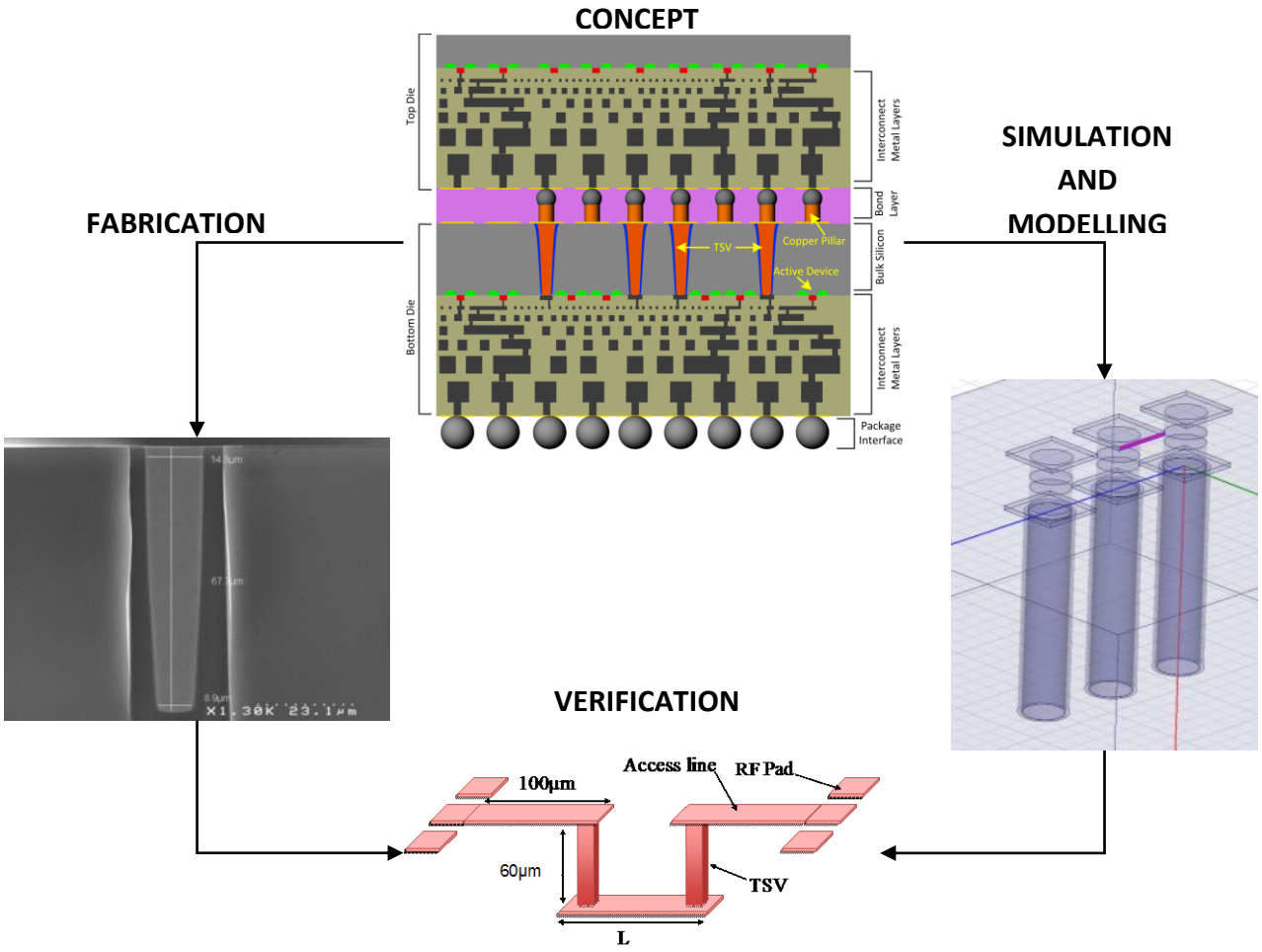


Figure 2 - Development and Modeling of 3-D technology.

TSV Technology

The ELITE project was dedicated to the full development of several technological modules mandatory for 3-D multiple chip stacking. The potential 3-D stacking technology investigated is through silicon via (TSV). A via middle process has been chosen, meaning the TSV's are built after the CMOS process steps and during the global interconnect process steps. The TSV size requirement for this project is tapered from 15 µm in front size to 12 µm in back side. And the targeted final silicon thickness is in the range of 50 µm to 60 µm. As the handling of thinner wafers is very problematic below 100µm, the use of an additional substrate (named here a handle) bonded on top of the wafer is mandatory. The temporary bonding used here has to allow handling of temperature variation in the back side process and the de-bonding step temperature must remain below the maximum storage temperature of the chip.

Technologies that have been addressed are:

- **Through Silicon Via process**: TSV processing including high aspect ratio silicon etching, isolation layer deposition, metal filling
- **Temporary Handle**: low temperature bonding and de-bonding and compatibility with all other processes.
- **Rear side pad reconstitution :** back side alignment lithography, passivation, metallization, pad definition, pad opening and copper pillar
- **Pre applied underfill.**
- **Chip-to-wafer stacking**: a bonding technology has been developed to be able to stack multiple layers.

Process flow has been discussed and the ownership of each technology step has been defined as in the following figure:

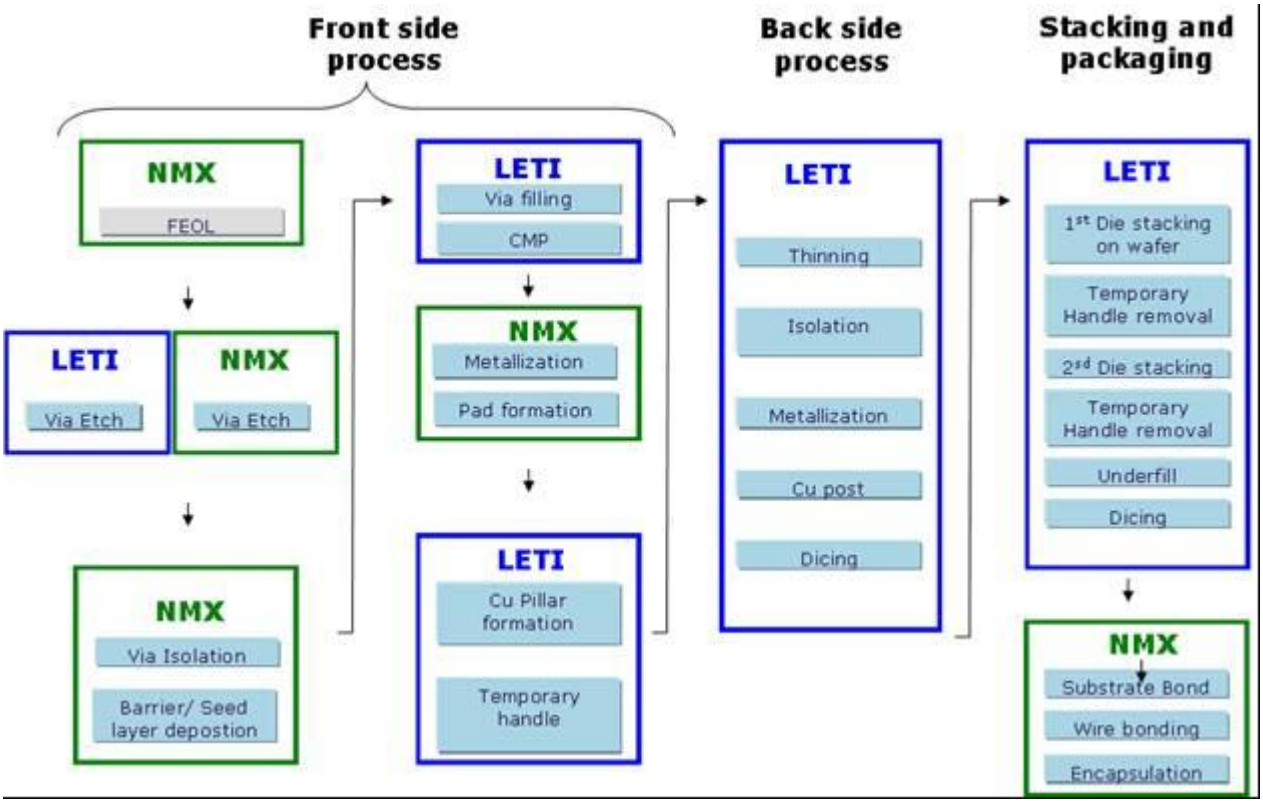


Figure 3 Process Flow for "Via middle" approach

These technologies were individually optimized on dummies wafers and the full process was integrated on test vehicle wafers in order to demonstrate their full compatibility.

The test vehicle consists of two dies (top and bottom die) including TSV and pads redistribution on both sides. These dies are stacked on silicon interconnection network which allows extracting electrical signal on PCB through wire bonding.

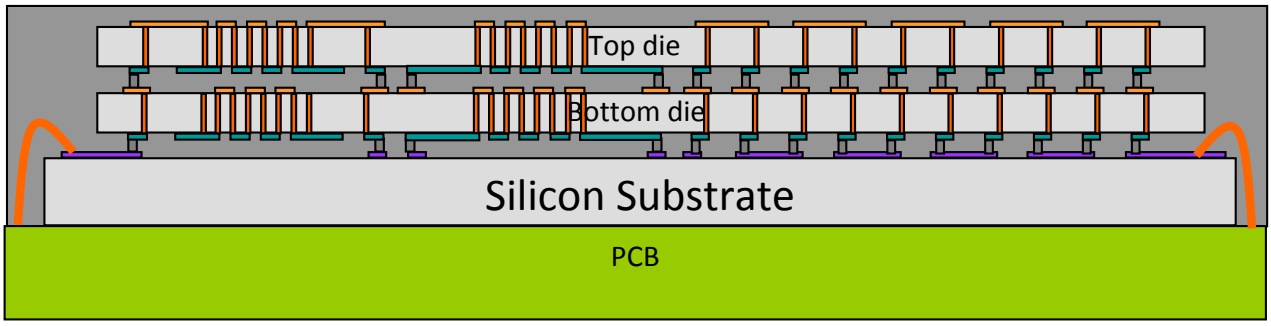


Figure 4 – Test vehicle

Within the ELITE project, a process for TSV mid process has been developed. The process includes via dry etching, via insulation and via filling. Seed layer deposition with good continuous coverage on sidewall and via bottom and filling without voids was demonstrated.

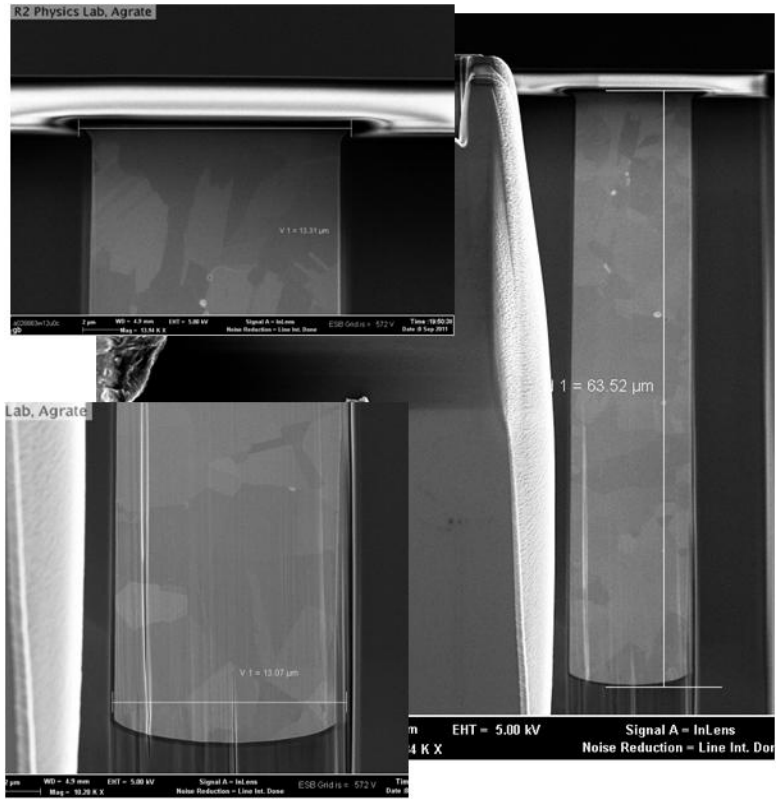


Figure 5 TSV filling of the ELITE test vehicle

As the handling of thinner wafers is problematic the use of an additional wafer bonded on top of the wafer is mandatory. For major developments on going in the CEA LETI, this handle consists of a glass wafer. The transparency of glass allows to align back side to front side during photolithography using metallic patterns visible through the glass on the front side. However, the CTE mismatch between silicon and glass induces a warpage which is an issue for alignment with high accuracy. In the ELITE project the TSV are made from front side and copper cross-sections are revealed during backside thinning.

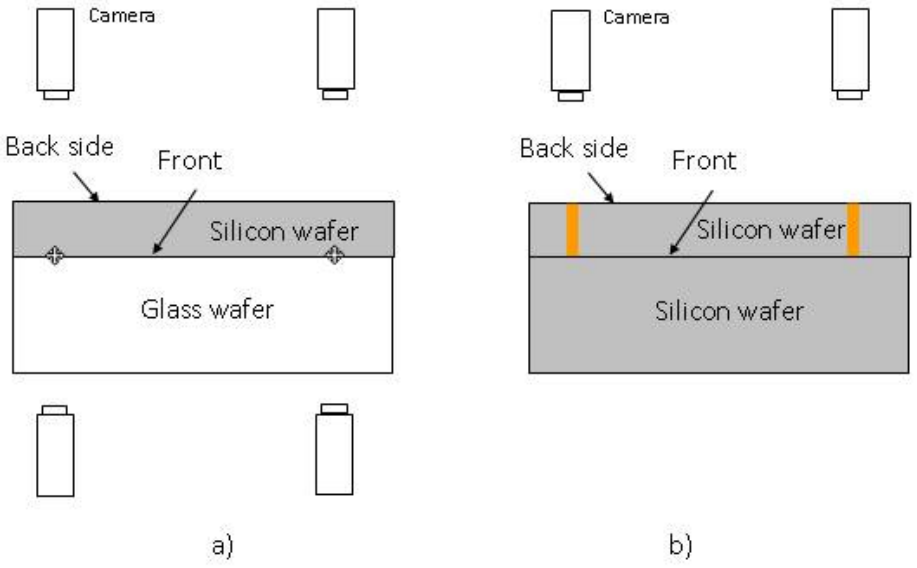


Figure 6 - Backside alignment a) using front side patterns b) using copper cross-section

The wafer back side process in via middle approach for the ELITE project is described in the following figure. A selective silicon etching is performed in order to leave a few µm TSV protrusions and an oxide is deposited before to perform the CMP process and to reveal the copper cross section. This process avoids a lithography step and limits the risk of short circuit between back side RDL and silicon substrate

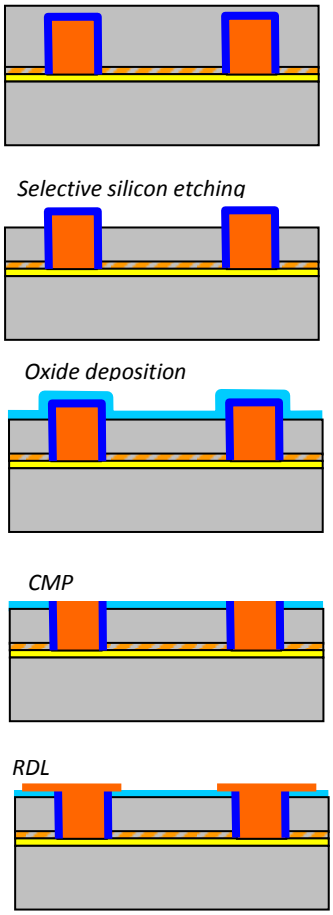


Figure 7- Wafer back side process in via middle approach for the ELITE project

The RDL process has been validated on test vehicle thanks to electrical characterization.

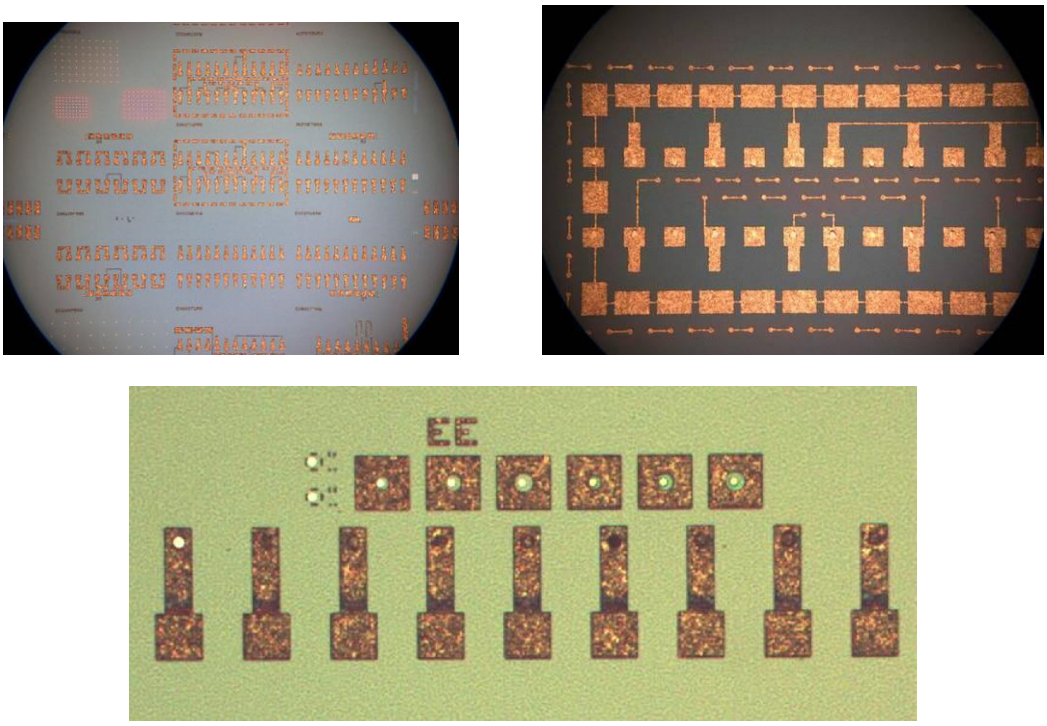


Figure 8 - Copper line and TSV on backside wafer

The test vehicle has been designed in order to characterize the metal properties and connection between front side and back side. Several contact resistance measurements were performed using Kelvin probe structure along a 2, 18 and 98 contact daisy chain. Mappings of measurements are presented in figure 10.

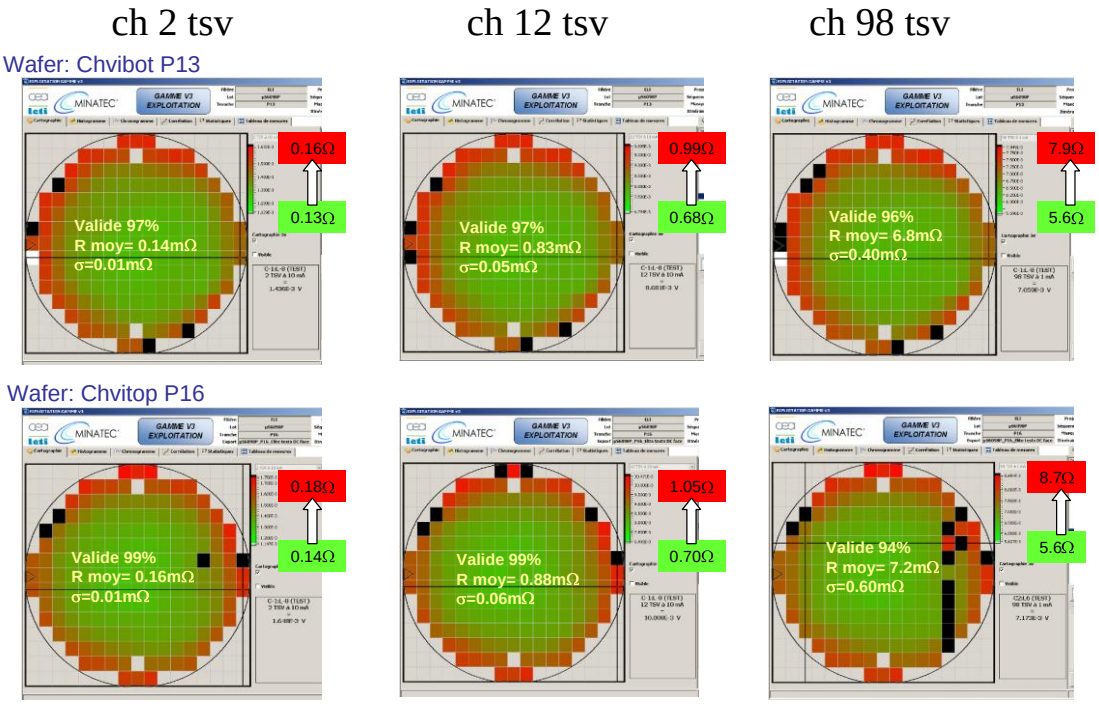


Figure 9 resistance measurements of daisy chains (P13 and P16)

Stacking Technology

For 3D interconnections, the solution chosen in the ELITE project was based on pillars, formed by a copper post on the bottom wafer (only Cu) and a copper pillar (Cu and lead free alloy) on the top die.

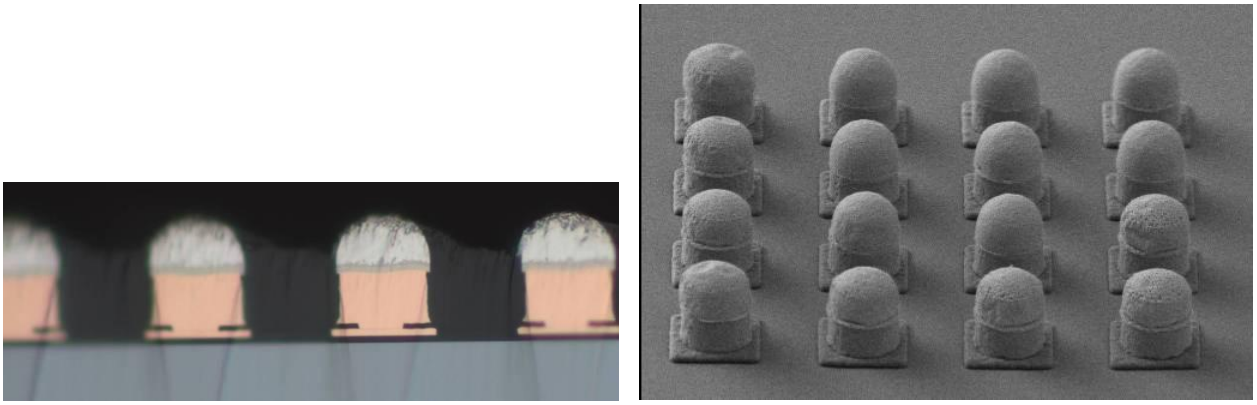


Figure 10 : Pictures of Copper pillar (Cu and reflowed lead-free) on the top chip

In the ELITE project it has been ruled out the possibility to slide off 60 µm thick wafer because of its fragility. The strategy proposed is to release handle after dicing and stacking by chemical etching.

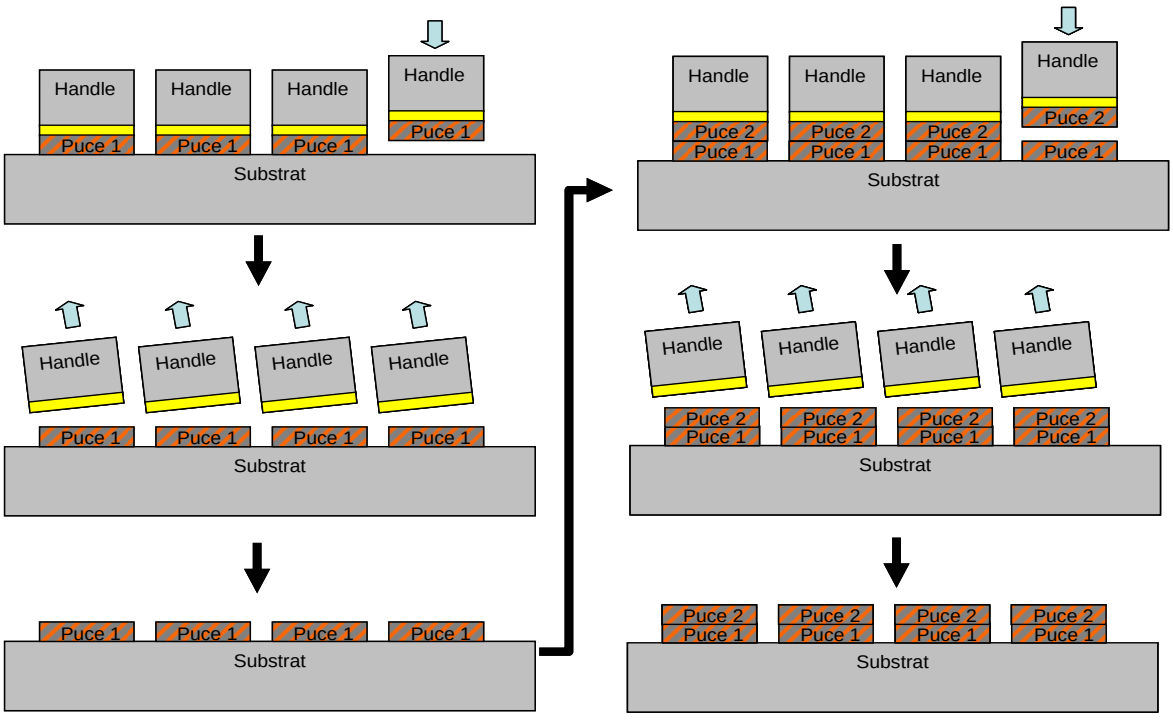


Figure 11 Strategy proposed in ELITE

Dice were stacked on a wafer and a collective chemical process using the HT1010 solvent "WaferBOND Remover" was used to remove the silicon handle.

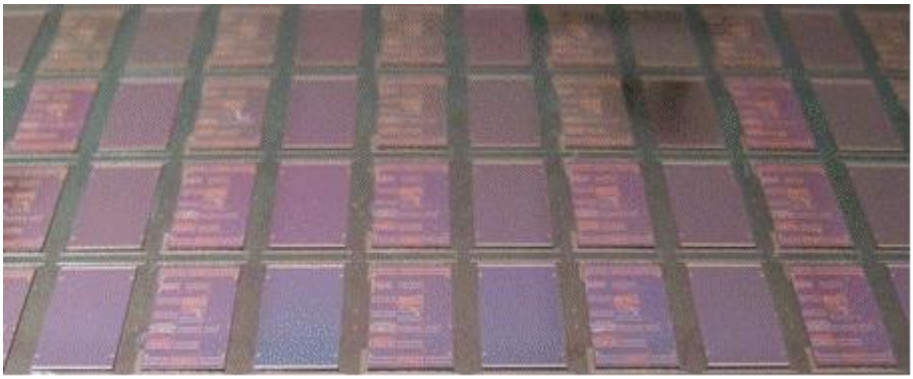
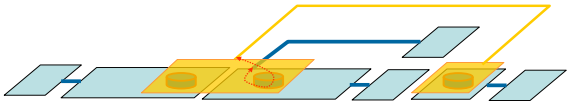
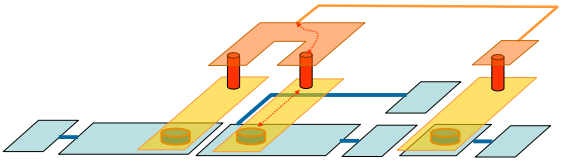
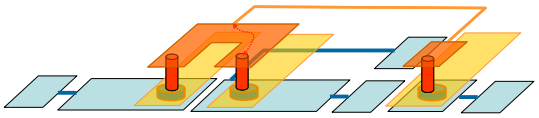
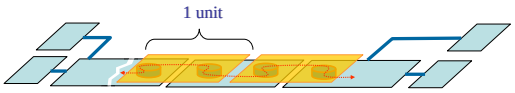
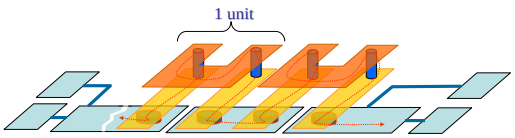


Figure 12 Stacked test vehicle

Electrical Kelvin and Daisy chain structures were measured from the substrate to estimate the contact resistance through copper pillar bump and TSV and results are summarized in the following table.

	R calculated Ω	**R measured Ω**
Resistance of bump + RDL 	-	0.03
Resistance of bump + RDL +TSV 	0.193	0.21 ± 0.03
Resistance of bump + RDL +TSV (TSV aligned to Cu pillar) 	0.108	0.12 ± 0.02
Daisy chain of (Bump +RDL) 	2.489	2.8 ± 0.1
Daisy chain of (Bump +TSV +RDL) 	6.740	6.9 ± 0.1

The average measured values are in good agreement with the calculations. An important result is that there is no negative effect to build the copper pillar directly aligned to the TSV. So, it may be investigated the possibility to omit the step of back side RDL. This could allow a better integration ratio in case of dense routing, and will be part of the future design rules.

Finally, a multi-stacking of 3 dies was carried out. A photo is presented in the figure 14 below.

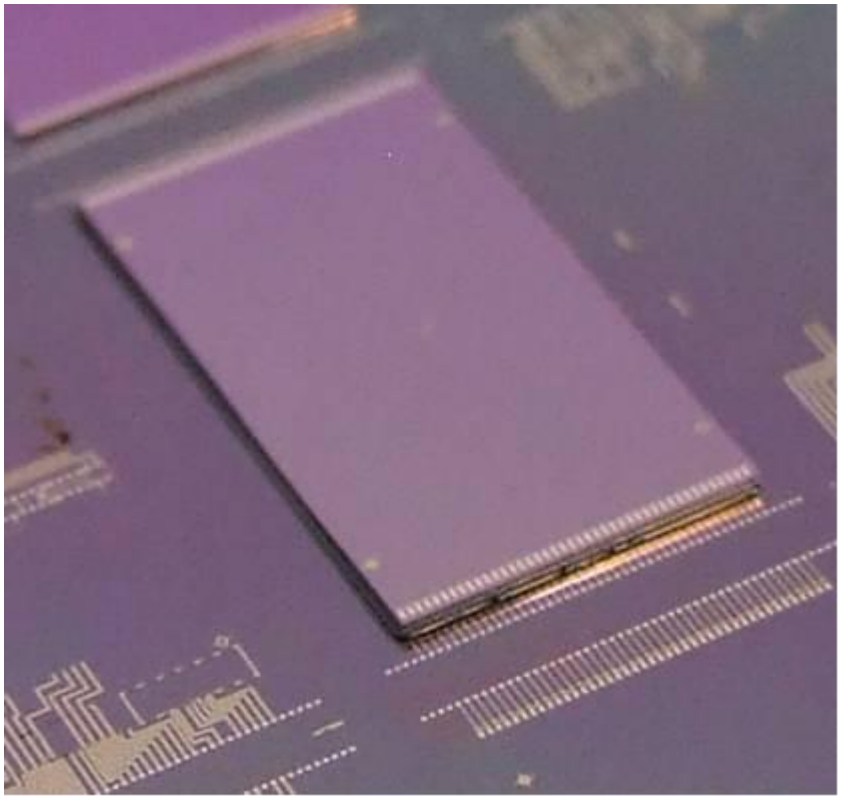


Figure 13 Multistacking of 3 dies

Modelling and Analysis of 3-D ICs

Throughout the ELITE project, we have adopted a modelling and analysis hierarchy that begins at the physical-level and extends to the communication architecture and finally the system-level performance of a full 3-D system. This section summarises the achievements and models developed throughout the course of the project, which is separated into five distinct areas:

- electrical modelling of a range of TSVs;
- signalling conventions for 3-D die stacks;
- thermal models for integrated circuit packages;
- communication infrastructure for massively parallel and stacked systems;
- system-level performance of 2-D and 3-D computational units.

Electrical Modelling of Through Silicon Vias

The physical processes by the which the TSV is fabricated differ considerably, based on the type of bonding to be carried out, such as wafer-to-wafer or die-to-wafer, and the order in which TSV processing takes place with respect to the processing of the active layers and interconnect stack, such as via-first, -middle and –last. These different schemes have different limitations associated with them, related to thermal budgets, alignment accuracy, and the material and density of the TSVs. Hence these choices are driven by constraints related to system-level performance and cost.

In spite of the myriad ways of fabrication, a representative structure for a TSV in most processes that promise a high density (greater than 106 vias per square micron) is a copper or tungsten via having a uniform circular

cross-section and an annular dielectric barrier (usually SiO2) surrounding the conducting cylinder. There is also usually a very thin (approximately 10 nm thick) layer of material acting as an etch-stop between the Cu/W and the dielectric layer, with TiN being a common choice. TSVs can also be placed electrically far apart, with no significant coupling to neighbouring vias, within a row with coupling to two nearest neighbours or within a bundle with coupling to eight neighbours. These topologies are sketched in figure 15.

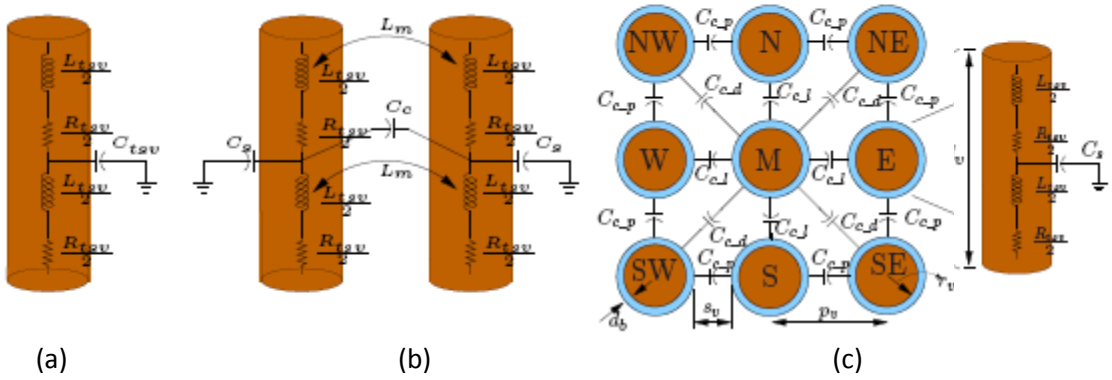


Figure 14 TSV structures connecting adjacent wafers have different electrical properties depending on proximity to other TSVs: (a) an isolated TSV, (b) two coupled TSVs, and (c) a TSV bundle

The key point in analyzing signal propagation over TSVs and the associated power/energy consumption is the ability to abstract the physical structure by an electrical circuit valid for the mode of propagation. To this end we have modelled all of these likely structures for copper, and present closed-form equations to extract resistive, capacitive and inductive components including coupling terms as a function of the TSV geometry. This has been achieved by simulating all structures in a 3-D/2-D quasi-static electromagnetic-field solver specifically used for parasitic extraction of electronic component. These extracted values are functions of the structure's geometry and the material constants. The underlying variables have been combined into dimensionless quantities according to the principles of dimensional analysis in order to reduce the number of independent variables where possible, and joined in functional forms suggested by insight into field theory and empirical validation.

RF Modelling of Through Silicon Vias

To model the high-frequency behaviour of the TSVs a dual via chain was constructed in simulations and on test wafers consisting of two transmission line segments and two TSVs separated by a BRDL (Back Redistribution Line). The Dual Via Chain characterisation gives the scattering matrix (Sij) of one TSV, after a specific calibration and de-embedding operation. The measurements were compared to 3D simulations using a full wave 3D software suite. A SPICE-like model was then extracted with frequency dependence for R, L, C and G parameters (see figures below for details).

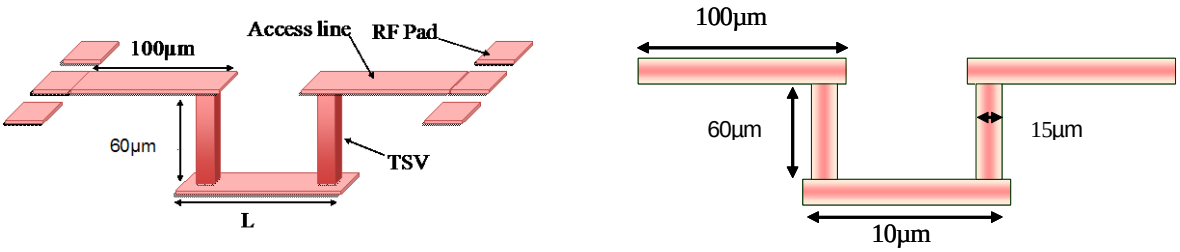


Figure 15 - Description of the dual via chain for high density TSV

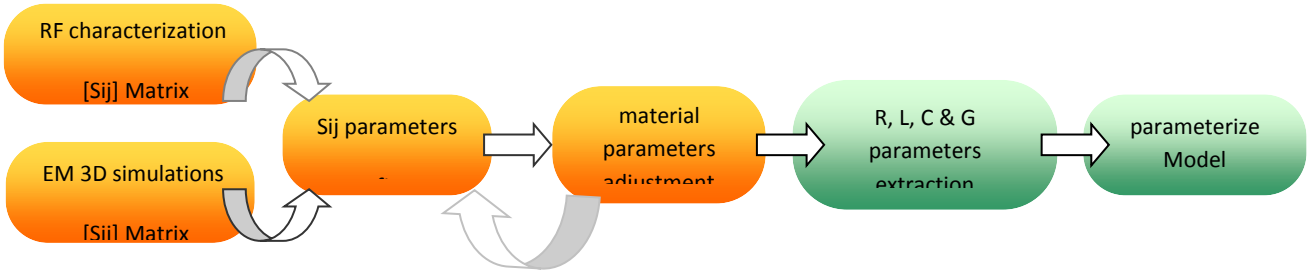


Figure 16 - Methodology for RF modelling of TSVs

Model usage

These TSV models can be used for equivalent circuit formulation when calculating performance, signal integrity (SI) and power integrity (PI) related metrics in design space and architectural explorations of 3-D ICs with good accuracy. What they reveal is that the TSV has a delay and energy comparable with local interconnects, providing the possibility to stack modules with high data interconnectivity on top of each other, greatly reducing the cost of global communication, including removing off-chip transactions. The parasitic models for TSVs in various coupled configurations have been packaged as a web-enabled tool (see figure 18).

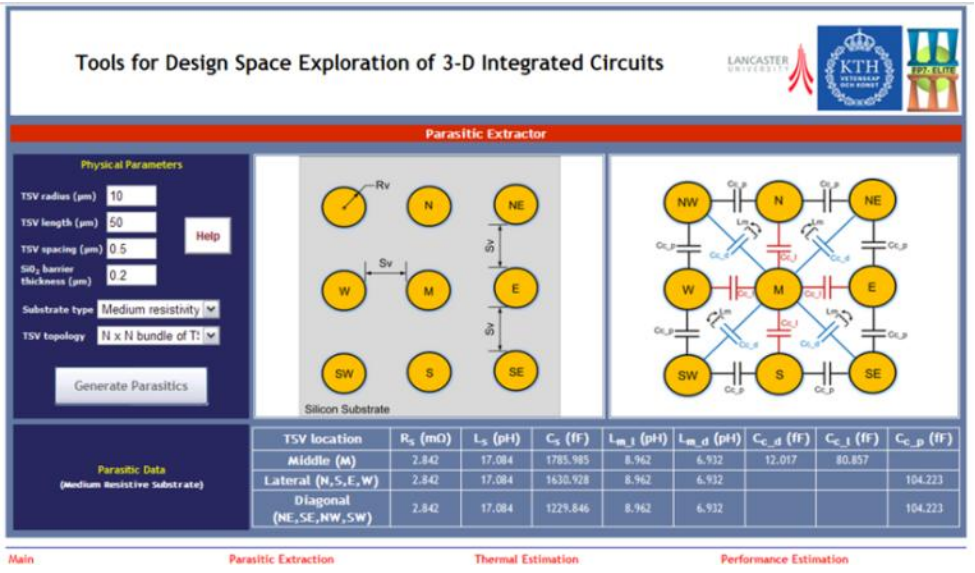


Figure 17 - TSV parasitic extraction tool

Stacking dies provides the opportunity to continue the exponential growth of transistor count by doubling the number of layers with every generation. Some applications with obvious benefits are high performance systems where DRAM or Flash can be stacked on top of the processor core, potentially reducing both the latency and energy of a memory read/write operation by up to several orders of magnitude. At the architectural level, this means a fundamental shift away from the interconnect centric nature of high performance system design. With an architecture that matches the physical peculiarities of 3-D ICs, namely the shorter average interconnection length and the reduced latency and energy over the vertical

interconnects, continuous improvements in performance that we have come to expect with technology node changes are possible.

Signalling over Through Silicon Vias in 3-D die stacks

The shift to 3-D TSV packaging and potentially higher data-rates on-chip opens up a new topic of interest to digital IC designers: What is the best way to send information over multiple chip layers? In this work, we aim at answering this question by evaluating several common signalling circuits to develop further understanding of signalling conventions for 3-D ICs. We conduct SPICE simulations using a 65 nm CMOS technology for Voltage Mode (VM) with and without shielding, Low-Voltage single-ended (LVSE), Current Mode (CM), and Low-Voltage Differential signalling (LVDS) to extract performance information in terms of delay, energy, area, and signal integrity.

Voltage Mode

Rail-to-rail CMOS Voltage Mode signalling is the most widely-used and familiar signalling convention in digital ICs. In its most basic form, the driver consists of a simple inverter, in which the channel widths of the PMOS and NMOS transistors are sized to be several times larger than a minimum-sized transistor. The sizing relates directly to the drive strength of the output signal. The size of the driving inverter, HD, usually depends on the parasitic resistance, inductance and capacitance of the transmission medium and any minimum delay criteria. For on-chip and off-chip planar wires, these parasitics can be significant, thus the driver size can be hundreds of times larger than a minimum-sized inverter to meet the required delay constraints. Increasing the size of the driver comes at the cost of more active area and dynamic energy.

In our Voltage Mode simulations, we choose a mid-range energy-delay trade-off by sizing the driver to 50 times the minimum-sized inverter. We simulate a row of three TSVs where the centre TSV is considered the victim, from which we measure the performance metrics, and the two adjacent TSVs serve as aggressors.

Shielding

Parasitic coupling between TSVs is certainly of concern, as the delay and signal integrity of any of the vias in a row or bundle is dependent on the switching pattern of its surrounding neighbours. The capacitive coupling between TSVs dominates the signalling behaviour and the inductive coupling can be neglected for signalling in CMOS circuits due to the comparatively large parasitics of the output drivers, which mask the small RL properties of the TSV. Coupling between wires can be dealt with in a number of ways, such as intelligent driver circuits, encoding, or programmed delays. The most simple and common technique to mitigate coupling effects however is to shield signals by interspersing ground wires between signal wires. In our Voltage Mode simulations we consider a shielding scheme where every other TSV in a row is grounded at both ends to reduce the effect of capacitive crosstalk. The cost of shielding is increased area, of especial concern in 3-D ICs.

Low-Voltage Differential Signalling

The effect of crosstalk can be detrimental to high-speed applications, where clock frequency requirements are tight and signal integrity is of principle concern. One signalling mode designed to reduce the effect of crosstalk is low-voltage differential signalling. This technique can eliminate common-mode noise by sending the reference signal with the data signal differentially. We simulate an LVDS circuit which uses inverters and low-gain output on the driver side to produce a differential low-voltage transmission over two TSVs. The output is recovered and restored by a differential sense amplifier. The main advantages of LVDS are increased noise immunity due to the differential output and decreased noise emission, hence reduced coupled switching effects. However, these advantages come at the cost of increased energy consumption due to the complexity of the circuit and increased area from the additional TSV per signal.

Low-Voltage Single-ended

We also consider a low-voltage single-ended transmitter and receiver circuit which requires only one TSV. This circuit reverses the position of the PMOS and NMOS transistors in an inverter such that the driver output is either a weak '1' or a weak '0.' This type of signalling mode is typically used in low-power applications. This circuit's main advantages are reduced energy and emitted noise at the cost of increased circuit complexity and higher delays.

Current Mode

Finally, we consider a current mode circuit to drive signals over TSVs. The configuration is much the same as the voltage mode case, with an inverter sized to 50 times the minimum inverter as a driver, however there are two additional transistors on the receiving end to form termination resistance on the TSV between V_{DD} and ground. This effectively forms a potential divider on the output signal, which reduces the voltage swing of the transmission. The size of the termination transistors, called H_R, directly controls the swing of the signal, and hence the time it takes for the driver to charge the interconnect capacitance. The current mode circuit in this work can reduce the delay of the output drive significantly, but at the cost of high static power consumption.

Performance characterization of 3-D ICs with TSVs

The driver circuits were each given the same stimuli, with controlled worst- and best-case switching patterns and induced random bit patterns through the victim and aggressor TSVs. The energy-per-bit, delay, and signal integrity characteristics were extracted directly from spice simulations. Eye diagrams for each signalling scheme shown in figure 19 dictate delay variation by the horizontal opening of the eye and signal integrity effects such as coupled noise amplitude relating to unwanted undershoot and overshoot characteristics. Figure 19 shows the worst- and best-case delay from the switching patterns in a row of TSVs for each scheme.

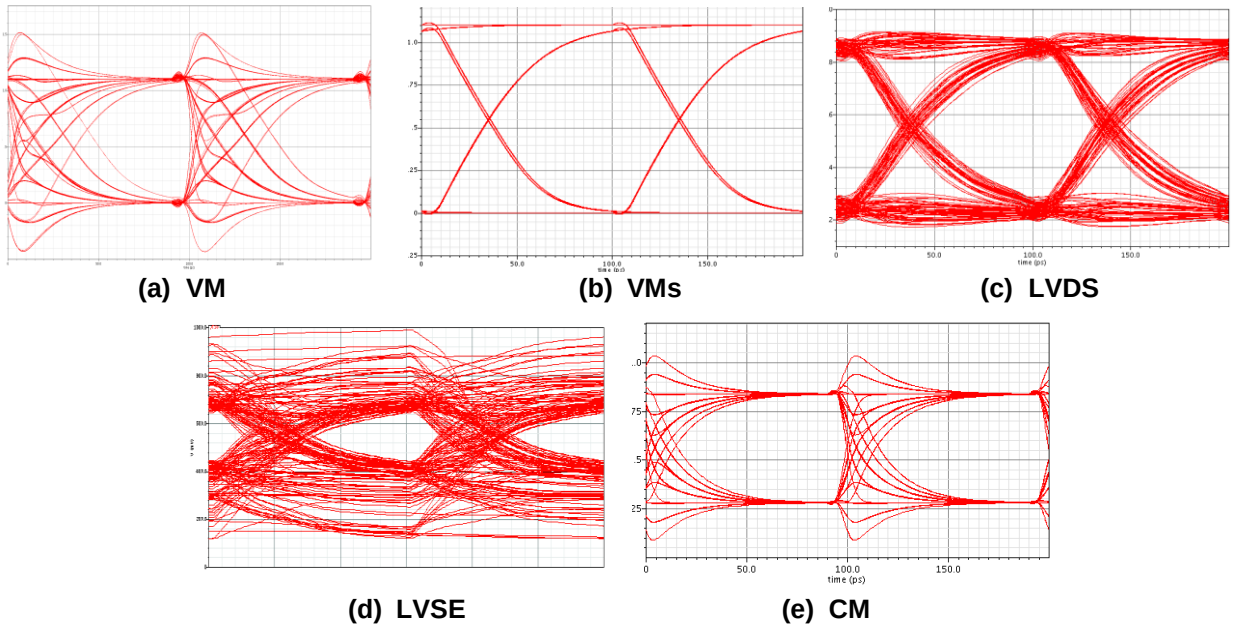


Figure 18 - Eye Diagrams extracted from the TSV (between the driver and receiver) showing delay variation and signal integrity for (a) Voltage Mode (b) Voltage Mode Shielded (c) Low-voltage differential (d) Low-voltage single-ended and (e) Current Mode

Using the representative 65 nm CMOS technology, we have shown that CM signalling can provide a higher data-rate than all cases, although at a cost of higher power consumption. LVDS signalling maximizes noise rejection and benefits from minor delay variation but at the cost of greater power and an additional TSV per

signal link. LVSE signalling can improve power consumption significantly, but suffers from higher delays. The signalling speed and noise over TSVs can be significantly improved with VM shielding but at a loss of area for grounded TSVs. However as can be seen from Table I, this results only in a relatively small drop in data-rate, implying that shielding may be a simple and effective strategy for improving noise resilience while maintaining a high bandwidth if the application is able to utilize the higher data rates. An ideal situation is if the shield wires comprise existing power and ground lines are interspersed with signal lines.

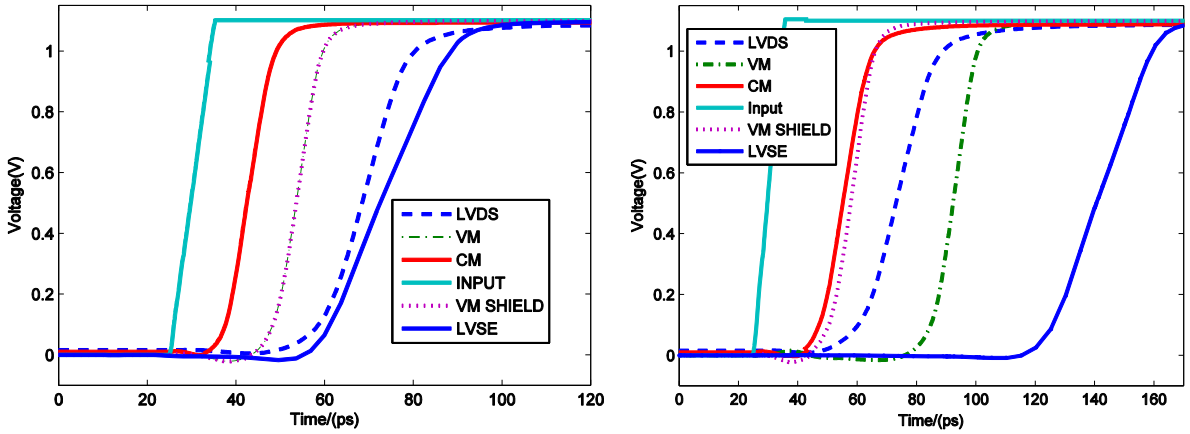


Figure 19 - Best and worst-case coupled rise times for CM, VM, VM shielded, LVDS and LVSE signaling schemes. Cs=3 fF and Cc=89 fF. Worst-case occurs when both adjacent TSVs switch simultaneously against the center victim TSV. Best-case occurs when all TSVs switch in the same direction.

As with on-chip signalling over planar wires, conventional rail-to-rail voltage mode signalling with inverters represents a simple and effective scheme with a reasonably high performance for a low-energy and area footprint, with all other schemes trading off one or more of the metrics of speed, noise, power, energy and area to achieve an improvement over the rest. The quantification of these trade-offs provides guidelines for 3-D Integrated Circuit designers to build their application around the performance of various signalling schemes for TSVs.

Table I - Data rate and energy consumption for VM and CM signalling techniques

Scheme	Configuration	Data rate (Gbps)	Normalised Energy per Cycle	Coupled Noise Amplitude (mV)
VM	Signal-Signal-Signal-Signal	18	1	612
	Signal-Ground-Signal-Ground	17	1	0
CM (With various receiver sizes= H_r)	5	20	1.8	471
	10	22	2.52	427
	20	27	3.78	357
	30	31	4.80	303
	40	36	5.63	259
	50	40	6.27	220
LVDS	Signal Pair – Signal Pair	11.2	7.8	68
LVSE	Signal-Signal-Signal-Signal	7.3	0.62	162

Thermal Modelling of 3-D Packages

The thermal limitations of packages are of great importance to the overall performance and reliability of an integrated circuit. The thermal behaviour of 3-D die stacks becomes even more important due to the increased power density and reduced access to heat sinks for the middle dies. Under the ELITE project, we have developed a stand-alone thermal simulation tool based on 3-D compact thermal models.

Compact Thermal Models

The thermal behaviour of any system has a close resemblance to the electrical behaviour of a circuit. Figure 21 shows the electrical equivalent components of a thermal model for any physical system. The thermal resistance can be determined from the thermal conductivity of the material, the length, and cross-sectional area of that material. A power source on a die can be represented by an ideal current source and the ambient temperature of the environment is a constant voltage source. The current injected into a node induces a voltage across the equivalent resistance, which can be calculated by the thermal "Ohm's law".

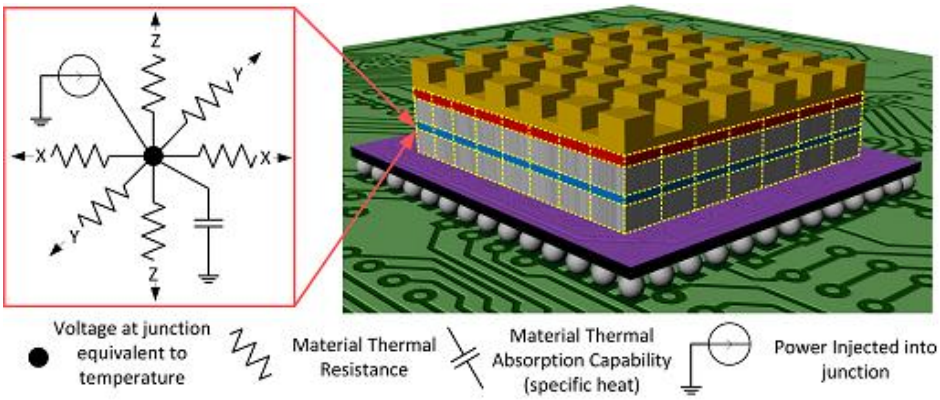


Figure 20 - Electrical Equivalent circuit of a 3-D grid cell for a compact thermal model of a 3-D package.

The specific heat of a material can be modelled as an equivalent capacitance, but in this work we are interested in the steady-state behaviour only. A common quality metric of an IC package is its thermal resistance to the ambient environment or a specific junction. The junction-to-case (or board) and junction-to-ambient thermal resistances are two common resistances provided by a package manufacturer. Alternatively, the two parallel resistances can be extracted from simulations or measurements.

This thermal modelling methodology provides a simple way to calculate the ability of a package to release the heat generated from the die to the outside environment. The thermal resistance in turn can provide the board or package designer with the maximum thermal limitations of that particular package.

Thermal Simulation Tool

We use this well-established methodology to create a fast thermal simulation tool (shown in figure 22) which can enable design space explorations of 2-D and 3-D packages for the early-chip planning phase. The application is written in MATLAB with a custom GUI to accept both user input parameters and power maps. The GUI allows the user to define the inner package dimensions and configuration of the active die or dies (the thickness, area, number of dies in the stack, number and area of TSVs etc.) and the global parameters (ambient temperature, package type, heatsinks). Each chip layer is separated into four discrete materials: the die attach, the bulk silicon of the die, the active layer and the metal interconnect stack. The thermal conductivity of each layer depends on the material, the number of metal layers and the number, size and material of the TSVs.

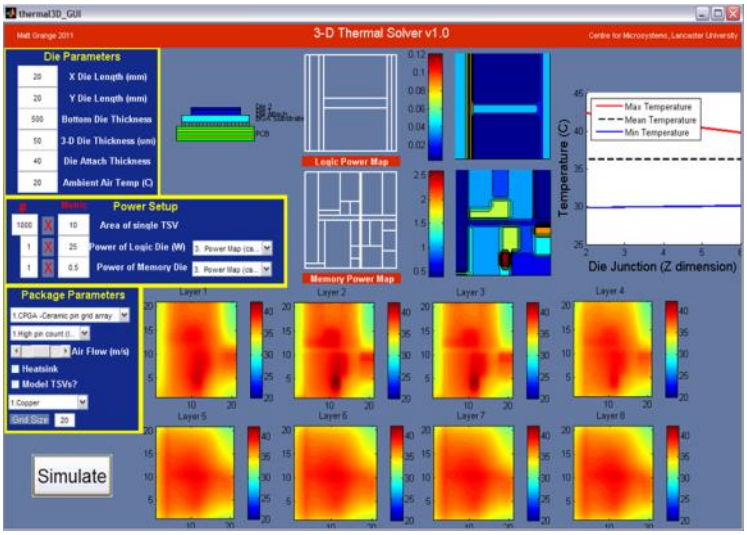


Figure 21 - Thermal simulation tool interface.

Communication Architecture for 3-D Systems

The shift from single-core to multi-core processors has long since occurred and new designs are migrating towards many-core systems. The performance bottlenecks imposed by unfavourable on-chip interconnect delays and congestion in shared buses has finally enabled the packet-switching Network-on-Chip framework to become a viable architecture for high throughput computing. By standardising the communication hardware, multifunctional resources can be seamlessly integrated into a system with the promise of scalable performance for the future.

We have extensively analysed the communication behaviour of parallel systems to optimise the configuration of on-chip mesh networks. We have derived the correct model for average distance in mesh networks and shown how it can be used to optimise the placement of hotspots and configure asymmetric networks under different clocking schemes. We then developed a cycle-accurate simulation model to investigate the performance and scalability of various 2-D and topologies under physical constraints, different vertical communication routing schemes and traffic patterns.

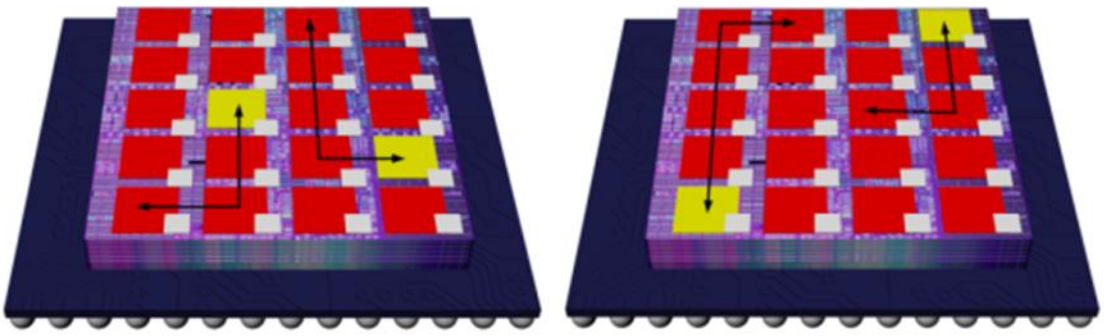


Figure 22 - The model average distance in mesh networks can be used to optimise a large multicore system by exploiting faster vertical links, placing hotspots, and partitioning the nodes to achieve minimum latency in 2-D and 3-D networks.

As a design aid, the average travelling distance in Networks-on-Chip was proposed as a topological characteristic that allows the optimal system architecture to be derived without resorting expensive packet level simulations. Exhaustive simulations reveal excellent fidelity of the metric in achieving the true optimal architecture, 100% for the switching and routing strategy employed.

3-D Router Micro-architecture

Our studies in interconnect level show that TSVs are at least ten times faster than the horizontal wires. Thus there is a possibility of running the system with multi-clock domains where the vertical clock input is separate and faster than the horizontal clock input. Such domain create a condition which exploits the fast TSVs while the horizontal wires are operating in their nominal speed as detailed in. We have used both cycle accurate simulations and analytical models to quantify the performance of 2-D and 3-D networks under multiple constraints to optimise their partitioning, configuration and clocking scheme.

The cycle accurate models we have developed router are pipelined in 3 stage routers implementing a bufferless adaptive routing strategy based on non-minimal deflective type packet switching that is in use in the KTH-Nostrum architecture. A relative addressing scheme is implemented which simplifies the duplication of identical routers when network structures of varying sizes are designed.

3-D Network Architecture: Performance Simulation

A simple example shown in Figure 24a, a total of 64 nodes are used to construct a 2-D many-core processor with 8x8 mesh network topology. Each node is a router connected to a specific resource (in our case a processor) which is fully capable of injecting and ejecting packets. The same 64 nodes can be arranged in 3-D as 4x4x4 cube network topology as shown in Figure 24b. The distance from a source node to a destination node is measured in terms of hopcount.

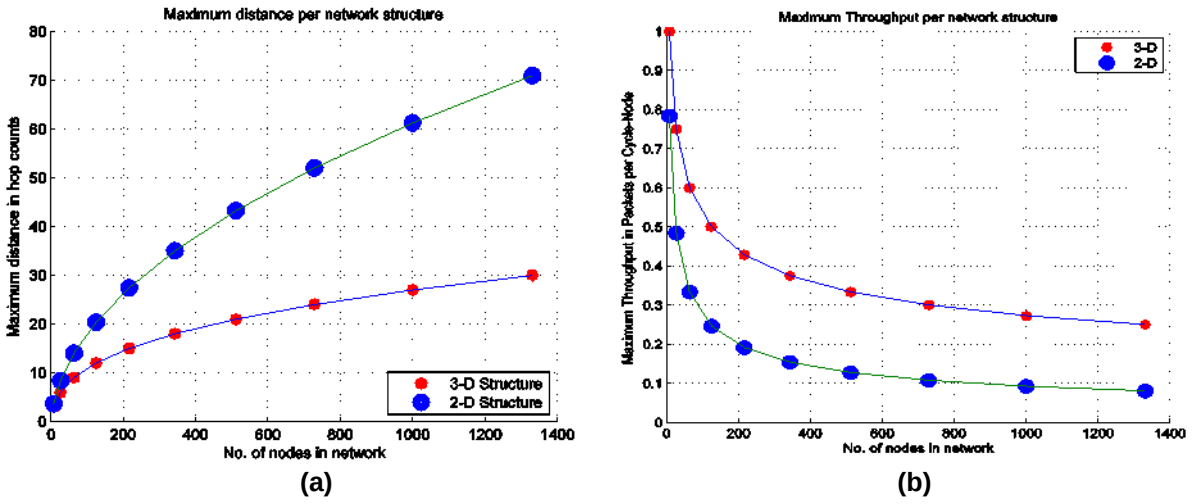


Figure 23 - Scalability of 2-D and 3-D network size (a) Maximum distance and (b) Maximum throughput.

For the same network size, the latency and throughput is shown for 2-D mesh and 3-D cube on-chip network architecture. For small network sizes, the difference is small. But the 2-D network distance increases in higher margin than the 3-D. For example, when 1000 cores, the 2-D distance is more than twice that of the 3-D. The throughput in 2-D degrades to less than 0.1 packets per node when the network size reaches 500 nodes whereas the 3-D throughout is more than twice in the same size.

The addition of vertical links gives the 3-D network architecture a wide performance excellence over its 2-D counterpart in terms of latency and throughput. Also, since the challenges to parallelize communication while scaling up the network size are high, qualitatively and quantitatively, the 3-D on-chip network architecture is

one of best solutions. The trends are now obvious that such architecture will be part and parcel of every system architecture design.

3-D Integration and the Limits of Silicon Computation

The semiconductor industry has relied on the continued scaling down of the transistor size to achieve exponential growth in transistor counts, but this scaling will soon end. As pointed out recently [1], three obstacles stand in the way: the rising costs of fabrication, the limits of lithography, and the size of the transistor. Two other benefits of scaling are reduction in latency and energy consumption of a binary switching transfer, directly attributable to the step increase in performance from one technology node to another. Wires scale less well, and have dictated a multi-core engineering solution for the highest performance processors.

Three-dimensional stacking of dies within a single package presents an opportunity to continue to gain appreciable improvements in performance without technology node shifts, essentially due to the ability to place logic and memory in close proximity, connected through very high speed through-silicon vias and eliminating the memory bottleneck that limits performance in complex SoCs. Moreover, utilising the third dimension allows the number of transistors per packaged chip to bypass the 2-D limit imposed by fundamental material constraints. Finally, economic benefits can be realised by avoiding costly capital investments in new fabrication facilities associated with a new process technology.

We have examined both performance and cost benefits of 3-D integration and quantified them under physical, technological and design constraints. We use an architectural abstraction and a hierarchical set of models that bridge the physical, circuit and computational levels of modelling to show how the computational efficiency of 3-D systems compares with equivalent 2-D implementations within allowable thermal limits and the physical behaviour of devices and TSV and planar interconnects. We conclude that 3-D systems with stacked DRAM can attain 2 to 3 times higher computational efficiency (shown in figure 25) due to lower interconnect power with an increase of 20-30% in performance-per-watt for every doubling of stack height. We also show how the improved energy efficiency (see figure 26) is achievable at a favourable cost.

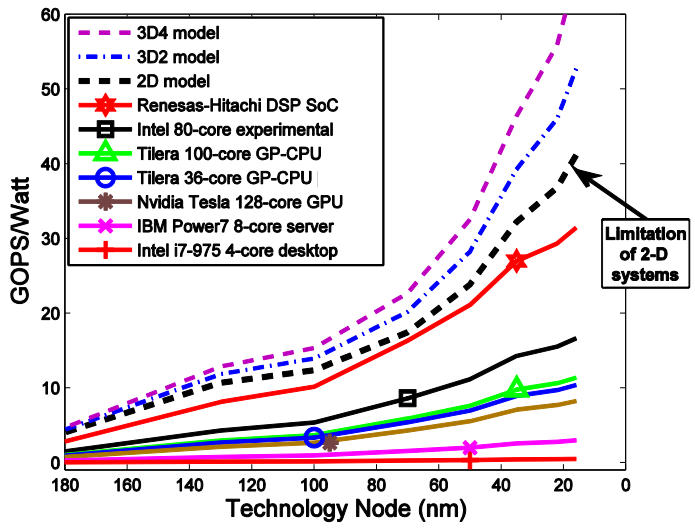


Figure 24 - The Effective Computational Efficiency of recent multi-core processors (where markers indicate actual performance data) compared to our model. The limitation of 2-D systems shown by our model for 2-D computational efficiency is for a specific set of parameters (memory locality, bus width etc.). The model parameters can be altered to represent virtually any system, where the difference between our ideal and the actual implementation is dictated by the efficiency of the control circuitry..

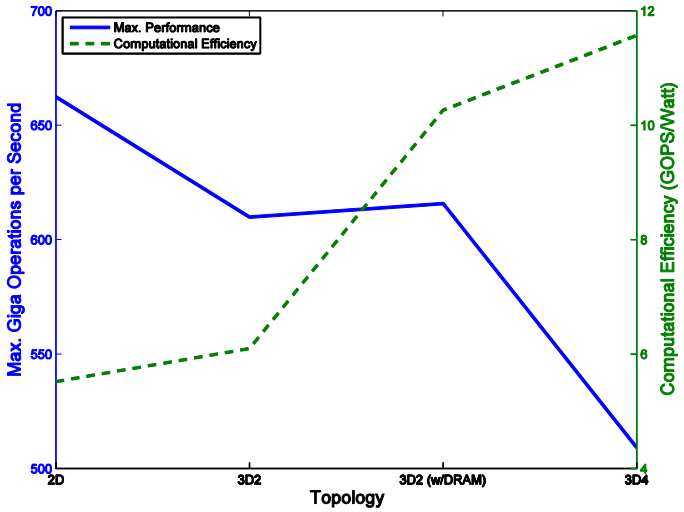


Figure 25 - The performance of different topologies is plotted under a power budget limited by the maximum temperature (TDP) per topology. The computational efficiency (the amount of operations achievable within the envelope of 1 Watt) is also shown.

Controlling a multi-tier Flash system: Solid State Disk Controller Development

A Solid State Disk (SSD) and CompactFlash controller has been specified, logic and analog design has been done. In parallel, the system level application firmware has been development and FPGA verification have been concluded, and finally the first silicon has been produced. A firmware development board as well as Firmware together with reference designs of a CF card and SSD have been developed and manufactured. The products market introduction to customers has started.

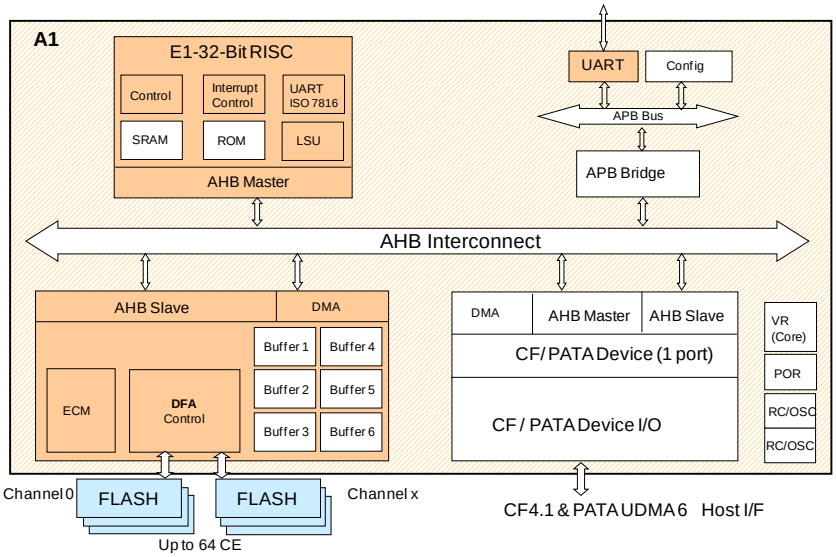


Figure 26 - Block Diagram of Hyperstone A1 SSD and CF Flash Memory Controller

Scientific Achievements Summary

In the frame of this work, technological elementary bricks for 3D integration have been developed such as thin die handling and stacking on wafer interconnections based on Cu pillars technology. Moreover the electrical results obtained on the test vehicle are in good agreement with the calculations. The feasibility of 3D integration technologies has been demonstrated thanks to this project and pathways for improvement were identified.

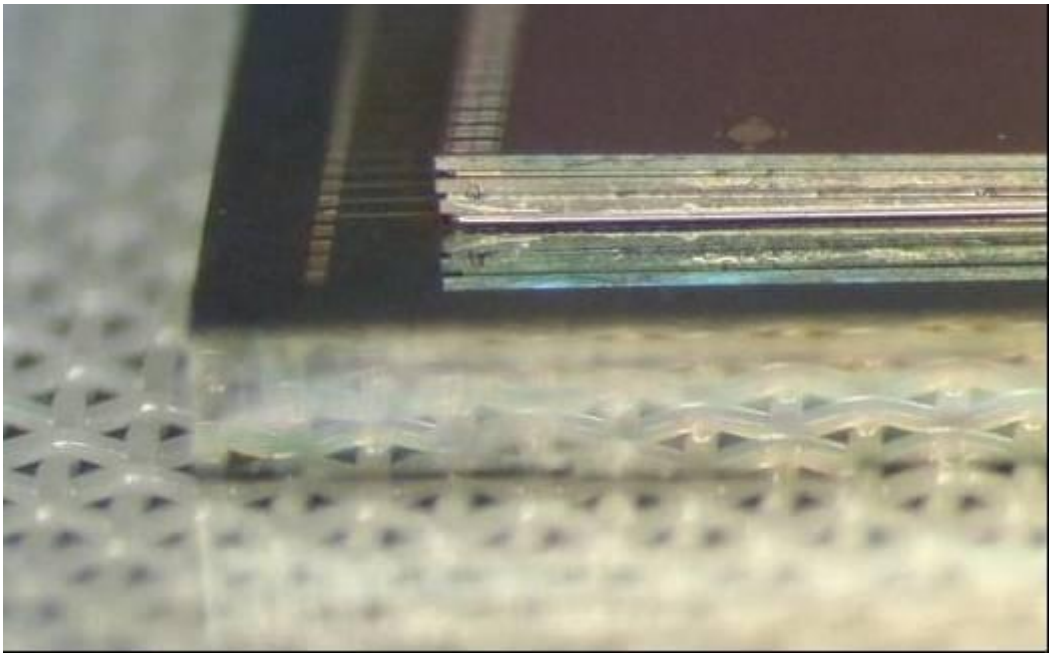


Figure 27 – Multistacking of 3 dies

Measurements and modelling of the TSVs coincide and an SSD and CF controller has been designed and completed. The TSV parasitic parameter models and the thermal estimation models have been made available to the general public via a web portal This initiative has been carried out in order to make the knowledge gained in 3-D IC design in this project available to the wider European community, and increase the benefit of the research carried out in ELITE. A snap shot of the website front-end showing the collection of tools available is given in *Figure 28*.

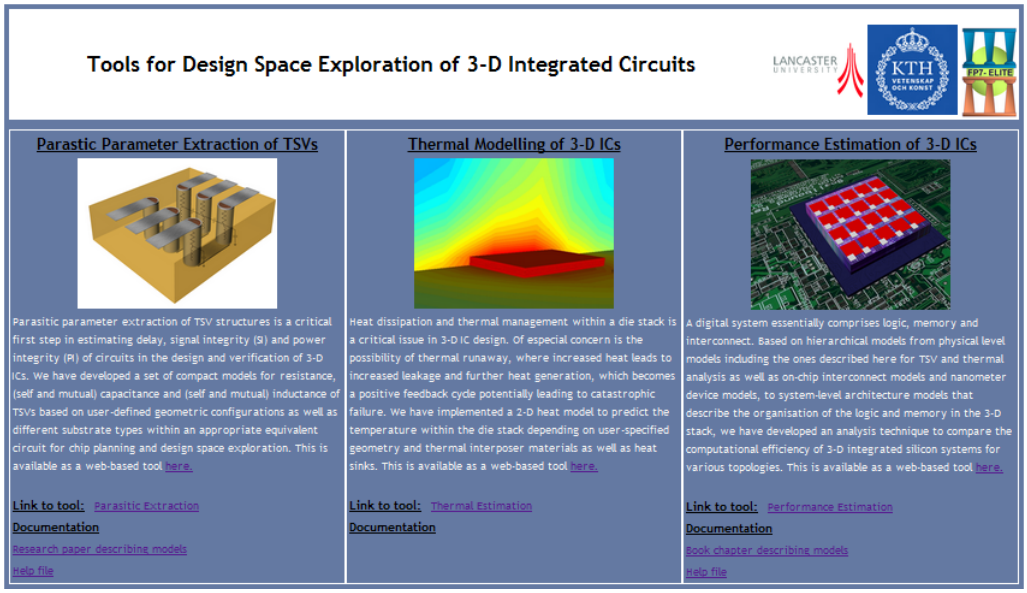


Figure 28 - Web-based tools for parasitic trends, thermal analysis and system performance

Potential impact

The primary objective of the ELITE project is to design flexible and scalable system architecture for 3-D packages that will facilitate design technology for cutting-edge electronic systems. The era of ubiquitous mobile computing has a high impact on European citizens, with diverse, computationally intensive applications requiring massive amounts of cheap, non-volatile memory communicating autonomously. The need for more and more memory is shared by all applications, which impact the quality of daily life in many spheres, including security, leisure, education, and work productivity.

Novel applications can be envisaged in the future, such as storage of one's entire life in a lightweight, low power, small-sized single packaged unit, with real time updates for personal services such as banking, medical information, shopping and entertainment. All these applications require massive amounts of cheap, local, non-volatile storage, the processing power to perform extremely high speed data processing, and a system architecture that allows effective communication to utilise the full potential of the memory and the processors. This project is a first step to providing that complete solution.

Through silicon vias (TSV) represent the most promising high-density interconnect solution for 3D integration technology at the chip or wafer level, to address many of the limitations of current chip-stacking methods. TSVs enable enhanced electrical performances when compared to wire bonding or long on/off-chip wires as a result of the reduced parasitics. This lowers the intra-die interconnect delays, noise-sensitivity and power consumption, enabling high performance, low-footprint designs. In addition, TSV technology enables tight integration of a variety of heterogeneous architectures – such as memory and logic, analogue circuits, signal processing, radio frequency, or MEMs systems. The combination of high-performance electrical characteristics and diverse technologies provided by 3-D integrated packages with TSVs will enable Moore's law scaling to continue for the foreseeable future. There are many promising applications that can exploit the enhanced signalling characteristics of the TSVs and the close integration of disparate technologies, which are soon expected to find their way into commercial products. The memory stacking technology developed in ELITE is one such application.

High-density, low-cost memory is in demand. By bringing multiple memory dies into a single package, both the footprint area and the power consumption can be reduced. Avoiding wire bonding in 3-D stacks by using TSVs can increase the signalling performance and reliability as well as reduce the routing congestion and increase the maximum I/O count. The technology developed in ELITE and the modelling and analysis hierarchy pursued throughout the project has shown promise for 3-D stacked flash memory to increase signalling performance and still operate well within the thermal budget of standard CMOS logic and flash technology. Stacked memory packages are expected to find applications in high-density storage solutions that require high memory bandwidth, such as in solid-state drives to replace magnetic hard disks.

The electrical, thermal and system-level modelling and characterisation activities conducted with ELITE concretely define the impact of TSVs on the physical architecture of a 3-D system. By providing an openly available web-portal to the models, the wider European community can quickly estimate circuit- and system-level performance metrics and insight into a wide range of 3-D topologies and designs, which can significantly aid in the chip-planning phase of a design. Similar works such as CACTI and the predictive technology models for transistors have exhibited a wide impact on the general design community.

The proliferation of multi-core architectures into high-performance processing systems is expected in increase in the coming years. The complete analysis and modelling of networks-on-chip has shown that that 3-D mesh-based processing systems have the potential to provide excellent scalability in terms of bandwidth to meet the demands of future processing applications. Additionally, as a result of the shorter interconnect paths, higher performance can be achieved at lower power than an equivalent 2-D package. These studies have the potential to motivate further development into highly-scalable network architectures for future parallel computational systems.

Commercial exploitation of memories

Stacked flash memory with low-latency TSVs can find applications in most stand-alone memory products such as Solid State Drives and other non-volatile portable media. There is a large interest in the integration of logic and DRAM into Wireless designs. One example is a multimedia processor with direct high-performance communication with its own stacked volatile memory array (DRAM). Multimedia applications are memory intensive, and TSVs could enable an acceptable interface for demanding applications.

The logic and DRAM die can be placed “face-to-face” with an bump array across the two pad sequences, which allows perfect alignment the stack. This solution eliminates the unwanted parasitic effect caused by inductive wire bonds and the substrate routing. However, the bandwidth demand and memory density will increase the number of I/Os, necessitating vertical interconnect structures across the DRAM die. This means that a scalable and high-density TSV process, such as the one developed in ELITE, will be necessary to match the data rate and the number of I/Os. This will allow I/O numbers to approach ~ 1000.

The Device Partitioning architecture is one of the most advanced applications in the Wireless field. Here, the division of the memory array with respect to the circuitry will improve the manufacturing process, capability and yield by using two different process fabrication flows.

The circuitry die can serve either the NAND device only or both, NAND and DRAM devices. However this approach will require several challenges to be addressed: architectural, large numbers of TSVs (here in the range of thousands), signal integrity and power delivery, full integration into the memory process fabrication flow and a very enhanced stack up process capability.

The System Integration architecture is latest solution for Wireless applications. The enhanced capability and performance as adopted by the previous scheme (partitioning) is integrated with logic functions of the microprocessor normally devoted to control the NAND/DRAM devices. With this approach even the microprocessor can enhance its own capability having the opportunity to be embedded with circuitry part of the memory devices. Large gain in terms of performances and power saving (I/O buffers can be in principle avoided) are expected.

Commercial exploitation of Flash controller

The purpose of the A1 flash memory controller is enabling raw NAND flash for industrial mass storage applications. In the consumer computing market Solid State Disks (SSD) have started to substitute Hard Disk Drives (HDD). The trend to ultra-mobile computing, tablets and smart phones is also pushing flash as the storage media of choice. Finally, in the industrial markets flash has enabled many new form factors and storage solutions with ruggedized endurance and fail safe features. The latter is where Hyperstone’s focus is today.

The chip level A1 product together with own proprietary firmware will be marketed by Hyperstone to customers that build Solid State Disk and/or memory card products. The development throughout the project has introduced a new more complex but more flexible modular architecture to be Hyperstone’s platform for future controller generations. Within the development hardware and firmware have been co-developed. Several patents and exploitable IPR has been generated based on and extending Hyperstone’s long term know how in the area of flash handling. IPRs are preferably used in own products but generally could be licensed if beneficial.

The evolution towards more advanced technology nodes is requiring the introduction of more complex data handling algorithms to guarantee the reliability of Flash memories against the parasitic effects of deep submicron devices.

Commercial exploitation of TSV technology

Due to well-known challenges within electronics research, the subject of 3D interconnections between or within chips has emerged as a possible solution technology to increased functionality and density of CMOS devices. As a result, international research institutes are positioning themselves to attract industrial funding in this field. To remain ‘competitive’ or ‘attractive’, a European research institution needs to be able to demonstrate credible state-of-the-art programs in this technology. The ELITE project has enabled CEA-LETI to develop state-of-the-art solutions for 3-D TSV technology which has complimented momentum from other existing 3D programs (industrial, government, European, etc.). A broad based wealth of research is fundamental in order for a research institution to remain credible, pertinent and attractive to industrial partnerships and also to attract and develop researchers of an international standard.

The effect of this project has been very positive for CEA-LETI. It has enabled the institution to maintain competitive state-of-the-art technology and mature its 3-D integration toolset. As an outcome of ELITE, IP has been generated which will enable further benefits to collaborative industrial partners, boost their own funding channels and to continue to establish a very pertinent and leading technological roadmap from which European partners can benefit.

Impact from a University point of view

The ELITE project has benefited both KTH and ULANC in numerous areas. The research work carried out in the modelling and analysis work packages representing cutting-edge design of integrated circuits has resulted in a large number of peer-reviewed publications both in Europe and internationally. This has increased the international profile and presence of the universities which has enabled further collaboration and exchange of knowledge between academia and industry. The impact of 3-D technology in integrated circuit design is high, which has attracted quality researchers to both institutes. The research work carried out on massively parallel computational systems has been incorporated into coursework, which has given European students further knowledge of advanced design techniques in future systems.

Contact Details

Hyperstone GmbH – Germany

Hyperstone GmbH headquartered in Konstanz, Germany is a member of the CML Microsystems Plc (London Stock Exchange symbol: CML) holding. The group is maintaining operating subsidiaries in the UK, United States, Germany, Singapore and Taiwan. Group total revenues during fiscal year 2006 were about 38 Mio. EUR or 26.3 Mio. GBP, the average number of employees during 2006 was 227. Hyperstone, the competence center in digital front end design, including an own proprietary 32-bit unified RISC/DSP processors core, as well as hardware and firmware design for flash memory controllers, employs about 30 mostly R&D engineers.

Hyperstone is dedicated to the design, manufacture and world-wide marketing of a range of semiconductor products, primarily for flash memory, network communications, and digital imaging applications. Products are mainly application specific standard products (ASSP's) supplied stand alone or along with either firmware or programmable platforms. Technical development takes place in Konstanz, whereas product sale is carried out through Hyperstone's worldwide network of distributors and representatives. The company has established presence (local office) in Taiwan and in USA. Most of the actual wafer production is done by reputable Far East silicon foundries providing wafer subcontracting services.

URL: http://www.hyperstone.com/

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University of Lancaster – ULANC - UK

Lancaster University is a broad-based research institute that prioritises excellence in research and teaching and has over 12,000 students in four faculties. The Centre for Microsystems Engineering is based within the Engineering Department of Faculty of Science and Technology. The Centre carries out industrial research under national, European and Industry funding in the areas of integration technologies, embedded test and reliability engineering and design methodology research. The main focus is on SoC, SiP and Integrated MEMS related activities.

URL: www.engineering.lancs.ac.uk/

Royal Institute of Technology – KTH - Sweden

KTH is responsible for one-third of Sweden's capacity for engineering studies and technical research at postsecondary level. KTH has over 11,000 undergraduate students, 1,500 active postgraduate students and a staff of 3,100 people. KTH was founded in 1827 and is the largest of Sweden's universities of technology. KTH is an international institution with established research and educational exchanges all over the world, especially in Europe, the USA, Australia and Southeast Asia. It is KTH's ambition to play an even stronger role in the EU research programmes than today.

The department of electronics, systems (ES) at KTH ICT school located in Kista Science city covers a broad research area, from radio electronic circuit and systems, system-on-chip, networks-on-a-chip, to computer architectures and performance evaluation. The following relevant research topics comprise the department's expertise:

Initiated Networks-on-a-Chip (NoC) research since 1999 for sub-100nm technologies and nano-meter technologies;

Interconnect modelling and interconnect-centric SoC design for nano-meter CMOS technology;

System-in-package/system-on-package design and integration for radio and missed-signal applications;

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Commissariat à l'Energie Atomique CEA-LETI, France

A CEA laboratory installed in Grenoble, CEA-LETI is one of the major European research centres for applied electronics. More than 85% of its activity is dedicated to research finalised with external partners. Nearly 1,600 men and women are serving innovation and the transfer of technology in key domains. As the preferred contact of the industrial world, CEA-LETI has sparked the creation of nearly thirty high-technology start-ups, including Soitec, world leader in silicon on insulator. The main research themes at CEA-LETI are: Micro- and Nanotechnologies, Microsystems and heterogeneous integration, Ambient intelligence, Imaging chain, and Systems for Biology and Health. The laboratory secures more than 170 patents every year and implements a dynamic strategy in managing its patent portfolio (watch, creativity, extension, abandon, disposal).

CEA-LETI is today one of the main scientific and technological players in Minatec, the leading European centre of excellence specialising in research into micro- and nanotechnologies. Concentrating on the infinitely small, Minatec is home to 4,000 researchers, from industry and universities, working together in the

nanoscience and nanotechnology fields. CEA-LETI benefits from platforms within Minatec which group expertise and resources found nowhere else in Europe, such as the 300 mm silicon technology platform, the 200 mm microelectronics platform, the 200 mm MEMS200 microsystems platform, the nanocharacterisation platform, the Upstream platform and the Design platform. DCIS, the Division for Systems Design and Integration, DIHS, the Division for Silicon Heterogeneous Integration and DPTS, the Technology Platform Division will be the CEA-LETI Divisions involved in the present project.

URL: http://www.leti.fr/

Micron Semiconductor Italia S.r.l.

Micron Semiconductors Italia is part of the Micron group, one on the top ten semiconductor manufacturers, with a specialization in DRAM and Flash memories. Micron Semiconductors Italia (previously Numonyx) has been leading the technology development of NOR and Phase change Memories and has now the mission to develop advanced memory concepts in its 200mm pilot line of Agrate Brianza.

URL: http://www.micron.com

Project website

http://www.ipack.kth.se/ELITE/

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Use and dissemination of foreground

Section A (public)

A1: LIST OF SCIENTIFIC (PEER REVIEWED) PUBLICATIONS, STARTING WITH THE MOST IMPORTANT ONES										
NO.	Title	Main author	Title of the periodical or the series	Number, date or frequency	Publisher	Place of publication	Year of publication	Relevant pages	Permanent identifiers (if available)	Is/Will open access provided to this publication?
1	System Interconnection Design Trade-offs in Three-Dimensional Integrated Circuits,",	Roshan Weerasekera	PhD thesis		The Royal Institute of Technology (KTH)	Stockholm, Sweden	2008		KTH page	Yes
2	High level modelling and performance evaluation of address mapping in NAND flash memory	Walid Lafi, Didier Lattard and Ahmed Jerraya	Electronics, Circuits, and Systems, 2009. ICECS 2009. 16th IEEE International Conference on		IEEE	Yasmine Hammamet Tunisie	2009	pp. 659 - 662	IEEE	Yes
3	Performance Optimisation of Through Silicon Via Integrated 3-D Die Stacks	Matthew Grange	PhD thesis		Lancaster University	Lancaster, UK	2011			Yes
4	Two-Dimensional and Three-Dimensional Integration of Heterogeneous Electronic	R. Weerasekera, D. Pamunuwa, L-R. Zheng	IEEE Transactions on Comp.-Aided Design of Integrated		IEEE		2009	vol. 28, no. 8 pp. 1237-	IEEE TCAD	No

	Systems under Cost, Performance and Technological Constraints	and H. Tenhunen	Circuits and Systems					1250		
5	Low-cost Through Silicon Vias (TSVs) with Wire-bonded Metal Cores and Low Capacitive Substrate-Coupling	A. C. Fischer, N. Roxhed, M. Grange, R. Weerasekera, D. Pamunuwa, G. Stemme and F. Niklaus	Journal of Micromechanics and Microengineering		IOP		2011		IEEE Xplore, IOP	No
6	Peak-to-peak Ground Noise on a Power Distribution TSV Pair as a Function of Rise Time in 3D Stack of Dies Interconnected through TSVs	Waqar Ahmad, Li-Rong Zheng, Qiang Chen, and Hannu Tenhunen,	IEEE Transactions on Components Packaging and Manufacturing Technologies		IEEE		*2011*		IEEEXplore	No
7	The Computational Efficiency of 2-D and 3-D Silicon Processors for Early-Chip Planning	M. Grange, A. Jantsch, R. Weerasekera, and D. Pamunuwa	Proc. International Conference on Computer-Aided Design (ICCAD)		IEEE/ACM	CA, USA	*2011*	In press		No
8	Optimal Network Architectures for Minimizing Average Distance in k-ary n-dimensional Mesh Networks,	M. Grange, R. Weerasekera, D. Pamunuwa, A. Jantsch, A. Y. Weldezion,	Proc. International Symposium on Networks-On-Chip (NoCS)		ACM/IEEE	PA, USA	*2011*	pp. 57 - 64	IEEE NOCS 2011	No
9	Scalability of the Network-on-Chip communication architecture for 3-D meshes	A.Y. Weldezion, M. Grange, D. Pamunuwa, Z. Lu, A. Jantsch, R. Weerasekera and H. Tenhunen.	Proc. International Symposium on Networks-On-Chip (NoCS)		ACM/IEEE	CA, USA	2009	pp.114 - 123	IEEE NOCS 2009	No
10	3-D Memory Organization and Performance Analysis for Multi-processor Network-On-Chip Architecture	Awet Yemane Weldezion, Z. Lu, R. Weerasekera, and H. Tenhunen,	Proc. IEEE International Conference on 3D System Integration (3DIC 2009)		IEEE	CA, USA	2009	pp. 1-7	IEEE 3DIC	No
11	Compact Modelling of Through-Silicon Vias (TSVs) in	Roshan Weerasekera, M. Grange, D.	Proc. IEEE International Conference on 3D System		IEEE	CA, USA	2009	pp. 1-8	IEEE 3DIC	No

	Three-Dimensional (3-D) Integrated Circuit	Pamunuwa, H. Tenhunen, and L-R. Zheng,	Integration (3DIC 2009)							
12	Physical Mapping and Performance Study of a Multi-Clock 3-Dimensional Network-on-Chip Mesh	Matt Grange, A. Y. Weldezion, D. Pamunuwa, R. Weerasekera, H. Tenhunen and D. Shippen	Proc. IEEE International Conference on 3D System Integration (3DIC 2009)		IEEE	CA, USA	2009	pp. 1-7	IEEE 3DIC	No
13	Modeling of peak-to-peak switching noise along a vertical chain of power distribution TSV pairs in a 3D stack of ICs interconnected through TSVs	Ahmad, W.; Qiang Chen; Li-Rong Zheng; Tenhunen, H.	Proc. IEEE NORCHIP Conference		IEEE	Tampere, Finland	2010	pp. 1-6	IEEE NORCHIP	No
14	Power Distribution TSVS Induced Core Switching Noise	Waqar Ahmad, Kanth, R.K.; Qiang Chen; Li-Rong Zheng; Tenhunen, H.;	Proc. IEEE Electrical Design of Advanced Packaging & Systems Symposium (EDAPS),		IEEE	Singapore	2010	Pp 1-4	IEEE EDAPS	No
15	Trends of terascale computing chips in the next ten years	Zhonghai Lu and Axel Jantsch	Proc. IEEE International Conference on ASIC (ASICON)		IEEE	Chang Sha, China	2009		IEEE ASICON	No
16	Power Integrity Optimization of 3D Chips Stacked Through TSVs	Waqar Ahmed, L. Zheng, R. Weerasekera, Q. Chen, A. Y. Weldezion and H. Tenhunen	Proceedings of the Electrical Performance of Electronic Packaging and Systems (EPEPS 2009),		IEEE	Portland USA	2009	pp. 105-108	IEEE EPEPS	No
17	On Signalling Over Through-Silicon Via (TSV) Interconnects in 3-D Integrated Circuits,	R. Weerasekera, M. Grange, D. Pamunuwa, and H. Tenhunen,	Proc. Design Automation and Test in Europe (DATE) Conference		IEEE/ACM	Dresden, Germany	2010	pp. 1325-1328	DATE 2010	Yes
18	Fast Transient Simulation Algorithm for a 3D Power Distribution Bus	Waqar Ahmad, Rajeev Kumar Kanth, Qiang Chen, Li-Rong Zheng	Proc. Asia Symposium on Quality Electronic Design (ASQED)		IEEE	Penang, Malaysia	2010	pp 343 – 350	IEEE ASQED	No

		and Hannu Tenhunen								
19	Peak-to-peak switching noise and LC resonance on a power distribution TSV pair	Ahmad, W.; Qiang Chen; Li-Rong Zheng; Tenhunen, Hannu.	Proc. IEEE 19th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS),		IEEE	Austin, USA	2010	Pp 173-176	IEEE-EPEPS	No
20	Decoupling Capacitance for the Power Integrity of 3D-DRAM-over- Logic System	Waqar A, Qiang Chen, Li-Rong Zheng, and Hannu Tenhunen	Proc. IEEE 13 Electronics Packaging Technology Conference (EPTC)		IEEE EPTC	Singapore	2011		IEEE EPTC	No
21	Comparative Cost Analysis of 3-D Integrated Circuits,	Roshan Weerasekera , Dinesh Pamunuwa , Matt Grange , Axel Jantsch, Andrew Richardson, Mark Scannell	in Workshop Notes, Special Interest Workshop on 3D Integration - Applications, Technology, Architecture, Design, Automation, and Test, Design Automation and Test in Europe (DATE) Conference		IEEE/ACM	Grenoble, France	2011		lancs eprints	Yes
22	Modeling the Efficiency of Stacked Silicon Systems: Computational, Thermal and Electrical Performance	M. Grange, A. Jantsch, D. Pamunuwa and R. Weerasekera	Workshop Notes, Special Interest Workshop on 3D Integration - Applications, Technology, Architecture, Design, Automation, and Test, Design Automation and Test in Europe (DATE)		IEEE/ACM	Grenoble, France	2011		lancs eprints	Yes
23	Closed-Form Equations for Through-Silicon Via (TSV) Parasitics in 3-D Integrated Circuits	Roshan Weerasekera, Matt Grange, Dinesh Pamunuwa, Li-Rong Zheng and Hannu Tenhunen	Workshop Notes, Special Interest Workshop on 3D Integration - Applications, Technology, Architecture, Design, Automation, and Test, Design Automation and Test in Europe (DATE)		IEEE/ACM	Nice - France	2009	pp. 247-250	DATE 2009	Yes
24	Power Integrity Estimation of 3D Integrated Chips,	Waqar Ahamd, Hannu Tenhunen	Workshop Notes, Special Interest Workshop on 3D Integration - Applications, Technology, Architecture, Design, Automation, and Test, Design		IEEE/ACM	Dresden, Germany	2010	pp. 357-360	DATE 2010	Yes

			Automation and Test in Europe (DATE),							
25	Examination of delay and signal integrity metrics in TSVs	Matt Grange, Roshan Weerasekera, Dinesh Pamuwa and Hannu Tenhunen	Workshop Notes, Special Interest Workshop on 3D Integration - Applications, Technology, Architecture, Design, Automation, and Test, Design Automation and Test in Europe (DATE)		IEEE/ACM	Nice - France	2009	pp. 260-264.	DATE 2009	Yes
26	Bandwidth Optimization for Through Silicon Via(TSV) bundles in 3D Integrated Circuits	Awet Yemane Weldezion, R. Weerasekera, D. Pamunuwa ,L. Zheng and H. Tenhunen,	Workshop Notes, Special Interest Workshop on 3D Integration - Applications, Technology, Architecture, Design, Automation, and Test, Design Automation and Test in Europe (DATE)		IEEE/ACM	Nice - France	2009	pp. 283-287.	DATE 2009	Yes
27	Power Integrity Issues in 3D Integrated Chips Using TSVs (Through Silicon Vias),	Waqar Ahamd, Qiang Chen, Roshan Weerasekera, Hannu Tenhunen, Lirong Zheng.“	Workshop Notes, Special Interest Workshop on 3D Integration - Applications, Technology, Architecture, Design, Automation, and Test, Design Automation and Test in Europe (DATE)		IEEE/ACM	Nice - France	2009	pp. 274-275	DATE 2009	Yes

A2: LIST OF DISSEMINATION ACTIVITIES								
NO.	Type of activities	Main leader	Title	Date	Place	Type of audience	Size of audience	Countries addressed
	Book chapter publicatoin	Axel Janstch	The Promises and Limitations of 3-D Integration,"	2010	Morgan Kaufmann publishers	Scientific and Industrial research community		Worldwide
4	Invited special session at conference	Dinesh Pamunuwa	Memory Technology for Extended Large-Scale Integration in Future Electronics Applications	2008	DATE 2008	Scientific and Industrial research community	50	Worldwide
1	articles published in the popular press	Roshan Weerasekera	Analysis of the Communication Architecture in 3D ICs: Physical Models of TSVs	April 2010	Future Fab International	Scientific and Industrial research community	online	Worldwide
2	articles published in the popular press	Awet Yemane Weldezion	Performance of Scalable 3D on-Chip Networks Architecture: A Comparable Analysis Circuits	July 2010	Future Fab International	Scientific and Industrial research community	online	Worldwide
3	articles published in the popular press	Matt Grange	Signaling Conventions for Through Silicon Vias in 3D Integrated Circuits	July 2010	Future Fab International	Scientific and Industrial research community	online	Worldwide
4	Workshop	Jean-Charles Souriau	Technology Experiments on 3-D interconnect and die stacking	Septemb 2011	Helsinki, Finland	Scientific and Industrial research community	50	Worldwide
5	Workshop	Jean-Charles Souriau	3D Integration technologies at Leti: A versatile 3D toolbox	Septemb 2011	Helsinki, Finland	Scientific and Industrial research community	50	Worldwide
6	Workshop	Dinesh Pamunuwa	Limits of Digital Computation in 3-D Integrated Silicon Systems	Septemb 2011	Helsinki, Finland	Scientific and Industrial research community	50	Worldwide
7	Workshop	Christine Fuchs	RF modelling of Through Silicon	Septemb	Helsinki,	Scientific and Industrial	50	Worldwide

			Vias (TSV) for 3-D integration	2011	Finland	research community		
8	Workshop	Andreas Fischer	Through-silicon via technologies for 3-D MEMS	Septemb 2011	Helsinki, Finland	Scientific and Industrial research community	50	Worldwide
9	Workshop	Matt Grange	Physical-level modeling and performance analysis of 3-D integrated circuits	Septemb 2011	Helsinki, Finland	Scientific and Industrial research community	50	Worldwide
10	Workshop	Waqar Ahmed	Modeling of core switching noise for the power distribution network in a 3-D stack of dies interconnected through TSVs	Septemb 2011	Helsinki, Finland	Scientific and Industrial research community	50	Worldwide
11	Workshop	Awet Yemane Weldezion	Vertical on-chip Networks (3DNOC) - design challenges & opportunities	Septemb 2011	Helsinki, Finland	Scientific and Industrial research community	50	Worldwide

Report on societal implications

A General Information *(completed automatically when **Grant Agreement number** is entered.*

Grant Agreement Number:	215030
Title of Project:	ELITE – Extended large (3D) integration technology (ELITE)
Name and Title of Coordinator:	PAGE, Marie-Laure

B Ethics

1. Did your project undergo an Ethics Review (and/or Screening)? • If Yes: have you described the progress of compliance with the relevant Ethics Review/Screening Requirements in the frame of the periodic/final project reports? Special Reminder: the progress of compliance with the Ethics Review/Screening Requirements should be described in the Period/Final Project Reports under the Section 3.2.2 *'Work Progress and Achievements'*	***No***
2. Please indicate whether your project involved any of the following issues (tick box) :	***No***
RESEARCH ON HUMANS	
• Did the project involve children?	N
• Did the project involve patients?	N
• Did the project involve persons not able to give consent?	N
• Did the project involve adult healthy volunteers?	N
• Did the project involve Human genetic material?	N
• Did the project involve Human biological samples?	N
• Did the project involve Human data collection?	N
RESEARCH ON HUMAN EMBRYO/FOETUS	
• Did the project involve Human Embryos?	N

• Did the project involve Human Foetal Tissue / Cells?	N
• Did the project involve Human Embryonic Stem Cells (hESCs)?	N
• Did the project on human Embryonic Stem Cells involve cells in culture?	N
• Did the project on human Embryonic Stem Cells involve the derivation of cells from Embryos?	N
PRIVACY	
• Did the project involve processing of genetic information or personal data (eg. health, sexual lifestyle, ethnicity, political opinion, religious or philosophical conviction)?	N
• Did the project involve tracking the location or observation of people?	N
RESEARCH ON ANIMALS	
• Did the project involve research on animals?	N
• Were those animals transgenic small laboratory animals?	N
• Were those animals transgenic farm animals?	N
• Were those animals cloned farm animals?	N
• Were those animals non-human primates?	N
RESEARCH INVOLVING DEVELOPING COUNTRIES	
• Did the project involve the use of local resources (genetic, animal, plant etc)?	**N**
• Was the project of benefit to local community (capacity building, access to healthcare, education etc)?	**N**
DUAL USE	
• Research having direct military use	N
• Research having the potential for terrorist abuse	N

C Workforce Statistics

3. Workforce statistics for the project: Please indicate in the table below the number of people who worked on the project (on a headcount basis).

Type of Position	Number of Women	Number of Men
Scientific Coordinator		3
Work package leaders	0	3
Experienced researchers (i.e. PhD holders)	5	34

PhD Students		4
Other	1	

4. How many additional researchers (in companies and universities) were recruited specifically for this project?	**4**
Of which, indicate the number of men:	4

D Gender Aspects

5. Did you carry out specific Gender Equality Actions under the project?

x Yes
○ No

6. Which of the following actions did you carry out and how effective were they?

	Not at all effective				Very effective
❑ Design and implement an equal opportunity policy	○	x	○	○	○
❑ Set targets to achieve a gender balance in the workforce	○	○	○	○	○
❑ Organise conferences and workshops on gender	○	○	○	○	○
❑ Actions to improve work-life balance	○	○	○	○	○

○ Other:

7. Was there a gender dimension associated with the research content – i.e. wherever people were the focus of the research as, for example, consumers, users, patients or in trials, was the issue of gender considered and addressed?

○ Yes- please specify

X No

E Synergies with Science Education

8. Did your project involve working with students and/or school pupils (e.g. open days, participation in science festivals and events, prizes/competitions or joint projects)?

○ Yes- please specify

X No

9. Did the project generate any science education material (e.g. kits, websites, explanatory booklets, DVDs)?

X Yes- please specify

Project website: http://www.ipack.kth.se/ELITE/

Online 3-D tool collection available to general public:

○ No

F Interdisciplinarity

10. Which disciplines (see list below) are involved in your project?

○ Main discipline[1]: 2.2

○ Associated discipline1:1.1, 2.3 ○ Associated discipline1:1.2

G Engaging with Civil society and policy makers

11a Did your project engage with societal actors beyond the research community? *(if 'No', go to Question 14)*

○ Yes
X No

[1] Insert number from list below (Frascati Manual).

11b If yes, did you engage with citizens (citizens' panels / juries) or organised civil society (NGOs, patients' groups etc.)?

- ○ No
- ○ Yes- in determining what research should be performed
- ○ Yes - in implementing the research
- ○ Yes, in communicating /disseminating / using the results of the project

11c In doing so, did your project involve actors whose role is mainly to organise the dialogue with citizens and organised civil society (e.g. professional mediator; communication company, science museums)?	○ Yes X No

12. Did you engage with government / public bodies or policy makers (including international organisations)

- X No
- ○ Yes- in framing the research agenda
- ○ Yes - in implementing the research agenda
- ○ Yes, in communicating /disseminating / using the results of the project

13a Will the project generate outputs (expertise or scientific advice) which could be used by policy makers?

- ○ Yes – as a **primary** objective (please indicate areas below- multiple answers possible)
- ○ Yes – as a **secondary** objective (please indicate areas below - multiple answer possible)
- X No

13b If Yes, in which fields?

Agriculture		Energy		Human rights	
Audiovisual and Media		Enlargement		Information Society	
Budget		Enterprise		Institutional affairs	
Competition		Environment		Internal Market	
Consumers		External Relations		Justice, freedom and security	
Culture		External Trade		Public Health	
Customs		Fisheries and Maritime Affairs		Regional Policy	
Development Economic and Monetary Affairs		Food Safety		Research and Innovation	
Education, Training, Youth		Foreign and Security Policy		Space	
Employment and Social Affairs		Fraud		Taxation	
		Humanitarian aid		Transport	

13c If Yes, at which level?

- ○ Local / regional levels
- ○ National level
- ○ European level
- ○ International level

H Use and dissemination

14. How many Articles were published/accepted for publication in peer-reviewed journals?	**3 published, 2 under review, 1 to be submitted**
To how many of these is open access[2] provided?	**3**
How many of these are published in open access journals?	**1**
How many of these are published in open repositories?	**2**
To how many of these is open access not provided?	**1**
Please check all applicable reasons for not providing open access:	
× publisher's licensing agreement would not permit publishing in a repository ❑ no suitable repository available ❑ no suitable open access journal available ❑ no funds available to publish in an open access journal ❑ lack of time and resources ❑ lack of information on open access ❑ other[3]: ……	

15. How many new patent applications ('priority filings') have been made? *("Technologically unique": multiple applications for the same invention in different jurisdictions should be counted as just one application of grant).*		**1 - PCT/EP2007/062785**
16. Indicate how many of the following Intellectual Property Rights were applied for (give number in each box).	Trademark	**N**
	Registered design	**N**
	Other	**N**
17. How many spin-off companies were created / are planned as a direct result of the project?		**N**
Indicate the approximate number of additional jobs in these companies:		**N**

18. Please indicate whether your project has a potential impact on employment, in comparison with the situation before your project:

×	Increase in employment, or	×	In small & medium-sized enterprises
×	Safeguard employment, or	×	In large companies
❑	Decrease in employment,	❑	None of the above / not relevant to the project
❑	Difficult to estimate / not possible to		

[2] Open Access is defined as free of charge access for anyone via Internet.
[3] For instance: classification for security project.

quantify			

19. For your project partnership please estimate the employment effect resulting directly from your participation in Full Time Equivalent (*FTE = one person working fulltime for a year*) jobs: Difficult to estimate / not possible to quantify	*Indicate figure:* *22.6 FTE within project*

I Media and Communication to the general public

20. As part of the project, were any of the beneficiaries professionals in communication or media relations?

○ Yes X No

21. As part of the project, have any beneficiaries received professional media / communication training / advice to improve communication with the general public?

○ Yes X No

22 Which of the following have been used to communicate information about your project to the general public, or have resulted from your project?

×	Press Release	×	Coverage in specialist press
❑	Media briefing	❑	Coverage in general (non-specialist) press
❑	TV coverage / report	❑	Coverage in national press
❑	Radio coverage / report	❑	Coverage in international press
❑	Brochures /posters / flyers	×	Website for the general public / internet
❑	DVD /Film /Multimedia	×	Event targeting general public (festival, conference, exhibition, science café)

23 In which languages are the information products for the general public produced?

❑	Language of the coordinator	×	English
❑	Other language(s)		

***Question F-10*:** Classification of Scientific Disciplines according to the Frascati Manual 2002 (Proposed Standard Practice for Surveys on Research and Experimental Development, OECD 2002):

FIELDS OF SCIENCE AND TECHNOLOGYS

1. NATURAL SCIENCES

1.1 Mathematics and computer sciences [mathematics and other allied fields: computer sciences and other allied subjects (software development only; hardware development should be classified in the engineering fields)]

1.2 Physical sciences (astronomy and space sciences, physics and other allied subjects)

1.3 Chemical sciences (chemistry, other allied subjects)

1.4 Earth and related environmental sciences (geology, geophysics, mineralogy, physical geography and other geosciences, meteorology and other atmospheric sciences including climatic research, oceanography, vulcanology, palaeoecology, other allied sciences)

1.5 Biological sciences (biology, botany, bacteriology, microbiology, zoology, entomology, genetics, biochemistry, biophysics, other allied sciences, excluding clinical and veterinary sciences)

2 ENGINEERING AND TECHNOLOGY

2.1 Civil engineering (architecture engineering, building science and engineering, construction engineering, municipal and structural engineering and other allied subjects)

2.2 Electrical engineering, electronics [electrical engineering, electronics, communication engineering and systems, computer engineering (hardware only) and other allied subjects]

2.3. Other engineering sciences (such as chemical, aeronautical and space, mechanical, metallurgical and materials engineering, and their specialised subdivisions; forest products; applied sciences such as geodesy, industrial chemistry, etc.; the science and technology of food production; specialised technologies of interdisciplinary fields, e.g. systems analysis, metallurgy, mining, textile technology and other applied subjects)

3. MEDICAL SCIENCES

3.1 Basic medicine (anatomy, cytology, physiology, genetics, pharmacy, pharmacology, toxicology, immunology and immunohaematology, clinical chemistry, clinical microbiology, pathology)

3.2 Clinical medicine (anaesthesiology, paediatrics, obstetrics and gynaecology, internal medicine, surgery, dentistry, neurology, psychiatry, radiology, therapeutics, otorhinolaryngology, ophthalmology)

3.3 Health sciences (public health services, social medicine, hygiene, nursing, epidemiology)

4. AGRICULTURAL SCIENCES

4.1 Agriculture, forestry, fisheries and allied sciences (agronomy, animal husbandry, fisheries, forestry, horticulture, other allied subjects)

4.2 Veterinary medicine

5. SOCIAL SCIENCES

5.1 Psychology

5.2 Economics

5.3 Educational sciences (education and training and other allied subjects)

5.4 Other social sciences [anthropology (social and cultural) and ethnology, demography, geography (human, economic and social), town and country planning, management, law, linguistics, political sciences, sociology, organisation and methods, miscellaneous social sciences and interdisciplinary , methodological and historical S1T activities relating to subjects in this group. Physical anthropology, physical geography and psychophysiology should normally be classified with the natural sciences].

6. HUMANITIES

6.1 History (history, prehistory and history, together with auxiliary historical disciplines such as archaeology, numismatics, palaeography, genealogy, etc.)

6.2 Languages and literature (ancient and modern)

6.3 Other humanities [philosophy (including the history of science and technology) arts, history of art, art criticism, painting, sculpture, musicology, dramatic art excluding artistic "research" of any kind, religion, theology, other fields and subjects pertaining to the humanities, methodological, historical and other S1T activities relating to the subjects in this group]