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PROJECT PUBLISHABLE REPORT
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1. PUBLISHABLE REPORT

The objective of the IDESA Support Action was to develop and make available didactic training material on the design flow for integrated circuits for advanced deep sub-micron technologies, free of intellectual property rights, for the benefit of European academia.

The IDESA project addressed training of academic staff (professors, lecturers and PhD assistants) from all interested European academia. New didactic material was made available for reuse in the course portfolio of bachelor and master engineering curricula. Training was organised in class-based hands-on sessions and advanced seminars using state-of-the-art multimedia technology was recorded and made available over the web or on DVD.

- **4 different advanced implementation courses** toured different sites in Europe. These courses were hands-on courses using a train-the-trainer philosophy. Each of these courses was repeated 7 times, to reach a significant proportion of the 600+ European academia. All of these courses addressed the advanced implementation issues relating to the 90 nm nodes initially. This brought the universities to a more advanced level of implementation skills to start engaging in 65- and 45-nm issues.

  28 sessions of the 4 courses have been organised and were attended by representatives from over 40 different academia. These are:

  - Advanced analog implementation flow. 7 Sessions were organized:
    1. *16-20 Jun 2008 – EPFL– 17 participants*
    2. *8-12 Dec 2008 – IMEC – 24 participants*
    3. *19-23 Jan 2009- Thessaloniki- 20 participants*
    4. *22-26 Jun 2009- Krakow-Poland- 15 participants*
    5. *20 Jun-3 Jul 2009 -Mons- Belgium-16 participants*
    6. *25-29 Jan 2010- Bratislava- Slovakia- 16 participants*
    7. *1-5 Jan 2010 - Grenoble- France- 14 participants*
  - Advanced RF implementation flow: 7 Sessions were organized:
    1. *19-23 May 2008, TU Delft, NL: 20 participants*
    2. *1-5 Dec 2008, imec, Leuven BE: 25 participants*
    3. *16-20 Feb 2009- CNM, Seville ES: 20 participants*
    4. *30 Mar-3 Apr 2009, Newcastle University, UK: 14 participants*
    5. *15-19 Jun 2009, Warsaw University of Technology, PL: 10 participants*
    6. *25-29 Jan 2010, CIME Nanotech, Grenoble FR: 16 participants*
    7. *26-30 Apr 2010, Lund University, SE: 16 participants*
  - Advanced digital physical implementation flow: 7 Sessions were organized:
    1. *27-31 Oct 2008, imec, Leuven, BE, 24 participants, Cadence favour*
    2. *24-28 Nov 2008, STFC-RAL, Didcot, UK, 18 participants, Synopsys flavour*
    3. *16-20 Feb 2009, Aristotle University, Thessaloniki, GR, 20 participants, Cadence*
    4. *1-5 Jun 2009, Slovak University of technology, Bratislava, SK, 11 participants, Synopsys*
    5. *28 Sept-2 Oct 2009, Technical University of Lodz, Lodz, PL, 18 participants , Cadence*
    6. *14-18 Dec 2009, Université de Mon, Mons, BE, 13 participants, Synopys*
    7. *22-26 Feb 2010, Università degli Studi di Napoli Federico II, Napoli, IT, 24 participants, Cadence*

- Design-for-manufacturing: 7 Sessions were organized:
    1. *5-8 May 2008, imec, Leuven, BE, 18 participants*
    2. *4-7 Nov 2008, STFC-RAL, Didcot, UK, 12 participants*
    3. *12-15 May 2009, INFN, Padova, IT, 9 participants*
    4. *15-18 Sep 2009, CTU, Praha, CZ, 7 participants*
    5. *26-29 Jan-2010, imec, Leuven, BE, 11 participants*
    6. *30 Mar-2 Apr 2010, imec, Leuven, BE, 12 participants*

- The consortium has built a portfolio of **public domain didactic seminars**, addressing issues that are not addressed in the design flow courses but that are of dominant importance for the 65 and 45 nm generation design flows. The availability of 32 seminars was announced to the academic public.
    1. Low Power Digital Design in Sub-90nm CMOS Technologies by Wim De Haene (KULeuven)
    2. Component matching: best practices and fundamental limits by Marcel Pelgrom and Maarten Vertregt (NXP Research)
    3. Automotive Interferences: EMC and Transients by Herman Casier
    4. Reliability of future advanced CMOS circuits and technologies by Guido Groeseneken (IMEC)
    5. Two important transistor innovations: strained silicon and FinFETs by Geert Eneman - Nadine Collaert (IMEC)
    6. Risk free, 65 nm and beyond, digital low power design by François Thomas (Cadence)
    7. Variability Aware Modeling and Yield Aspects by Bart Dierickx (IMEC)
    8. Variability and Litho-aware digital implementation by François Thomas (Cadence)
    9. Leakage physics and modeling by Wieslaw Kuzmicz (Warsaw University of Technology)
    10. Techniques to control leakage power at technology and device level : application to a fully power aware SoC design by Edith Beigné (CEA)
    11. Compact models for DSM by Christian Enz (EPFL)
    12. Statistical Static Timing Analysis and Optimization - François Thomas (Cadence)
    13. CMOS front-end design at millimetre wave frequencies - Alexandre Siligaris (CEA LETI)
    14. Analog design in scaled technologies - Andrea Baschirotto (University of Lecce)
    15. Design of ADC in advanced technologies - Andrea Baschirotto (University of Lecce)
    16. Design of analog filters in advanced technologies - Andrea Baschirotto (University of Lecce)
    17. Low power CMOS 65 and 45 nm industrial technologies - Thomas Skotnicki (STMicroelectronics)
    18. ESD and Latchup - Fabrice Blanc (ARM)
    19. DFT to meet Nanometer Test Challenges - Philippe Rossant (Synopsys)
    20. Ultra-low Voltage Analog Circuit Design - Christian Enz (CSEM SA, Neuchatel - EPFL, Lausanne)
    21. Advanced circuit design in ermerging 2D & 3D SOI technologies - Thierry Poiroux (CEA LETI)
    22. SOI and multiple gate transistors - Thierry Poiroux (CEA LETI)
    23. Thermal issues in nanoscale VLSI devices and circuits - Nicolo Rinaldi (University of Naples)
    24. Statistical Memory Analysis for robust SRAM design - Paul Zuber, Petr Dobrovolny (imec)
    25. Metric Driven Verification - Hans Zander (Cadence)
    26. Assertion-based verification - Kawe Fatouhi (Cadence)
    27. A guided tour of the Interconnect road map from 90 nm down to 32 nm designs in the analog and digital domains - Roberto Suaya
    28. Electrostatic discharge protection for DSM RF circuits - Dimitri Linten
    29. Fundamentals of digitally-assisted RF - Robert Staszewski
    30. SOC in 65 nm and below. Concepts, design, implementation and application - Fabien Clermidy, CEA-LETI
    31. Heterogeneous Design - Nicolas Delorme, Asygn
    32. Millimeter-wave Design in Silicon Technologies - Didier Belot (STMicroelectronics)
    33. CMOS Radio Wave Design for MM-Wave applications - Piet Wambacq
    34. Nonlinear distortion analysis in circuits and systems - Prof. dr. ir. Gerd Vandersteen – Dr. ir. Ludwig De Locht (Vrije Universiteit Brussel)
    35. On-chip Passive Components and Deep Submicron RF IC Design - John R. Long (Delft University of Technology)

- This seminar portfolio was be **supplemented with fully documented didactic lab exercise-material** that can be reused free of intellectual property rights in the curricula of European engineering students. Only one lab exercise was published..
    1. Analog design in scaled technologies – Andrea Baschirotto (university of Milan-Bicocca / Salento)
    2. Leakage physics and modeling (Wieslaw Kuzmicz - Warsaw University of Technology)
    3. CMOS Physics using MASTAR (Thomas Skotnicki - STMicroelectronics)

A Program Board consisting of representatives of the industry (both IDM and EDA) and of the Education and Training Working Group (ETWG) of ENIAC helped defining the content of the 65- and 45-nm seminar portfolio and advised on how to best guide the transition from a 90-nm focus to a 65- and 45-nm.

The project website is available on www.idesa-training.org

=== End-of-Report ===