



Project acronym: Project title: Project number: Call identifier: Start date of project:

SACRA

Spectrum and Energy Efficiency through multi-band Cognitive RadioEuropean Commission – 249060FP7-ICT-2007-1.101/01/2010Duration: 36 months

Document reference number:	D6.2
Document title:	Integration specification
Version:	2.0
Due date of document:	Month M24 (December 2011)
Actual submission date:	13/04/2012
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P	Project co-funded by the European Commission within the 7th Framework Programme		
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FC contract	249060	Document title:	Integration specification
	210000	Document version:	2.0
		Date:	13/04/2012

EXECUTIVE SUMMARY

This deliverable D6.2 of the FP7 ICT SACRA project provides the specifications for the system integration.

• Connection to WP4/5

System integration consists of the hardware (HW) integration, which is closely linked to WP4.4. In order to verify the demonstrator, terminal has been built. This document describes the technical and electrical specifications needed for the HW integration. The integration specification for this radio system is also characterized in this document.

• Connection to WP2/3/5

System integration also consists of the SW integration, which is closely linked to WP2, WP3 and WP5. Integration specification for the detection algorithms and classification is given in chapter 5.

• Description of contents of D6.2

In order to realize the scenarios described in D6.1, general specifications for the user equipment are given. Chapter 2 summarizes the equipment specification like the SACRA terminal (user equipment), and base station. Chapter 3 consists of the system overview and general specifications for the test scenario, also described in D6.1. To ensure an efficient HW and SW integration, chapter 4 and 5 specifies the HW and SW parts. Chapter 6 gives information about metrics of the SACRA terminal and base station, in order to evaluate spectrum efficiency / occupancy, energy efficiency, or reducing the number of components. Finally a detailed schedule for HW and SW integration is given in chapter 7.

• Conclusion to D6.2

In this document, we have refined the specifications of the building blocks that will be conducted to the WP6. An equipment specification shows the components used for the selected scenarios described in D6.1 and D1.1. SACRA indicators like spectrum efficiency / occupancy, energy efficiency, or decreasing the bill of material are detailed described for the used scenarios. Furthermore it is shown, with which WP or task we are going to handle these indicators. The present document can be seen as a schedule for the activities in WP6, especially illustrated in chapter 7 (Step by step integration).

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1 INTRODUCTION

1.1 PURPOSE OF THE DOCUMENT

This document is the deliverable D6.2 of the project and defines the specifications for the system integration including software and hardware integration. Moreover it describes the step-by-step integration procedure to enable the validation of efficient cognitive radio communications.

Indeed D4.2 (performed in WP4) has defined the specifications for each RF modem component but for WP4.4 integration specifications are needed. Digital interfaces defined in WP5 are also taken into account in this deliverable.

In order to integrate WP2 and/with WP3, SW integration specifications are needed. For SW system integration we take into account the input of D2.2.

WP3 plans an additional verification and validation for their developed radio resource management and networking for cognitive radio systems, which needs a higher amount of user equipment (UE). This additional verification and validation is going to be described in D6.3.

It is planned to validate the use cases described in D6.1, therefore the D6.2 only includes integration specifications for WP2, WP4, WP5, and partially WP3.

D6.2 proposes a timetable for step-by-step integration in chapter 7. With that schedule, a good integration at the end of the project is ensured.

Besides the rework of the document with respect to technical review of the second period, following key changes had been made in the latest version D6.2 v2.0 compared to D6.1 v1.0:

- Section 1.3: New section regarding "integration overview"
- Section 5.2: Add a description of the WP3 integration
- Section 5.3: New section regarding "summary of the integration SW"
- Section 6: Complete new "SACRA metrics" chapter
- Section 7: Extend "demonstrator integration stages" and split the schedules in HW and SW

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1.2 DOCUMENT VERSIONS SHEET

Version	Date	Description, modifications, authors	
0.1	24.11.2011	Initial document, Alexander Jaschke (IIS), Robért Glein (IIS)	
0.2	02.12.2011	Addition of chapters, Alexander Jaschke (IIS), Robért Glein (IIS)	
0.3	08.12.2011	Addition of chapters, Dominique Nussbaum (Eure), Dorin Panaitopol (NTUK)	
0.4	13.12.2011	Addition to chapter 5.3.1, Tapio Rautio (VTT)	
0.5	23.12.2011	Edited chapter 2 and 5, Alexander Jaschke (IIS), Robért Glein (IIS),	
0.6	23.12.2011	Chapter 5.1.1 update by Bassem Zayen (Eure)	
0.7	23.12.2011	Addition to chapter 6 and update of the document, Alexander Jaschke (IIS), Robért Glein (IIS)	
0.8	28.12.2011	Contributions by IT	
0.9	03.01.2012	Review by Philippe (NTUK) and Sylvain (Thales)	
0.95	05.01.2012	Chapter 5 – updated, Dorin (NTUK)	
0.96	09.01.2012	Addition of executive summary and chapter 7, Alexander Jaschke (IIS)	
1.0	11.01.2012	Final updates of the D6.2 by Alexander Jaschke (IIS), Robért Glein (IIS)	
1.1	15.03.2012	Addition to SW integration schedule, Renaud Pacalet (IT)	
1.2	16.03.2012	Chapter 6 added by Dominique Nussbaum (Eurecom)	
1.3	16.03.2012	Addition to Summarize Executive, Chapter 6, Conclusion; Review by Alexander Jaschke (IIS) and Robért Glein (IIS)	
1.4	23.03.2012	Integration of comments from internal reviewers	
1.5	05.04.2012	Chapter 1.3 added by Alexander Jaschke (IIS)	
1.6	12.04.2012	Rework of review by Dominique Nussbaum (Eurecom)	
2.0	13.04.2012	Final updates of the D6.2 v2.0 by Alexander Jaschke (IIS), Robért Glein (IIS)	

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1.3 INTEGRATION OVERVIEW

This chapter gives an overview of the system integration for the SACRA modem. Figure 1-1 depicts the block diagram of the SACRA modem in order to specify the system integration.



Figure 1-1 Block diagram of the SACRA modem integration

Step by step integration explanation:

- WP2 is getting data samples for the sensing algorithms by the hardware developed in WP4
- In order to evaluate the sensing algorithm, WP3 will be supplied with sensed signals (e.g. first a coarse sensed signal and after an iteration of configuration/control a high resolution sensed signal).
- The soft modem is used as a reference to compare SACRA sensing and classification results with each other.
- If the sensed signal is occupied, the baseband processor and the sensing algorithms will be reconfigured by WP3.
- Also the HW components parameters (e.g. bandwidth, center frequency, number of samples) will be reconfigured by WP3.
- The soft modem achieves new data sample for verification if needed by WP4.

Thus, the cognitive radio system is a closed loop. The several units of the block diagram and its integration specification is described in this document.

2 EQUIPMENT SPECIFICATION

This section summarizes the requirements needed for the SW and HW system integration. The implementation is already described in the specific deliverables of WP4 and WP5.

2.1 USER EQUIPMENT

Table 2-1 shows the necessary user equipment for the test scenarios described in D6.1.

Parameter	Description	Relevant scenarios	Described in deliverable
UE1	SACRA terminal	Intra-cell scenario	D4.2
UE2	Primary user (e.g. microphone)	Intra- and inter-cell scenario	D6.2
UE3	Unused mobile terminal		
UE4	Unused mobile terminal		
UE5	SACRA terminal	Inter-cell scenario	D4.2

Table 2-1: Specification user equipment

The unused mobile terminals UE3 and UE4 are not used in the chosen SACRA test scenario. These UEs are other mobile terminals out of the test cells, shown in D6.1 chapter 2.2.2.2.

2.1.1 SACRA terminal

The SACRA terminal integration specification is already described in D4.2.

2.1.2 Primary user

As primary user a microphone is planned to be used. The primary user should have the following parameters:

- FM modulation (because of the widely used wireless programme making and special events (PMSE) devices) or DVB-T signal
- Adjustable channels for channel selection
- UHF TVWS frequency range

The primary user should be utilized during the test scenario. In case of a microphone, an audio signal should be transmitted.

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2.2 BASE STATION

Table 2-2 shows the necessary base station (eNodeB) for the test scenarios described extensively in D6.1.

Parameter	Description	Relevant for system integration	Described in deliverable
eNB1	Operation in UHF TVWS and 2.6GHz LTE bands	Intra- and inter-cell scenario	D6.1
eNB2 – eNB7	Unused		D6.1

Table 2-2: Specification user equipment

The unused base stations eNB2 - eNB7 are not used in the chosen SACRA test scenario. These eNBs are base stations out of the inter-cells, shown in D6.1 chapter 2.2.2.2.

2.3 FREQUENCY RESOURCE

Corresponding to the eNodeB's the frequency resources for the test scenarios are described in D6.1 chapter 5.2.4.

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3 SYSTEM OVERVIEW AND GENERAL SPECIFICATION

As described in D6.1, the overall SACRA system will aim at demonstrating a Spectrum Aggregation (SA) Use case, with a cognitive access to the TVWS band. The overall system will comprise:

- The SACRA terminal (dual band, developed in the WP4 for RF modem, and WP5 for the baseband)
- A TVWS (470-790 MHz) and 2.6 GHz LTE NodeB: those logical entities can be co-localized, or even can be the same equipment, depending on the scenario.
- A Joint Radio Resource Management (JRRM) entity, which attributes the radio resources in both bands, UHF and 2.6 GHz. In spectrum aggregation (use case 1), it allows the combination of the 2 bands resources to increase the throughput. In a Femto Cell usage (use case 3), it allows the handover (soft or hard) between the 2 bands.
- A Mobility Management entity: as in classical cellular network, there is a need to manage the mobility of the terminal to allow the routing of the data from/to the terminal to/from the rest of the world (outside the Domain).



Domain

Figure 3-1: SACRA system overview

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As stated in D6.1, the SA scenario that will be implemented can be divided into 5 steps:

- Step 1: The SACRA terminal is connected to LTE base station through the 2.6 GHz band. The SACRA system monitors the available/free TVWS band in the area (continuous sensing). Here we can simulate interference on some part of TVWS if necessary and hence sensing is able to detect which band is free and which is in use. Indeed, there is no guaranty that a primary user can enter in our coverage at a given time; we will therefore emulate a primary user thanks to a microphone. We will transmit in a specific channel, in order to validate the sensing algorithms.
- Step 2: Better QoS is required and the system sends a request to the TVWS base station asking for allocation of resources in TVWS.
- Step 3: The SACRA terminal gets a TVWS resource (the same it asked) from the TVWS base station. From now it is receiving one 2.6GHz carrier (from LTE base station) and one TVWS carrier (from TVWS base station). During this period, the sensing system monitors the band in order to ensure an efficient evacuation of the used band. The list of the available/free TVWS channels is also maintained.
- Step 4: A primary user (a microphone) appears on the TVWS carrier used by the SACRA terminal. The system detects the primary user (detection distributed between the TVWS base station and the UE). The information is sent to the JRRM.
- Step 5: The TVWS carrier of our SACRA terminal is changed from the initial carrier and from now it is receiving the same 2.6GHz carrier but a new TVWS carrier.

The specifications of the SACRA system are derived from this scenario, and are mainly described in D6.1.

The following figure visualises the test scenario activities in the described five steps with the mobile phone as SACRA terminal and a microphone as PU.

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Figure 3-2: Test scenario activities

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4 INTEGRATION OF THE HW PARTS

In this section, the integration of WP4 and WP5 parts are described in a coherent way in the SACRA terminal. The integrated terminal will allow us to implement the spectrum aggregation use case.

4.1 INTEGRATION OF THE SACRA TERMINAL

In this section, we assume that WP4.4 has been performed. The WP4.4 task consists of the RF modem integration. The overall RF modem developed in the WP4 is illustrated in the figure below:





The components, as well as the interfaces, are extensively described in D4.1 and D4.2. We assume that the RF modem including antennas, RF FE, the motherboard and the PC, has been tested and is functional. In particular, the RF modem shall be capable to receive and transmit a LTE signal according to the specifications (see D4.1 and D4.2).

In WP5, it has been decided to connect Express MIMO to the WP4 modem through the FMC HPC connector (see D5.2). The resulted integration is given in the figure below:

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Figure 4-2: Integration of ExpressMIMO in the WP4 modem

Hence, the target for WP5 remains unchanged, on Virtex 5 (Express MIMO board), and the integration in WP6 will consist to connect motherboard to Express MIMO board. Therefore, we will have 2 settings for WP6:

The first setting, with external ADC, is used specifically to validate the ADC and the compare its performance to the state-of-the-art.

The second setting, with Express MIMO, is used to validate the motherboard with the internal ADC of the Lime transceiver and the dedicated algorithms from WP2.

In WP6, WP2 algorithms will be implemented in Express MIMO thanks the library, and WP3 algorithms will be implemented on the PC, since they are a part of higher layers (L3 and above). This integration is described in the SW related sections (chapter 5.1) of the present document.

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4.2 OVERVIEW OF THE BASE STATION PARTS

The base station comprises:

- An express MIMO board (host PC) and a distribution card
- An equipment to be installed in the control room beneath the mast, namely the RF Conversion TX/RX. This part is based on 4 LIME LMS6002D evaluation boards [4]. LMS6002D is a fully integrated multi-band, multi-standard single-chip RF transceiver for 3GPP (WCDMA/HSPA and LTE), 3GPP2 (CDMA2000) and WiMAX applications.
- An RF equipment to be co-located with the antennas, namely the **PA-LNA Subsystem** (PA in the Figure 4-7).



Figure 4-3: base station overview

The aim of the Express MIMO is to handle 4 data flows (MIMO 4*4), both for TX and RX. Express MIMO includes AD and DA conversion, as well as the base band processing. The interface of EXPRESS to the rest of the system in the following:

- Data interface: Express MIMO has 4 RX and 4 TX. The signals are analog (EXPRESS MIMO includes ADDAC) in base band (IF=0) and complex. The signals can be single ended (16 SMA cables, 8 for TX and 8 for RX)
- Control of the 4 LIME LMS6002D transceivers

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The host PC and the RF conversion subsystem (MIMO 4 by 4, 4 TX and 4 RX) are located in the control room beneath the mast. The RF conversion subsystem is connected to the PA-LNA subsystem trough coaxial N-type cables on the order of 30 m. The signals (8 signals, 4 RX and 4TX) are analog, at the RF frequency (800, 1900 MHz or 2600 MHz). The PA-LNA subsystem is co-located with the antennas and is contained in hermetically sealed enclosures. The eNB antennas (as an example) are from Kathrein. These are typical antennas with dual (cross) polarized ports per sector, and are furnished by EURECOM.

4.2.1 RF conversion subsystem

The figure below gives an overview of one RX/TX path in the RF conversion subsystem. This module is based on the LIME LMS6002D evaluation board.



Figure 4-4: RF conversion TX/RX

The RF conversion box (that includes the 4 TX/RX paths) is depicted in the following figures.



Figure 4-5: RF conversion sub system

4.2.2 PA/LNA subsystem description

The PA/LNA subsystem is collocated with the antennas on the pylon. As described in the below figure, the Tx signal is received from the RF conversion at a relatively low level (- 15 dBm). The signal is amplified by a 2-stage PA sub-system and feeds the switching system. On the RX side, the signal is received on the antenna, is separated from the Tx signal thanks to the switching, and filtered and then amplified by an LNA.

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Figure 4-6 : functional view of the PA/LNA sub-system

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The PA/LNA subsystem is depicted in the following picture



Figure 4-7 : PA/LNA picture

5 INTEGRATION OF THE SW PARTS

In this chapter, the integration of the WP2 and WP3 algorithms is addressed. The requirements for those algorithms were given in D6.1, and the scope of this chapter is to describe how the algorithms will be integrated in the overall demonstration activities. The software development environment that will be used to develop the applications running on the baseband processor is detailed in WP5 deliverable D5.2 "Report on SACRA embedded software library, RF/BB co-design, RF/BB interface, functional and performances validations". It is not described again in the following section.

5.1 INTEGRATION OF THE WP2 ALGORITHMS

The WP2 algorithms, described in the WP2 deliverables (from D2.1 to D2.5), will be implemented in the WP5 library. In summary, we have identified the following Phases/Tasks:

- Fixed point C implementation of the selected algorithms (sensing, signal classification techniques)
- Non real-time simulation of the algorithms in software
- Embedded software implementation of selected sensing algorithms and classification techniques using the software development kit from WP5.

As mentioned before in the introductory chapter, different algorithms provided by WP2 are serving as inputs for WP6, for implementation purposes on SACRA platform. As mentioned in Section 5.1.1, WP2 is providing a detection algorithm used to check the availability of a certain TVWS frequency band. If this band is not used by a primary (licensed) user, the platform will start using the opportunistic band as a non-licensed (secondary) user. However, during this opportunistic transmission process, there are cases when, at a given unknown time, a primary user starts reusing, or it starts using for the first time the same frequency band currently used by the SACRA platform. If this happens, classification algorithms implemented on the SACRA platform are necessary to discriminate between the primary user transmissions and secondary user transmissions received by the SACRA platform. This concept is further described in Section 5.1.2.

5.1.1 Detection - Proof of Concept

The goal of this chapter is to describe integration settings of the detection algorithms used to check the availability of certain TVWS band. Three algorithms will be integrated to the demonstrator: energy detection, Welch periodogram based detection and pilot based detection.

Welch periodogram based detection

Welch periodogram based detector can be used in sensing both PMSE and DVB-T primary systems. Integration requires a SACRA platform, embedded software implementation of the detector and a signal generator for generating PMSE and DVB-T signals. The purpose of integration is to find proper settings for the algorithm parameters to be able to perform the demonstrations. Welch periodogram based detection algorithm is configured with the following parameters:

- FFT size
- Number of frequency domain samples in the band of interest
- Frequency bin number of lower edge of the band of interest

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- Number of segments
- Target false alarm probability

The following data are to be monitored by user:

- Sensing status (signal found / not found)
- Detected energy value

The most important thing in the integration is to find out required sensing time of the algorithm for both the possible primary systems according to the requirements specified in D6.1. Sensing time is controlled with two parameters: FFT size and Number of segments. All the other parameters are needed in the search as well. Performance of the sensing is critical to detection threshold setting. For a proper setting, the target false alarm probability should be user defined and noise variance should be estimated precisely. This can be done best by receiving noise only signal until the estimate is precise enough. Welch periodogram based sensing algorithm demonstrations will be started in noise only situation and after certain time the primary user(s) are turned on.

Welch periodogram based detector demonstrations will produce data for performance comparison of different detection algorithms in real situation.

Energy detection

Energy detector will be used to detect PMSE primary signal. This detector can be simply implemented like spectrum analyser. It measures the received energy during a finite time interval and compares it to a predetermined threshold. The main advantage of this detector is its non-coherency and low complexity. To implement this detector, we need to estimate the noise variance and to define false alarm probability.

Pilot based detection

Pilot based detector is described in D2.2. This detector will be implemented for DVB-T primary signal detection. We will exploit pilot sequences which are integrated in the transmitted signal. These predefined pseudo-noise sequences are used generally in order to estimate the channel conditions. Alternatively, in multicarrier transmissions such as DVB-T some subcarriers may be dedicated for transmitting pilot signals. Pilot signals may be scattered over the subcarriers and over the time depending on the coherence time and coherence bandwidth of typical channel. The primary user standards are usually known and these sequences are defined correspondingly. Based on the knowledge of these sequences, we will implement this detector with a simple correlation between the received primary user signal and the pilot sequence. As in the case of energy detector and Welch detector, we need to estimate for this detector false alarm probability value.

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5.1.2 Classification - Proof of Concept

The goal of this section is to describe the integration settings to be used by a demonstration platform which performs signal classification in order to discriminate between the primary user (PMSE or DVBT) transmissions and own secondary system transmissions (LTE).

It is important to mention that an alternative for the proposed method is to use a technique employing Quiet Periods (QPs), and the advantage of this method would be that it requires a detection algorithm similar to the one used in Section 5.1.1, which is less complex. However, such a technique using QP is very disadvantageous:

- Firstly, if the secondary system uses QPs, this will directly impact different Quality of Service (QoS) parameters of the secondary system such as the transmission delay. For example, it will be impossible to use such a system for voice calls or other services which demand very low transmission delays. If the system stops transmitting more often (for sensing purposes in our case), the expected communication quality of the user will be very low.
- Secondly, the entire secondary system has to synchronize its users to stop transmitting at a
 given time, otherwise own secondary transmissions would be interpreted as primary
 transmissions. In this case, false alarm probabilities will be imminent even if very low target
 false alarm probabilities are imposed by the system itself, and this will affect again the
 secondary system Quality of Service (QoS), as the secondary system will stop transmitting
 even if primary users are not present. As previously mentioned, QP is a possible option
 used to overcome this problem, but this option is very expensive from the secondary
 system point of view, as it demands huge amount of signalling between the secondary
 users for synchronization.

For all these reasons, SACRA opted for classification instead of using Quiet Period techniques, and as explained in the next sections.

5.1.2.1 LTE incumbent classification without Quiet Period

As shown in the figure below, the proposed solution for the demonstration platform consists of the following materials:

- 1 LTE transmitter operating in TVWS (eNodeB from EURECOM), which will transmit the signal (2)
- 1 LTE transmitter operating in 2.4GHz (optional for this demo), which will transmit the signal (1)
- 1 PU generator (PMSE or DVB-T provided by EURECOM) with manual/automatic ON/OFF switch, which will transmit the signal (3)
- 1 Classification device (e.g., SACRA Platform) capable of detecting PU while LTE is transmitting





Figure 5-1: Demonstration Platform

This demonstration scenario considers a DL FDD LTE transmission coming from an eNodeB using the non-opportunistic frequency band (see signal (2) on the figure). The SACRA platform aggregates spectrum from two different frequency bands: (1) the licensed LTE band (2.4GHz) and (2) the non-licensed (TVWS) band. The signal classification will be performed only on the non-licensed TVWS band, as shown in the figure. Finally, the demonstration platform informs only if PU (3) is transmitting or not.

The MATLAB analysis from WP2 shows that the cyclostationary property, and more precisely the cyclic autocorrelation function (CAF) of the PU (PMSE or DVBT), can be used to discriminate PU from SU (LTE in our case) – as shown in the Figures below and in D2.2.





Figure 5-2: LTE / DVBT discrimination (a) and LTE / QPSK PMSE discrimination (b)

Simulations performed in MATLAB (see D2.2) have considered a 8 MHz DVB-T signal with 224 µs useful symbol and a cyclic prefix equal to ¼ of the useful symbol period, while the LTE configuration was of 10 MHz bandwidth, with normal cyclic prefix. However, as described in D2.2, other configurations are also possible.

The platform will use parameters obtained from D2.2, such as necessary classification time or the classification period (see Figure below).

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Figure 5-3: Classification Time and Classification Period

Simulation results from D2.2 show that there are several design parameters that have to be taken into account, with respect to the FCC sensing requirements. Some of these parameters are the classification time, the SNR received in DL from the non-licensed LTE system, the LTE bandwidth configuration (which will impact both the noise power and the sampling frequency being used), and the noise figure of the amplification chain.

The main goal of the contribution is of course to demonstrate the classification capabilities. However, the purpose is also to deal with the possible implementation issues on the platform such as:

- System-related implementation issues, e.g., processing time, quantization problems, differences between floating point (MATLAB representation) and fixed point (Hardware Platform).
- Memory-related implementation issues, e.g., the memory necessary to save all samples useful for signal classification, from the measured signal.
- Hardware-related implementation issues, e.g., extra noise generated by the RF amplifiers, the noise figure, the variation of the noise temperature, or other interfering sources which would be interpreted as noise.

5.1.2.2 Signal Classification combined with Signal Separation

In a wideband cognitive network cognitive terminals continuously sense the entire wideband spectrum to locate spectrum holes. Once a spectrum hole has been identified, cognitive terminals can access the frequency band under certain utilization or allocation strategies. While one spectrum hole is in use, other cognitive terminals keep on sensing, so that once the spectrum hole is available again, it can be detected immediately.

The proposed solution to classify the multiple signals occupying the same spectrum bands, can be summarized in three steps:

- 1) Separate mixed signals occupying wideband frequency.
- 2) Analyze separated signals.
- 3) Classify the separated signals.

We propose a two-step algorithm to separate signals over the wideband spectrum in a cognitive network. As a result, the separated signals can be references for cognitive networks to develop new communication strategies against hostile terminals. The steps are listed as follows:

1) Frequency Edge Location: Frequency edge is a frequency point where spectrum changes intensely. Detecting frequency edges would provide brief information about the occupancy of the wideband frequency.

2) Signal Separation: Separating signals occupying the wideband frequency will provide detailed information about the usage of wideband spectrum.

5.2 INTEGRATION OF THE WP3 DEMONSTRATION

As described in chapter 1.1, WP3 will be verified in a separate demonstration. The main reason of this separated demonstration is that the WP3 work deals with scenarios where a large number of UEs are present. The restrictive case with one UE equipment has a very limited interest for RRM algorithms, and for instance resource allocation. These integration settings will be described in a subsequent deliverable of WP6. However, a brief description of the forthcoming plan will be provided here. This analysis will set the basis for the side demo activities of WP3 which will be reported in the upcoming deliverables of WP6.

The WP3 algorithms have been described in the WP3 deliverables (D3.1 and D3.2). The algorithms are applicable in scenarios that involve the existence of multiple primary and secondary users. These scenarios go beyond the scope of the demo scenarios that were identified in D6.1. Moreover, platform's capabilities are limited and do not allow us to tune the values of specific parameters required for the execution of CRRM algorithms. These barriers cannot be surpassed and based on the fact that an emulation driven approach is of no interest (as the application of the algorithms in other wireless technologies besides LTE, is out of SACRA scope) the only option for a side demo activity is a simulation driven demo that will provide the Proof of Concept (PoC) of the CRRM system. This demo activity could potentially be divided in the Phases/Tasks given below:

- Separate and non real-time simulation of the algorithms in software
- Integrated simulation of the CRRM components based on a side demo scenario

During the first phase WP3 partners will conduct separate simulation experiments which will be based in a common scenario. Thus, the same set of inputs and parameters will be used as a basis

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for these experiments and afterwards, during the second phase WP3 partners will collaborate to provide an integrated simulation of the CRRM components based on the identified scenario.

The algorithm for Cooperative Power Control, developed in terms of WP3 (D3.1 and D3.2) focuses on the case of nodes of different secondary systems (e.g. different operators in the TVWS bands). Each user selects its transmission power level by trying to maximize a utility function which takes into account the benefit of the transmission power level to the bit rate and the interference this transmission power causes to the neighbouring users. An asynchronous message exchange scheme ("interference prices") is required for the cooperation between the nodes; such asynchronous scheme has the deficiency that the network elements may not have the latest view of the network. Thus, a fuzzy logic scheme is utilized so as enhance situation awareness of each node, and alleviate uncertainties that cause underestimation of the interference. Finally, supervised learning techniques are enforced to improve the environmental perception of each node.

The demo scenario that will be considered for the evaluation of Cooperative Power Control is illustrated in Figure 5-4.



Figure 5-4: Cooperative Power Control algorithm scenario

In this scenario we assume the presence of five cognitive users in the area under consideration; these users are assigned into two different operators. Each eNodeB gathers information from the aforementioned users and disseminates it to the others attached to it and through X2 interface, to terminals operating in other eNodeBs. The information exchanged includes the interference each user perceives from other users (that are associated to other operators) and the transmission power of the user.

The two asynchronous phases of the algorithm are illustrated in Figure 5-5 (a)**Erreur ! Source du renvoi introuvable.** and in Figure 5-5 (b). More specifically, these figures show how each node autonomously calculates the transmission power and the interference it perceives from the others.

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Figure 5-5 (a) Transmission Power calculation phase (b) Interference Price calculation phase

Finally, Figure 5-6 shows the message exchange scheme where each user disseminates its transmission power as well the interference it perceives from other users. Furthermore each user receives from the eNodeB a message with the interference prices of the other users that are present in the area under consideration.

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Figure 5-6: Message exchange scheme of the Cooperative Power Control Algorithm

5.3 SUMMARY OF THE INTEGRATION SW

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As described in the above paragraphs, some parts of the SW development of WP2 and WP3 will be integrated in the final demonstrator of WP6. Some other parts will be only simulated.

The following table illustrates the various demonstration activities that will be on the one hand implemented in the overall demonstrator in real time and on the other hand the activities that will be only simulated.

Demonstration Activities			
Spectrum Aggregation	Real Time On Air		
Sensing	Real Time On Air		
Classification	Real Time On Air		
CRRM	Simulation		
Polarization MIMO	Simulation		

Table 5-1 Demonstration activities

6 SACRA METRICS

6.1 INTRODUCTION

This chapter gives information about the metrics of the SACRA terminal and the base station used in the described scenarios. The metrics are related to:

- Energy efficiency,
- Spectral efficiency and occupancy
- The minimization of the number of electronic components.

The major outcome of the implementation of the SA scenario is a proof-of-concept able to:

- Communicate cognitively in real time, which corresponds to concrete needs today in Europe
- Validate the WP2 techniques for spectrum efficiency and occupancy
- Validate the WP4 techniques for the energy efficiency in a realistic environment
- Validate the WP5 approach of baseband architecture in term of minimization of the number of components in terminals.

The WP6 demonstration will provide figures for those metrics for a specific USE CASE, the spectrum aggregation of a licensed 2.6 GHz band with the TVWS band.

6.2 SPECTRUM EFFICIENCY AND OCCUPANCY METRICS

In the TVWS band, the primary users are mainly TV channels. The following picture illustrates a typical use of the band 400 to 800 MHz.



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Figure 6-1: Spectrum occupancy in TVWS

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This picture, taken with a spectrum analyser, represents the spectrum occupancy in Sophia Antipolis. We can distinguish some channels, but also many holes in the spectrum. In this area we assume spectrum occupancy of 30 %.

With the technique developed in SACRA, we can use our sensing algorithms to monitor the TVWS, and therefore we can use these channels opportunistically. In this case, we can occupy the overall band theoretically (fill all the spectrum holes). Therefore the spectrum occupancy increases by a factor 3 in this band. Since the resources are allocated in the TVWS band, we can save resources in the licensed band, and more users/services can be handled by the licensed eNodeB. Thus the overall system is more efficient.

6.3 ENERGY EFFICIENCY

As stated in D6.1, the integration of all the building blocks in the SA scenario in WP6 will be inefficient from an energetic point of view. Indeed, the SACRA demonstrator (with its FPGA and the PC) will have an electric consumption of more than 100 Watts. This is founded in the prototype development that is relatively far from a commercial terminal or a femto base station.

However, we can have some figures concerning energy efficiency, for example at the terminal point of view. On the TX of the terminal, one objective is to enhance the efficiency of the Power Amplifier (PA). A good way to measure the effective gain in power is to compare the transmitted power at a given Adjacent Channel Leakage power Ratio (ACLR) with, and without the techniques developed in WP4. This approach is developed in the next sections.

6.3.1 Tx signal quality in LTE

As stated in the 3GPP 36.101, the output UE transmitter spectrum consists of the three components; the emission within the occupied bandwidth (channel bandwidth), the Out Of Band (OOB) emissions and the far out spurious emission domain.



Figure 6-2: Transmitter RF spectrum

The out of band emissions, are unwanted emissions immediately outside the assigned channel bandwidth resulting from the modulation process and non-linearity in the transmitter but excluding spurious emissions. This out of band emission limit is specified in terms of a spectrum emission mask and an Adjacent Channel Leakage power Ratio (ACLR).

Adjacent channel leakage power ratio is the ratio of the filtered mean power centred on the assigned channel frequency to the filtered mean power centred on an adjacent channel frequency.

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ACLR requirements are specified for two scenarios for an adjacent E -UTRA and /or UTRA channel as shown in Figure 6-3.



Figure 6-3: Adjacent Channel Leakage requirements

E-UTRA Adjacent Channel Leakage power Ratio (E-UTRA_{ACLR}) is the ratio of the filtered mean power centred on the assigned channel frequency to the filtered mean power centred on an adjacent channel frequency at nominal channel spacing. The assigned E-UTRA channel power and adjacent E-UTRA channel power are measured with rectangular filters. If the measured adjacent channel power is greater than -50 dBm then the E-UTRA_{ACLR} shall be higher than the value specified in Table 6-1.

	C	Channel bandwidth / E-UTRA _{ACLR1} / measurement bandwidth				
	1.4 MHz	3.0 MHz	5 MHz	10 MHz	15 MHz	20 MHz
E-UTRA _{ACLR1}	30 dB	30 dB	30 dB	30 dB	30 dB	30 dB
E-UTRA channel Measurement bandwidth	1.08 MHz	2.7 MHz	4.5 MHz	9.0 MHz	13.5 MHz	18 MHz
Adjacent channel centre frequency offset (in MHz)	+1.4/-1.4	+3.0/-3.0	+5/-5	+10/-10	+15/-15	+20/-20

Table 6-1 : General requirements for E-UTRA_{ACLR}

6.3.2 Energy efficiency improvement

Granted that without the WP4 techniques, i.e. with the SOTA, we can achieve a transmitted power of +23 dBm (200 mW) with an output signal compliant to the E-UTRA requirements. If we can increase the transmitted power by 3 dB (+26 dBm) with the techniques developed in SACRA (DPD and PAPR), it means that we have gained a factor 2 in term of efficiency.

This improvement has to be compared with the processing power we need for the processing of the algorithms. If we subtract the loss due to the extra-processing from the gain in efficiency in the PA, it will give us the actual figure in terms of energy efficiency improvement.

6.3.3 Energy efficiency of the baseband processor

As described in WP5 deliverables, WP5 aims at developing a baseband architecture (hardware and software) with the Software Defined Radio (SDR) approach, that is, capable of handling

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completely different radio access technologies with the same, fixed, set of processing units. WP5 reuses existing hardware blocks designed in the context of other projects. Some of them are slightly adapted to better suit the needs of SACRA but most of the WP5 work aims at providing tools and software libraries to ease the design and validation of SACRA baseband applications. WP6 demonstration will validate this approach, thanks to a realistic demonstration, for example we will be able to switch between 2 different waveforms.

As already stated, the SACRA baseband processor is FPGA-based and its energy figures are orders of magnitude higher than that of a real baseband Integrated Circuit (IC). The complete design and manufacturing of a baseband IC is out of scope of SACRA because the costs and efforts would be much higher than what is actually available. Even pre-tape-out power simulations require the full design effort that would be necessary to manufacture an IC and the available resources are not sufficient to reach this point. FPGA-based target technologies are preferred for their much shorter design cycles and much lower prices in low volumes. It is thus very difficult to provide accurate silicon area or power consumption figures of the SACRA baseband processor. However, the baseband architecture is 100% compatible with the manufacturing technology of ICs and, in a commercial product, the FPGA-based prototype would be replaced by a single baseband IC, with much smaller silicon area and much better performance and energy efficiency.

Even without accurate power estimates, a fair reasoning shows that, compared to more classical approaches, the SACRA baseband processor improves the energy efficiency of the terminal:

With the SDR approach, and in a commercial product, the power management would be more efficient than with classical approaches, as it would optimize the power across all current baseband activities (communication, sensing, etc.) instead of a local-only optimization. The clock frequency and voltage level of each processing unit would be selected according the full instantaneous load of the unit, not only the load due to a specific Radio Access Technology (RAT). With several baseband processors, each dedicated to a given set of RATs, the clock frequencies and voltage levels of some processors would be high while others would be idle, depending on what actually takes place in the terminal. This highly imbalanced load is a well known source of energy inefficiency that every system designer tries to avoid. The following example illustrates this on a single processing unit:

We assume a classical system, S1, and a SDR one, S2. S1 embeds two completely independent vector processors, in two different ICs, for two different RATs. They share about the same characteristics because the two RATs, while different, have about the same vector processing needs. In S2, a single, twice more powerful vector processor, is used to implement both RATs simultaneously if required. In both systems the power management uses a Dynamic Voltage and Frequency Scaling (DVFS) strategy to reduce the instantaneous power. When the two systems are fully loaded, their vector processors consume the same power:

$$P(S_1) = P(S_2) = 2 \times K \times F_{high} \times V_{high}^2$$

where *K* is a normalization factor, F_{high} is the highest clock frequency and V_{high} is the highest voltage. When only one of the two RATs is active, it fully loads one of the two vector processors of S1; the second is idle (we neglect its static power consumption). In S2, the clock frequency is divided by two and the voltage is also scaled down:

$$P(S_1) = K \times F_{high} \times V_{high}^2 > P(S_2) = 2 \times K \times \frac{F_{high}}{2} \times V_{low}^2$$

where V_{low} is the lowest voltage at which the vector processor of S2 runs at a F_{high} / 2 clock frequency. In average, the savings are significant, especially when considering not only one processing unit and two RATs but all processing units and all baseband processing.

The sharing of processing units among all baseband activities allows more efficient power savings than separate dedicated units. It is the strategy used in the SACRA platform and the reason why we claim that the SACRA baseband is beneficial in terms of energy efficiency. Moreover, as

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already explained, its flexibility can be used to implement specific power saving digital processing, like Peak to Average Power Ratio reduction and Digital Pre-Distorsion.

6.4 MINIMIZATION OF THE NUMBER OF ELECTRONIC COMPONENTS

In SACRA, 2 activities address this topic, namely the WP5 baseband architecture and the WP4 modem.

6.4.1 WP5 baseband architecture

Compared with more classical approaches, and even without accurate silicon area estimates, we can state that the SDR approach significantly reduces the number of components: one single processor handles all RATs, plus the specific Cognitive Radio (CR) baseband processing, like sensing or classification. With more conventional solutions, a high end terminal would embed dedicated ICs for several RATs (Bluetooth, GPS, GSM, GPRS, EDGE, UMTS, HSPA, LTE, WiFi,...) and the number of components would be significantly larger. So, the SACRA approach indeed reduces the number of components.

Of course, if manufactured with an IC technology, the silicon area of a SDR baseband processor as the one of SACRA would be much larger than the silicon area of a single very optimized GSM IC, for instance. But if we consider the sum of all the silicon areas of all dedicated ICs, an SDR solution is obviously less expensive.

Moreover, advanced RATs, like LTE-A, are so rich and so flexible in nature that a LTE-A dedicated baseband processor would already embed almost everything that is also required by most of the other RATs and would already be almost as flexible as required by an SDR processor.

Last but not least, our approach allows software adaptations to new RATs or modifications of existing RATs without hardware redesign, which is really beneficial in such a fast moving environment.

6.4.2 Tuneable elements in WP4

As described in D4.2, IIS is developing a 32-position tuneable filter. The frequency response (depending on the position) is depicted in the figure below.

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Figure 6-4: frequency response of the tuneable filter prototype

In order to implement the SA scenario on the overall TVWS band, it is clear that such a filter is needed. The other solution is to implement a switched filter bank, which is not very practicable. The gain in terms of reducing the number of component is obvious, since it allows the use of the same filter for different bands.

An exact figure of the gain profits by this approach in the overall RX/TX chain is difficult to calculate, since filtering is only a part of the processing. According to our experience in modem design, a coarse figure is 10 % in terms of decrease the number of components.

7 DEMONSTRATOR INTEGRATION STAGES

This chapter gives a schedule for the step by step integration procedure and corresponds to the integration stages of the WP6 demonstrator. It consists of two tables, separated for HW and SW integration. With this schedule a good integration is ensured at the end of the project. Furthermore these tables show, with which WP or task we are going to handle the test to be performed in order to validate the various stages of integration.

Of course, in order to perform the integration, the building blocks have to be ready for integration, according to the specifications

WP/Task	Planned deliverable time	Action item until deliverable time	Responsibility	Test for the validation of stage
WP4/Task 2/ ADC	February 2012	Design of the test card and evaluation of the stand-alone ADC	Hussein Fahkoury (IT)	Evaluation of ADC performance (SNR,)
WP4/Task 2/tBPF	February 2012	1 st prototype of the tBPF-600	Alexander Jaschke (IIS)	Insersion loss, programmability test with a Network analyzer
WP4/Task 1/Antenna	February 2012	Antenna Design for diversity including UHF TVWS lower freq.band	Alexander Popugaev (IIS)	S11 measurement (or ROS) with a Network analyzer
WP4/Task 1/Antenna	February 2012	Manufacturing and measurement of several prototypes of antennas	Anne Claire Lepage (IT)	S11 measurement (or ROS) with a Network analyzer
WP4/Task 2/AFE Extension	February 2012	AFE extension PCB for versatile MIMO investigations	Andreas Mayer (DMCE)	Measurement of Insersion loss, programmability test with a Network analyzer
WP4/Task 2/tBPF	Juliy 2012	2 nd prototype of the tBPF-600 and tBPF-2000	Alexander Jaschke (IIS)	Geometry, Insertion loss, attenuation in stop-band
WP6/Task 3	September 2012	Eurecom platform available for integration	Dominique (Eurecom)	Test of RX/TX from the PC to the antenna port, with a LTE signal as an input
WP6/Task 3	September 2012	Dual TX demonstration setup	Andreas Mayer (DMCE)	Test of the 2 TX, measurement of

Schedule for the HW integration:

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				synchronization
WP4/Task 4	October 2012	Integration of the SACRA modem Control	Dominique (Eurecom)	Test of the various modes (FDD/TDD), bands, gains
WP6/Task 4	November 2012	Trials in real time with the overall SACRA platform	Dominique (Eurecom)	End-to-End communication with SA on 2 bands
WP6/Task 4	December 2012	Measurements of the SACRA indicators	Dominique (Eurecom)	Validation of the expected improvements (see chap.6)

Schedule for the SW integration:

WP/Task	Planned deliverable time	Action item until deliverable time	Responsibility	Test for the validation of stage
WP5/Task 3	July 2011	Design of software library	R. Pacalet (IT)	Design of example applications (synchronous version). Validation on PC. Done end Feb. 2012 for Energy and Welch Periodogram Detectors.
WP5/Tasks 2,3 and 4	July 2012	Updates of SW library, design of SW generators, integration in SDK	R. Pacalet (IT)	Parallelisation of example applications. Validation on virtual prototype. Done end Feb. 2012 for Welch Periodogram Detector.
WP6/Task 2.1	July 2012	Implementation of WP2 algorithms using SW library (fixed point, untimed)	R. Pacalet (IT)	All selected applications (synchronous version) designed.
WP6/Task 2.2	July 2012	Validation of fixed point, unitimed, implementation of WP2 algorithms	R. Pacalet (IT)	Functional validation on PC by comparison with Matlab reference model.

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WP6/Task 2.3	September 2012	Refinement of fixed point, unitimed, implementation of WP2 algorithms for real time, parallel execution on SACRA platform	R. Pacalet (IT)	All selected applications parallelized.
WP6/Task 2.3	September 2012	Validation of real time implementation of WP2 algorithms on SystemC virtual prototype	R. Pacalet (IT)	Validation on virtual prototype by comparison with Matlab reference model and performance specifications.
WP6/Task 2.3	October 2012	Validation of real time implementation of WP2 algorithms on SACRA platform	R. Pacalet (IT)	Validation on SACRA platform by comparison with Matlab reference model and performance specifications.
WP2	December 2011	WP2 algorithms delivered in WP2 deliverables	A. Hekkala (VTT)	Evaluation of algorithms by simulations
WP2	April 2012	WP2 algorithms implemented using C library	A. Hekkala (VTT)	Validation of algorithms functionality in C

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8 CONCLUSION

In this document, we have refined the specifications of the building block that will be conducted to WP6. An equipment specification shows the components used for the selected scenarios described in D6.1 and D1.1. Chapter 3 describes the specification needed for the selected SACRA scenario. Closely linked to WP5, chapter 4 (Integration of HW parts) and chapter 5 (Integration of SW parts) consists of integration specifications to combine all parts developed in WPs 2, 3, 4 and 5.

Chapter 6 consists of information about SACRA metrics like spectrum efficiency / occupancy, energy efficiency and decreasing the number of components. Moreover this chapter describes the handling of these indicators for each WP.

The present document can be seen as a schedule for the activities in WP6, especially illustrated with tables in chapter 7 (step by step integration).

Summarized this document consists of:

- Refine the specifications of the building blocks
- Ensure efficient integration at the end of the project

The next steps will be:

- To integrate HW components to experimental sites
- To integrate SW components to experimental sites

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10 ACRONYMS

ADC	Analog Digital Converter
BB	Baseband
CAF	Cyclic Autocorrelation Function
ChX	Channel X
DAC	Digital Analog Converter
DL	Downlink
DVB-T	Digital Video Broadband Television
eNodeB /eNB	Enhanced Node B
FCC	Federal Communications Commission
FDD	Frequency Division Duplex
FFT	Fast Fourier Transformation
FPGA	Field Programmable Gate Array
HW	Hardware
JRRM	Joint Radio Resource Management
LNA	Low Noise Amplifier
LTE	Long Term Evolution
МІМО	Multiple Input Multiple Output
РА	Power Amplifier
PMSE	Programme Making and Special Events
PU	Primary User
QoS	Quality of Service
QP	Quiet Period
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RRM	Radio Resource Management
Rx	Reception
SA	Spectrum Aggregation
SNR	Signal to Noise Ratio
SU	Second User
SW	Software
tBPF	tunable Band Pass Filter
TVWS	TV White Spaces
Тх	Transmission
UE	User Equipment
UHF	Ultra High Frequency