GREEN Silicon: ICT FET Project No. 257750
Deliverable D5.10 Identification of Potential Production Process

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Discussions for this section of the report were held with members of the GREEN Silicon industrial advisory committee and included:

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The above list of companies represents a complete supply chain from the material supply (Johnson-Matthey) and growth (IQE, Oerlikon) through MEMS fabrication (Semefab & Micropelt) to thermoelectric device manufacturers and suppliers (Micropelt, O-flexx and European Thermodynamics). Production would require this complete supply chain to be in position although some of the areas could be integrated into the fabrication line e.g. the epitaxial growth.

From the start, the GREEN Silicon project has developed material and fabrication processes that can be undertaken on 200 mm diameter silicon wafers and for the majority of steps, commercially available tools have been used. The project design had the aim to allow successful technology to be exploited on silicon MEMS foundries if the research became successful. Here we will detail the processes and explicitly state where processes will have to be changed for production of modules at a wafer scale.

The growth in the project has used low-energy plasma enhanced chemical vapour deposition with systems capable of growing on 200 mm diameter silicon wafer. Such epitaxial growth systems are not available commercially but ASM, Leybold and Applied Materials all sell 200 and 300 mm SiGe epitaxial growth systems that are used in a large number of CMOS, BiCMOS and MEMS foundries and could easily be used to grow the epitaxial designs from this project. In all cases, the turbo pumped options for all of these systems is required due to the partial pressure of water vapour so that low temperature epitaxy can be undertaken without substantial oxygen content. Also there are a number of epi-houses who could supply the superlattice designs grown on 150, 200 or 300 mm diamater wafers such as IQE.

It is clear from the work in GREEN Silicon that all epitaxy is required on SOI substrates to provide electrical substrate isolation. In a production process, CMP could potentially be used to remove the SOI requirement from at least one of the substrates thereby reducing cost. Also the SOI used in the GREEN Silicon project had a 1 μm SiO_2 layer and required a strain relaxation buffer. IQE and SOITEC sell relaxed SiGe on insulator wafers that would allow higher performance thermoelectric modules to be designed and produced with far thinner buffers and electrical isolation oxides. For example, the performance of the modules will increase as the buried SiO_2 layer is reduced in thickness and so a 10 nm or so SiO_2 or Si_3N_4 buried layer is more than adequate for a production process. Indeed the Si_3N_4 would be superior to SiO_2 as the thermal conductivity is 19 times higher thereby improving the thermal resistance from the heat source and cold sinks to the module legs for electrical generation.

For the fabrication of the devices, most MEMS foundries with the addition of epitaxy (or the purchase of epitaxy from a subcontractor such as IQE) already have all the tools required to produce thermoelectric modules. Some CMOS or BiCMOS foundries would require additional packaging for the flip-chip bonding but most would be able to process the modules.

The fabrication process at UGLA used contact printing optical lithography which could be used in production but a stepper would be more appropriate in production processes. As the minimum resolution for modules is > 5 μm and layer-to-layer alignment of > 5 μm is required, the optical lithography requirements are not difficult to achieve in a production environment. An anisotropic SiGe etch is required and in the GREEN Si project, a commercial STS ICP deep Si etch tool using a variety of the Bosch process with SF_6 and C_4F_8 gases was used. Many manufacturers produce similar tools and STS tools using similar processes are common on many MEMS foundries. Applied Materials, Alcatel and Oxford Instruments also sell appropriate tools.

A sputter tool is required for the Ohmic contacts and the metal interconnects. Most MEMS foundries al-

ready have suitable tools. Ni is required for the Ohmic processes and a silicide like process was used which is similar to that used by Intel, TSMC and Global in their 45 nm CMOS processes. For GREEN Silicon no diffusion barriers were used but a TaN or TiN diffusion barrier would be required especially if Cu interconnects would be used in place of Al to prevent diffusion of interconnect metal into the thermoelectric legs. For GREEN Si, Al interconnects were used but Cu would be the preferred option to minimise the series resistance. Some MEMS foundries have Cu interconnect processes although most use Al.

For production thermoelectric devices, a "barrier" layer is normally placed around each leg to minimise oxidation or any reactions with the environment so that the thermoelectric material does not degrade. Time prevented such barrier layers being developed in GREEN Silicon although at the < 100 ˚C temperatures this was not an issue for the SiGe materials used. This can be a major issue with some exotic materials but for SiGe it is not a major issue unless the module is expected to perform above 500 ˚C. PECVD SiN or preferable ALD SiN could be used to form thin (< 5 nm thick) barrier layers around each leg after the Ohmic contacts have be produced. Such thin SiN barrier layers should not have any significant effect on the thermal or electrical properties as the legs are many 100s of μm in diameter.

The GREEN Si project has used In bumps for flip-chip bonding. This is a fairly standard bump bonding process which is used by many MEMS foundries in production and is appropriate for modules with operating temperatures up to ~100 ˚C. If the modules are to be used with higher temperatures then a new production process would be required. There are some examples of bumps that can withstand 220 ˚C [1] using Cu bumps but most of the Cu bump processes use AuNi eutectics which reflow at 260 ˚C and are therefore not suitable for high temperature operation of the modules. A Au free process would have to be developed for production if high operating temperatures for the modules was required for e.g. automotive applications.

In the GREEN Silicon project, the Si substrates were not thinned. The module performance could be improved by thinning the silicon on each side to improve the thermal conductance to the legs. These thinning processes are standard in many MEMS foundries either using polishing or CMP and could easily be added in a production process for higher performance.

A final process that could be added at the production stage is metal on the backside of the (thinned) wafers to improve the thermal contact to the heat source and cold sink to the device. Again time prevented this being developed in the GREEN Silicon project but the appropriate processes are already available on many MEMS production lines.

Before the thermoelectric modules could be sold, accelerated lifetime testing is essential to understand if the production processes and materials are sufficiently robust for a range of the potential applications. This has not been undertaken inside the GREEN Silicon project but it should be noted that a range of MEMS products such as gyroscopes and accelerometers are used in similar environments and using similar production processes. Therefore with the appropriate integrated production processes, such microfabricated thermoelectric modules should have sufficient lifetimes for the majority of the proposed applications for thermoelectrics.

References

[1] S.A. Khan et al., "Multichip embedding technology using fine-pitch Cu-Cu interconnections" IEEE Trans. Componets, Packaging & Manufacturing Technol. 3(2), 197 (2013)