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Glossary of Abbreviations

BER	Bit Error Rate
BERT	Bit Error Rate Test set-up
BCB	Benzo-chloro-butene
CPM	Clock Phase Margin
CPW	CoPlanar Waveguide
DC	Direct Current
DCF	Dispersion Compensating Fibre
DFB	Distributed FeedBack laser
DFF	D-Flip-Flop
DEMUX	Demultiplexor
DER	Dynamic Extinction Ratio
DUT	Device Under Test
EAM	ElectroAbsorption Modulator
EML	Electroabsorption Modulated Laser
ESD	ElectroStatic Discharge
FWHM	Full Width at Half Maximum
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
MBE	Molecular Beam Epitaxy
MOVPE	Metal Organic Vapour Phase Deposition
MZM	Mach Zehnder Modulator
NRZ	Non Return to Zero
OEIC	OptoElectronic Integrated Circuit
OOK	On Off Keying
OSNR	Optical Signal to Noise Ratio
OTDM	Optical Time Division Multiplexing
PD	PhotoDiode
PDL	Polarisation Dispersion Loss
PMD	Polarisation Mode Dispersion
PMMA	Poly Methyl Metacrylate
PRBS	Pseudo Random Bit Sequence
QAM	Quadrature Amplitude Modulation
QCSE	Quantum Confined Stark Effect
QPSK (D-, PM-)	Quadrature Phase Shift Keying (Differential-, Polarization Multiplexed-)
QW	Quantum Well
RMS	Root Mean Square
RX	Receiver
RZ	Return to Zero
SDH	Synchronous Digital Hierarchy
SMF	Single Mode Fibre
SIBH	Semi Insulating Buried Heterostructure
TX	Transmitter
TWA	Travelling Wave Amplifier
WDM	Wavelength Division Multiplexing
3R	Reamplifying, Retiming, Reshaping regenerator

1 Executive Summary

The "Monolithic InP-based Dual Polarization QPSK Integrated Receiver and Transmitter for CoHerent 100-400Gb Ethernet" (MIRTHE) project was a 40-month duration (2010-2013) FP7 EU project (Proposal No. IST-257980) founded by the European Commission whose goal has been to achieve a component technology support for 10-fold increase in the capacity of the Internet backbone network, by developing innovative highly integrated transmitters and receivers that make use of Photonic Integrated Circuits (PICs) on Indium Phosphide, the unique semiconductor material family providing all-monolithic integration ability of all passive and active functions for high-speed integrated circuits at telecommunication wavelengths.

MIRTHE's partners represent a broad cross-section of the European Information and Communications Technology ICT industry and academia who played the following roles: **III-V Lab** for transmitter PICs fabrication; **Fraunhofer Heinrich-Hertz-Institute** for development and fabrication of receiver PICs; **Alcatel Lucent Bell Labs** for system environment testing and validation of modules; **U2T Photonics AG** for packaging and integration; **VPIphotonics GmbH** CAD model development and simulations; **University of Málaga Communications Engineering Group** passive photonic device design for polarization multiplexing and novel receiver concepts. Very complementary partnership covered all required MIRTHE expertise. Low number of partners played in favor of prefect identification of all with common targets, of personal contacts and very efficient exchanges making easier the project work and management.

MIRTHE introduced major innovative concepts to produce advanced format transmissions with all-monolithic InP circuits as optical phase switching transmitter, multi-format universal electronics DAC driver and receiver with on-chip polarization management. The project work included therefore important realization risks which have been worthy to be taken as the proposed solutions promised lowest footprint and low energy consumption in addition to full monolithic integration, the keys to cost sensitive markets. These risks made the project life technically complex with exciting but also with hard periods leading often to delays and contingency managements.

Finally however, MIRTHE has delivered all major project commitments. Specifically the following goals have been demonstrated:

- Novel monolithic InP QPSK transmitters based on prefixed phase switching using very small size Electro-Absorption Modulators operating up to 130 Gb/s
- New close to product, all monolithically integrated, dual polarization receiver has been developed and has shown operation with 16QAM at 56Gbaud thus showing a total bit rate of 450 Gb/s.
- New packaging technologies required by high compactness of TX and RX chips
- Novel universal multi-format Digital-to-Analog-Converters directly providing digital output compatible with Electro-Absorption Modulator switching
- World first all-monolithic InP PIC to PIC experiment has been successfully realized at 32 Gbaud (130 Gb/s) providing OSNR above the FEC limit.
- Models and simulation tools for Photonic Integrated Circuit on InP

MIRTHE advanced format modulation chip-set remains as a very interesting option for the concerned industry versus competing technologies.

Direct exploitation of MIRTHE results depends on maturity of different achievements realized during the project time. Two of them are certainly very close today to be brought to markets: packaged DP-RX showing already the highest performance and industry standard modelling tools with InP-PIC designing and system simulations.

Dissemination and promotion of MIRTHE has been carried out by means of different strategies. The main activities to spread new achievements were extremely rich: papers in international journals (13) and contributions to national and international conferences (32). Mirthe's website www.ist-mirthe.eu has been set up to communicate the evolution and achievements of the project.

2 Project context and objectives

Due to the constant telecom traffic increase, a capacity growth by a factor of 30 to 100 will be required by the end of the next decade. Following an evolutionary path based on the simple introduction of additional channels will just not bring the appropriate solution [1]. New technological breakthroughs have to be proposed to face this challenge. This is why optical **multilevel modulation formats** coded in amplitude, phase and polarization, with both **coherent and direct-detection**, are presently receiving great attention as they provide a more efficient use of spectral bandwidth. For example, four bits of information can be encoded per symbol when QPSK is used in conjunction with polarization multiplexing. This is advantageous as a large increase in data rate can be obtained with minimal changes to the installed base of optical filters and chromatic and polarization mode dispersion mitigation devices. Moreover, multilevel coding can rely on more mature and lower speed electronics providing lower cost and energy consumption of transmission equipment.

100 Gb/s Dual Polarization QPSK (Quaternary Phase Shift Keying) is of special interest because of (i) its industrial developments already going on, taking advantage of the compatibility with the present standard **50-GHz WDM channel spacing** [2,3], (ii) the current **standardization work** (OIF). At the same time, 400 Gb/s is discussed as a possible next deployment stage inducing intensive research on formats with a higher compression ratio such as 8-PSK and 16-QAM.

However, increased spectral efficiency inevitably leads to optoelectronic transmitters and receivers of increased complexity and larger footprint, consumption and cost. **Monolithic integration** is known to help solving these problems typical of discrete components. Practical usable components should preserve high modulation performance specially while increasing the data rate. Therefore, MIRTHE is aiming at the integration of established photonic functions into InP chips (**Photonic Integrated Circuits** or **PICs**). This approach is expected to improve dramatically the yield of low complexity optical functions as found in DP-QPSK optoelectronic front ends and to reduce the number of costly package connections/interfaces.

The proposed development is motivated by the required reduction of power consumption and cost of 100GbE industrial equipment as well as by the definition of future-proof next generation terabit component technology. It primarily addresses Ethernet links which may use either coherent or direct detection. But MIRTHE is also providing attractive solutions for line applications where coherent technology is considered today as mandatory.

This project targets new multilevel-modulation all-monolithic integrated TX and RX Photonic Integrated Circuits (PICs), eventually able to achieve 100-400 Gb/s aggregated speed on a single wavelength. This project, in line with the Objective 2009.3.7 of the Work Plan, is motivated by:

- the reduction of cost and power consumption of 100GbE transmission equipment,
- increasing the bit rate to 100 G and higher, while still staying within a given 50 GHz channel grid
- the need of future-proof component technologies for next generation terabit networks.
- The chips will be packaged and driven at 28 and then 56 GBauds in order to realize first PIC-to-PIC Terabit range transmissions.
- It is expected that the innovation introduced by the monolithic integration of RX with low polarization loss and TX having novel vector EAM-based sources brings a breakthrough to the cost, size and consumption of Terabit components.

Five scientific and technical specific objectives have been identified in MIRTHE.

- **Demonstration and mastering of a monolithic integration technology of InP-based TX and RX chips suitable for handling QPSK-type modulation formats for 100 Gb/s transmission:**

While several medium complexity PICs have already been reported, e.g. the 10-channel TX and RX from Infinera, the realization of PICs intended to be developed within MIRTHE is facing specific challenges, in particular in terms of balance control: balance of power splitter, balance of characteristics vs polarization …

But the target objectives of reduced footprint, reduced power consumption and **lower overall cost** are definitely worth the challenge.

- **Demonstration of a future-proof approach by enhancing the bit rate to 200 & 400 Gb/s:**

Actually, it is of major importance to make sure the solution derived to provide a "low cost" solution to tomorrow transmission needs, is also future-proof, and that the solutions proposed will also be able to withstand higher bit rate,

- **Module packaging of the TX and RX PICs with driving electronics:**

The challenge is there to provide the most efficient industry compatible packaging solutions according to emerging standards, able to support the multi-paths high-frequency electrical drive signals of the TX and RX PICs.

- **Demonstration of PIC to PIC transmission at 100 and 200 Gb/s:**

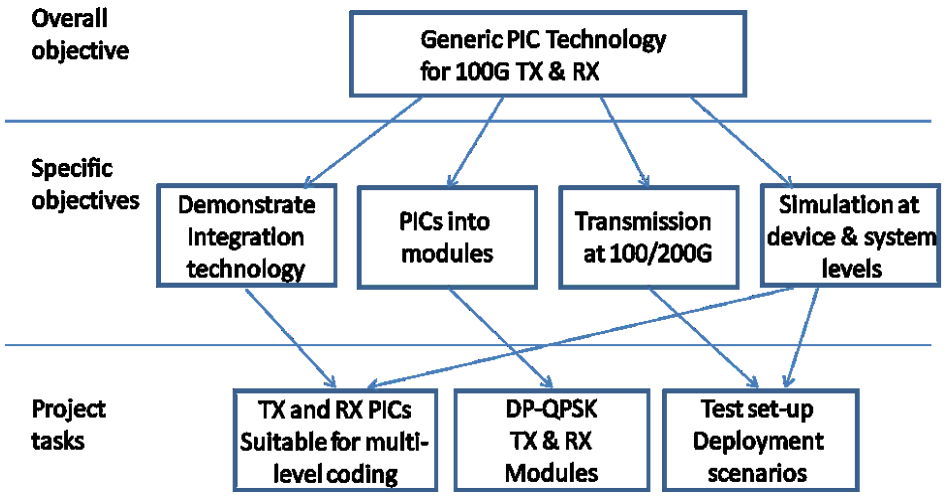
An important objective of MIRTHE is the system assessment of PICs developed in the project. Back to back, but also transmission experiments will be performed to reach a full evaluation of the integrated TX and RX.

- **Simulations at the device and system levels to identify capabilities and limitations and to contribute to specifications:**

A complementary objective to the previous one is the interactive modelling of devices and sub-systems, in order to feedback system requirements to device design, and vice versa, and to contribute to specific future components improvements.

The **innovations** claimed are:

- Small size TX chips suitable for multi-level coding (QPSK, QAM), based on phase switching in EAM-based PICs,
- Fully integrated RX chips demultiplexing both polarizations of the incoming light signal (DP-QPSK),
- Evaluation and prototype fabrication of novel monolithic coherent receiver types, applying multiport approaches in the phase demultiplexing hybrid to increase the bit rate for a given baud rate (higher compression ratio),
- Demonstration of low-power low-footprint multi-level coding TX and RX,
- Coplanar coherent receiver package with gain-controlled linear electrical amplifiers.
- Demonstration of 200 – 400 Gb/s capability of InP-based TX and RX PICs
- Integrated approach for photonic circuit numerical modelling and design.



Overall strategy and objectives of the project

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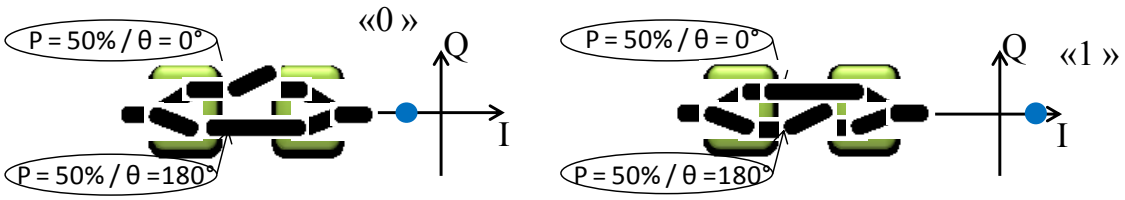
3 Main scientific and technical results

3.1 Transmitter

InP circuits for advanced modulation formats were previously inspired by the LiNbO3 Mach-Zehnder architectures and were able to generate DPSK [3.1.1], DQPSK [3.1.2] or 16-QAM [3.1.3] signals. However, they showed issues with a very large footprint, high optical losses, high power consumption and integration compatibility with a laser. A novel, very simple way, to generate the advanced formats was proposed by Inuk Kang who used short Electro-Absorption Modulators (EAM) in an interferometric arrangement [3.1.4]. Low power consumption EAMs acting as a prefixed optical phase switch were shown to simplify and reduce the circuit size. Several subsequent demonstrations of such modulators working at 80 Gb/s DQPSK and a 43 Gb/s 16-QAM signals [3.1.5] were realized by C.R. Doerr. However, those PICs applications were limited by their high optical losses and lacking of full source integration with a single frequency laser.

In order to solve the issues of the previous art, MIRTHE introduces first all-monolithic transmitters integrating on InP a DFB laser emitting at 1.550 µm and interferometer arrangements based on the prefixed optical-phase switching concept. The integration complexity may reach several tens of active/passive photonic functions.

Electro-Absorptioon Modulators are known as ones of the smallest Electro-Optic converters which genuinely modulate optical power using absorption edge shift induced by Quantum Confined Starck Effect. Due to their high speed and low chirp they can also act as simple switches to block or pass optical signal. This is the basis of the prefixed optical phase optical switching. As explained in figure below, EAM in each arm switches on/off appropriate phase reflecting modulation data. The waveguides are then combined in 2:1 MMI into a single output. Interestingly, EAM switch is suitable to provide multiple power levels easily enabling simple spectrally-efficient multi-level phase-amplitude formats.



Operation principle of a simple Binary Phase Shift Keying circuit.

Due to the innovative concept to produce advanced formats, the TX activity took important risks as to the validity of such sources. These risks have been taken because the proposed solution promised lowest footprint chips and low driving energy in addition to full monolithic integration with lasers. Such small and "green" sources cannot be obtained by any competing technology and remains as a very interesting option for the concerned industry.

All MIRTHE TX Photonic Integrated Circuits (PIC) are fabricated using a common platform providing relatively simple technology based on a single active layer growth composed of AlGaInAs quantum wells, Selective Area Growth (SAG) gap engineering and a single regrowth semi-insulating buried hetero-structure (SIBH). Independently of designing complexity such as integration degree or number of photonic function, this platform makes the integration technology identical to that of a simple EML one.

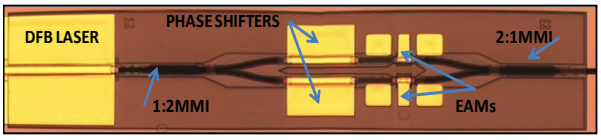
MIRTHE technology realized three types of full monolithic transmitters:

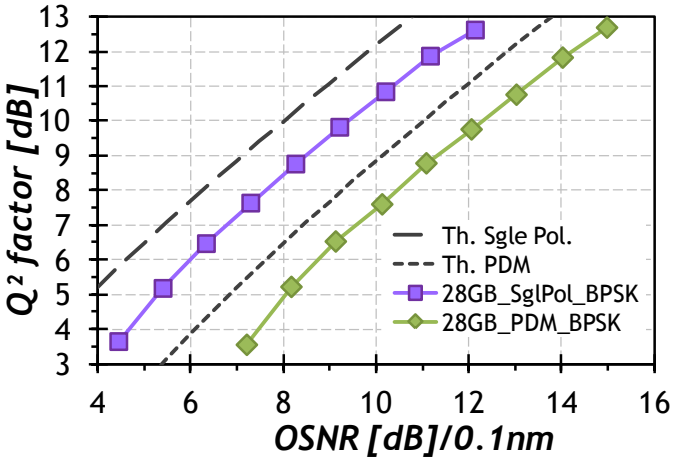
- simplest BPSK TX chips integrating a DFB laser, 2 phase shifters and two phase switching EAMs (2.6mm x 0.5mm)

- Single Polarization QPSK/IQ TX integrating a DFB laser, two BPSK cells with 4 independent phase shifters and output SOA (5.1mm x 0.5mm)
- Dual Polarization QPSK/IQ TX integrating a DFB laser and two QPSK cells (7.1mm x 1mm)

Thanks to the optical phase switching concept, all these full monolithic transmitters have the smallest footprint ever made for their respective vector modulation functionality in a single wavelength channel.

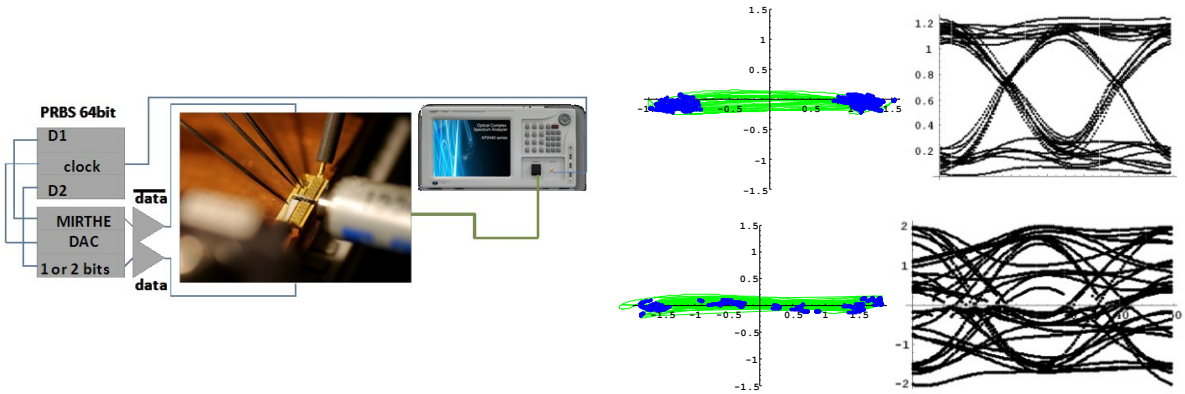
Novel BPSK TX has been used in several close-to-system or system environment experiments. In a direct detection experiment the component allowed to transmit 12.5 GB signal over 40km without errors [3.1.6]. Next, a system environment BPSK experiment at 56 GB demonstrated an OSNR penalty less than 1.5dB versus theory [3.1.7]. This result is actually only ~1dB worse that the best current commercial LiNbO3 MZM performance is spite of the very different operation principle of our PIC. We believe that it demonstrated the interest of the monolithic integration with a laser which cancels intrinsic switching loss of our modulator architecture. Therefore, we definitely validated novel prefixed phase switching concept as able to compete with traditional phase modulation present today on the market.





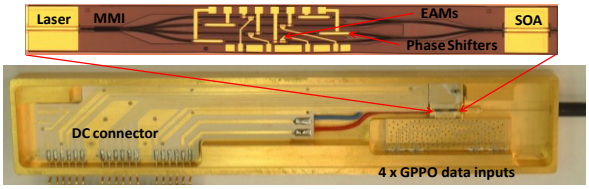
28/56GB experiments with BPSK TX (chip size is 2.6mm x 0.5mm)

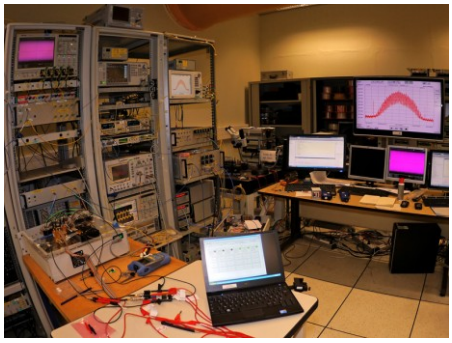
BPSK TX chips have also been used to prove the modulation speed rise and multilevel modulation capability of the MIRTHE technology.



MIRTHE BPSK TX experiment at 40GB (left); 40Gb/s NRZ constellation and tributary eye (upper right); 80Gb/s multilevel constellation and tributary eye (lower right)

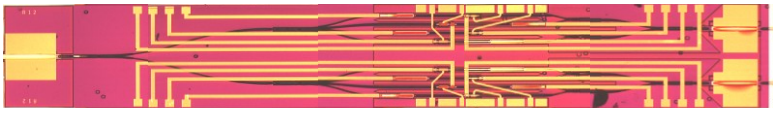
In its research version SP-TX chips included 20 photonic functions. They were assembled in OIF packages standardized for LiNbO3 type modulators. 50 times smaller MIRTHE InP chip seems to be lost inside. The components followed by a polarization emulator were successfully used in QPSK PIC-to PIC transmission experiments up to 32GBaud (130Gb/s cumulated speed).

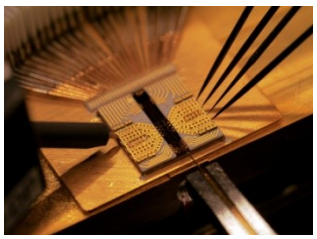




SP-QPSK TX PIC chip photograph assembled into OIF package imaging well 50 times footprint gain. On the right is a photograph of system environment experiments with QPSK 32G modulation.

DP-TX chips included 40 photonic functions being probably the most complex InP integration for a single channel ever made. All photonic functions were operational confirming a possibility for a good fabrication yield provided by our InP-integration platform. One of important target of this run was a demonstration of increased modulation speed. Small signal modulation measurements were done after packaging in modules showing bandwidth above 30GHz which should allow modulation baud rate up to 56GB.





Realized monolithic DP-TX PIC and its assembly photographs (chip size is 7.1mm x 1mm)

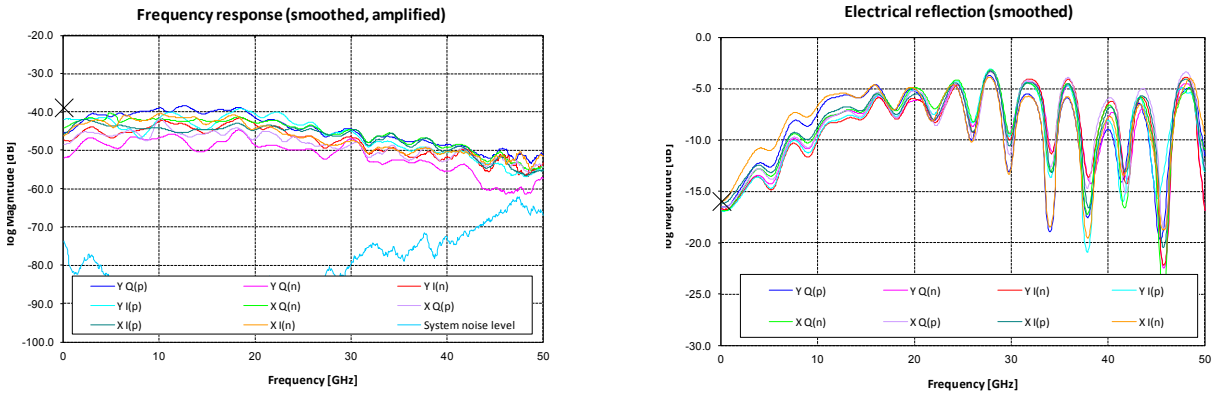
Speed scalability, ultra-small footprint and low power drive of the monolithic circuits are also attractive for advanced format migration towards low-cost applications.

Assembled 28Gbaud DP-Tx module

After the packaging of the first 28Gbaud single polarisation (SP) coherent module at the end of the first project year, and the packaging of the first 28Gbaud SP-QPSK transmitter modules at the second project year, the remaining period focussed on the concept development, the packaging and module characterisation of the final goal 28Gbaud and 56Gbaud dual-polarisation (DP) QPSK / 16QAM transmitter.

The package concept for the 56 Gbaud dual-polarisation (DP) transmitter modules is based on the experience from the assembly and characterisation of the 28 Gbaud single-polarisation (SP) transmitter modules. In general it is a doubling of the functionality of the chip and module and therefore requires twice as many terminals. However, due to the fact that the package can no longer be compliant to the OIF implementation, we could now reduce the size of the module taking into account the very small size of the dual-polarisation transmitter chip..Due to the small size of the chip in comparison to the module, a complex internal dc- and rf-wiring and packaging technology had to be chosen. However compared to the single polarisation module the length of the module was reduced from 100 mm to only 76 mm for the dual polarisation module.

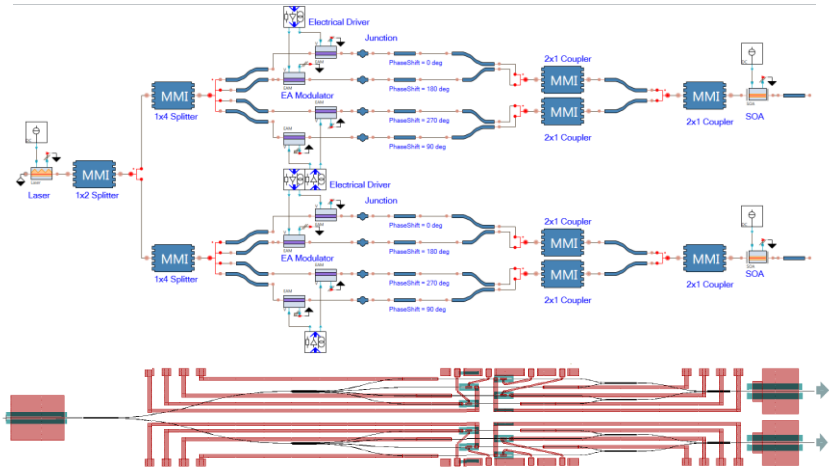
After checking correct DC behaviour separately of all integrated functions of the modules, we carried out rf-characterisation with the 50 GHz Lightwave Component Analyzer (LCA) to measure the e/o transfer characteristic of the different EAM sections and the e/e reflection parameter (S_{xx}) of the different rf-inputs. The curves of the LCA measurements are shown in **Erreur ! Source du renvoi introuvable.** next figure. Due to the slight inductive enhancement around 15 GHz the 3 dB bandwidth lies for all curves at > 40 GHz and the electrical reflection parameter (Sxx) is better than -5 dB up to 25 GHz and still less than -3 dB up to 50 GHz.



E-O Transmission ($S_{xy,}$,left) and E-E reflection (S_{xx}, right)
measurement of the assembled 28G / 56Gbaud Dual-Pol. Tx-module YAG.00009

This 56Gbaud TX version showed some minor bandwidth limitations and the overall cw-laser performance of the second final fabrication run was not as good as wished for. Nevertheless both Tx-modules proved a reasonable (state of the art) 32.5 Gbaud performance.

MIRTHE TX development was supported by specific modelling and simulations by analysing the component concept limits and explaining or solving issues. An actual DP-QPSK realistic component model was implanted in VPI Component Maker. The simulation confirmed the PIC ability to produce 28/32GB and even 56GB modulations with QPSK and 16-QAM formats.



Dual-polarization transmitter. Top: simulation schematic of the complete component-model design; bottom: actual mask layout of the fabricated device

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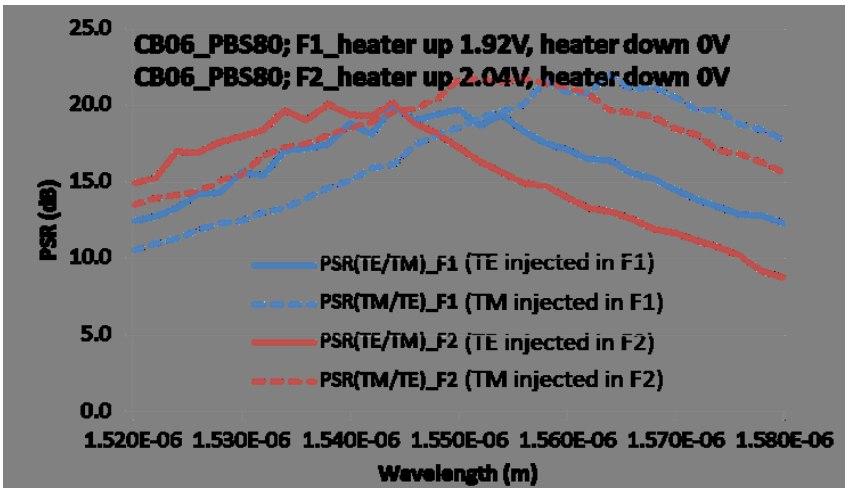
3.2 Receiver

The 100G Ethernet standard has found its way into commercial applications. Advanced modulation formats such as dual polarization quadrature phase shift keying (DP-QPSK) are approved to increase the spectral efficiency [3.2.1]. Generally, in the receiver module the polarization beam splitter (PBS) is implemented due to hybrid integrated [3.2.2]-[3.2.4]. Monolithic integration of optoelectronic receivers makes the deployment of such advanced modulation formats successful, because of its low cost and compact size. However, only few monolithic polarization diversity receivers have been reported [3.2.5],[3.2.6].

Within the MIRTHE project, we demonstrate DP-QPSK receiver modules with an InP based chip for 400G Ethernet applications. The chip comprises monolithic integrated PBSs with 90° hybrids. Contrary to the 400G DP-QPSK receiver module in [3.2.4] where the PBS is implemented as a free-space optic, the PBS of presented receiver module is monolithically integrated.



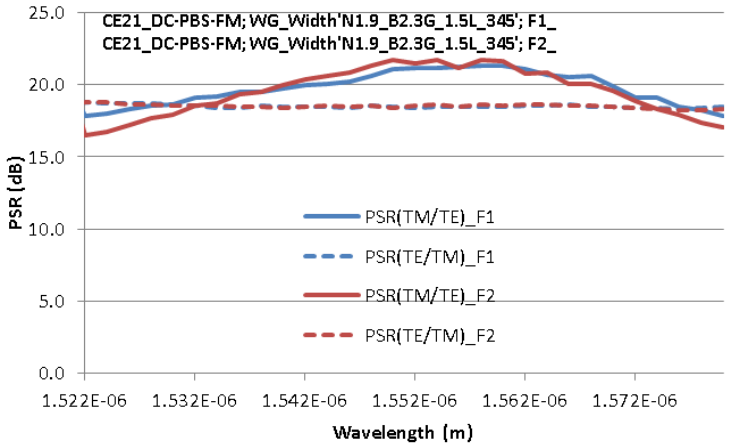
Measured PSR of a fabricated DP-QPSK receiver chip with MZI as PBS
(blue lines for signal input, red lines for LO input, solid lines for TM and dashed lines for TE)

For the receiver chip the main focus was on the monolithic integration of the PBSs to the receiver chip. Two types of polarization beam splitter were found that were compatible with the receiver platform. One

of the PBS is based on a directional coupler with metal overlay and the other one on a MZI. For each PBS type one wafer run of DP-QPSK receiver chips has been fabricated and characterized.

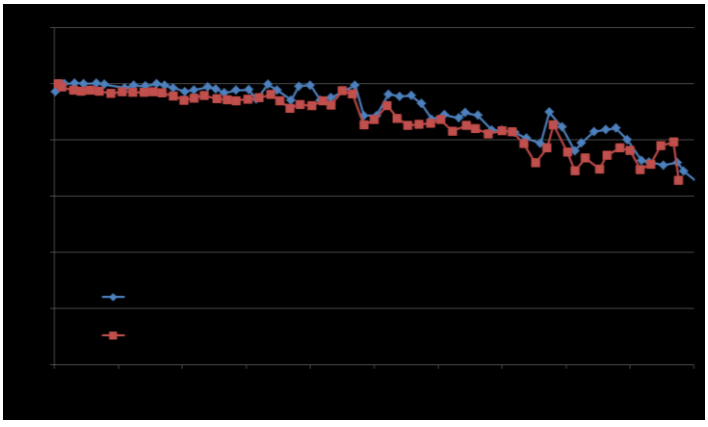
The most important property of the DP-QPSK receiver chips is the PSR obtained from the PBSs developed within the MIRTHE project. The following two pictures show the measured PSR of DP-QPSK receiver chips with a MZI-PBS and a directional coupler PBS. The DP-QPSK receiver chips with a MZI-PBS have been fabricated in the first generation receiver wafer run while the DP-QPSK receiver chips with a directional coupler PBS have been fabricated in the second generation receiver wafer run. For both DP-QPSK receiver types four balanced PDs were designed on the chip. Measurements of the RF bandwidth of the balanced photodiodes showed a response of -1.8dB at 50GHz.

For the DP-QPSK receiver with MZI-PBS the PSR at 1550nm is better than 17dB, while in the C-Band for different inputs and polarizations we achieve a minimal PSR of 12dB. From simulations it is known that even better results should be achievable. With a design optimization of the MZI-PBS structure the center wavelengths should be at the same wavelength, increasing the PSR.Moreover, due to the heaters on the MZI-arms, the fabrication tolerances could be improved.



Measured PSR of a fabricated DP-QPSK receiver chip with directional coupler PBS
(blue lines for signal input, red lines for LO input, solid lines for TM and dashed lines for TE)

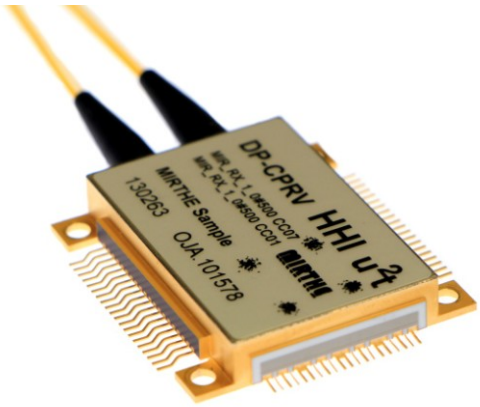
Regarding the demands of the receiver chip for later applications the following facts can be pointed out for the fabricated receiver chips with PBS. For the MZI-PBS active tuning is needed in order to compensate the phase walk-off in the MZI arms. For this reason, the receiver chips with directional coupler PBS are a preferred solution for monolithic integration of PBS to the receiver chip. For receiver chips with directional coupler PBS the chip size, the absence of tuning the PBS, the simple fabrication, the PSR and the CMRR meet typical specifications. However, the TE signal is attenuated due to the metal on the DC. In later application the reduced responsivity may result in shorter transmission distances of the data signals.



Typical frequency response up to 50 GHz for a fabricated balanced PD

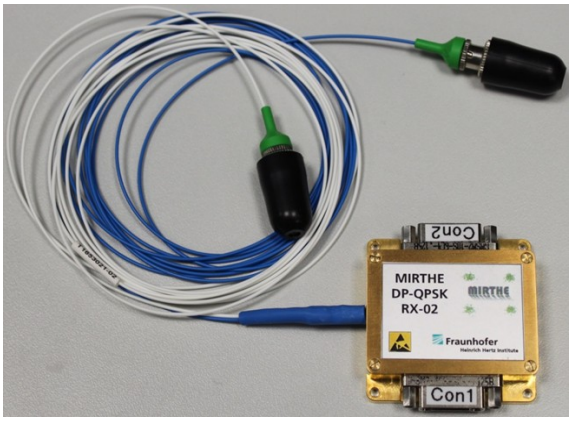
After the DC characterization of the the receiver chips, we measured the frequency responses of the balanced PDs (normal and an inverse photodiode). The measurements are up to 50 GHz by using the heterodyne principle. A typical frequency response is shown in the figure above. The blue line and the red lines stand for the normal and the inverse photodiodes of the balance photodiode, respectively. The frequency response is better than -1.8 dB for both photodiodes up to 50 GHz.

In this project 28/56Gbaud single and dual-pol. coherent receiver modules are being developed. After the packaging of the first 28Gbaud single polarisation (SP) coherent module at the end of the first project year, the remaining period focussed on the concept development, the packaging and module characterisation of the final goal 28Gbaud and 56Gbaud dual-polarisation coherent receiver modules.



28Gbaud DP coherent receiver module with two SP chips

In the case of the 28Gbaud DP coherent receiver **two** fully integrated DP coherent receiver channels have been integrated into a single module, making this module suitable for the detection of the next generation 400G dual-carrier dual-polarisation 16QAM format. These 28Gbaud DP coherent receiver modules have shown operation with dual-channel dual-polarization 16QAM at 56Gbaud resulting in a total bit rate of 450 Gb/s.



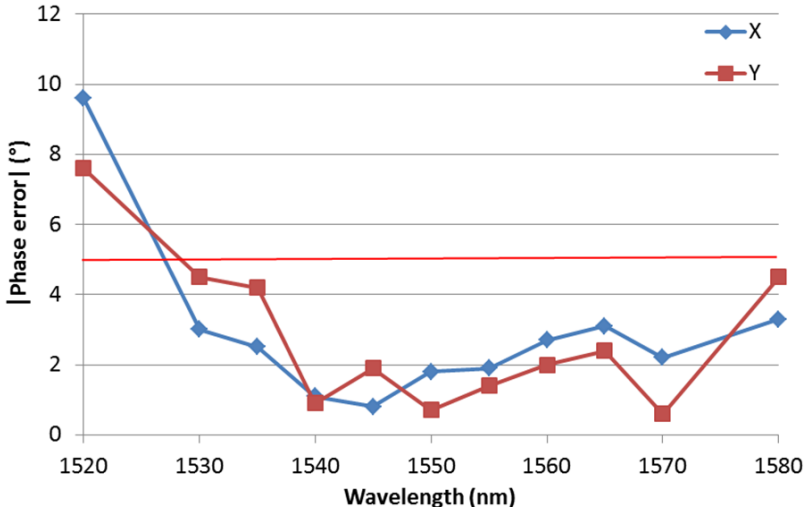
56Gbaud DP coherent receiver module packaged by the HHI

56Gbaud DP coherent receiver module packaged by U2T

For the realisation of the final 56Gbaud dual-pol. coherent receiver module suitable for 56Gbaud 16QAM transmission, resulting again in a total bit rate of 400 Gb/s, the fully integrated DP-receiver chip was

packaged in a GPPO-style package. Two different styles of packages were used, resulting two slightly different versions of this 56Gbaud DP coherent receiver.

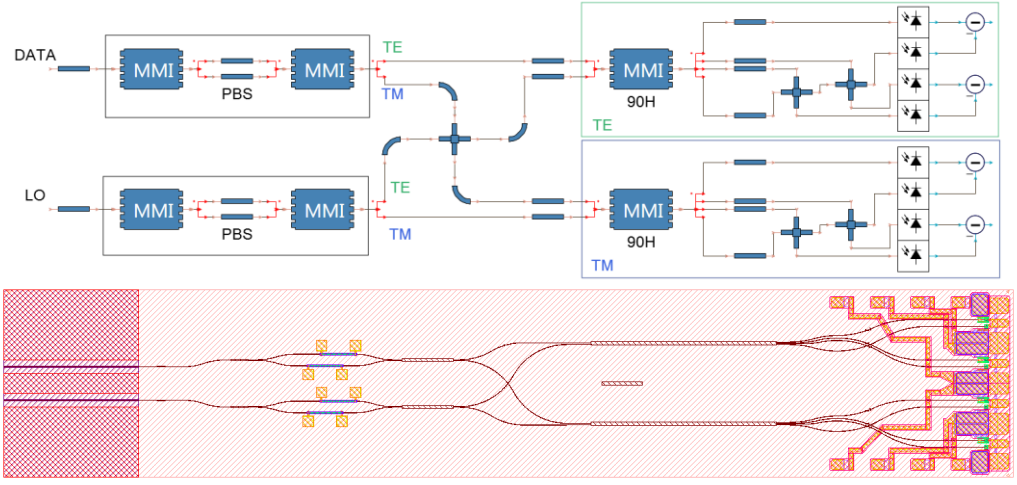
For measuring the phase error two CW lasers with a frequency detuning have been used. Both lasers illuminated the two inputs of the receiver at the same time. In this way, the phases of the different channel were measured. The measured phase deviations are for the TE and the TM receiver below 5° over the whole C-band. Hence, the OIF spec limits of 5° are fulfilled.



Maximum phase error of the 56Gbaud DP-QPSK receiver module as a function of the wavelength; (X – TE, Y - TM)

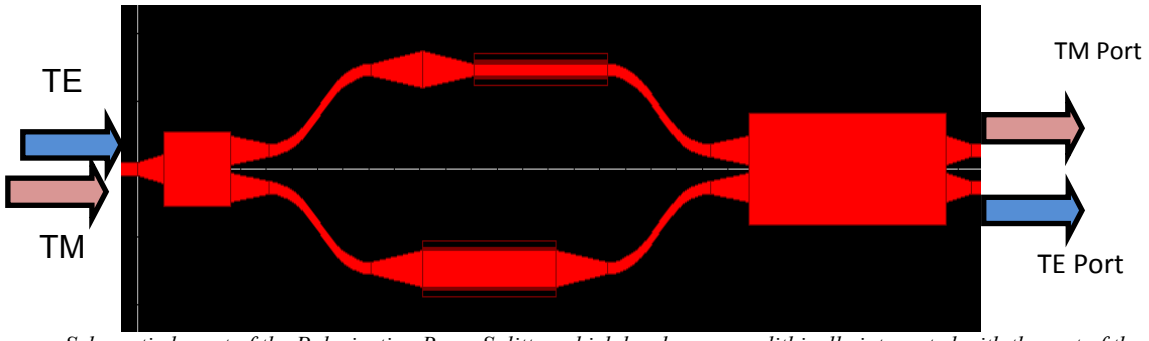
Finally the module characterisations proved the as-expected excellent performance of all receivers, which has been confirmed in system environment tests providing state-of-the-art improvement and better performance than standard available discrete or hybrid receivers. 56GB DP-RX worked up to 44GB 16QAM above FEC limit delivering 352 Gb/s cumulated bit rate.

MIRTHE RX development was supported by specific modelling and simulations by analysing the component concept limits, explaining or solving issues and the development of a full analytical model of the dual-pol. coherent receiver module.



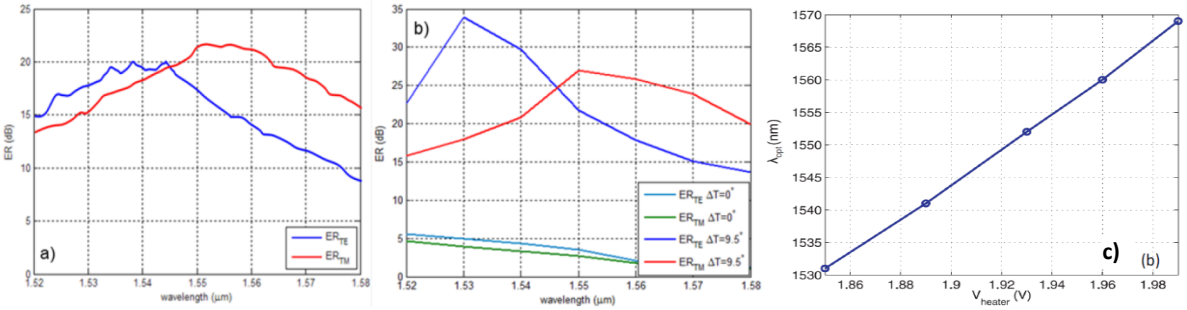
Dual-polarization receiver. Top: simulation schematic of the complete component-model design; bottom: actual mask layout of the fabricated device

One of the important achievements in RX design has been to get a PBS, compatible for integration with previously existing high performance InP coherent receiver, exhibiting good tolerance to fabrication deviations. A MZI based PBS, comprising two MMI couplers interconnected by two waveguides with properly designed birefringence, and thermal tuning was used in the final design. Two thermal heaters have been included in both arms of the MZI to compensate the fabrication errors and to tune the device along the complete C band.



Schematic layout of the Polarization Beam Splitter which has been monolithically integrated with the rest of the components to get the monolithically integrated dual polarization coherent receiver (thermal heaters shown in black)

The model of the MZI-PBS with heaters has been validated comparing the simulations with the measurements of the DP-QPSK receiver. From the simulations it was expected that Extinction Ratio (ER) for TE and TM polarizations would be slightly detuned due to fabrication errors and that modifying the heaters voltages this effect could not be corrected. However, voltage adjustment of the heaters could allow moving both TE and TM ER curves simultaneously to the desired centre wavelength. This effect was clearly observed in the device measurement.



Validation of the MZI-PBS with heaters model, a) measurements on the DP-QPSK receiver, b) simulation results obtained using the model (width error 50nm), c) Wavelength at which PER is maximum as a function of heater voltage

One of the most important results of the theoretical model is the wavelength tunability of the device. This means that heaters can not only compensate fabrication errors but they also enable tuning of the PBS response to any wavelength within the C-Band. Experimental validation of this idea is provided in figure c) which shows the wavelength at which PER is maximum (λ_{opt}) as a function of the heater voltage (V_{heater}). This curve has been obtained by measuring the PER within a wavelength range of 1520 - 1580nm for different heater voltages, and then extracting the wavelength with maximum PER for both polarizations. From this figure it is clear that a nearly linear tuning of the wavelength response is obtained, which allows us to cover the complete C-Band applying a heater voltage between 1.85 - 1.99V. Heating power, calculated as $P_{heater} = V^2_{heater}/R_{heater}$, (measured R_{heater} ~50Ω) , is around 80mW. The measured PER at each λ_{opt} is always better than 16dB.

More details regarding the model and its experimental validation can be found in [3.2.7.].

References to Chapter 3.2

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[3.2.5] *C. Doerr, L. Buhl, Y. Baeyens, R. Aroca, S. Chandrasekhar, X. Liu, L. Chen, and Y. Chen, "Packaged Monolithic Silicon 112-Gb/s Coherent Receiver," Photon. Technol. Lett. 23, 762-764, 2011.*

[3.2.6] *C. Doerr, L. Zhang, P. Winzer, N. Weimann, V. Houtsma, T. Hu, N. Sauer, L. Buhl, D. Neilson, S. Chandrasekhar, and Y. Chen, "Monolithic InP Dual-Polarization and Dual-Quadrature Coherent Receiver," Photon. Technol. Lett. 23, 694-696, 2011.*

[3.2.7] *D. Galacho, R. Zhang, A. Monux, R. Halir, C. Ramos, P. Runge, K. Janiak, G. Zhou, H.-G. Bach, A. Steffan, and I. Fernandez, "Integrated Polarization Beam Splitter for 100/400GE Polarization Multiplexed Coherent Optical Communications," J. Lightwave Technol. 32, 361-368, 2014.*

3.3 Specific electronics

According to the objective of Mirthe project to demonstrate optical transmitters operating in QPSK at 28 and 56 GBd and in 16-QAM at 28 GBd, it has been planned to leverage III-V Lab's InP DHBT very high speed electronic circuit technology in order to provide state-of-the-art electronic driving capability to the project.

All electronic ICs have been realised using InP HBT process. A twin 2-bit DAC module operating at up to 40 GBd has been realised. It allows generating a 16-QAM signal at 40 GBd. A NRZ selector-driver module operating at 56 Gb/s to allow generating a QPSK signal at 56 GBd has been also realised.

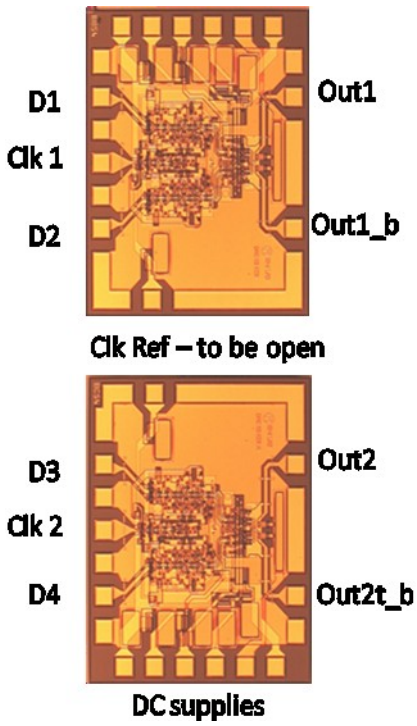
3.3.1 Circuit and twin-module for multilevel driving operation

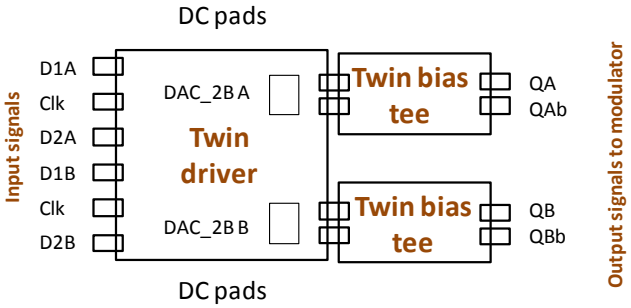
In MIRTHE a specific dual driver to be interfaced with MIRTHE TX was proposed..This circuit was based on an original concept consisting in simultaneous combination of DAC and amplification (driver) functions directly compatible with EAM switch without need for a linear amplifier. Additionally a universal architecture suitable for both binary and multilevel formats has been proposed and realised.

Based on power-DAC concept with first circuit realisations and taking into account MIRTHE project objectives and in particular plans for 16-QAM demonstrators and experiments, we designed and implemented two circuits. Both circuits have the same architecture and electrical performances. They differ by physical implementation (layout) which is customized for the twin-chip package. Such twin-module driver will be providing electrical input signals for I/ Q modulator.

The microphotograph of a pair of circuits is presented in figure above (left). These circuits have been designed for operation either as multilevel or binary driver.

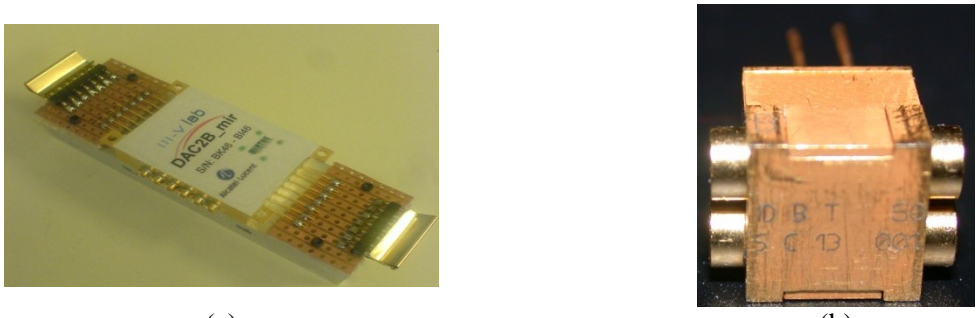
The module package concept consists in a multi-level twin driver module (integrating two mirror 2-bit DAC chips presented above) with two pairs of differential outputs directly connected to two twin bias tee modules. The input of the module is fed with single-ended data and clock signals at respectively the same symbol rate and frequency than the output signal's symbol rate.





Two mirror DAC2B driver ICs for I/Q modulator *Package concept for the 4-ASK twin driver module*

A photograph of the realised module is shown below. Two InP DHBT 2-bit DAC chips with mirror-like implementation of DC pads are reported in the module. Wedge ribbon bonding is used to optimise RF performance of interconnections from the chips to input and output RF alumina substrates as well as for the power supply decoupling elements. All connectors are of GPPO type, with centre-to-centre spacing of 3.6 mm.



(a) (b)

Photograph of the 4-ASK twin driver module(a) and of dedicated bias tee(b)

In order to drive the EAM sections of the Tx PIC with suitable DC components for optimum biasing, a bias tee must be used between the driver and the EAM. A dedicated GPPO-based twin bias tee module has been designed and fabricated. GPPO connectors' centre-to-centre spacing is equal to 3.6 mm.

Measurements of 4-ASK electrical signal @ 40 GBd produced by our twin driver are shown below. Clearly open 4-ASK 2x1.6 V_{pp} eye diagrams are obtained. A binary output signal realized with the same driver module is also presented.

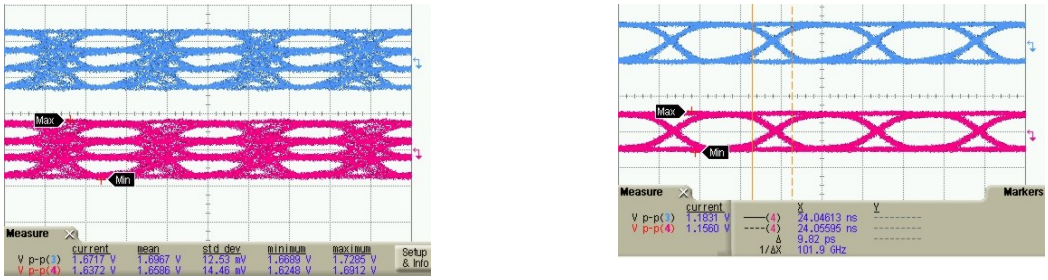


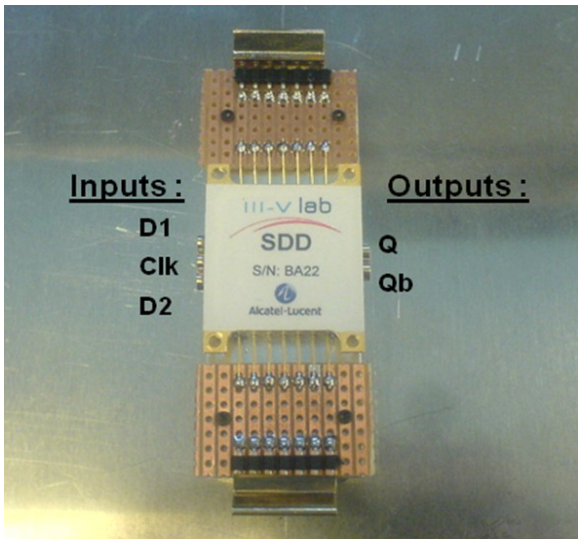
Figure 3.4: (a)4-ASK eye diagrams (oscilloscope screenshot) at 40 GBd, measured at the output of the first channel of the module.(b) Binary output signal at 40 Gb/s with CPM markers (~9.8ps)

Power-DAC driver circuits were operating correctly up to 40 GB. However all technical elements indicate that operation at 56 Gbd symbol-rate and higher is possible for the proposed architecture in InP HBT semiconductor process.

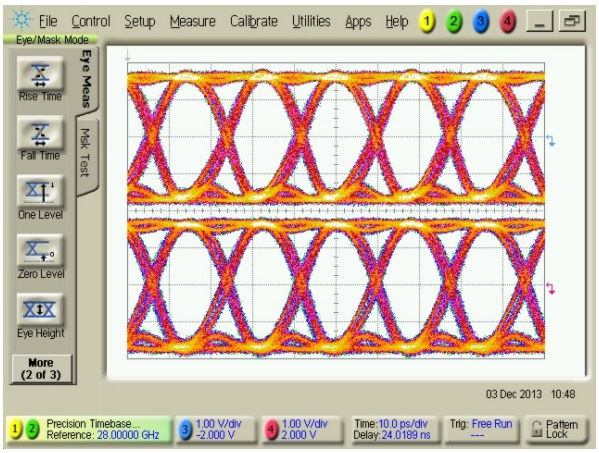
3.3.2 Binary driver module

III-V Lab demonstrated equally the suitability of InP HBT process to realize driver circuits operating at very high speeds in OOK mode. Driver using distributed architecture with important output signal amplitude has been designed, fabricated and measured. The driver module has been realized.

A photograph of the module is presented below. The module integrates an InP DHBT 2:1-selector-driver chip. All connectors are of GPPO type with 3.6-mm centre-to-centre spacing. The module is directly reported on a dedicated heat-sink. DC connection pins are soldered to two small dedicated PCBs for easy connection to power supplies.



Photograph of the OOK driver module



OOK 56-Gb/s eye diagrams measurement (oscilloscope screenshot)

Eye diagrams measurements of the module are presented for the two driver outputs. Clearly open OOK 2x3 V_{pp} eye diagrams at 56 Gb/s are obtained.

The work provided confirms the operation of a novel InP-HBT universal (e.g. switchable from NRZ to 4-ASK) power-DAC multilevel driver suitable for direct EAM switching in MIRTHE TX (~2Vpp). This circuit is to replace more standard CMOS-DAC followed by highly consuming-linear amplifier. The digital concept of power-level generation in our DAC provides not only lower consumption but also a higher quality signal than these of linear amplification. Although the realised version speed was limited to 40GBd (**320 Gb/s**

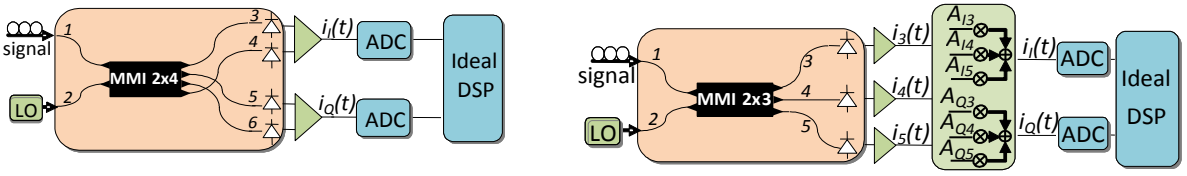
cumulated) we showed that the technology is ready for further speed increase to 56GBd at least. Therefore, we think that MIRTHE TX driver technology will shortly achieve performance compatible with 450 Gb/s cumulated speed.

3.4 Modeling and simulations

Modeling and simulations were essential for MIRTHE component development. On a one hand, we provided support by developing academia tools and specific software's for new designs and component ideas. On the other hand we worked with professional software tools to use them in realistic simulations and to developing their content for industry designers.

Specific modelling of new multi-port RX

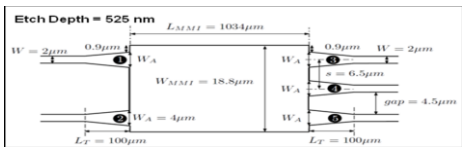
A new optical coherent receiver based on a multiport approach inherited from previous approaches at microwave and optical frequencies [3.4.1] has been proposed and studied. Specifically, a novel 120º monolithically integrated downconverter, based on a 2x3 MMI, has been analyzed, numerically evaluated under hardware impairments and compared to the conventional 90º downconverter.



a) b)

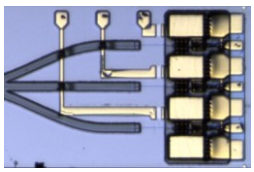
Coherent receiver architectures: a) 90º hybrid based receiver , b) 120º based receiver with analog IQ recovery

Conventional 90º hybrid integrated downconverter, is based on a monolithically integrated 2x4 MMI with four photodiodes followed by differential transimpedance amplifiers (TIA) with DC offset cancellation. Output electrical IQ signal components are then digitized in two analog-to-digital converters (ADC) and combined to be further processed in the digital signal processor (DSP). The proposed multiport downconverter is based on a 2x3 MMI coupler monolithically integrated with three photodiodes followed by their respective TIAs. Two different strategies have been used to recover I/Q signals from these three outputs: 1) Analog I/Q recovery (as seen in previous figure) and 2) Digital I/Q recovery (not shown in the figure) in which the three output photocurrents are digitized with the help of three A/D converters and then the I/Q signals are obtained from them by an algorithm. In both cases the required coefficients (A_{Ii}, A_{Qi}) to get the I/Q signals form the three photocurrents are obtained following a simple calibration method applied at the central wavelength of the band. It is shown that, the calibration procedure of the multiport receiver, allows full compensation of the optical hardware (MMI coupler and photodiodes) imbalances thus leading to an extended dynamic range and a broader operating bandwidth also allowing colorless operation in a multicarrier scenario.



Schematic of 120º coupler based on 2x3 MMI

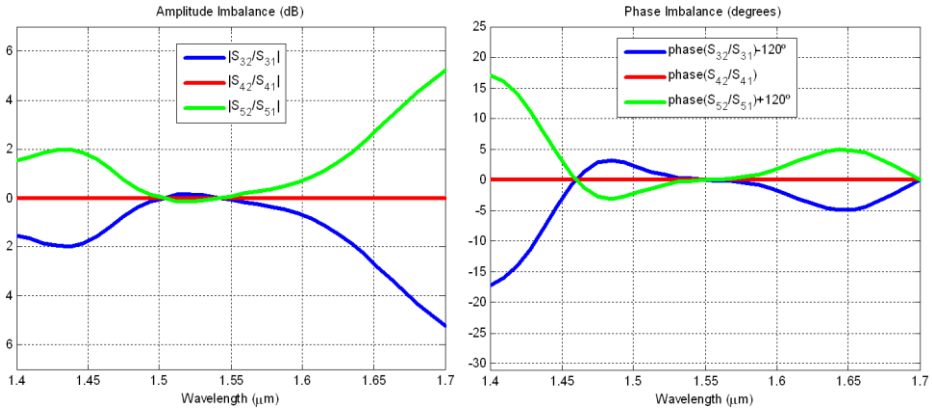
Fabricated 2x3coupler



Integrated photodiodes

The multiport receiver is based in a 2x3 MMI which consists in two input and three output waveguides interconnected by a wide central multimode section (MMI zone). All the MMI core, access waveguide and bends are done with a single etch depth of 525 nm. Because of the different widths between the interconnection waveguides (2µm) and the input/output waveguides of the MMI (4µm) the access to MMI is made through tapers, the length of these tapers is 100µm. The dimension of the MMI zone is 18.8 µm wide

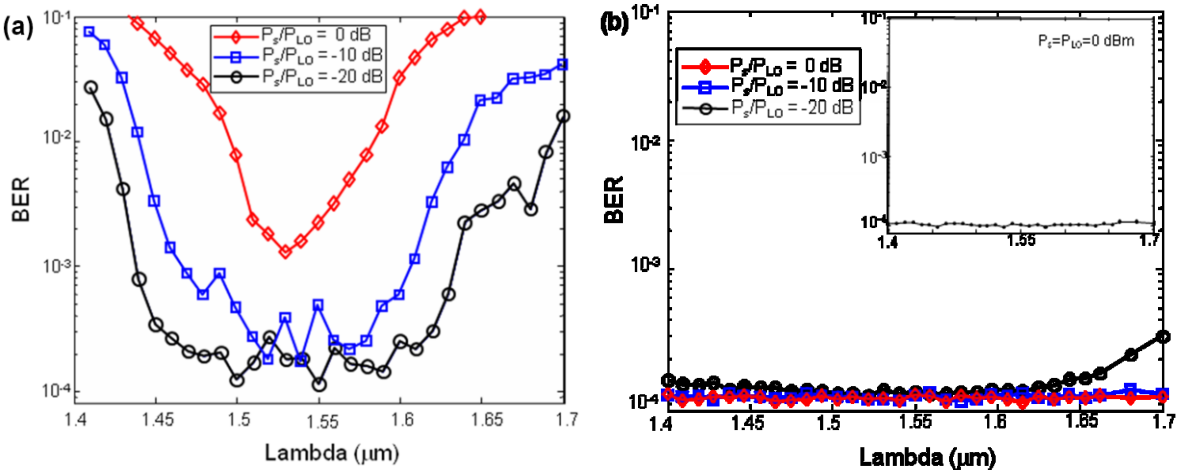
by 1034 µm long, which is smaller than the 2x4 MMI (25.2µm wide by 1379µm long). This size reduction makes that the 2x3 MMI has intrinsically a better performance than the 2x4 MMI.



Amplitude (left) and phase imbalance (right) of 2x3 MMI 120º coupler obtained from electromagnetic modeling

The wavelength response (amplitude and phase imbalance) of the considered 2x3 MMI (120º coupler) for the in-plane (TE) polarization wave (TM polarization exhibits god performance as shown in figure.

The proposed monolithically integrated 120º downconverter has been numerically evaluated under realistic hardware unbalances and compared to the standard 90º downconverter. Notice we are assuming here polarization control or a polarization diversity scenario. Special attention has been paid to constellation distortion appreciable in each scheme and its consequences in terms of bandwidth and dynamic range. In all the simulations performed, incoming optical signal-to-noise ratio (OSNR) has been adjusted for a BER=10^{-4} in an ideal coherent receiver in absence of internal noise-sources. More details of these simulation scenarios can be found in [3.4.2]. Results show that the main advantage of the calibrated 120º downconverter with respect to 90º hybrid with GSOP is that it fully compensates the nonlinear constellation distortion induced by hardware unbalances even for high signal power or P_s/P_{LO} levels. This leads to a much better dynamic range and broader bandwidth operation, as it can be clearly seen in the figures.



BER performance for a 64-QAM as a function of the wavelength for different signal-to-local oscillator power ratio (P_s/P_{LO}) when noise sources and hardware impairments are considered for (a) 90º hybrid downconverter (b) 120º coupler downconverter (P_{LO} fixed to 10 dBm except in the inset where signal and LO power are equal to 0 dBm)

Modelling of Complex Photonic Integrated Circuits

Based on design information and typical/measured data furnished by all project partners, VPI performed numerical simulations and analytical studies of various different aspects related to the transmitter and receiver concepts developed in MIRTHE using the modelling environment VPItransmissionMaker / VPIcomponentMaker plus prototyped extensions and co-simulations in Matlab and Python.

One of the main achievements brought massively forward in MIRTHE is our hybrid time-and-frequency domain modelling (TFDM) approach suitable for circuit-level modelling of complex photonic integrated circuits (PICs) that are composed of several optical and linear electrical sub-elements. The method is based on segmentation of the modelled PIC into building blocks which are coupled via guided modes of channel optical waveguides. In that way, each of these sub-elements is considered as black box that produces outgoing waves carried by guided modes of the device ports from the corresponding incoming waves [3.4.3].

Beside this new modelling method we developed or improved several photonic device and sub-element models, emulating realistic characteristics of EAM, SOA, waveguides, s-bends, crossings, MMI devices, splitters and couplers, phase shifters and more. We used them to investigate component limitations and critical design parameters of the transmitter and receiver structures in MIRTHE.

We also developed a family of fundamental electrical elements, which allow the simulation of transmission and reflection characteristics of linear electric circuits (ECs). Besides modelling the characteristics of individual ECs, the design of complex PICs drives the necessity of modelling electronic-photonic interactions as well, in order to optimize the overall performance of the device. We showed for instance that an optimized design of driving circuits of optical transmitter chips is very crucial for its performance in high speed operation.

In the following we list a few of the design studies we performed.

Transmitter characteristics

We carried out simulations investigating the impact of EAM chirp described by voltage-dependent alpha factors on transmitter performance. We found that modulator chirp may cause a rotation in the constellation diagram, as well as longer, symbol-dependent transitions between symbols. This limits the achievable modulation bit rate. A constant rotation in the constellation can be easily rectified by means of phase correction mechanisms at the receiver. However, when applying EAMs with different voltage characteristics, it would cause an unequal rotation of the points in the constellation diagram. This affects the system performance, especially in the denser 16QAM constellation.

Operating the EAMs in their respective saturation regions causes a compression of the constellation diagram, which may result in reduced signal quality. For modulation formats with multiple amplitude levels the outermost points of the constellation move closer to the inner ones increasing the impact of additive noise on signal performance. Further on, the detrimental influence of the modulator chirp might prohibit large driving amplitudes. The impact of non-ideal synchronization of the four electrical paths can be tested by adding a deterministic jitter to the driving signals. Results for a sinusoidal jitter (10GHz) reveal a high response to synchronization offsets. On the other hand, such a transmitter is relatively robust to random jitter variations. This is also due to the nature of the coherent detection configuration.

We applied the library of electrical elements to create the equivalent electrical circuit model of the EAMs. The electrical element parameters have been selected such that the equivalent electrical circuit characteristics correspond to the EAM characteristics reported by measurements. Based on this design we could vary individual values of electrical element parameters to investigate their impact on the overall EC performance. The obtained characteristics are very similar to results obtained by measurements. For example, for 50um length, we found that the 3dB-bandwidth is approximately 65GHz for 35Ohm and 55GHz for 50Ohm impedances.

Investigations from 3-5Labs showed [3.4.4] that the phase shifters employed in the MIRTHE transmitter exhibit a nonlinear dependence of phase and loss with applied current. Based on the provided data, we studied the influence of these realistic phase shifter characteristics on the overall transmitter performance. We analyzed the statistical variation of constellation points when currents fluctuate around their nominal value and found that the different branches have different tolerances with respect to allowable current fluctuations.

Further we found that current offsets in the individual branches do not cause strictly additive constellation point variations.

We studied the impact of unwanted feedback signals within the transmitter device, paying special attention to reflections at the active-passive material interface and at the output interface of the transmitter [3.4.5]. We found that the impact of reflections at the active-passive interface remains constant for different levels of amplification and is slightly lower than the one caused by reflections at the end of the device. Reflections at the end of the device are enhanced due to re-amplification in the SOA and might be critical for high levels of output power. Consequently, it is generally of high interest to increase the output power of the laser and work on decreasing the loss of passive waveguides and other connecting elements. Additionally, our studies suggested that reflections at the SOA-air interface have a strong impact on the broadening of the laser linewidth. Further we found that even when the total output power remains constant in average, strong power fluctuations at the laser output may occur, causing increased pattern effects in time-domain of the transmitted output.

We analyzed the impact of non-optimal splitting/coupling operations in the transmitter using either a single 4x1-MMI coupler or two stages of 2x1-MMI couplers. Our results revealed the tendency that both structures behave similarly: the optimum phase shift is slightly different from the theoretical one as signals at each branch are not in phase due to 1x4-MMI splitter outputs being not in phase and EAM chirp. From the obtained curves we gather that the configuration with a single 4x1-MMI coupler is more sensitive to such imperfections. We demonstrated further that small width variations introduce already detectable signal performance degradations. Imperfections in the first and last MMI elements are not critical for small deviations. However, for the transmitter with two-stage 2x1-MMI couplers, the margin of tolerance is tighter.

We proposed and investigated an alternative 16QAM transmitter realization using two modulation stages. The first stage consists of the standard QPSK architecture with 4 EAM sections driven by two binary signals and their complements. A second interferometric modulation stage with one EAM section in each of the two arms is added. Each EAM is driven by a binary drive signal. The phase difference between the two arms is 90°; a 45° phase shift compared the 90° phase differences in the interferometer arms of stage 1 is applied. The advantage of this realization is that only binary drive signals are needed to create the centred 16QAM constellation. The second stage can be made optically transparent by applying all Ones as bit sequence to the binary drives realizing a simple logical switch between QPSK and 16QAM modulation.

Receiver characteristics

The 90°-hybrid has been characterized by measuring the relative power and phase at the outputs as function of the phase at input 2, to check the impact of possible instabilities in the local oscillator signal. The relative power is not strongly affected. However, as expected, the phase of the demultiplexed ports fluctuates. In order to test tolerances to dimensions due to the fabrication process, length and width dimensions have been varied. The CMRR between two inputs keeps constant to imperfections in device length, but might increase significantly for deviations of device width beyond 0.2 um. The relative phase difference, is slightly affected by geometrical imperfections, a maximum of 15deg difference is measured for 0.5um tolerance in width.

We investigated the effect of crossing waveguides at the receiver on the system performance. We found that even small amounts of crosstalk between TE and TM signals affect significantly the PER. Further, crossings of the waveguides in front of the photodiodes may cause imbalances at the output of the photodiodes between I and Q components in a non-linear manner, which cannot be completely compensated by the DSP unit. However, one can compensate the impact of these types of crosstalk in the circuit by adding extra attenuators to balance the powers. This technique has been included in the last batch of fabricated samples of the MIRTHE receiver.

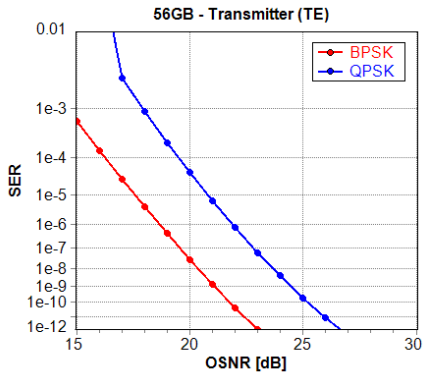
The influence of the photodiodes and electrical amplification has been analyzed in simulations with the limiting frequency response turned on/off. The calculated EVM demonstrates that these effects are important to be considered. The phase of the electro-optical frequency response deteriorates the signal significantly. A clear picture of the effect is observed in the eye diagram and the constellation plots. The non-ideal magnitude response produces different levels of amplitude due to its ripple. The non-ideal phase response additionally introduces a time delay between bits.

Three different implementations emulating a coherent dual-polarization receiver have been analyzed, corresponding to different types proposed during the project. Performing several parameter variations, we could show the necessity of using carefully adapted DSP algorithms in the system to compensate for distortions resulting from crosstalk and phase noise. Irrespective of this, all three designs are more or less equivalent. However, some elements, for instance the PBS, are more sensitive to fabrication tolerances and therefore, geometrical imperfections would affect differently when integrating the sub-elements. We showed the high sensitivity of the PBS design to geometrical imperfections for small deviations from the nominal width of the waveguides. We found a very strong degradation of PER for the first 0.01um width deviation. The frequency dependency of the PER is also noticeable, however, shouldn't represent a practical issue in this project. With the proposed temperature control on one of the arms of the MZI building the PBS, the structure is much more robust to width imperfections, and thus, easier controllable.

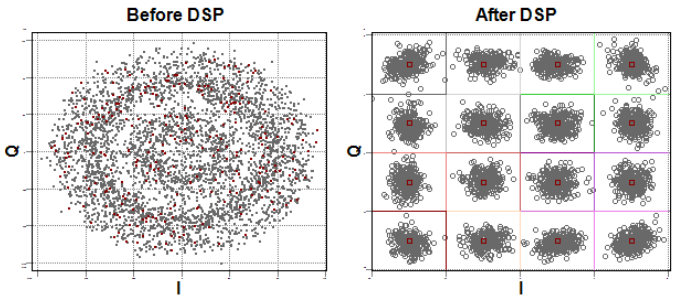
System studies

As an early initiation task in MITHE we performed a detailed comparable analysis on the differences of concepts for differential direct detection and coherent detection evaluated by means of analytical review and numerical simulation studies. We evaluated signal performance limitations due to CD and PMD for different values of OSNR. Further we elaborated on the difference of the two detection schemes if Kerr nonlinearities have a non-negligible impact on performance limitations and investigated the influence of imperfections of the coherent receiver on signal performance. For the coherent receiver investigations we limited ourselves to standard DSP-algorithms that had been proposed numerously in the literature. We showed, for instance, that coherent detection of 112 Gb/s DP-QPSK with DSP using the standard frequency-domain CD compensation algorithm allows the toleration of accumulated dispersion of more than 1000 km of SSMF. Further we demonstrated that standard DSP algorithms of low complexity allow compensation of PMD-induced impairments avoiding the need for sophisticated optical PMD compensation mechanisms. Important: fast and high-resolution ADCs are required in order to apply efficient DSP functions after coherent detection to compensate for the diverse propagation effects. We also demonstrated that the achievable system performance depends strongly on the characteristics (sampling speed, resolution) of available ADC.

Finally, we investigated the system performance for PM-BPSK, QPSK and 16QAM for several symbol rates using combinations of system-models and detailed component-models of the DP-transmitter and receiver developed in MIRTHE. For example, we performed noise loading simulations applying 100GHz optical filtering in front of the receiver and typical DSP algorithms for carrier frequency and phase recovery after conversion from analogue electronic to digital domain. We found that for PM-BPSK and QPSK, 28 and 32GB baud rates deliver about the same system performance without that an error floor is recognizable. For PM-16QAM however, our simulation results suggested that system performance worsens significantly. Error floors limit the achievable SER for all investigated cases; differences between TE and TM are detectable when using the MIRTHE receiver.



SER versus OSNR for PM-BPSK and QPSK for baud rate of 56GB per polarization using MIRTHE transmitter and ideal receivers with DSP performing CFR and CPR



Constellation diagrams of TE channel of PM-16QAM for 56GB before DSP (left) and after DSP (right) performing CFR and CPR for OSNR of 35dB

Moving up to 56GB, our simulations predicted OSNR penalties of only 0.5 – 1dB compared to 32 and 28GB for PM-BPSK and QPSK (left figure below). For 56GB PM-16QAM, we found that no acceptable

performance could be achieved when keeping all other component characteristics the same as applied for the cases with 28 and 32GB. However, when reducing for instance the optical filter bandwidth, and thus, reducing the amount of optical noise reaching the receiver SER values below 1e-3 could be achieved. Right figure shows below exemplary constellation diagrams before and after DSP for OSNR of 35dB. No significant non-stochastic limitations are recognizable. With improved characteristics of transmitter/receiver sub-components as well as optimized DSP algorithms, we could reduce the error floor below SER of 1e-5

References to Chapter 3.4

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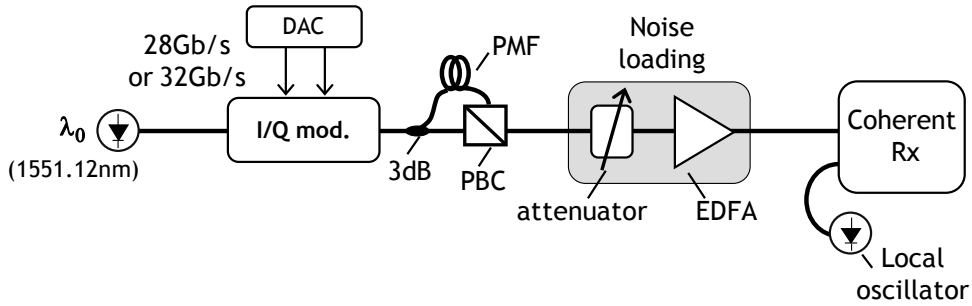
3.5 System environment testing

Up to 2011, the most common forward error correction (FEC) in wavelength-division multiplexed (WDM) transmission systems at 10Gb/s and 40Gb/s bit-rates uses a concatenated code assuming hard-decision, with 7% overhead and a net coding gain (NCG) of ~8.5dB, leading to an FEC bit-error rate (BER) threshold of $4 \cdot 10^{-3}$ or a Q^2-factor of 8.5 dB. An alternative is to use a much powerful soft-decision FEC. With a 23.6% overhead, such a FEC could correct BERs up to $2 \cdot 10^{-2}$ (6.25 dB Q²-factor)**Erreur ! Source du renvoi introuvable.**. We study here the use of this late FEC since it should be compatible with 56-GBaud receivers.



Experimental set-up for noise sensitivity assessment involving a standard transmitter on $LiNbO_3$ and the dual polarization receivers developed in MIRTHE

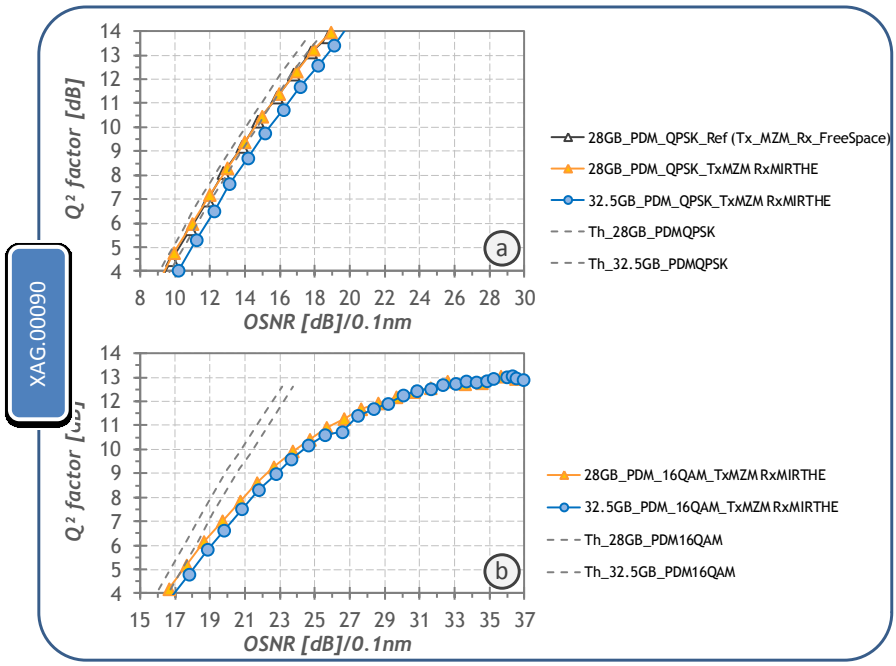
The experimental setup used here is represented in figure below**Erreur ! Source du renvoi introuvable.**. We considered here a higher baudrate, 32.5 GBaud. Each DAC provides a multi-level delayed-decorrelated sequence of length 2^{13}-1 at 28 or 32.5 Gbaud with based on root-raised cosine function with roll-off of 1 to obtain QPSK and 16QAM signals. Polarization multiplexing is performed as previously explained. At the receiver side, we used here the 56-GBaud dual-polarization MIRTHE receiver. Its 4 outputs are detected and sampled at 40 GS/s using a digital oscilloscope with a 20-GHz electrical bandwidth. For each measurement, we store ten different data sets of 20-µs duration. Afterwards, the waveforms are processed off-

line in a computer, as in previous section. The recovered data are decoded, using differential decoding, and errors are counted. We compute then the bit-error ratio (BER), and convert it into Q²-factor.

Results obtained with 28 and 32.5 GBaud PDM-16QAM show a performance close to theoretical expectation for low values of Q^2-factor while they show a performance saturation (error floor) at around 13-dB of Q^2-factor. Lowering the FEC limit is even more important for complex signal such as PDM-QAM. As a matter of a fact, the FEC limit (8.5 dB of Q²-factor) if obtained for an OSNR of 22 dB in 0.1 nm when considering 28 GBaud. On the contrary, 32.5 GBaud PDM-16 QAM achieves the FEC limit (6.25 dB of Q²-factor) performance for ~19.5 dB of OSNR, i.e. 2.5 dB better than the performance at 28 GBaud.

According to our results, MIRTHE receivers presented a very good performance, at least as good as the best state-of-the-art receivers.

MIRTHE WP1 fabricated dual-polarization QPSK TX chips including 40 photonic functions which is probably the most complex InP integration for a single channel ever made. All functions are operational confirming a possibility for a good fabrication yield provided by InP-integration platform. As only this second technology iteration was possible during MIRTHE project, some issues remained. As suggested by the first testing campaign, gap alignments between all integrated components, especially this of SOA overlaps now correctly the laser line emission. Also, intra-chip reflections previously due to low-loss passive waveguide technology were removed. However, two harming points were not solved: low power of integrated lasers due to SIBH technology drift after epitaxial equipment change and accidentally not good enough AR coating of TX output facet. Low laser power and exacerbated SOA amplification led to whole cavity erratic influence on the laser emission due to a large return power.



Optical noise sensibility of 28 and 32.5 GBaud of (a) PDM-QPSK and (b) PDM-16QAM signals received with XAG.00090 MIRTHE receiver and standard transmitter based on $LiNbO_3$ modulator

In spite of mentioned limitations these chips were successfully packaged by U2T in WP3. This work confirmed significant improvement of the modulation bandwidth being now in the range 30-40GHz which is, in principle, compatible with 56GB data rate. The fabricated packages demonstrated the development of full technology chain up to system testable prototypes by the project.

However, the self-pulsation behavior and erratic cavity FP lasing was confirmed for packaged devices. These phenomena happened in GHz range and could be suppressed by EAM bias producing 4dB loss

in each interferometer arm. Unfortunately as we observed during system pretests, they were fast enough to reappear again under data modulation preventing from correct operation. In spite of lot of work provided, we could not find favorable biasing points for both fabricated packages. By working with these devices, we gained more expertise as to the component adjustment and parameter control procedures.

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With this new experience we took the decision to reuse **SP-TX** module in MIRTHE final PIC-to-PIC experiment.

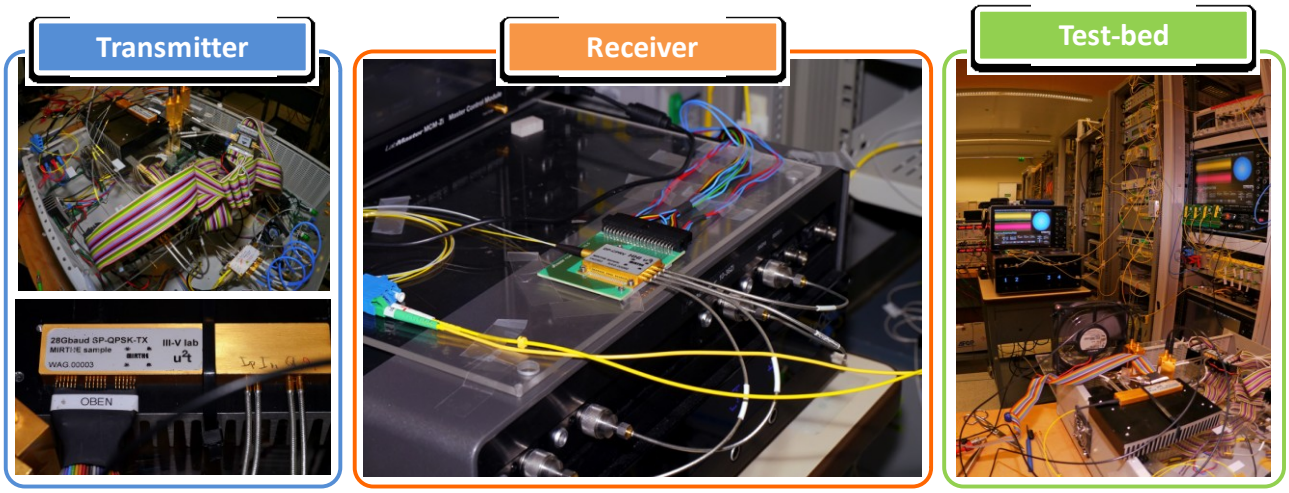
3.6 PIC to PIC experiment

Unlike all the preceding experiments, we used here MIRTHE components at the transmitter and at the receiver end at the same time. At the transmitter side, modulator is fed by 2^{15}-1 bit-long sequences at 32.5 Gb/s, including forward error correction (FEC) and protocol overhead. After being modulated, the test channel is passed through a noise loading stage. 4 outputs of RX are detected and sampled at 80 GS/s using a digital oscilloscope with a 36-GHz electrical bandwidth. The recovered data are decoded, using differential decoding, and errors are counted. We compute then the bit-error ratio (BER), and convert it into Q^2-factor.

Different pictures of the actual PIC-to-PIC system experiment show on the left hand side the transmitter setup and a detail of the transmitter module. We distinguish in this figure the PIC module, the electrical alimentation, the rack used for PRBS generation and the bias tee modules used to feed the module. In the center we see the 56-GBaud dual-polarization RX module connected to the 36-GHz 80-GSamples/s sampling oscilloscope. The figure at the right hand side depicts in turn the whole systems setup. The transmitter can be appreciated in foreground whereas the receiver is in background. In the middle of this figure at the right hand side, is placed the noise loading stage involving an attenuator, a dual stage amplifier and an optical pass-band filter.

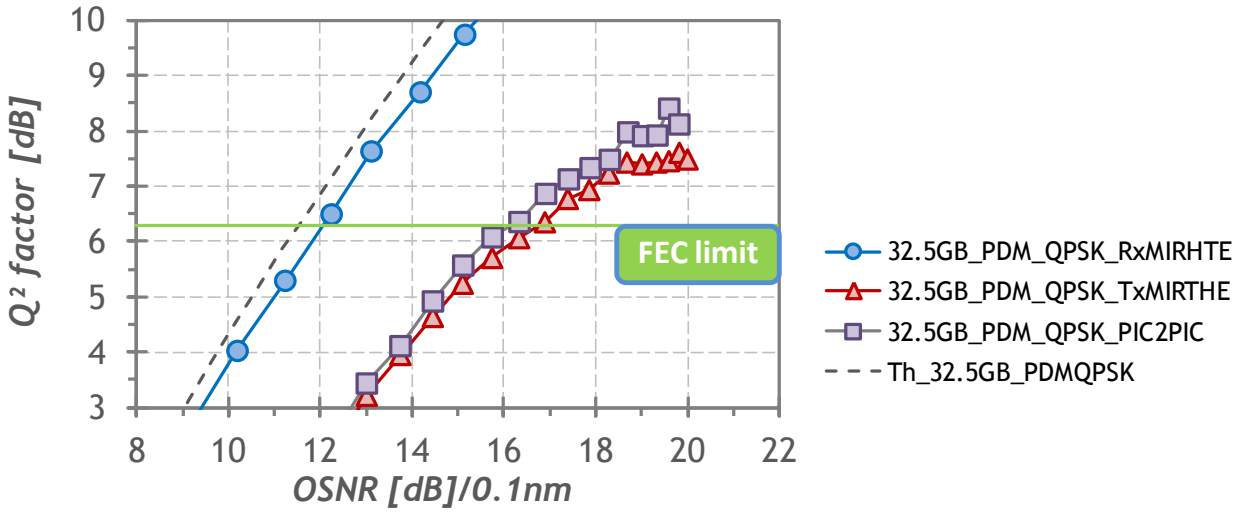
We measured the optical noise sensitivity of the 32.5-GBaud PDM-QPSK PIC-to-PIC system and compared with the one of each PIC component independently. The performance of 56-GBaud dual-polarization receiver (blue circles) is very close to the theoretical expectations, represented by the dashed line in Fig below. No error floor is observed and measured performance is less than 1-dB away from the theory.

Further on, we also demonstrate error-free operation (after FEC correction) for MIRTHE transmitter with PDM-QPSK at 32.5 GBaud. We observe a significant penalty of ~5.5 dB in terms of required OSNR for 6.25 dB of Q^2-factor (red triangles) when compared to the theoretical performance and as error floor at around 7.dB of Q^2-factor. We attribute these penalties in performance to the phase-noise coming from the transmitter and to the transmitter/receiver bandwidth limitation and imperfect frequency response. Finally, violet squares depict the performance of a PIC-to-PIC system. Surprisingly, this performance is even better than that of MIRTHE transmitter with free-space receiver.



Pictures of the experimental setup. (left) PIC transmitter showing electrical branching, PRBS generation, detail of PIC module. (center) PIC received installed and connected to the sampling oscil°loscope. (right) overall view of the system resting showing the transmitter in foreground and the receiver in background

In summary, concentrating all partner's work **PIC-to-PIC experiment with all-monolithic InP packaged TX and RX has been successfully realized in system environment at 32.5GBaud** (130Gb/s) providing OSNR above the FEC limit. This is very likely **the world first experiment** of this type. The PIC-to-PIC experiment demonstrated also excellent **performance of the close-to-product 56GB dual-polarization all-monolithic RX which has to be considered as the most significant technical achievement of MIRTHE.**



Optical noise sensibility of 32.5 GBaud PDM-QPSK over different conditions (blue circles) generated with $LiNbO_3$ MZM and detercted with a dual-polarization 56-GBaud MIRTHE receiver, (red triangles) generated with MIRTHE transmitter and detected with free-space optics based coherent mixer paired with balanced photodiodes and (violet squares) generated and received with PIC MIRTHE components.

3.7 Towards 400 Gb/s

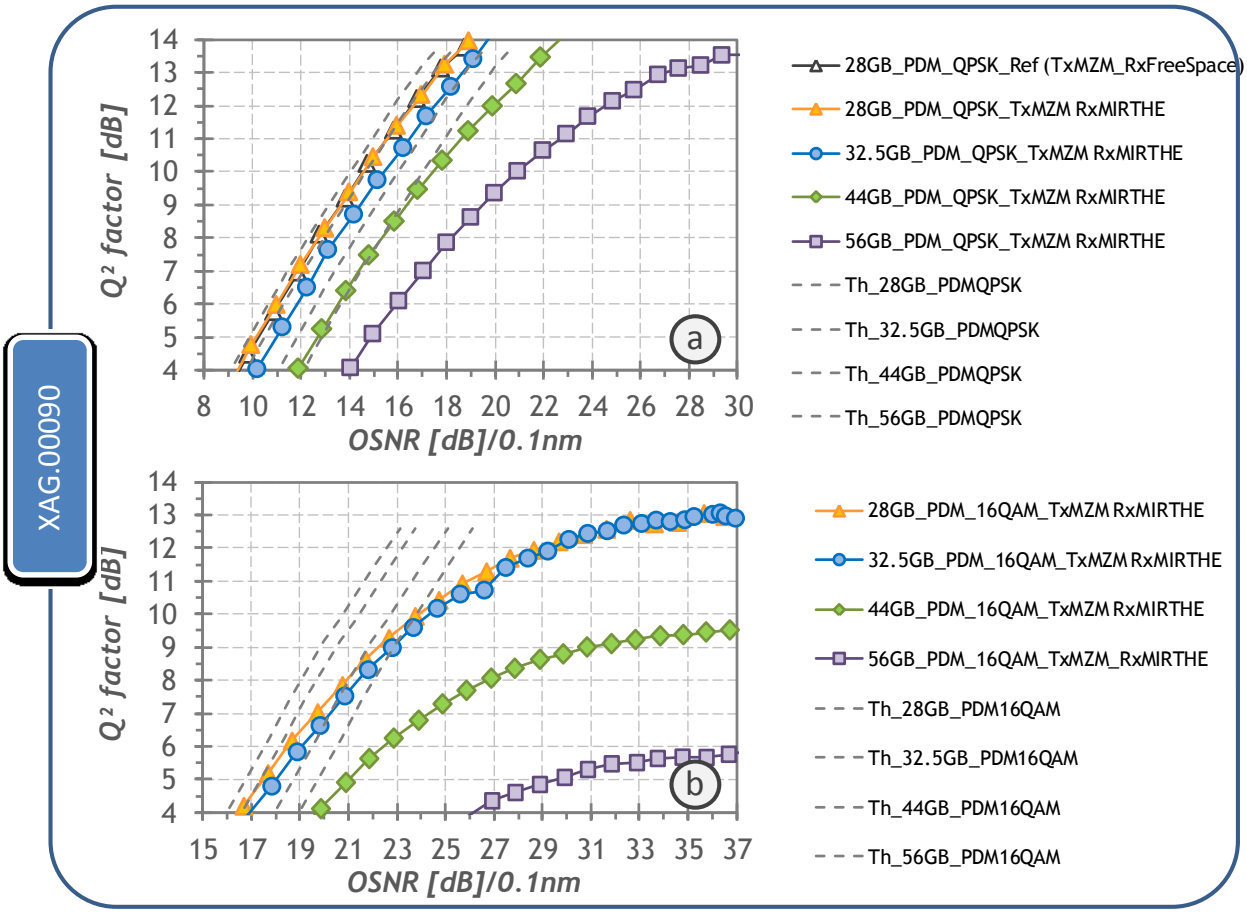
At the transmitter side, we used here a relatively standard transmitter based on LiNbO3 modulator and external laser. To produce different signals, the light from a continuous wave (cw) laser is sent into two dual-drive I-Q modulators driven by a pair of digital-to-analog converters (DAC) operating at 56-GSamples. This provides PDM-QPSK signals at 112, 128, 176 and 224 Gb/s; and PDM-16QAM signals at 224, 256, 352 and 448 Gb/s. At the receiver side we used here a 56-GBaud dual-polarization receivers developed within the MIRTHE project.

MIRTHE receiver gives the same performance as the reference curve obtained with free-space optics and balance photodiodes for 28-GBaud PDM-QPSK. The 28-GBaud PDM-QPSK signal requires an OSNR of about 14.5 dB for 9.8-dB Q²-factor performance (corresponding to 10-3 BER), only ~0.5-dB away from the theory. Moving from 28 GBaud to 32.5GBaud implies a higher OSNR for the same BER. In theory, this higher OSNR requirement is 10*log(32.5/28)=0.64dB. However, we observe that 32.5 GBaud PDM-QPSK requires about 15.5 dB of OSNR for 9.8-dB Q²-factor, 1-dB higher OSNR requirement compared to 28 GBaud results. This indicates a slight limitation in bandwidth. The limitation may come from three different sides; the transmitter, the coherent receiver and the sampling oscilloscope. Nevertheless, we achieve error-free operation for 224-Gb/s (56 GBaud) PDM-QPSK after FEC correction as the FEC limit is 8.5 dB of Q2-factor.

Results obtained with PDM-16QAM signals. 28, 32.5 and 44 GBaud PDM-16QAM, show a performance relatively close to theoretical expectation for low values of Q2-factor while 56 GBaud PDM-16QAM are already far away from theoretical performance at 4-dB Q2-factor. All PDM-16QAM results show performance saturation (error floor). The level of the error floor depends on the baud-rate, as expected. Contrary to 56GBaud QPSK signals, we were not able to achieve here a better performance than the FEC limit.

In summary, the project eventually delivered all expected packages with single-polarization and dual-polarization all monolithic chips. Finally, most successful experiments were possible with all RX versions and with single polarization TX. This PIC combination allowed us to eventually carry out a successful 32.5 GB (130 Gb/s) PIC-to-PIC experiment and thereby fulfill the main MIRTHE commitment. DP-RX is shown to operate over FEC limitation up to 44GB 16-QAM delivering 352Gb/s cumulated data rate being limited rather by experimental setup.

The system environment testing in MIRTHE project allowed to understand better the level of maturity of integrated Tx or Rx solutions, as well as the remaining challenges. It is expected that this will enable the concerned industrials to make some selections of transmitters and receivers for the development of their products.



Optical noise sensibility of (a) PDM-QPSK and (b) PDM-16QAM signals for different baudrates: 28, 32.5, 44, 56 GBaud. The signals are generated by a LiNbO3 –based modulator and received with XAG.00090 MIRTHE receiver