Project objectives:
To develop the Charge Trapping Technology for very high density Non Volatile Memories for mass storage, targeting the 22 nm technology node.

Start date: January 1st, 2008
Duration: 3 years

Memories for the mobile world

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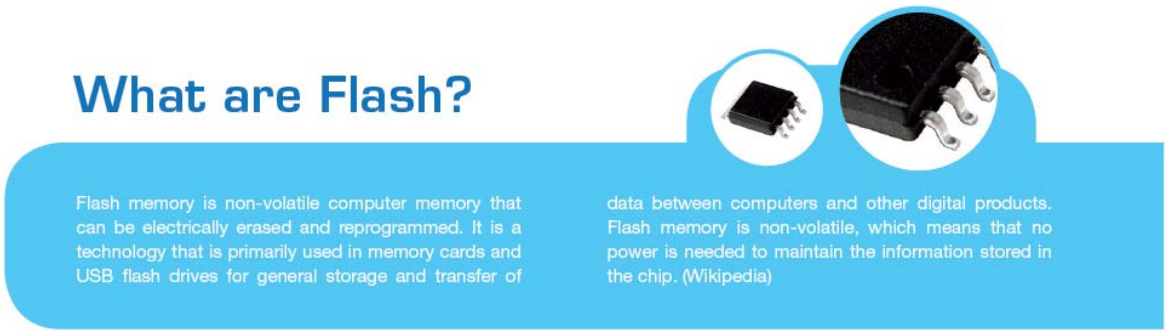
During the last 15 years, ICTs have provided a number of radically new devices / techno-toys that have improved the daily life of the EU citizen: mobile phone, digital camera, MP3 players, PC, PDA, credit cards, video on discs, flat screen, HD TV, fast communications (ADSL)…

Solid-state memories are the preferred solution for mobile applications. Their main advantages are the use of consolidated technology, the lack of any mechanical parts, which results in stronger ruggedness, lighter weight, smaller form-factor, better reliability and, above all, **lower power dissipation**.

And solid-state mass-storage today means NAND Flash memories



Pushing the limit of Flash

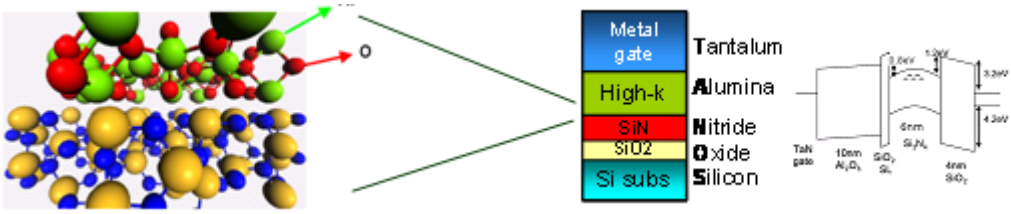
NAND Flash is by far the dominant technology for solid-state mass-storage. However, the floating gate concept is predicted to face technological limits around the 32nm node. The main physical limits that prevent further scaling of the cells are:

- cell to cell interference, due to the parasitic capacitive coupling among neighbouring floating gates;
- low coupling ratio with the control gate, which results also in a small stored charge.

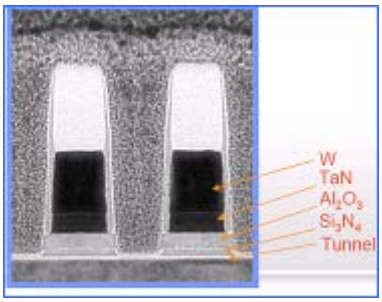
year	2004	2006	2008	2011	2014
Node	90nm	65nm	45nm	32nm	22nm
NOR					
NAND					

On the other side, trap-related leakage currents in the dielectrics prevent any scaling of the cell dielectrics, which could relieve this issue. Further reduction of cell size will increase the requirements for error correction beyond the feasibility limits.

The most promising option to overcome these scaling limitations, while retaining the very high integration density of NAND Flash architecture seems to be the replacement of the conventional floating gate with a charge trapping layer.



Project Approach



The consortium is build around two major European semiconductor companies, Numonyx and Qimonda, with a strong experience and a technical leadership in different types of memories (DRAM for Qimonda and NOR Flash for Numonyx) and have a great interest for NAND Flash memories, because of their strategic importance for a variety of applications.
The consortium includes a balanced combination of all types of research performers: Large Industry, Small and Medium Industry, Research Centres and Universities

The key to the success of the project will be in the tight integration of allocated resources and their focalization, inside 7 Work Packages:

WP0 Management
WP1 Material Development
WP2 Cell Architecture
WP3 Process Integration
WP4 Demonstrator
WP5 Characterization & Reliability
WP6 Higher density Architectures
WP7 Dissemination & Training