Section 1 - Publishable Summary

1.1 Project objectives

- To develop a technology suitable for the realization of gigabyte Non Volatile Memory devices for mass storage, in the 3x and 2x technology nodes (x=2-8), based on charge-trapping NAND Flash architecture.
- To define material, cell architecture and processing technology.
- To realize a technology demonstrator with a memory size in the order of Gigabytes.

Start date: January 1st, 2008
Duration: 42 months

1.2 Memories for the mobile world

During the last 15 years, ICTs has provided a number of radically new devices / techno-assistants that have improved the daily life of the EU citizen: mobile phone, digital camera, MP3 players, PC, PDA, credit cards, video on discs, flat screen, HD TV, fast communications (ADSL), car navigators, assisted driving**…. None of them could work without Flash memories!**
Driven by the market of mobile telecom devices, NAND memories have become a serious contender to DRAM in production volumes and have become the main technology driver for Nanoelectronics. The latest market data show that in 2010, the severe economic downturn of 2008 has been fully recovered, and sales of NAND memories have exceeded the values of 2007. Expected total sales in 2011 will be around 23B US$, mostly for mobile applications (mobile phones, consumer electronics, netbooks and tablet PC)

1.3 Pushing the limit of Flash

NAND Flash is by far the dominant technology for solid-state mass-storage. Constant cell scaling and memory size increase have kept pace with the increasing demands of applications

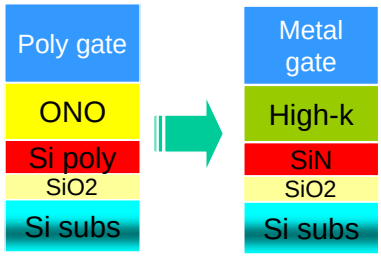
year	2004	2006	2008	2011	2014
Node	90nm	65nm	45nm	32nm	22nm
NOR					
NAND					

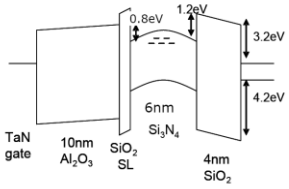
However physical limits are appearing: cell to cell parasitic capacitive coupling; low coupling ratio with the control gate; small stored charge; charge loss through gate dielectrics.

The GOSSAMER project aims at finding solutions to overcome these limits

1.4 From capacitor storage to trapped charge

The most promising option to overcome these scaling limitations, while retaining the very high integration density of NAND Flash architecture seems to be the replacement of the conventional floating gate with a charge trapping layer.





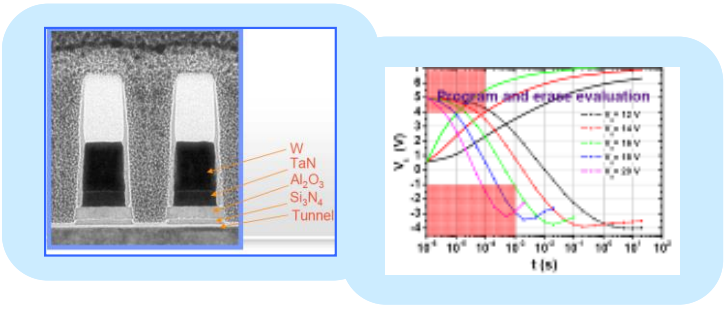
1.5 Project Consortium

The consortium was initially built around two major European semiconductor companies, Numonyx and Qimonda, with a strong experience and a technical leadership in different types of memories (DRAM for Qimonda and NOR Flash for Numonyx) and included a balanced combination of

- Equipment suppliers: Active Technologies, ASMI, Jordan Valley
- Research Centers: IMEC, CNR-MDM, Tyndall, Fraunhofer CNT
- Universities: IUNET; University of Braunschweig, University of Freiberg
- SME's: Jordan Valley, Active Technologies

Unfortunately Qimonda had to leave the consortium in 2009, due to financial problems, while University of Freiberg was replaced by NamLab. During 2010 Numonyx has been acquired by Micron and it is now part of the Micron group.

1.6 First results



Developing the cell

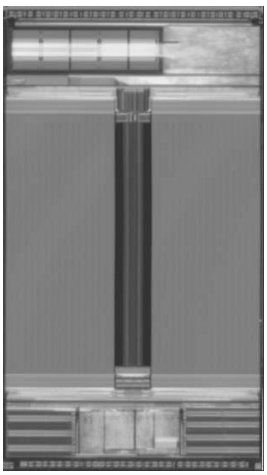
In the first years of the project material and cell architectures were developed leading to the characterization of functional mini-arrays.
Optimized stack composition and programming conditions were defined thus leading to a second more ambitious target.

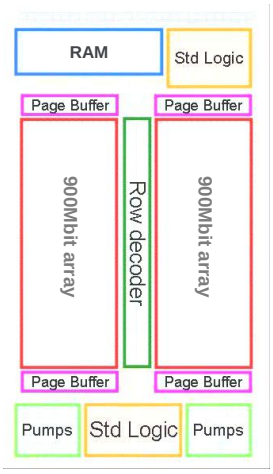
A fully functional 1Gbit NAND Flash device

In 2009 it was decided to anticipate a full industrial demonstrator, making use of the most advanced single exposure litho technology available.

A 1 Gbit NAND memory device was modified by Numonyx to become compatible with the new cell architecture. With the new architecture 1.8 Gcells could be accommodated in the same device area, even if only 1Gbit is addressable.

Fully functional samples have been obtained with good programming performances and acceptable reliability. Innovative technology steps were





introduced for the first time on a large scale, like barrier engineered tunnel dielectric, which showed the capability for further enhancing device performances.

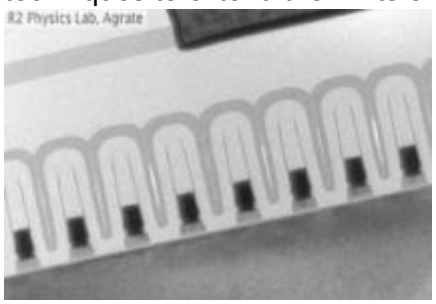
Dedicated testing equipment has been developed for fast and reliable assessment of development memories, and it has been demonstrated on the 1Gbit device

1.7 The next step

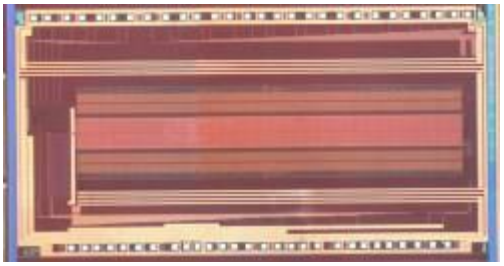
In the course of the project it became evident that the original target of developing a 32nm generation technology was ambitious enough. Due to the faster than foreseen progress of conventional Flash devices, with 24nm devices entering production, it was decided to focus the effort in proving the scalability of the technology to the 20nm generation. At the same time a new trend was emerging for high density memories: 3-D architectures, and the partners decided to investigate this approach for TANOS memories.

20nm technology

Active cell size was scaled down in the 20-25nm range by using special lithographic techniques to extend the limits of available immersion lithography. Active area definition, high aspect ratio trench etching and filling and edge rounding problems were solved. A Self-Aligned Architecture was selected for the cell after extensive experimentation and modeling and a correct gate profile was achieved.



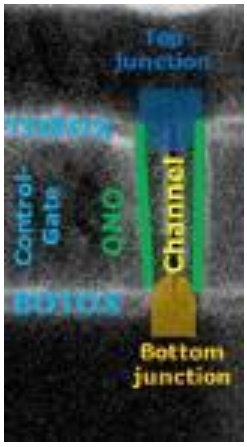
In the end functional cell blocks were obtained. The same mask set used for the large scale demonstrator was processed. Due to the limitations of the lithography it was not possible to have fully functional samples of the 1Gbit demonstrator, but mini-arrays of 4Mbit, with simplified control circuitry were realized and successfully tested.



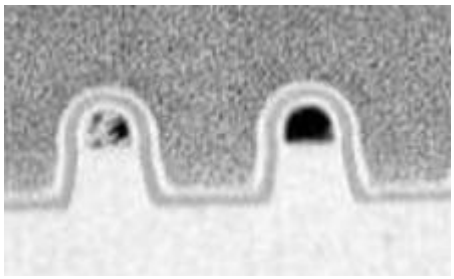
The scalability of the TANOS technology down to the limits of the available lithography has therefore been demonstrated.

Exploiting the third dimension

Stacking memory cells in several layers is getting increased attention as a way to overcome lithography limitations. SONOS architectures are the only viable choice for these approaches. Therefore the partners have decided to include in the next step the exploration of architectures suitable for the 22nm node, exploiting the capability of 3D integration. Two approaches have been investigated.



Vertical channel (Toshiba approach) has been investigated from IMEC and Fraunhofer-CNT. Several combinations of layers and etching steps have been tested for achieving a good bottom contact and preserving layer integrity. Basic functionality has been achieved of test structures (left).



Multilayer stacking (Samsung approach) has been tested by Numonyx/Micron both with single crystal channels on SOI and polycrystalline channel on thermally grown oxide, and full rounded channel (right). Functional cells have been realized and characterized for performances and reliability.

Section 2 - Project objectives and major achievements during the reporting period

2.1 General project objectives

The objective of the project was the development of large size NAND Flash memories based on the charge trapping mechanism, instead of the conventional floating gate concept, with the target of addressing the technology generations in the range of 36-28nm. The final result expected was the realization by the industrial partners of two industrial demonstrators of the new concept with a target size close to the foreseen upper limit of the technology, in the order of the Gigabyte (=8 Gigabit).

The project aimed also at realizing a close cooperation between public research and industry, with the target to integrate the complete R&D chain, from basic technological research on the properties of new materials, based also on theoretical models, through equipment and material development, device modelling and characterization, down to industrial research and design, and to the realization of pre-competitive prototypes of high density memories.

In this way the project had also the objective to contribute to closing the gap between research and industrial exploitation, the so-called “European Paradox” that too often causes the results of promising projects to remain unexploited, or to be exploited in a second moment outside Europe.

The target performances of the final demonstrators are illustrated in the table:

Target Performances of final demonstrators		
Parameter	Value	Units
Memory Size	8	Gbit
Target technology generation (litho dependent)	32	nm
Cell Area	4	F^2 (*)
Programming Voltage	20-25	V
Threshold Window	~5	V
Reading Current	~100	nA
Endurance	$>10^4$	cycles
Retention time	10	Yrs
(*) F=technology node		

Following the faster than expected evolution of the floating gate NAND Flash technology, it was decided to anticipate a demonstration of the feasibility of the technology on a large scale device in 45nm technology, and to focus the final demonstration on the proof of the scalability of the TANOS technology towards the 20nm generation.