Section 1 - Publishable Summary

1.1 Project objectives

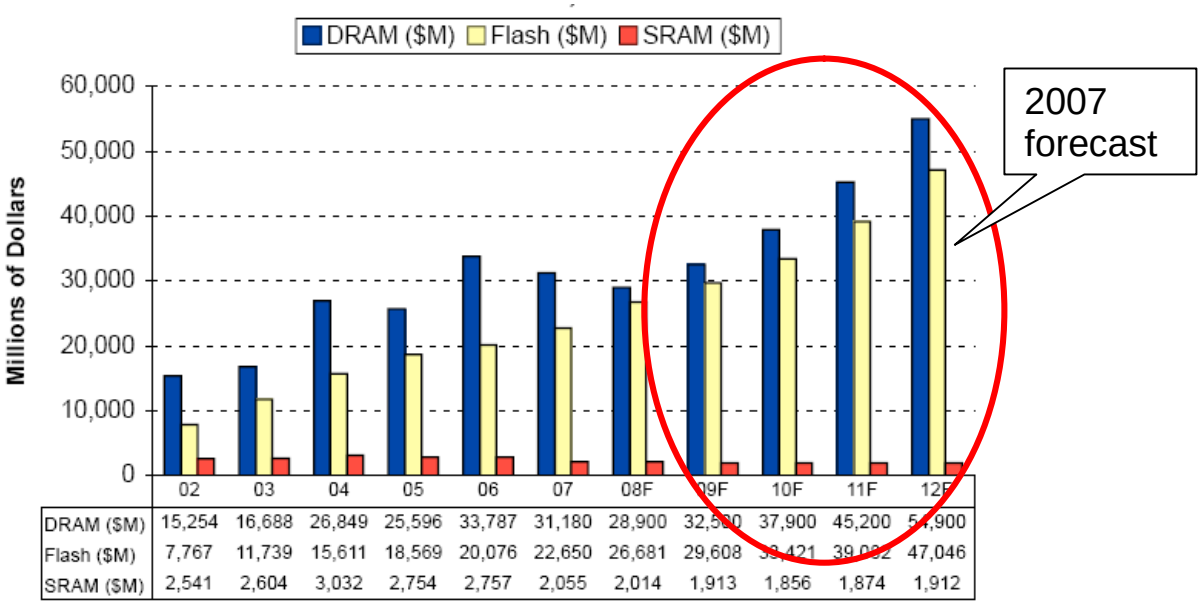
- To develop a technology suitable for the realization of gigabyte Non Volatile Memory devices for mass storage, in the 3x and 2x technology nodes (x=2-8), based on charge-trapping NAND Flash architecture.
- To define material, cell architecture and processing technology.
- To realize a technology demonstrator with a memory size in the order of Gigabytes.

Start date: January 1st, 2008
Duration: 3 years

1.2 Memories for the mobile world

During the last 15 years, ICTs have provided a number of radically new devices / techno-toys that have improved the daily life of the EU citizen: mobile phone, digital camera, MP3 players, PC, PDA, credit cards, video on discs, flat screen, HD TV, fast communications (ADSL)… Solid-state memories are the preferred solution for mobile applications. Their main advantages are the use of consolidated technology, the lack of any mechanical parts, which results in stronger ruggedness, lighter weight, smaller form-factor, better reliability and, above all, **lower power dissipation**.

And solid-state mass-storage today means NAND Flash memories



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DRAM ($M)	15,254	16,688	26,849	25,596	33,787	31,180	28,900	32,500	37,900	45,200	54,900
Flash ($M)	7,767	11,739	15,611	18,569	20,076	22,650	26,681	29,608	33,421	39,092	47,046
SRAM ($M)	2,541	2,604	3,032	2,754	2,757	2,055	2,014	1,913	1,856	1,874	1,912

Source: WSTS, IC Insights

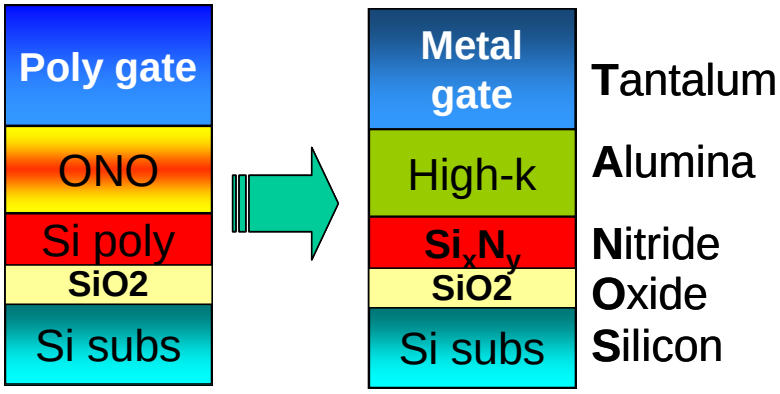
Driven by the market of mobile telecom devices, NAND memories have become a serious contender to DRAM in production volumes and have become the main technology driver for Nanoelectronics. The latest market data seem to show that in 2009, in spite of the severe economic downturn, sales of NAND memories will exceed the values of 2008.

1.3 Pushing the limit of Flash

NAND Flash is by far the dominant technology for solid-state mass-storage. However, the floating gate concept is predicted to face technological limits around the 32nm node. The main physical limits that prevent further scaling of the cells are:

- cell to cell interference, due to the parasitic capacitive coupling among neighbouring floating gates;
- low coupling ratio with the control gate, which results also in a small stored charge.

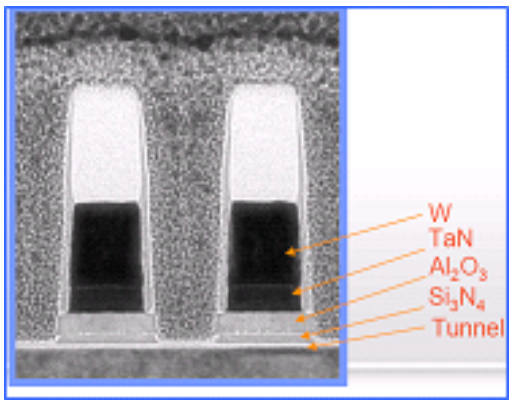
On the other side, trap-related leakage currents in the dielectrics prevent any scaling of the cell dielectrics, which could relieve this issue. Further reduction of cell size will increase the requirements for error correction beyond the feasibility limits.

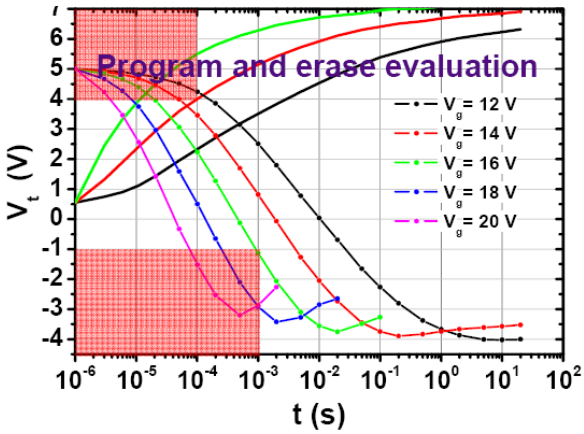


The most promising option to overcome these scaling limitations, while retaining the very high integration density of NAND Flash architecture seems to be the replacement of the conventional floating gate with a charge trapping layer. Even if apparently a direct evolution of conventional approach, the TANOS architecture implies the introduction of new materials, and will require a substantial progress in material science.

1.4 Project Approach

The consortium was built around two major European semiconductor companies, Numonyx and Qimonda, with a strong experience and a technical leadership in different types of memories (DRAM for Qimonda and NOR Flash for Numonyx) and includes a balanced combination of all types of research performers: Large Industry, Small and Medium Industry, Research Centres and Universities..

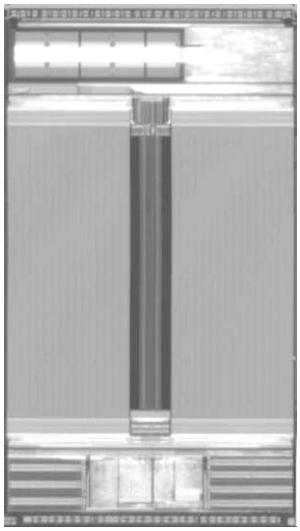


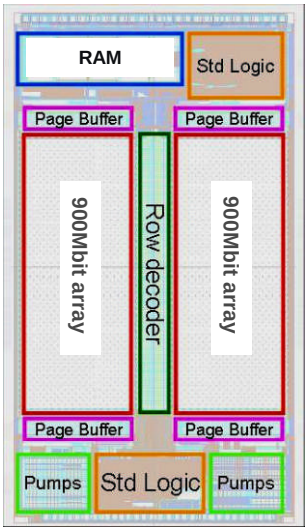


In spite of the economical problems the project achieved substantial progress, demonstrating the capability of the new technology on fully functional cells and cell arrays, developed and tested at Numonyx, Qimonda and IMEC. Good write-erase performances were obtained and first reliability tests were performed.

1.5 2009 results

Following the first promising results, in 2009 it was decided to anticipate a full industrial demonstrator, making use of the most advanced single exposure litho technology available.





A 1 Gbit NAND memory device was modified by Numonyx to become compatible with the new cell architecture and fully functional samples have been obtained.

First evaluation on the large statistical samples made available by the memory device did show good distribution of written and erased states, even if no programming algorithms were used to compensate for the threshold distribution, and confirmed the absence of cell to cell interference, which is the most important limit to NAND cell scaling. The device was used also to test new technology approaches to the cell architecture, introducing the Band Engineered Tunnel architecture (BET for short). Based on the replacement of the tunnel oxide by an oxide-nitride sandwich, the new structure allows for better programming characteristics and better reliability.

Unfortunately in 2009 Qimonda had to leave the consortium, due to financial problems that eventually led the company into bankruptcy.

Given also the progress in conventional NAND technology, that in 2009 saw several companies announcing the early availability of 32-34nm NAND Flash memories, based on the floating gate approach, the Consortium decided to focus the effort towards the 22nm node, exploiting the availability of the 1Gbit demonstrator for trimming the basic architecture in an industrial environment.