NANOSIL

Silicon-based nanostructures and nanodevices for long term nanoelectronics applications

Network of Excellence

WP1

Deliverable D1.6
Devices containing new channel materials: assessment and comparison with simulations

Main Author(s):
D. Buca, Q.Zhao, S. Mantl, D Leadley

Due date of deliverable: 31 March 2011
Actual submission date: 31 March 2011

Project funded by the European Commission under grant agreement n°216171

LIST OF CONTRIBUTORS

Part. Nr.	Acronym	Organisation name	Name of contact
14	FZJ	Forschungzentrum Juelich	Siegfried Mantl
16	TUBS	Technische Universität Braunschweig	Bernd Meinerzhagen
3	Warwick	University of Warwick	David Leadley
26	GU	University of Glasgow	Asen Asenov
8	IMEC	Interuniversitair Micro-Electronica Centrum	Jerome Mitard

Deliverable Summary

This report is devoted to the assessment of integration of new channel materials, like strain-engineered Si/SiGe semiconductors, with novel higher-k materials. A *self aligned full replacement gate* process was developed to fabricate *n*- and *p*- FD MOSFETs on biaxial tensile strained SOI. Large mobility enhancement for the strained silicon devices in the presence of $TbScO_3$, $LaScO_3$ and $LaLuO_3$ gate dielectrics and a good quality of the high-k/Si interface is demonstrated.

The improvement of p-MOSFETs is addressed by using compressively strained $Si_{0.5}Ge_{0.5}$ as channels. For this study FD quantum well (QW) devices using a *gate first* process were fabricated. A complete evaluation of p-MOSFETs with gate length down to 65 nm with <100> and <110> channel orientations were studied first. Two strain states in the SiGe channels, obtained by epitaxial growth on SOI and SSOI substrates, were studied. The influence of different high-k dielectrics on hole mobility is addressed via long channel devices and the experimental results are compared with theoretical simultations. Hole mobility benchmarking for strained Si and SiGe channels with different higher-k dielectrics is presented.

Strained Ge channels are also considered, with results presented for p-MOSFETs with high mobility. The effects of processing and channel length reduction are considered showing how these can degrade the optimal mobility. Simulations of mobility in pure Ge channels on various orientations are presented along with an analysis of the effect of heavy channel doping.

Table of contents

1. Introduction

According to the ITRS the implementation of high-*κ*/metal gate technology and strained high mobility channels is mandatory [1]. Moreover, in order to improve the transistor properties and lower the power consumption, it is also suggested to use SOI and high mobility strained SOI (sSOI) substrates [1-2]. This combination provides faster transistors with simultaneously lower leakage currents and less power consumption.

State-of-the-art p-MOSFETs currently in production utilize embedded Si_xGe_{1-x} source and drain to induce uniaxial compressive strain in the Si channel as a means to increase the drive current through enhancement of hole mobility [28]. However, saturation of both hole mobility and carrier velocity in strained Si (100) channels set natural boundaries for performance enhancement below the 45 nm node. Therefore, new channel materials are required for the performance scaling trend to continue.

Strained SiGe is seen as a very promising Si channel alternative for p-MOSFETs. The carrier mobility in SiGe is increased through compressive strain induced valence band splitting and band warping if the layer is pseudomorphically grown on Si, resulting in substantially enhanced drive current. Also, SiGe is fully compatible with the mainstream Si processing technology and does not impose the challenges involved in the integration of pure Ge channels. Ultimately, once technological issues have been solved, pure Ge channels may have superior properties and are also being investigated for longer term implementation.

In order to suppress short channel effects, it is desirable to improve the electrostatic control of the gate over the channel, by going to thinner gate oxides. However, as the SiO_2 gate oxide gets very thin, quantum mechanical tunneling causes a gate leakage component of current to flow (~3 times for every 0.1 nm of thickness reduction) and compromise proper logic gate operation. State of the art devices already implement high-k gate dielectrics such as HfO_2. These enable a high gate capacitance with physically thick insulators through which tunneling is low. However, it is very challenging to introduce such new gate-stack materials without an accompanying degradation of mobility and reliability; this remains an area of intensive ongoing research.

1.1 State-of-the-art

Implementing strain into semiconductors has become an efficient method to improve the transport properties. “Local Strain” methods are already successfully applied in industry. For the n-channel numerous strain boosters are employed. The latest approach makes use of stress of the high-k/metal gate stack in a replacement gate process.

Ge has been successfully used as channel material for p-MOSFETs [3,4], but the progress of Ge n-MOSFETs has lagged behind Ge p-MOSFETs. Ge n-MOSFETs can potentially provide even higher electron mobility than strained Si [1], while the major challenges include reduction of interface state density, dopant activation, high-k integration and so on. Researchers from The University of Tokyo systematically investigated Ge interface passivation methods and reported dramatic reduction of D_{it} through self-passivation and valency passivation, achieving an electron mobility of 1920 cm^2/Vs and hole mobility of 725 cm^2/Vs [2]. Taiwan National Nano Device Laboratories fabricated n-MOSFETs on Ge substrate with GeO_2 passivation, remote O_3 plasma, two-step S/D activation and gate-last integration with high-k, exhibiting high mobility and high on/off ratio [5]. National Chiao-Tung University reported low EOT Ge n-MOSFETs using laser annealing, with EOT scaling down to 0.95nm and sheet resistance of 73 Ω/sq [6].

SiGe p-MOSFET also got some new progresses. IMEC reported an implant-free SiGe quantum well pFET, with drive currents improved by 50%, and a 0.85nm-EOT SiGe pFET, with hole mobility improved by 50% [7]. FZ-Jülich reported a SiGe quantum well pFET with novel higher-k gate dielectric, achieving high hole mobility, 2.5 times higher than the universal hole mobility [8]. Intel reported good progress with a pFET [9].

References:

[1] K. Morii et al. IEDM 2009-681
[2] C.H. Lee et al. IEDM 2010-416
[3] R. Loo et al. J. ECS 157, H13-H21, 2010
[4] Duygu Kuzum et al. IEDM 2009-453
[5] Yen-Chun Fu et al. IEDM 2010-432
[6] W.B. Chen et al. IEDM 2010-420
[7] J. Mitard et al. IEDM 2010-249
[8] W. Yu et al. EUROSOI 2010
[9] R. Pillarisetty et al. IEDM 2010-150

1.2 Present challenges

Ways of optimizing channel mobility need to be explored in order to overcome the limitations on the scaling down of devices and further improve the speed of CMOS circuits. The introduction of tensile strained-Si on strained/relaxed SiGe for *n*-MOSFETs or compressively strained-SiGe layer on bulk-Si for *p*-MOSFETs can enhance electron and hole mobility. Therefore, the design of a CMOS process combining both a tensile-strained-Si for *n*-MOSFETs and a compressively strained- SiGe for *p*-MOSFETs, fabricated on one structure or one chip, to enhance the electron and hole mobility simultaneously will be required. A good solution to this problem is to use dual-channel structures with tensely strained-Si layer and compressively strained-SiGe layer on SOI or strained SOI substrates. This approach was intensively studied by FZJ and the results are presented in this report.

2. Replacement gate Strained Si / Higher-k MOSFETs

Intrinsic SOI (100) and strained SOI (100) wafers with top Si thickness of 88 nm and 70 nm, respectively, were used as starting materials. The thickness of the buried oxides (BOX) for both, SOI and strained SOI is 145 nm. The elastic strain in the strained SOI substrates amounts to 0.8%, corresponding to a stress of 1.35 GPa. After mesa isolation the top Si and strained Si layers were thinned down by cycling oxidation and HF etching. The final top Si thickness was 35 nm for SOI, and 40 nm for sSOI. The main device fabrication process steps are illustrated in Fig.1. N^+/p^+ S/D areas were implanted with As^+ and BF_2^+ ions, respectively, and activated at 950°C for 1 min.

Three different high-k gate oxides are investigated: $LaScO_3$, $TbScO_3$ and $LaLuO_3$. 7 nm of $LaScO_3$ and 6 nm of $LaLuO_3$ were deposited by MBD and the $TbScO_3$ of thickness of 7 nm by e-beam evaporation. During the deposition the substrate temperature was kept at 350°C for $LaScO_3$, 450°C for $LaLuO_3$ and 600°C for $TbScO_3$. The structures were annealed at 400°C in oxygen and in forming gas (FGA) (10% H_2 + 90% N_2) each for 10 min, to compensate possible oxygen vacancies in the high-k film and provide a better silicon/high-k interface. A 40 nm thick TiN layer was deposited with reactive magnetron sputtering and then patterned with optical lithography and reactive ion etching to define the gate contact. After the deposition of a 100 nm thick PECVD SiO_2 layer, to passivate the structure, contact windows were opened for the gate and S/D. Finally, aluminum was used for contact metallization. FGA at 400 °C for 10 min was performed in order to provide low resistivity S/D contacts.

In the following we will address mainly the $LaScO_3$ and $LaLuO_3$ devices while the comparison with the $TbScO_3$ is presented in Table I.

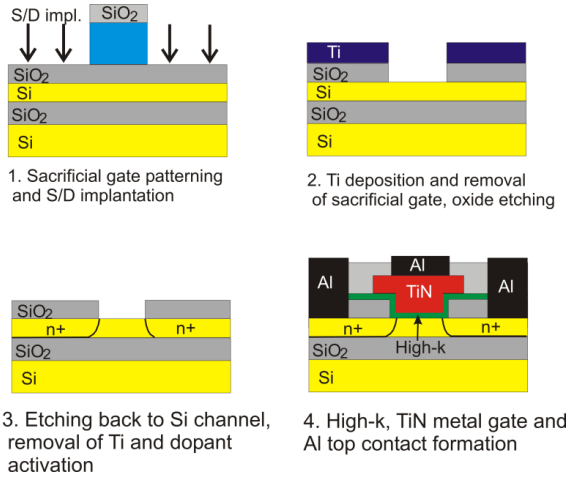

Figure 1: Schematic diagrams of the replacement gate process.

Interface and gate stack characterization

Figure 2 shows the XPS spectra of 3 nm $LaScO_3$ deposited on RCA cleaned Si. For the as-deposited sample, the observed peaks are attributed to the Si substrate located around 150.7 eV, the silicate with different composition of Si-O-La/Sc at ~152.4 eV, and Si rich SiO_x at ~153.8 eV. No SiO_2 signal typical at 154.8 eV is detected. After 10 min at 400°C annealing in O_2 ambient followed by FGA the SiO_2 signal appears indicating the formation of a silicate/SiO_2 interfacial layer.

Figure 3 shows an XTEM image of the TiN/$LaScO_3$/SOI device structure. The thickness of $LaScO_3$ is ~7 nm and the measured SiO_2/silicate like interfacial layer thickness is 1.5 nm.

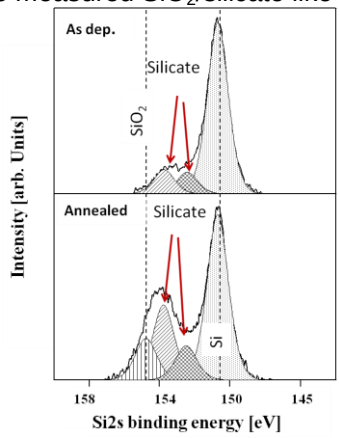

Fig. 2: XPS Si 2s signal for as-deposited and annealed 3 nm LaScO3 films deposited on Si surface.

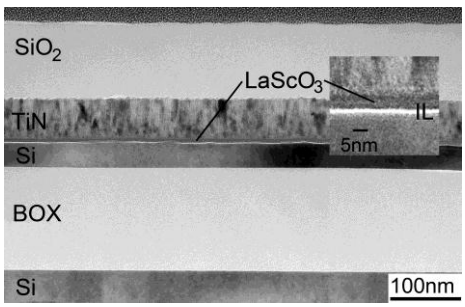

Fig. 3: XTEM micrograph of the TiN /LaScO3/SOI channel stack. The inset shows a zoom on the interface region.

The as-deposited 3.5 nm $LaLuO_3$ film presents a silicate interface layer with a small contribution of SiO_2. After 400°C 10 min O_2 annealing followed by FGA an increase of both silicate and SiO_x components are observed, as shown in Fig. 4a. Fig.4b presents the density of interface states D_{it}, extracted from high frequency C-V on bulk silicon using the method shown in [1], as a function of energy position related to Si valence band.

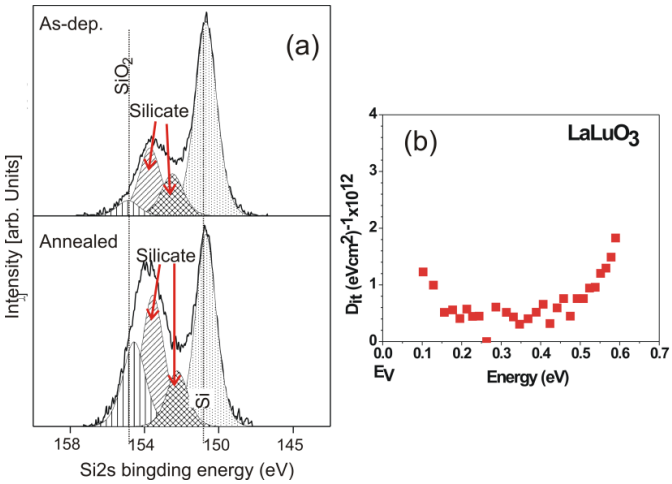

Fig. 4 (a) XPS Si 2s spectra of as-deposited and annealed 3.5 nm $LaLuO_3$ films. (b) D_{it} function of energy in the band gap of crystalline silicon.

Device characterization and mobility extraction

The transfer characteristics of the $LaScO_3$ long channel devices are displayed in Fig. 5a. Ideal inverse subthreshold slopes of 72 mV/dec and maximum I_{on}/I_{off} ratios up to 10^9 were achieved. A V_t of 0.2 V and 0.05V is measured for SOI and strained SOI devices respectively. The V_t shift in attributed to the strain induced change of the electron affinity and to a lower band gap energy of strained SOI [2, 3]. The ΔV_t value is in a good agreement with the theoretical values of Ref.[3], and was also found in devices with $LaLuO_3$ as gate dielectric [4].

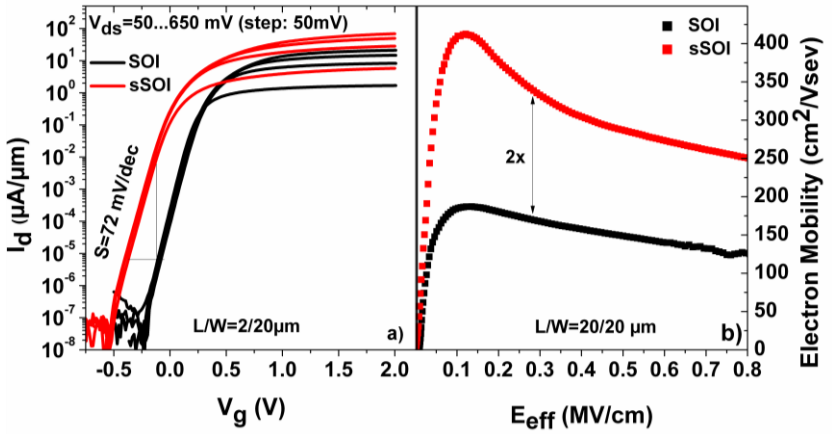

Fig. 5 a) Transfer characteristics of fully depleted SOI and sSOI MOSFETs with $LaScO_3$/TiN gate stacks, b) electron mobility extracted from split-CV measurements of FD SOI and sSOI MOSFETs.

In order to determine the electron mobility in the presence of the novel high-k dielectrics split C-V measurements were performed. The gate to channel capacitance, C_{gc}, was obtained from the C-V characteristics following the procedure proposed by Romanjek *et al* [5]. The effective mobility was evaluated using the equations:

$$\mu_{eff} = \frac{L}{W}\frac{I_d}{Q_{inv}\cdot V_d}; \; Q_{inv}(V_g) = \int_{V_{acc}}^{V_G} C_{gc}(V)dV,$$

where L and W denote the gate length and gate width, $Q_{inv}(V_g)$ the inversion charge density calculated from the corrected $C_{gc}(V_g)$. To correct for high R_{sd}, I_d is replaced by $I_d/(1-R_{sd}\cdot I_d/V_d)$ to obtain more accurate mobility extraction. The interface trap level density was extracted from the subthreshold slope using the equation: $S = 60\,[1+(C_D+C_{it})/C_{ox}]$, taking into account that the highest capacitance is the oxide capacitance, C_{ox}. For $LaScO_3$ film a CET of 2.6 nm for SOI, and 2.7 nm for strained SOI, respectively, and D_{it} ≈$5x10^{11}$ $(eV/cm^2)^{-1}$ were extracted.

The corrected mobilities for SOI and strained SOI derived from split C-V are plotted in Fig 5b. A large enhancement of 100% for the electron mobility was obtained for strained SOI MOSFETs. For SOI and strained SOI with $LaScO_3$/TiN gate stacks low field mobilities of 180 cm^2/Vs and 375 cm^2/Vs, respectively, were extracted. The improvement stems from the elastic strain lifting the degeneracy of the six fold conduction band valleys and the population of the lower energy Δ_2 subband. As a result, in biaxially strained silicon only the smaller effective transversal mass contributes to the electrical transport and, in addition, the energy splitting between the two subbands reduces intervalley scattering [2].

Fig. 6a shows well behaved output characteristics of $LaLuO_3$ FD *p*-MOSFET on SOI and *n*-FETs on SOI and strained SOI substrates with 2 µm gate length and 23 µm gate width. The on-current of the strained SOI *n*-FET was enhanced by a factor of 1.5 due to the biaxial tensile strain. Under a biaxial tensile strain of 0.8%, no enhancement was found for strained SOI *p*-FETs. Therefore, only the results for SOI *p*-FETs are shown in Fig.6b. The transfer characteristics of the devices, shown in Fig.6(b), yielded a subthreshold slope S of 72 mV/dec for *n*-FETs, and 65mV/dec for p-FETs. The maximum I_{on}/I_{off} ratio is in the order of 10^8 at V_{ds}=0.65V. The threshold voltages, extracted by linear extrapolation method from the transfer characteristics, are 0.22V for SOI *n*-FETs, and -0.8V for p-FETs. Further metal work function tuning is needed to obtain more suitable V_t values. The strained SOI *n*-FETs show a smaller V_t than SOI devices. The observed threshold voltage shift between the strained SOI and the SOI *n*-FETs of $\Delta V_t \approx$-190 mV, is mainly caused by a strain induced change of the electron affinity and the lower band gap energy of strained SOI [2,7]. The ΔV_t value is in a good agreement with the theoretical values of Ref.[7].

The mobility for both, holes and electrons were extracted using split C-V measurements, and are shown in Fig.7. For electrons the strained SOI shows a mobility enhancement factor of ~1.7 compared to SOI. The obtained electron and hole mobilities on SOI are similar to those reported for HfO_2 [6, 8, 9] and HfSiON [10] with a similar EOT. All the high-k devices showed lower mobilities than SiO_2 devices [11] most probably due to Coulomb scattering caused by trapped charges in the high-k itself. The mobility increases with the decreasing EOT as reported for HfO_2 [8].

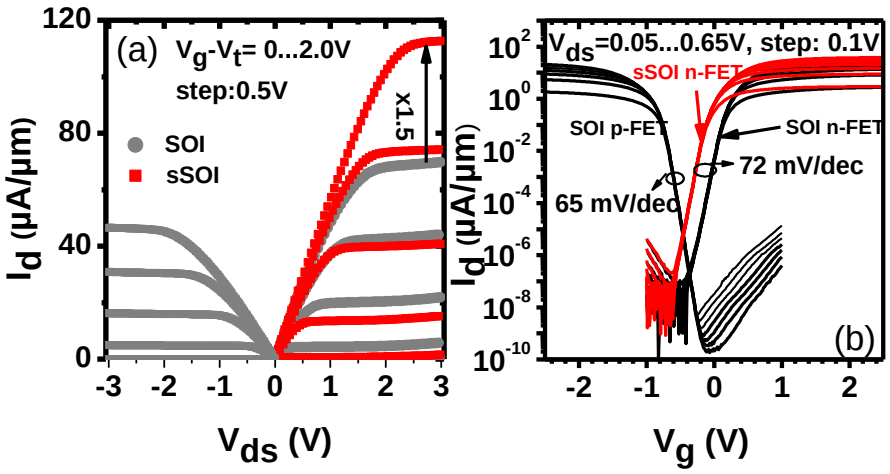

Fig. 6: Output (a) and transfer (b) characteristics of FD p-MOSFET on SOI and n-FETs on SOI and strained SOI substrates with 2 µm gate length and 23 µm gate width.

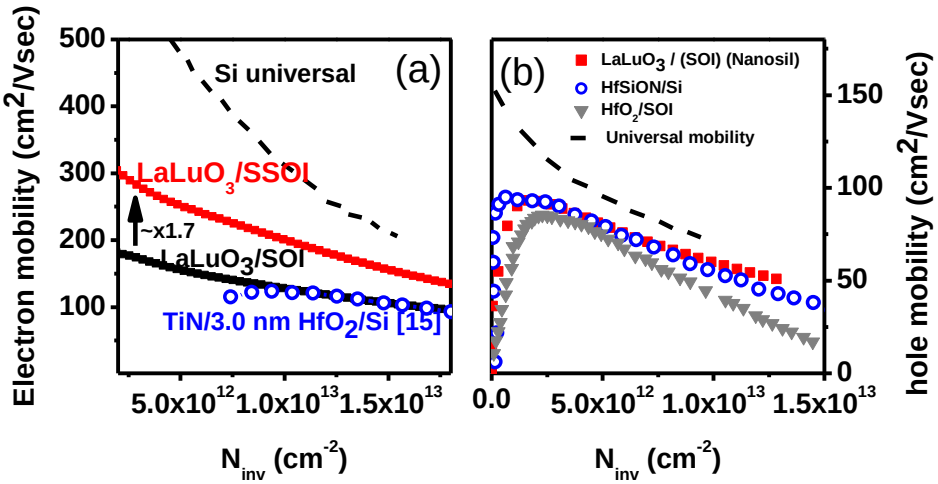

Fig. 7: Electron (a) and hole (b) mobilities measured for TiN/$LaLuO_3$/(s)SOI. $LaLuO_3$ on SOI shows similar mobilities compared with the reported mobilities for HfO_2 on Si.

3. Strained SiGe channels

In this section the fabrication and analysis of short and long and biaxial compressive strained SiGe quantum-well (QW) MOSFETs with high-k gate dielectrics is addressed. The goal is to assess the impact of channel orientation on the hole mobility and carrier velocity in such structures, as well as to evaluate the performance of SiGe strained channel/ high-k dielectric stacks. A thin body architecture is used to improve electrostatic control at short gate lengths. Also, the fabrication process was designed in order to avoid elastic strain relaxation of the channel.

Si/strained SiGe/SOI QW p-MOSFETs

Long and short channel MOSFETs were fabricated on 12 nm thick pseudomorphic $Si_{0.5}Ge_{0.5}$ layers epitaxial grown on 10 nm thin (100) SOI films. The biaxial compressive strain in the pseudomorphic $Si_{0.5}Ge_{0.5}$ layer corresponds to approx. -2.1%. The structure is capped with 3 nm Si, which confines the holes in the SiGe quantum well due to the valence band off-set between the strained SiGe and the Si top and bottom layers. If the Si cap layer is sufficiently thin the hole wavefunction is strictly confined to the SiGe layer even at high gate bias. Figure 8a displays the 1D SILVACO simulation of the band structure of the QW MOSFET, used in this work, at V_g=0, V_g=-1.0 and -1.5 V. At high gate voltage, a parasitic channel is formed in the Si cap.

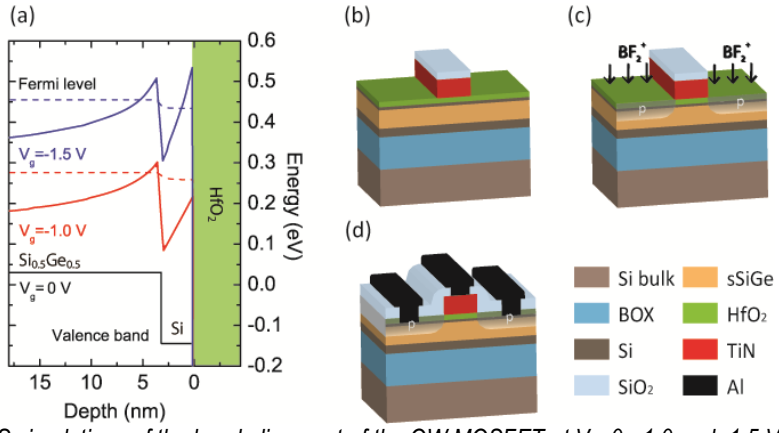

Fig. 8: (a) 1D SILVACO ATLAS simulations of the band alignment of the QW MOSFET at V_g=0, -1.0 and -1.5 V, and (c-d) Schematic of the gate first process used to fabricate Si/compressive SiGe/SOI MOSFETs with TiN/HfO_2 gate stack.

For the device fabrication a gate first process is used and is presented in Fig.8. Mesa structures with 10 μm width were patterned along the <110> and <100> directions. After standard RCA cleaning, a 4 nm amorphous HfO_2 film was deposited by atomic layer deposition followed by the deposition of 25 nm TiN metal layer. Subsequently, the gate was patterned with lengths ranging from L_g = 65 nm to 1.5 μm. S/D areas were formed by BF_2^+ implantation followed by 1 minute FGA. The FGA treatment contributes to the suppression of oxide charge in the high-k film and keeps the good quality high-k/Si interface as seen in the previous section. The S/D activation temperature conditions were adjusted in order to suppress the strain relaxation of the SiGe layer. Finally, a SiO_2 layer was deposited over the entire structure, followed by opening and deposition of S/D and gate contacts.

Characterization of short channel QW MOSFETs

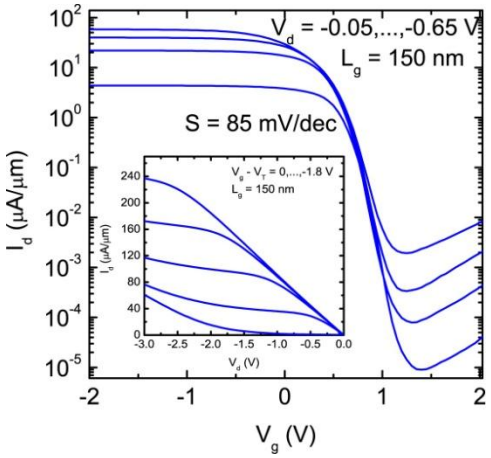

Figure 9: Transfer and output characteristics of 150 nm gate length QW MOSFET

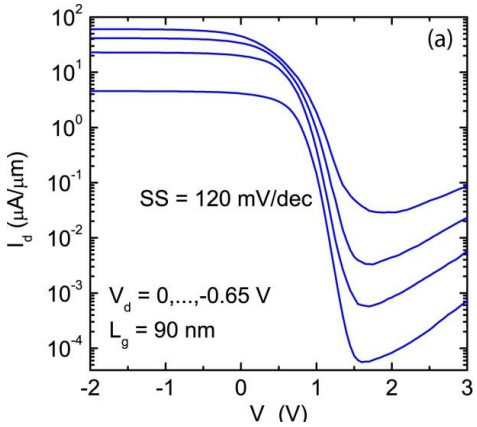

Figure 10: Transfer characteristics for a QW MOSFET with L_g=90 nm

Best transfer and output characteristics for a short channel SiGe QW MOSFETs with L_g=150 nm are shown in Fig.9. Down to this gate length, the transistors exhibit a relatively good electrostatic control, with small degradation of the subthreshold slope to 85 mV/dec. Also, the I_{off} increases of about one order of magnitude in comparison to long channel devices, resulting in a I_{on}/I_{off} ratio of 10^4. The output characteristic shows that the on-current does not saturate ideally due to the high S/D parasitic series resistance, and that punch-through occurs at high drain bias. Yet, high drain current values up to 240 µA/µm were measured.

The transfer characteristic of a SiGe QW MOSFET with 90 nm gate length is displayed in Fig. 10. The device presents a subthreshold slope of 120 mV/dev. Contrary to the long channel MOSFETs, the short channel devices are significantly affected by short channel effects (SCEs). The DIBL has a value of about 100mV/V and the threshold voltage shifts with the increase of the drain voltage.

Despite the electrostatic degradation, the short channel devices still allow to extract information about transport properties. As previously stated, the main goal of this study is to assess the impact of channel orientation on the performance and transport metrics of scaled QW MOSFETs. Since larger processing fluctuations are expected for shorter channel transistors, the variability of performance parameters for transistors with 65 nm gate length is evaluated by histograms (note shown). Figure 11 shows the subthreshold swing, threshold voltage, and DIBL as a function of the gate length for strained SiGe QW MOSFETs for <110> and <100> channel orientations. Reasonable electrostatic control is achieved for transistors with gate length down to 90 nm, below which DIBL increases from 100 mV/V to 350 mV/V for L_g=65 nm. Although the subthreshold swing dependence on gate length indicates slightly enhancement for transistors with <100> channel orientation, the electrostatic behavior is practically independent of transport direction. Small deviations are attributed to processing fluctuations.

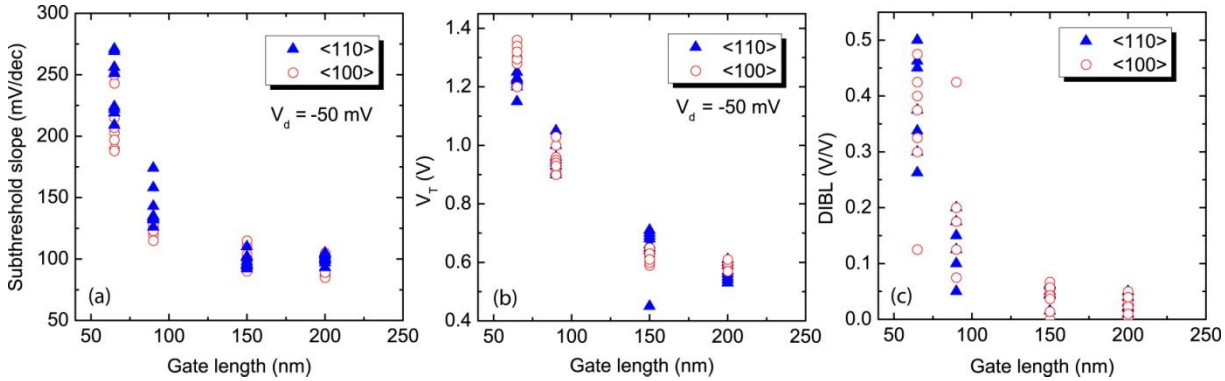

Figure 11: Comparison of subthreshold slope (a), V_t (b), and DIBL (c) vs. L_g for strained $Si_{0.5}Ge_{0.5}$ QW MOSFETs with<100> and <110> channel orientations.

Mobility evaluation

The effective hole mobility was extracted from long channel devices using split C-V method at small drain voltage (V_d=-0.02 V). Figure 12 presents the effective hole mobility extracted from strained SiGe QW MOSFETs for <110> and <100> channel orientation with average peak mobility of about 250 cm^2/Vs and 295 cm^2/Vs, respectively. At an inversion charge $6x10^{12}$ cm^{-2} the hole mobility is approximately 3 times higher than the universal Si hole mobility for the <100> crystal orientation. However, the mobility enhancement of 18% for the <100> transport direction translates to only 10% on-current improvement compared to <110> transport direction. It is in agreement with that reported by Shima *et al.* for SiGe layers with 20% Ge content [12].

Band structure simulations indicate that the HH valence band of SiGe under biaxial compressive strain is nearly symmetric near the top, at low energies, but is significantly warped at high energies. Thus, the effective mass in different transport orientations should impact mobility at high inversion charge regime [12, 13]. At the biaxial compressive strain level of -2.1% for the $Si_{0.5}Ge_{0.5}$/SOI structure used in this section, interband scattering is practically suppressed for both channel orientations. Therefore, it is suggested that the observed improvement in carrier mobility is mainly due to different effective masses in <110> and <100> transport directions.

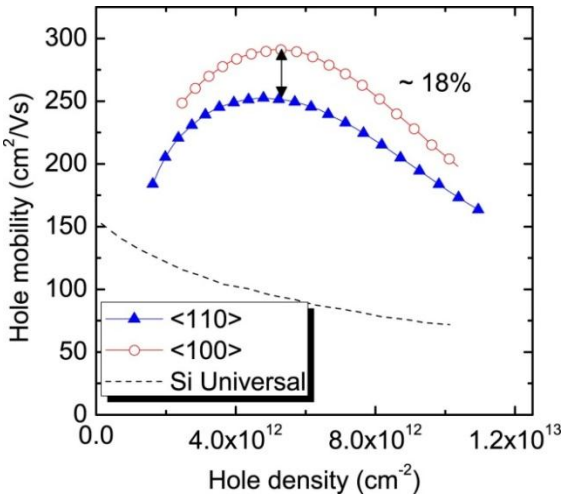

Figure 12: Effective hole mobilities measured for several QW MOSFET devices with channel oriented to <110> and <100>.

Strained Si/strained SiGe/SSOI QW p-MOSFETs

The device fabrication process is similar to that described in the past section, with exception of the starting substrate, and gate dielectric material/deposition method. Short and long channel MOSFETs were fabricated on 25 nm thin pseudomorphic $Si_{0.5}Ge_{0.5}$ layers epitaxial grown on SSOI substrates by RPCVD. The SSOI substrate consist of 12 nm thin strained Si layer and 145 nm buried oxide on lightly p-type doped Si(100). The starting SSOI material has a 0.8% tensile strain in the Si layers, while the biaxial compressive strain in the pseudomorphic $Si_{0.5}Ge_{0.5}$ layer amounts to -1.35%. HfO_2/TiN, $LaLuO_3$/TiN is used as gate stack.

Figure 13 illustrates the hole mobility as a function of inversion charge density for different gate dielectrics. As a comparison, the hole mobility of Si channel devices with different gate stacks are also shown. SiGe channel devices showed much higher hole mobility than Si channel devices. A hole mobility of about 200 $cm^2/V{\cdot}s$ was obtained for strong inversion conditions, which is about 2.5 times as high as Si universal hole mobility. We also see here that the mobility extracted from the QW transistor with $LaLuO_3$ is similar with the HfO_2 devices and equivalent EOT, and more interestingly, is comparable to the mobility for strained $Si/Si_{0.54}Ge_{0.46}$ channel devices with classic SiO_2 gate dielectric measured by Aberg *et al.* [14] and simulated by A.-T. Pham *et al.* [15]. The simulations are based on the self-consistent solution of the 6×6 **k·p** Schrödinger equation, the multi subband Boltzmann Transport Equation, and Poissons equation [16, 17]. This simulation method captures the influence of size quantization, strain, surface/channel orientations, and SiGe alloys on a solid physical basis. This suggests that the hole mobility is not as sensitive to the scattering effects at high-k/Si interface as electron mobility and no mobility degradation due to high-k integration is expected. In the simulations only a single layer of SiO_2 is considered instead of the high-k materials. Nevertheless, the simulation results predict quite well the measured mobility for inversion charges higher than $5x10^{12}cm^{-2}$. For smaller inversion charges the simulation results overestimate the experimental results. This is due to the fact that additional remote scattering mechanisms caused by high-k materials (HfO_2 and $LaLuO_3$) like remote Coulomb scattering, remote phonon scattering are neglected in the simulations. The mobility calculation results for strained SiGe QW PMOSFETs fabricated on (001) and (110) surface orientations with different gate oxide dielectrics are shown in Fig 14.

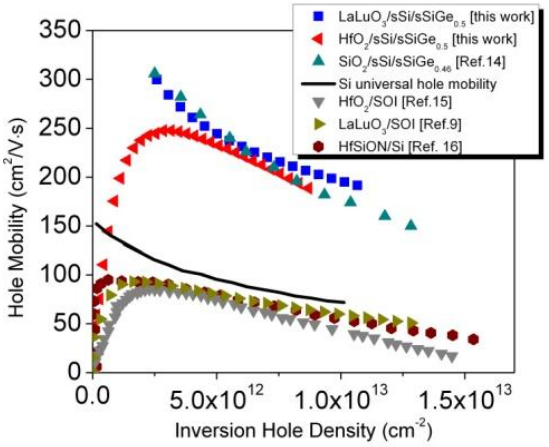

Figure 13: Hole mobility benchmarking: strained Si and strained SiGe channels with different high-k gate oxides.

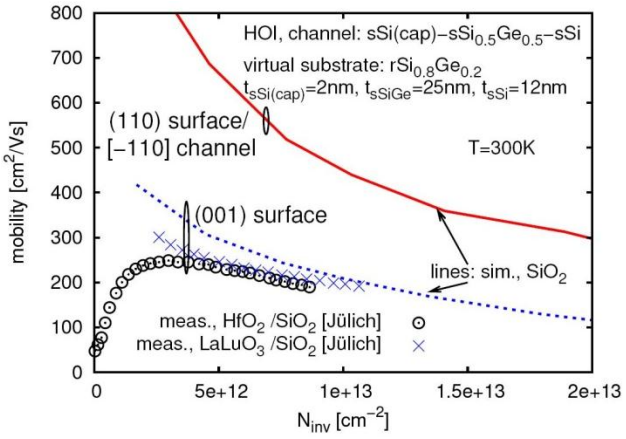

Figure 14: Mobility characteristics of strained SiGe HOI (001) and (110) PMOS with different gate oxide dielectrics.

4. Strained Ge Channel pMOSFETs

Epitaxial Growth Development of Strained Ge Channels

High quality biaxial compressively strained Ge channels suitable for high mobility pMOSFETs have been grown by reduced pressure chemical vapour deposition (RP-CVD) at Warwick [18]. The strained Ge channels were grown at low temperature on a reverse-graded $Si_{0.2}Ge_{0.8}$ strain relaxed buffer (SRB). The reverse-graded $Si_{0.2}Ge_{0.8}$ SRB was used due to its relatively low rms surface roughness (~ 2 nm) and threading dislocation density (TDD ~ 4×10^6 cm^{-2}) values. In addition, the reverse-graded SRB has a total thickness of just 2.1 μm, much thinner than that which can be achieved by conventional linear grading. All strained Ge layers were grown at temperatures below 450 °C using GeH_4 gaseous precursor. The critical thickness of the strained Ge layers was found to be strongly dependent on the growth temperature, and Warwick demonstrated fully strained Ge layers with thicknesses greater than 100 nm at a growth temperature of 400 °C. The growth of thick strained layers could be an advantage in the development of strained Ge on-insulator platforms by wafer bonding, which typically require a chemical mechanical polishing (CMP) step after bonding. Figure 15 shows a TEM image of an 80 nm fully strained Ge channel grown on a reverse-graded $Si_{0.2}Ge_{0.8}$ SRB. The layer was found to be defect-free, smooth and form an abrupt interface with the underlying buffer.

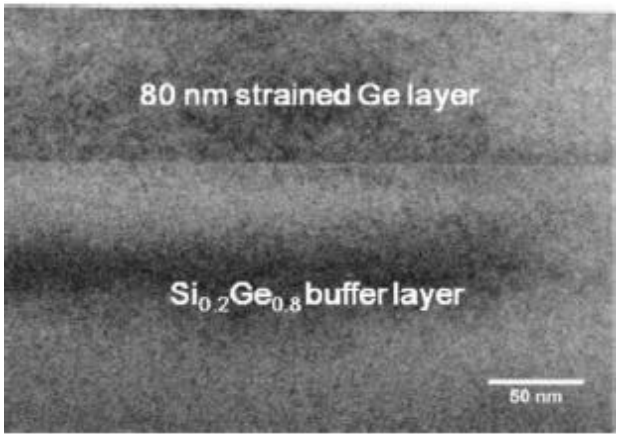

Figure 15. Cross-sectional TEM image of an 80 nm strained Ge layer grown on a reverse-graded $Si_{0.2}Ge_{0.8}$ SRB.

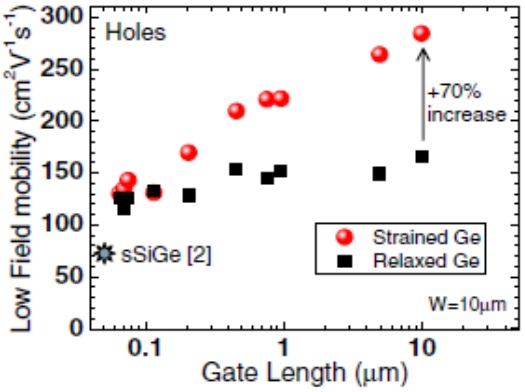

Figure 16. Low-field mobility of holes in strained and relaxed Ge pMOSFETs as a function of gate length.

Fabrication of Strained Ge Channel pMOSFETs at IMEC

Warwick supplied IMEC with strained Ge layers grown on a reverse-graded $Si_{0.2}Ge_{0.8}$ SRB for fabrication of pMOSFETs [19]. The strained Ge channels were grown with a range of thicknesses between 10 and 40 nm. The 500 nm capping layer of the SRB were grown with *in-situ* n-type doping using PH_3 to avoid the use of well implants that may cause undesired strain relaxation of the strained Ge channel. The strained Ge channel was passivated by growing a 6.5 monolayer (ML) epitaxial Si cap at low temperature (T < 500 °C). The gate stack consisted of 3.5 nm HfO_2/10 nm TaN/70 nm TiN. The combined gate stack resulted in an equivalent oxide thickness of 1.45 nm. Strained Ge pMOSFETs were fabricated with gate lengths ranging from 10 μm to 65 nm. The short channel transistors employed either As, P or no halo implants to control the short channel effects (SCEs). In the case where no halo implant was used the *in-situ* epitaxial doping of the SRB was increased. Relaxed Ge pMOSFETs were fabricated using an identical process flow as control devices on 1.5 μm-thick relaxed Ge epitaxial buffer layers deposited directly on Si (TDD ~ 2 x 10^7 cm^{-2}).

Electrical Chracterisation of Strained Ge pMOSFETs

Figure 16 shows the low-field mobility of hole in both strained and relaxed Ge pMOSFETs with As halo implants as a function of the transistor gate length. The strained Ge pMOSFETs showed an enhancement of around 70 % compared to relaxed Ge, with a peak hole mobility approaching 300 $cm^2V^{-1}s^{-1}$. However, this mobility enhancement is completely lost for gate lengths below 100 nm.

In order to investigate this phenomenon, different halo implant conditions were investigated. Figure 17 shows a high resolution TEM image of three different pMOSFETs with (i) P halo, (ii) As halo and (iii) no halo implants. The TEM images show that the As halo implant resulted in the formation of stacking faults/twinning defects in the strained Ge channel, whereas the P halo implants led to the formation of dislocations in the strained channel. No such defects were observed in pMOSFETs fabricated without halo implants, in which the SCEs were controlled by a higher epitaxial doping density in the SRB.

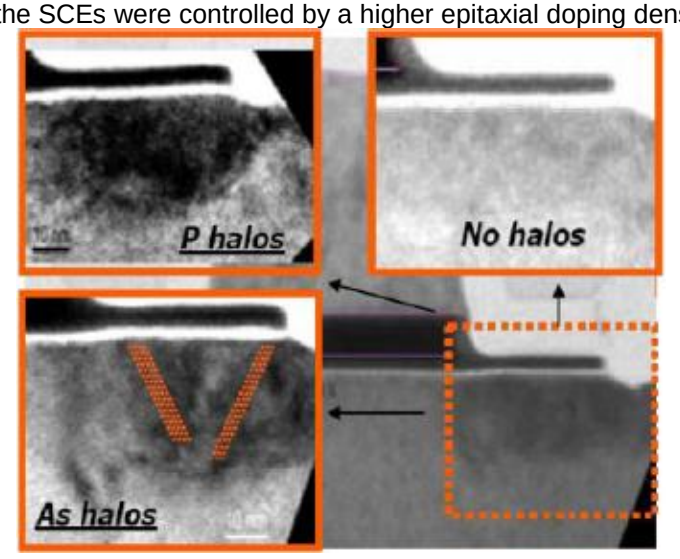

Figure 17 High-resolution TEM images of three strained Ge pMOSFETs with P, As and no halo implants.

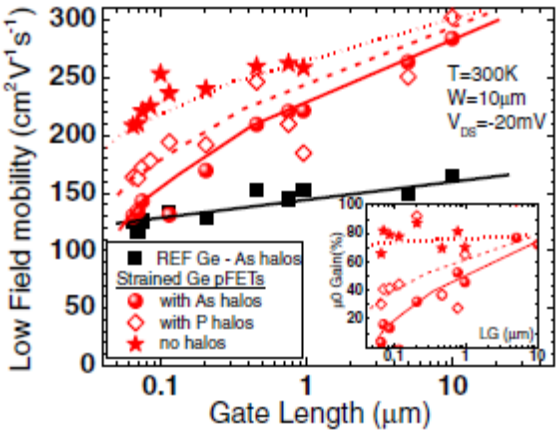

Figure 18. Low-field mobility of holes in strained and relaxed Ge pMOSFETs as a function of gate length showing the effects of different halo implants.

Figure 18 shows the effect of the three different halo implants on the low-field hole mobility. The impact of the halo implant is clearly evident and pMOSFETs with P and no halo implants showed mobility enhancements of around 40 % and 70 % over the relaxed Ge pMOSFETs for gate lengths below 100 nm.

The halo implants were also found to play a significant role in the low frequency noise of strained Ge pMOSFETs, where it was found that the defects responsible for the mobility degradation also resulted in higher low frequency noise. In general, the low frequency noise in strained Ge pMOSFETs was found to be lower than that in relaxed Ge pMOSFETs. This was attributed to the TDD value of the reverse-graded SRBs being around 1 decade lower than the relaxed Ge layer deposited directly on Si.

5. Simulation of hole-mobility in doped relaxed and strained Ge layers

Glasgow have employed full-band Monte Carlo to study hole transport properties in Ge [20]. We present mobility and velocity-field characteristics for different transport directions in p-doped relaxed and strained Ge layers. The simulations are based on a new method for over-coming the potentially large dynamic range of scattering rates, which results from the long-range nature of the unscreened Coulombic interaction. The model for ionized impurity scattering includes the effects of dynamic Lindhard screening, coupled with phase-shift and multi-ion corrections along with plasmon scattering (Fig 19). All these effects play a role in determining the hole carrier transport in doped Ge layers and cannot be neglected.

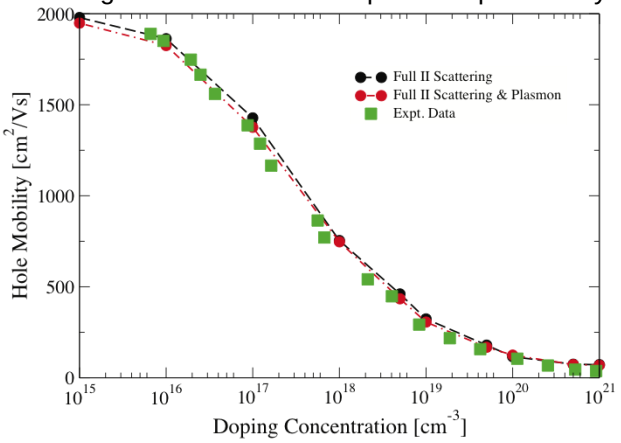

Figure 19: Mobility of majority holes in relaxed doped p-type Ge, employing our full model for ionized impurity scattering, with (black-dashed line) and without and (red-dashed line) plasmon scattering..

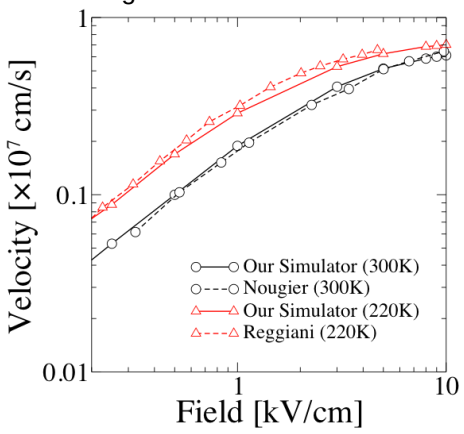

Figure 20: Simulated velocity-field characteristics at 220K and 300K in relaxed, bulk Ge including only acoustic and optical phonon scattering compared to experimental work from Reggiani at 220K [21] and Nougier at 300K [22]

It is known that hole mobility within Ge can be significantly enhanced due to biaxial strain from a relaxed $Si_{1-x}Ge_x$ buffer layer. In previous work [23] we investigated the hole mobility in undoped strained Ge layers for the three major substrate orientations: (001), (110) and (111), along with a variety of channel orientations, as shown in Fig. 21, comparing mobility for increasing levels of applied strain for each orientation. We argued that a general increase in mobility resulting from the application of strain came from the changes in the effective mass and increase in the splitting of the heavy and light hole bands; however, this does not determine why certain orientations (in terms of channel and substrate) are preferable over others. This though may be understood by examining in detail changes to the *E-k* relationship (*warping*) caused by the strain in different orientations. Thus while the increase in the mobility of holes in Ge due to the lifting of the degeneracy between the light and heavy hole bands can perhaps not be neglected, it is these subtle changes to the warping that is the dominant effect and is responsible for the significant differences in mobility for different orientations, similar to the situation in Si [24,25]. We have found that the best combination of channel and substrate orientation in terms of mobility is ⟨-110⟩ on a (110) substrate. Therefore this is the channel and substrate orientation we will investigate further here in terms of mobility transport in doped layers to determine whether this improvement is maintained at different doping concentrations.

Having calculated the strained bandstructure for Ge on different substrate orientations, we have employed the models described above and calculated the hole mobility as a function of doping in strained Ge layers as shown in Fig 22. From our simulations it is clear that the dramatic increase in mobility observed at low doping concentrations (ranging from a factor of 2 to over 4 for the highest strain level considered here (2.59%)) is significantly reduced at high doping concentrations (10^{19}cm^{-3} – 10^{20}cm^{-3}). The relative increase in mobility is reduced to no more than 50%, even for a strained Ge layer on a $Si_{0.6}Ge_{0.4}$ substrate. This reduction in mobility improvement will become more important as devices shrink as the degree of ballisticity will strongly depend on the backscattering coefficient determined mainly by the channel mobility which is greatly reduced with doping [26].

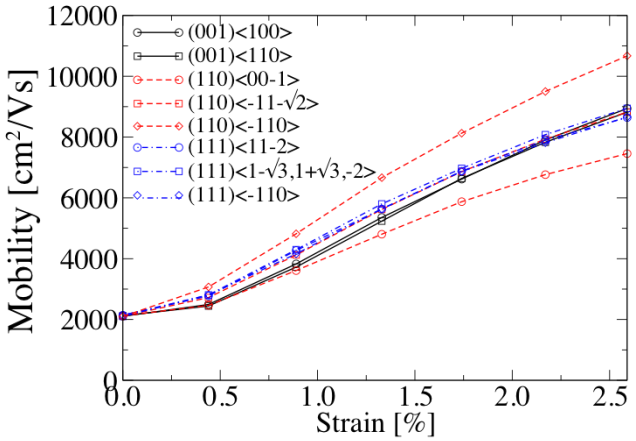

Figure 21: Variation of Ge hole mobility with strain for different substrate/channel orientations. The fraction of Si in the substrate varies from 0 (a Ge substrate) up to 0.6 in steps of 0.2. Fractions of Si above 0.6 are not considered, as the critical thickness of the Ge layer becomes impractical. The corresponding % strain is 0.89%, 1.74% and 2.59% respectively for a 0.2, 0.4 and 0.6 Si fraction in the relaxed Si1-xGex substrate.

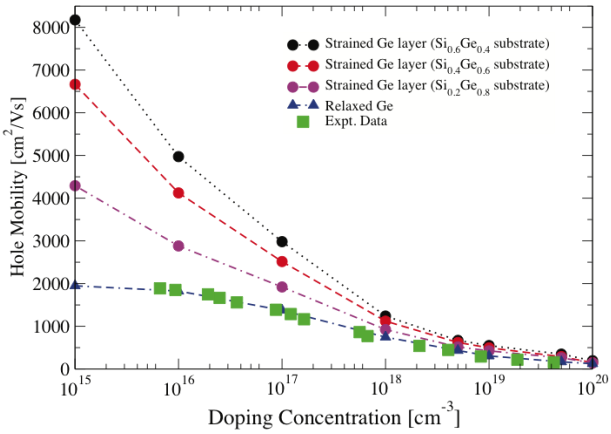

Figure 22 Mobility of majority holes in relaxed and strained p-type Ge, the strained layers are taken to be on (110) $Si_{1-x}Ge_x$ substrates with a <-110> channel orientation.

6. General conclusion and perspective

A full replacement gate process for long channel devices was developed which allows self-aligned gate-S/D fabrication. Table 1 summarizes the extracted D_{it} and the electron mobility extracted from long channel FD (S)SOI MOSFETs with $TbScO_3$, $LaScO_3$ and $LaLuO_3$ gate dielectrics with TiN metal gates. Large mobility enhancement for the strained silicon devices in the presence of higher- *k* dielectrics is proved. The improvement of 100% relative to SOI is as large as measured for HfO_2 transistors [2] despite of the different interface chemistry due to the silicate formation and the presence of the rare earth elements. It is also worth mentioning that the mobility enhancement maintains up to high electric fields (see Figs. 8b, 11). Compared to SiO_2/Si channel stack, all high-k/Si interfaces suffer from high D_{it} which degrades the carrier mobilities, primarily via Coulomb scattering. The achieved D_{it} values from the subthreshold slopes for both SOI and SSOI substrates are in the 10^{11} range, comparable to HfO_2. In summary, transistors with rare earth based dielectrics - although still at their infancy of development - show comparable mobilities as HfO_2 devices, while offering higher permittivity and thus potential for improved scaling.

Material	$TbScO_3$	$LaScO_3$	$LaLuO_3$	HfO_2
D_{it} $(eVcm^2)^{-1}$	~$5x10^{11}$	~$5x10^{11}$	$4.5x10^{11}$	~$5x10^{10}$
μ (cm^2/Vs) (SOI / SSOI)	181 / 350	180 / 375	188 / 385	178 / -

Table I: Extracted D_{it} and hole and electron mobility data from FD (S)SOI MOSFETs with $TbScO_3$,$LaScO_3$ and $LaLuO_3$ gate oxides.

High mobility short channel p-MOSFETs with compressively strained $Si_{0.5}Ge_{0.5}$/(S)SOI channel and TiN/HfO_2 or TiN/$GdScO_3$ gate stacks are demonstrated. The employment of a thin Si cap conserved the excellent high-k/Si interface with low D_{it} and small hysteresis. The channel/gate structure is thermally stable regarding the compressive strain in the SiGe layer and, for $LaLuO_3$, the amorphous phase maintains allowing the device fabrication using a gate first process. Hole mobilities as high as 260 cm^2/Vs were achieved for such devices. The successful demonstration of 100 nm p-MOSFETs suggests that ternary rare earth oxides on strained SiGe devices have high potential for implementation in scaled devices. Optimization of the quantum well devices by scaling the EOT and implementation of the silicide S/D contacts should further improve the QW MOSFET performance. Good agreement was achieved between experimental results on high-k materials and simulation by using SiO_2 gate oxides. This suggests that the hole mobility is not as sensitive to the scattering effects at high-k/Si interface as electron mobility and no relevant mobility degradation due to high-k integration is expected.

Strained Ge channel p-MOSFETs have been fabricated with high-k gates using a fairly standard Si process flow. It was shown that the mobility in long strained channels was enhanced by 70% over similarly fabricated relaxed channel devices, but this enhancement largely disappears at short gate lengths. Further modification of the process flow, and in particular in the gate metal thickness and level of doping at the channel extensions, demonstrated that the mobility could be largely recovered in the short channel devices.

We have developed a method for including inelastic acoustic phonon scattering in Monte Carlo transport simulations, and have been able to demonstrate good agreement for undoped Ge over a wide range of electric fields relevant to contemporary CMOS applications. A number of different factors, such as Lindhard momentum-dependent and multi-ion screening, have to be taken into account in order to accurately model

the carrier transport in highly doped materials commonly employed in the channel and in the source/drain regions of modern MOSFETs. The hole transport in doped strained layers has also been investigatedand shows that the significant improvement in mobility (~×4) observed in undoped materials is reduced by more than a factor of 8 at high doping concentrations. This will have a significant impact on the potential improvement in performance that can be obtained in aggressively scaled CMOS transistors with Ge channels. It also points to the need for electrostatic control in an architecture that does not require heavy doping.

7. References

[1] E. H. Nicollian and J. R. Brews, "MOS (Metal Oxide Semiconductor) Physics and Technology," Wiley interscience publication, New York, 1982, pp. 325-328 (1982).

[2] S.F. Feste, Th. Schäpers, D. Buca, Q. T. Zhao, J. Knoch, M. Bouhassoune, Arno Schindlmayr, and S. Mantl, "Measurement of effective electron mass in biaxial tensile strained silicon on insulator," Appl. Phys. Lett. 95, pp. 182101-3, November 2009.

[3] J.-S. Lim, S. E. Thompson, J. G. Fossum, "Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs," IEEE Electron Dev. Lett. 25, pp.731-733, Nov. 2004.

[4] E. Durğun Özben, J. M. J. Lopes, A. Nichau, M. Schnee, S. Lenk, A. Besmehn, K. K. Bourdelle, Q.T. Zhao, J. Schubert and S. Mantl, "Integration of LaLuO3 (κ ~30) as High-κ Dielectric on Strained and Unstrained SOI MOSFETs with a Replacement Gate Process", IEEE Electro. Device Lett. 32, pp.15-17, 2010.

[5] K. Romanjek, F. Andrieu, T. Ernst, G. Ghibaudo, "Characterization of the effective mobility by split C(V) technique in sub 0.1 lm Si and SiGe PMOSFETs," Solid-State Electron. vol. 49, pp. 721-726, August 2005

[6] O. Bonno, S. Barraud, F. Andrieu, D. Mariolle, F. Rochette, M. Cassé, J. M. Hartmann, F. Bertin, and O. Faynot, "High-field electron mobility in Biaxially-tensile strained SOI: Low temperature measurement and correlation with the surface morphology" Symp. On VLSI Tech. pp.134-135, 2007.

[7] J.-S. Lim, S. E. Thompson, J. G. Fossum, "Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs," IEEE Electron Dev. Lett. 25, pp.731-733, Nov. 2004.

[8] P. D. Kirsch, M. Quevedo-Lopez, S. A. Krishnan, S. C. Song, R. Choi, P. Majhi, Y. Senzaki, G. Bersuker, and B. H. Lee, "Atomic layer deposited HfO_2 and HfSiO to enable CMOS gate dielectric scaling mobility, and V_{TH} stability," ECS Transactions, Vol 1, No.10, pp.15-28, 2006.

[9] V. Barral, T. Poiroux, F. Andrieu, C. Buj-Dufournet, O. Faynot, T. Ernst T, "Strained FDSOI CMOS technology scalability down to 2.5nm film thickness and 18nm gate length with a TiN/HfO2 gate stack," 2007 IEEE Int. Conf. Communication, 61, (2007).

[10] L. Trojman, L. Pantisano, S. Severi, E. San Andres, T. Hoffman, I. Ferain, S. De Gendt, M. Heyns, H. Maes, G. Groeseneken, "Performance assessment of (110) p-FET high-κ/MG: is it mobility or series resistance limited?," Microelectron. Eng. vol. 84, pp. 2058–2062, 2007.

[11] F. Andrieu, T. Ernst, O. Faynot, Y. Bogumilowicz, J.-M. Hartmann, J. Eymery, D. Lafond,Y.-M. Levaillant, C. Dupré, R. Powers, F. Fournel, C. Fenouillet-Beranger, A. Vandooren, B. Ghyselen, C. Mazure, N. Kernevez, G. Ghibaudo, S. Deleonibus "Co-integrated dual strained channels on fully depleted sSDOI CMOSFETs with HfO_2/TiN gate stack down to 15 nm gate length," IEEE international SOI conference, December 2005.

[12] M. Shima, "<100> strained-SiGe-channel p-MOSFET with enhanced hole mobility and lower parasitic resistance", FUJITSU Sci. Tech, vol. 39(1), p. 78, (2003).

[13] L. Gomez, P. Hashemi, and J.L. Hoyt, "Enhanced Hole Transport in Short-Channel Strained-SiGe p-MOSFETs", IEEE Trans. Elect. Dev., vol.56 (11), p. 2644, 2009.

[14] Åberg, C.N. Chléirigh, and J. L. Hoyt, IEEE Trans. Electron Devices 53, 1021 (2006).

[15] T. Pham, C. Jungemann, and B. Meinerzhagen, 2010 ESSDERC, 230, (2010)

[16] T. Pham, C. Jungemann, and B. Meinerzhagen, IEDM Tech. Dig., 2008.

[17] T. Pham, C. Jungemann, and B. Meinerzhagen, J. Compu. Electr., vol. 8, pp. 242–266, 2009.

[18] M. Myronov A. Dobbie, V.A. Shah, Xue-Chao Liu, Van H. Nguyen and D. R. Leadley; "High quality strained Ge epilayers on a $Si_{0.2}Ge_{0.8}$/Ge/Si(100) global strain-tuning platform grown by reduced pressure chemical vapour deposition", Electrochemical and Solid-State Letters 13, H388-H390 (2010)

[19] J. Mitard,et al, "High hole mobility in 65nm strained Ge-pFETs with HfO2 gate dielectric"; Jap. J. Appl. Phys. (2011)

[20] J. R. Watling, C. Riddet, K. H. Chan and A. Asenov, "Simulation of hole-mobility in doped relaxed and strained Ge layers," *Journal of Applied Physics*, Vol. 108, p. 093715, 2010.

[21] L. Reggiani, C. Canali, F. Nava, and G. Ottaviani, "Hole drift velocity in germanium," Physical Review B, 16, 2781 (1977)

[22] J. P. Nougier & M. Rolland, "Mobility, Noise Temperature, and Diffusivity of Hot Holes in Ge," Phys Rev B, 8, 5728 (1973)

[23] C. Riddet, J. R. Watling, Kah. H. Chan and A. Asenov, "Monte Carlo simulation study of the impact of strain and substrate orientation on hole mobility in Germanium", J Phys: Conf Series, 242, 012017, (2010)

[24] J. M. Hinckley and J. Singh, 'Hole transport theory in pseudomorphic Si1-xGex alloys grown on Si(001) substrates', Phys Rev B, 41, 2912 (1990)

[25] M. V. Fischetti and S. E. Laux, 'Bandstructure, deformation potentials, and carrier mobility in strained Si, Ge and SiGe alloys', J. Appl. Phys. 80, 2234 (1996)

[26] M. Lundstrom and Z. Ren, 'Essential Physics of Carrier Transport in Nanoscale MOSFETs', IEEE TED, 49, 133 (2002).