NANOSIL

Silicon-based nanostructures and nanodevices for long term nanoelectronics applications

Network of Excellence

WP 5 “Integration and spreading of excellence”

Deliverable 5.1 “Annual review of integrating and spreading of excellence activities.”

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TABLE OF CONTENTS

Deliverable Summary 4
1. Integration 5
1.1. Coordination by WPs (FPs) leaders 5
1.2. Common PhD students 8
1.3. “Who is Who guide” and “open questions” list 8
1.4. Interaction with industrial partners 9
2. Collaboration with other European and national projects 9
3. Exchanges 10
4. Spreading of excellence 11
4.1. Support of International Schools/Workshops 11
4.2. Organization of seminars/courses/whorkshops/tutorials 11
4.3. University courses. 14
4.4. Nanosil experienced lecturers 14
4.5. Best practice training for technicians 14
5. Dissemination of knowledge 14
5.1. Inside of NoE 14
5.2. Beyond NoE 14
References 15
Appendix 1. 30
Summary on the “screening of national projects of relevance” (as at the beginning of 2008). 30

Deliverable Summary

This deliverable summarizes the integration/dissemination/spreading activities within NoE Nanosil performed during 2008.

Integration activities is addressed through the number of joint processing, joint characterization and modeling activities organized within each FP(s), WP(s) as well as cross-FP (WP) activities. Furthermore, the number of FP (WP) as well as cross FP (WP) meetings is chosen as a measure of integration activities. Common PhD students (12 in 2008) reinforced the integration between partners (particularly with industrial partners). “Who is Who Guide” was placed on the web-site to inform partners about specific competences available within Nanosil community. Regularly updated “open questions/technical problems” encouraged the exchange of ideas/knowledge. Exchanges of personnel (12 weeks in total during 2008) further strengthened the expertise exchange and complementarity between partners.

Additionally to the integration within Nanosil, the cooperation with another EU and national projects was stimulated. Screening of the national projects of relevance was performed at the first 6 months of Nanosil and then the most interesting projects have been selected by E&SC for the joint Workshop scheduled for January 2009. Number of EU and national projects launched by Nanosil members in 2008 demonstrates a high activity level of the network.

Spreading of excellence within and beyond Nanosil is addressed through the support and organization of workshops/schools/trainings, which were available for a wide scientific community.

Dissemination of knowledge was additionally implemented through the Nanosil-website, issued poster, presentations given by Nanosil partner at different international scientific events, as well publications in high-level international journals listed in the deliverable.

1. Integration

1.1. Coordination by WPs (FPs) leaders

Integration within Nanosil is carried out by WPs and FPs leaders through the coordinated programming of the partners' activities. 4 Work Packages (WPs) are defined within Nanosil. WP1 and WP2 are then subdivided to 3 and 4 Flagship projects (FPs), respectively. Additionally, these WPs are completed by Visionary projects (VP) in order to reinforce/stimulate the exchange of new ideas / provoke the disputes /exchange of opinions between partners.

38 joint processing (JP), characterization (JC) and modeling (JM) activities have been performed by Nanosil partners during 2008, among which 13 are cross-activities between different WPs (FPs).

#	Subject/Topic	Partners involved	Measurable progress (if identifiable)	Industrial contact
		FP1.1 – Strain materials		
1.	**JP:** Patterned strained SOI samples for strain relaxation studies	FZJ, UNEW	**4 structures**	C. Clayes (IMEC)
		FP1.2 – Schottky barriers		
2.	**JP**: Full demonstration of the segregation technique using 3 different flavors of dopant segregation: Implantation Before Silicidation (IBS), Implantation To Metal (ITM), Implantation To Silicide (ITS)	FZJ, KTH, ISEN-IEMN, UCL	4 types of silicides have been implemented NiSi, PtSi, $ErSi_{1.7}$, $YbSi_{1.8}$ – 4 types of dopants: As, Ph, B, In.	M. Goldbach (Qimonda)
3.	**JC**: benchmarking of Schottky barrier measurement	FZJ, KTH, ISEN-IEMN, UCL	3 measurement strategies compared	M. Goldbach
4.	**JP**: Joint processing of rare earth silicides	IEMN-ISEN, UCL	18 x 75 mm wafers	M. Goldbach
5.	**JP**: Processing of strained SOI layer	FZJ to provide to IEMN, KTH	4 wafers	M. Goldbach
6.	**JP**: Development of a local strain platform	USTUTT to provide to IEMN, KTH	In development	M. Goldbach
		FP1.3 – Gate stacks		
7.	**JC:** $LaLuO_3$-samples for MOS-CAP-Characterization	FZJ, Liverpool, Tyndall, WUT, Chalmers, AMO	2 samples send to each partner	S. Deleonibus (CEA-LETI)
		FP2.1 – Nanowires (NW)		
8.	**JP-JC**: NWs with W < 15 nm delivered to RWTH for low temperature characterization.	AMO, RWTH		T. Skotnicki (STM)
9.	**JC**: Investigation of carrier transport in NWs (incl. personnel exchange AMO/RWTH)	AMO, Chalmers, RWTH		T. Skotnicki
10.	**JP**: Thinning SOI wafers for the fabrication of very thin Schottky barrier MOSFETs	UCL, IEMN-ISEN	10 wafers processed	T. Skotnicki
11.	**JP**: suspended nanowires (e-beam lithography, dry etching, nanowires release with CPD, conformal gate deposition etc.) (incl. personnel exchange)	IEMN-ISEN, UCL	4 wafers processed	T. Skotnicki
12.	**JC**: Quantum dots embedded in Schottky diodes for DLTS characterization	Chalmers, ITE, USTUTT		T. Skotnicki
13.	**JP**: Si/ SiGe / Si heterostructure	USTUTT, UCL	1 wafer processed	T. Skotnicki
14.	**JC:** Investigation of current transport mechanisms in silicon nanowires in the 10 K temperature range. (incl.	Chalmers, AMO, RWTH		T. Skotnicki

	personnel exchange)			
15.	**JP**: fabrication of NW devices having various geometries (length, width). (incl. personnel exchange)	EPFL, UNEW	Numerous	T. Skotnicki
	FP2.2 – Carbon electronics			
16.	Information Exchange about "European activities in Carbon Electronics"	IUNET, ISEN-IEMN, UPS, AMO, WUT, URV/UGR	Deliverable D2.1	M. Goldbach
17.	Information Exchange about "comparison of carbon nanotube and graphene-based devices"	IUNET, AMO	Deliverable D2.12	M. Goldbach
	FP2.3 – Small-slope switches			
18.	**JP**: Study of oxidation conditions for induced tensile strain	EPFL, UNEW	4 wafers processed for strain investigation due to oxidation: 2 wafers: 850°C, after 1st oxidation and stripping 2 wafers: 1050°C, after 2nd oxidation and stripping	T. Skotnicki
	FP2.4 – Template self-organization			
19.	**JP**: Nanopatterned oxidized Si wafers (4-inch) and Ge dot growth	IMEL-NCSR, USTUTT	2 4-inch wafers patterned	T. Skotnicki
20.	**JP-JC**: Growth of Quantum dots embedded in Schottky diodes and DLTS characterization of the dots	USTUTT, Chalmers/ITE	3 4-inch wafers grown Schottky Diodes Processed First measurement results	T. Skotnicki
21.	**JP**: Fabrication of Single Electron memory with self aligned Process	USTUTT, UCL	5 3-inch wafers have been grown with Si / SiGe / Si heterostructure	T. Skotnicki
22.	**JC**: Development of Characterization method for QDs	Chalmers/ITE	Theory developed	T. Skotnicki
	WP3 – JOINT FABRICATION			
23.	**JP**: Bulk-Si devices with integration of $LaLuO_3$/TiN and dopant segregated SB-contacts	FZJ, AMO, KTH, IUNET	40 % of processing completed 8 wafers	
24.	**JP**: Fully Depleted SOI devices with integration of $LaLuO_3$/TiN and dopant segregated SB-contacts	FZJ, AMO, KTH, IUNET	40 % of processing completed 7 wafers	
25.	**JP**: Mobility test structures with Gd silicate dielectric and TiN gate	AMO, IUNET	3 samples processed	
26.	**JP**: MOSFETs on (110) substrates and in <110> channel direction for evaluation of uniaxial strain impact	Warwick, KTH, IUNET	One wafer processed	
27.	**JP**: Nanowire fabrication	EPFL, RWTH, UCL, AMO, KTH	6 wafers + one sample	
28.	**JP**: Development of low temperature DS SB-contacts	IEMN-ISEN, KTH	15 wafers in 3 batches completed	
	WP4 – JOINT CHARACTERIZATION			
29.	**JM**: Modeling of quasi-ballistic transport in decananometric devices and in Shottky contacts	IU.NET- IMEP	Development of boundary condition for SB contacts in the quasi-ballistic model	
30.	**JM**: Definition of template devices for benchmarking of device simulators.	IUNET, SNPS, Qimonda	Deliverable D4.1 released	Qimonda, STM
31.	**JC**: Experimental characterization of effective mobility in transistors with high-k dielectrics and corresponding physically based simulations	IUNET, SNPS, WUT, UCL, AMO, TYNDALL-UCC	Deliverable D4.2 released	STM

Joint cross-WP activities (notice, that all WP3 activities are jointas well)

#	Subject/Topic	WPs involved	Partners involved	Measurable indicators (if identifiable)
1.	**JP:** Integration of metallic junction on top-down nanowires arrays	FP1.2 & FP2.1	IEMN, UCL	12
2.	**JP**: NW samples shipped between EPFL and UNEW after partial/full device fabrication in order to assess strain build-up in NW (at UNEW) at various stages of processing (incl. personnel exchange)	FP1.1, FP2.1	UNEW, EPFL	
3.	**JP**: Design and fabrication of SOI base wafers for the comparison of the electronic properties of top down and bottom up Si nanowires.	FP2.1 & FP2.4	CEA, INPG-FMNT, UCL	
4.	**JP**: Fabrication of highly dense silicon nanowire array	FP2.1 & FP2.4	UCL, CEA-LETI	Exchange of wafers between UCL and CEA-LETI to build Si nanowires combining bottom-up and top-down approaches
5.	**JC**: Definition of template nanowire-MOSFETs	WP4, WP2	IUNET, AMO	Device structures defined in deliverable D4.1
6.	**JC**: influence on mechanical strain on high-k MOS interface states (incl. personnel exchange)	WP1, WP2	UCL, Chalmers	
7.	**JM:** Modeling of Schottky barrier MOSFETs	WP4&FP1.2	IEMN, IUNET, IMEP	Identification of the main modeling aspect to be addressed within WP4

18 meetings between partners were organized in order to stimulate the joint activities and discuss the obtained results, among which 2 cross WP (FP) meetings.

Date	Place	Topic	Participants (not names, but institutions/partners)	Number of persons present *
FP1.2 – Schottky barriers				
12 Mar 08	Udine	WP1 Meeting	All WP1 participants	
10 Jun 08	Lille	FSP1.2 Schottky Meeting	ISEN-IEMN, Warwick, KTH, FZJ, UCL	**10**
18 Sep 08	Edinburgh	WP1 Meeting	ISEN-IEMN, Warwick, KTH, FZJ, IUNET, ...	**12** ?
VP1.4 – More Moore Forum				
6 Sept 2008	Bertinoro After the III Sinano Summer school	Low Field Transport in Advanced MOSFETs	INPG IMEP, TUBS, IU.NET, ST, IEF, LETI, AMO, WUT	**17 all nanosil partners**
19 Sept 2008	Edimburgh After ESSDERC 2008	Cmos variability research in europe: from atomic scale to circuits and systems	Glasgow, LETI, IU.NET, ST, IMEC	*90 participants,* **34 nanosil partners**
FP2.1 – Nanowires (NW)				
March 08	IEMN	Etching of Si nanowires from a SOI wafer	IEMN-ISEN, UCL	**8**
June'08	IEMN	Establishment of a process flow for the fabrication of Si nanowires	IEMN-ISEN, UCL	**5**
Nov.'08	UCL	PhD thesis confirmation of Mr. Vikram Passi & Characterization of Si nanowires under mechanical stress	IEMN-ISEN, UCL	**7**
Jan 2008	Aachen	Kick-off meeting of WP2	All WP2 partners	**25**
FP2.3 – Small-slope switches				
July 2008	EPFL	Measurement of strain in nanowires	EPFL/UNEW	**4**

Sept. 2008	UNEW	Raman measurements	UNEW/EPFL	**3**
FP2.4 – Templated self-organization				
29 Jan. 2008	Grenoble	FP 2.4 kick-off meeting	CEA, Chalmers, IMEL-ISEN, INPG-FMNT, ITE UCL, UPS, USTUTT	**10**
03-04 Nov. 2008	Stuttgart	Templated Self-Organization Annual meeting 2008	CEA, Chalmers, IMEL, INPG, ITE, RWTH, TYNDALL, UCL, UPS USTUTT	**15**
VP2.5 – Beyond CMOS vision				
19 Sept. 2008	Edinburgh, UK	Brain-inspired Electronic Systems	LIVUNI, CHALMERS, UCL	**5 /** *34*
WP4 – JOINT CHARACTERIZATION				
12 March, 2008	Udine	Kick-off of activities	UG, Tyndall, SNPS, Quimonda, IUNET, IMEP, URV-UGR	**20**
16 Sept., 2008	Edinburgh	Monitoring of activities. Status of Deliverables. Interactions with other WP's.	IUNET, WUT, UG, ETH, TUBS, SNPS, Tyndall, IMEP, UNEW, IMEP, URV-UGR, Warwick	**24**

Cross-meetings

Date	Place	Topic	WPs	Participants	Number of persons present *
18 Sep 2008	Edinburgh	WP1 + WP4 Meeting	WP1/WP4		**12**
03 Nov. 2008	Stuttgart	Define common objectives for the fabrication and characterization of highly dense Si nanowires array.	FP2.1 & FP2.4	AMO, EPFL, INPG-FMNT, UCL, USTUTT	**10**

** in **bold** the ones inside NANOSIL, in Italic - outside NANOSIL)*

1.2. Common PhD students

NoE integration is reinforced by the common/joint PhD students between different partners. For the moment there are **12 common PhD students**.

Nanosil partner 1	Nanosil partner 2	Topic	WP(s)
INPG-IMEP	CEA-LETI	Innovative SOI substrates (Q.T. Nguyen)	WP1
INPG-IMEP	CEA-LETI	Advanced GeOI Materials and devices (W. Van den Daele)	WP1
INPG-IMEP	STM	Characterization and simulation of advanced SOI fully depleted MOSFETs (L. Pham Nguyen)	WP4
INPG-IMEP	CEA-LETI	Characterization and analysis of the influence of mechanical strain on electron transport in advanced MOS devices (F. Rochette)	WP4
INPG-IMEP	CEA-LETI	Experimental study of the influence of the gate stack on electron transport (L. Thévenod)	WP4
INPG-IMEP	IUNET	Monte-Carlo study of Silicon-On-Insulator Multiple-Gate MOS structures including band-gap engineering and self-heating effects (M. Braccioli)	WP4
INPG-IMEP	IMEL	Fabrication of slow wave propagation guide. Post-doc D. Kaddour supported by FAST (see collab. with other projects)	WP4
INPG-IMEP	URV-UGR	Characterization and simulation of SOI devices (N. Rodriguez)	WP4
INPG-IMEP	IUNET	Modeling of nano nMOSFETs with alternative channel materials in the fully and quasi ballistic regimes (Q. Rafhay)	WP4
UCL	IMEN-ISEN	Transport in nanowires under strain (V. Passi)	WP1, WP2
UPS	STM	Modelling of stress effect in CMOS devices for sub-65 nm node	WP4
UGR	INPG	Characterization, Modeling and Simulation of Decananometer SOI MOSFETs	WP4

1.3. "Who is Who guide" and "open questions" list

Who is Who guide is completed and available through the Nanosil web-site. Interactive information is introduced in the "partners list". Moreover, the search by "competence" is available.

Additionally, we encouraged partners to provide us information about "**technical problems** they encounter **and open questions** they imagine". Then, this information was discussed during E&S Committee meetings as well as put on the Nanosil web-site for the access of all Nanosil partners. It is planned to update this information regularly (twice per year).

1.4. Interaction with industrial partners

Interaction with industrial partners aims at roadmapping, assessing the results and assure theirs transferability to industry. With this regards, each FPs of Nanosil has industrial contact person or "**industrial monitor**". Additionally, common industry/academia **PhD students** (six for the moment) and common **projects** (about 15 nowadays) reinforce this exchange of knowledge. Furthermore, industrial partners are invited to participate in Executive & Scientific Committee Meetings to develop a general strategy of network progressing/developing.

2. Collaboration with other European and national projects

Good links are established between Nanosil and ongoing **FP6** (Pullnano, Metamos) and **FP7** (EuroSOI+, ANNA, …) **projects**.

Screening of **national projects** of relevance has been performed by the participants from each country. In total 61 national projects are mentioned in a complete list (see Appendix 1 for details). The repartition between countries is as follows: 17 in UK, 4 in Ireland, 1 in Switzerland, 8 in Spain, 7 in Germany, 16 in France, 1 in Sweden, 3 in Belgium, 1 in Greece and 3 in Poland. E&S Committee members have selected 11 among them to participate in a common **Workshop Nanosil/National projects** which will be held on January 30th 2009 in Grenoble.

Additionally, it is worth to mention that **13 new projects** have been launched during 2008 by members of Nanosil, among which 4 EU projects within FP7, one binational French-Spanish project and 8 national projects. Naturally, strong collaboration between Nanosil and these new projects is foreseen.

Nanosil partners	Other Partners	Title of the project	National/ European/ International	Funding source	Status
GU IMEC, LETI, ST Microelectronics	IBM, Democritos	DUALLOGIC: Dual-channel CMOS for sub-22 nm high performance logic	European	FP7	Accepted
GU, IMEC, ST	ARM, UNIBO, KUL	REALITY: Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies	European	FP7	accepted
URV, UCL, EPFL	UniK, TUC, ULP, TU-Ilmenau, ITE, Infineon Technologies, AMS, RFMD Ltd, AdMOS GmbH, DOLPHIN Integration SA, Melexis Inc, AIM-Software	COMON (Compact Modelling Network)	European	FP7, People Program, Industry-Academia Partnership & Pathway	Started
EPFL, LETI-CEA		NEMS-IC	STREP, European	FP7	started
URV	Université de	Characterization and	Binational	Spanish/	Started

	Montpellier 2	modeling of nanoscale Ultrathin Body (UTB) SOI MOSFETs valid for DC y RF analysis		French Ministries of Science, Spanish-French Integrated Action	
Grenoble INP, CEA,	CNRS	Quantamonde: QUANTum and Atomistic MOdeling of NanoDEvices	National	French ANR	Started
Grenoble INP, CEA	CEA-INAC, CNRS-GHMFL, CNRS-INeel	Dispograph: Graphene, from material to test devices	National	French RTRA	Accepted
RWTH	HZB-Berlin, BTU-Cottbus, FSU-Jena, IEF5-Jülich, IZM-Halle ER-C Jülich	Silicon based thin film materials for next generation solar cells (SINOVA)	National	BMBF	accepted
KTH		Dopant segregated contacts to nanowire MOSFETs – Influence of strain and channel direction	National	Swedish Science council	Accepted/ started 010109
KTH		Fundamental low frequency noise in nanoscale transistors with high mobility	National	Swedish Science council	Accepted/ started 010109
URV		Techniques of characterization and modeling of nanoelectronic devices for high performance applications	National	Spanish Ministry of Science / Catalan Governme nt / URV	Started
URV, UGR		MAGNUM (MedicAl imaGing using UWB technology by iNtegration of UltiMate nanoelectronic devices)	National	Spanish Ministry of Science	Accepted
GU, WARWICK, IMEC		Renascence Germanium	National	EPSRC UK	accepted

3. Exchanges

Four **calls for exchanges** have been issued electronically. Requests from partners have been then discussed during E&SC meetings (please, notice, that requests on the 4th call will be discussed during E&SC meeting in Grenoble on January 29th).

11 exchanges for the total **duration of 20 weeks** have been selected to be supported. 7 exchanges for the total duration of 12 weeks have already been done during 2008.

1. IMEL => IMEP, Post-doctoral researcher
Electrical characterization of 2-D ordered nanocrystal memories and free standing nanowires fabricated at IMEL, ***2 weeks***
EPFL => UNEW, PhD student **done**
Control and evaluation of process induced tensile strain for improved performance in silicon nanowire MOSFETs, ***2 periods of one week***
3. UNEW => EPFL, Researcher **done**
Engineering process induced strain in silicon nanowire MOSFETs, ***1 week.***
4. CHALMERS → UCL: PhD student, *1week* **done**
Investigate a possible existence of effect of mechanical strain on highK/Si interface properties

(UCL lab. has a set-up where wafers can be mechanically bent and at the same time investigated by electrical methods like Capacitance frequency spectroscopy)

5. ITE (Warsaw) => CHALMERS, PhD student, *2 weeks:* **done**

Resonant Differential Capacitance method for investigating electron states in Si/Ge QDs (*FP2.4*)
(this technique has been used by ITE previously to study InAs/GaAs QDs, Si/Ge QD-samples have been prepared by Stuttgart for additional preparation at Chalmers, new automatized setup at Chalmers will be further developed by PhD student from ITE)

6. UCL => UNEW, PhD student *2 weeks:*

Characterization of released micro and nanowires under mechanical stress, extraction of mechanical properties, piezoresistive coefficient (*FP2.1*)

7. UCL => IEMN, PhD student, *4 weeks:* **done**

Fabrication of SOI nanowires for electrical characterization with and w/o mechanical stress; determination of etch selectivity between implanted and unimplanted SiO_2 with vapour phase hydrofluoric acid (*FP2.1*)

8. FZJ => UNEW, PhD student, *2 weeks:*

Strain measurements on patterned samples prepared at FZJ using nano-Raman facilities at UNEW (*FP1.1*). The gained experience can then be used also for FP2.1

9. FZJ => UNEW, PhD, *max. 2 weeks:*

Electrical characterization of p/n-type doped strained Si material fabricated and processed in FZJ, investigation of dopant diffusion and activation in tensile biaxially strained Si (*FP1.1*)

10. IMEP-FMNT => Udine, *1 week*: **done**

Modeling of transport in Metal – Semiconductor contacts *(FP1.2 & WP4)*

11. Chalmers => AMO, *1 week*: **done**

Investigation of charge carrier transport in silicon nanowires in a temperature range between 10K and room temperature *(FP2.1)*

4. Spreading of excellence

4.1. Support of International Schools/Workshops

Four Calls were issued for the conference/workshops/seminars support to gather the requests for such actions. Since the budget for WP5 actions are rather limited E&S Committee decided to support only following workshops:

- MIGAS'08 (10kEuro);
- SINANO-NANOSIL Workshop (5kEuro),
- 3rd SINANO International Summer School (12kEuro),
- Postgraduate student meeting on electronic engineering (2.5kEuro).

4.2. Organization of seminars/courses/whorkshops/tutorials

First of all, common **SINANO-NANOSIL Workshop** "Si-based Nanodevices for ultimate CMOS and beyond-CMOS" aiming to establish a discussion forum in the field of nanoelectronics devices was organized on Sept. 17th , where all Nanosil partners were represented. Lectures were given mainly by Nanosil partners and workshop was open to a general public.

It is worth to mention **following events (8 in a total) organized by Nanosil partners** in 2008 and open to wide public. Additionally, as was already mentioned above, **two Visionary projects** (VP 1.4 "More Moor Forum" and VP 2.5 "Beyond CMOS vision") are launched within Nanosil WP1 and WP2 in order to stimulate discussions on the new hot-topics and identify areas where the partners of the Network can make a contribution. The **discussions/workshops organized by these VPs** are open to participants within Nanosil as well as to wide audience beyond Nanosil. **Two workshops** were organized **within VP1.4** during 2008: "Low Field transport in advanced MOSFETs" and "CMOS variability research in Europe: from atomic scale to circuits and systems" **One workshop** was

organized **within VP2.5**: “Brain-inspired Electronic Systems”. All details about these workshops and some other “technical” meetings organized by Nanosil partners are summarized in the table below.

Nanosil partner	Meeting/ seminar/ workshop	Topic	Date & Place	Participants (institutions)	Number of persons present *	Support from Nanosil
Tyndall	EUROSOI Workshop	SOI	Cork, Ireland, Jan 23-25th, 2008	Tyndall, VTT (Finland), UCL, EV Group (Austria), Queen's Univ. Belfast (UK), UGR, CEA, IUNET, ST, IMEC, Chalmers, CNM (Spain), Grenoble INP, Analog Devices (Ireland), Univ. of Sao Paulo (Brazil), Cissoid (Belgium), Univ. of Caen (France), Kobe Univ. (Japan), URV, Tohoku Univ., Univ. Autònoma de Barcelona (Spain), Infineon (Austria), NTUEE (Taiwan), ISP (Ukraine), WUT, Uppsala Univ. (Sweden), Meiji Univ. (Japan), Innovative Silicon Inc. (Switzerland), Incheon Univ. (Korea), Univ. of Salamanca (Spain), U. Twente (The Netherlands), ETHZ, Intel (Israel), TU Wien (Austria), ISEP (France), Meiji U. (Japan)	78 (about half from Nanosil)	no
IUNET-Udine	ULIS 2008	Ultimate Integration on Silicon Conference	March 12-14, 2008 Udine, Italy		80	No, supported by SINANO
IMEL	Workshop	Current trends in Nanoelectronics and MEMS	8.7.2008, NCSR Demokritos, Athens, Greece	IMEL, FORTH (Crete), Univ. of Athens, Univ. of Patras, Univ. of Thessaloniki, NTUA, Corallia, Hellenic SIA, Praxis-Help Forward, Broadcom Hellas	50	No
IMEL	Workshop	Micro&Nanoelectronics: Present status and perspectives	14.4.2008NCSR Demokritos, Athens, Greece	The participants were High School Professors from 15 different Greek High Scholls	250	No
URV	Meeting/ Workshop	Graduate Student Meeting on Electronic Engineering	Tarragona, June 19-20 2008	URV	**8**/*17*	yes
IUNET	Third SINANOSummer School	Modeling, Simulation and Characterization of Silicon Devices	September 1-5, 2008	Mostly involved in Nanosil and Pullnano projects	Students: **36** / *19* Lecturers **12** / *9*	Yes
UNEW	ESSDERC	CMOS at the bleeding	Sept 08,		60	no

	tutorial	edge	Edinburgh			
Grenoble INP	Workshop VP1.4	Low Field Transport in Advanced MOSFETs	6th Sept 2008 Bertinoro Italy	Grenoble INP, TUBS, IU.NET, ST, LETI, AMO, IMO	17	YES
GU	ESSDERC/ ESSIRC Workshop of VP1.4	CMOS variability research in Europe: From Atomic Scale to Circuits and Systems	19 Sept 2008	78	**10**	yes
LIVUNI	VP 2.5 Workshop	'Brain-Inspired Electronic System'	19 Sept., Edinburgh, UK	Univ. of Southampton, Univ. of Edinburg, IMNS, SEE, Edinburg Univ., Univ. of Wales, Electronics KTN, Univ. of West Scotland, LIVUNI, Univ. of Manchester, Chalmers, UCL, Univ. of Ulster, Gajit, e2V, NeuW Ltd, ETHZ, Amadeus Capital Partners, Univ. of Durham, MIRAI, PDD Group Ltd., Imperial College, London, Cascoda Ltd., Univ. of Bath, Senlac Services, Electronics Scotland, Univ. of Lincoln	**5** / *34*	yes
Grenoble INP	Sumer Scholol	MIGAS Nanoscale CMOS and Si-based Beyond CMOS Nanodevices	28th June - 4th July 2008, Grenoble France		80 / **40** (about)	YES
Grenoble INP	Workshop	Si based Nanodevices for Ultimate CMOS and Beyond CMOS	19th Sept. 2008, Edimburgh, UK	All	**40**	YES
RWTH	Meeting	Kick-off Meeting WP2 "Beyond CMOS"	Aachen, 15th May 2008	UNEW, USTUTT, EPFL, UCL, TUBS, Tyndall, URV, Chalmers, FZJ, IUNET, AMO, RWTH	**22**	yes
UCL	meeting	PhD thesis confirmation of Mr. Vikram Passi & Characterization of Si nanowires under mechanical stress	Nov. 2008	IEMN-ISEN, UCL	**7**	no
ISEN-IEMN	Meeting	FSP1.2 Schottky Meeting	10 Jun 08 in Lille	ISEN-IEMN, Warwick, KTH, FZJ, UCL	**10**	no
AMO	training	fabrication of ultrathin interlayers	13-25 July 2008 AMO Germany	AMO / LIVUNI	1 AMO 1 LIVUNI	no

***** *in **bold** the ones inside NANOSIL, in Italic - outside NANOSIL*

4.3. University courses.

One **new university course** (of 20h) in Nanosil field has been started during 2008 by GU: “Advanced CMOS devices and simulation techniques” (given by Profs. A. Asenov and S. Roy).

4.4. Nanosil experienced lecturers

A **database of NoE experienced lecturers** (similarly to IEEE distinguished lecturers) with existing high-level/high-quality lectures is created. It is planned to put pdf-version on web-site and distribute by e-mail to all partners.

4.5. Best practice training for technicians

Training on “fabrication of ultra-thin layers” was organized between AMO and LIVUNI in July 2008 at AMO.

5. Dissemination of knowledge

5.1. Inside of NoE

Dissemination of knowledge within Nanosil is provided through **the Executive & Scientific Committee meetings** (each 3 months), **Governing Board meeting**, **kick-off, regular and cross WPs/FPs meetings** (see aove). Additionally, **exchanges/ trainings** of personnel played an important role in information/ideas/competences exchange between partners.

5.2. Beyond NoE

Web-site of Nanosil was created. It is now accessible for a world-wide scientific community and used to promote NoE activities such as workshops/ trainings and competences of Nanosil partners. However, access to some information is restricted to Nanosil partners only (though the login-password).

12 workshops/schools/conferences/tutorials have been organized during 2008 by Nanosil partners. Such events accessible not only to Nanosil partners but to a wide scientific community are very important to disseminate a knowledge gathered by Nanosil members and to widely promote our Network.

Nanosil poster was prepared end of 2008. When printed it will be offered to all Nanosil partners to be posted in their lab and promote in such a way the research activities / networking within Nanosil.

Eight researchers (mainly FP leaders) represented NoE Nanosil at the **EU-Russia Workshop** organized in Moscow by the European Commission with support from the Russian National ICT Contact Point and the Ministry of Science and Education with objective of intensification of R&D cooperation between actors of the ICT value chain from both sides. Participation of Nanosil members in this event **has been supported through the “exchanges procedure”.**

Finally, achievements / knowledge gathered within Nanosil are widely disseminated through the **publications in major international journals** and **participation** of Nanosil members in **international conferences/workshops**.

38 joint publications (see list of references) in high-level international journals have been prepared by Nanosil members, among which 30 articles are already published and 5 are accepted for publication in 2009. Some (14) are already clearly linked to Nanosil's first year, whereas most are still obviously the outcome of previous projects such as Sinano NoE. We in purpose mention here only the number of joint publications to emphasize the value of networking, while surely this number will be much greater if we will take into account all single-partner publications. Furthermore, **82 conference/workshop presentations** (see list of references) are given (and 5 more accepted) by Nanosil partners, among which **28 are invited presentations**.

References

Publications (only joint)

Title	Authors	Nanosil partners	WP(s)	References (journal/conference/book; vol., No., pp.)	Status (published /accepted/ submitted)	Acknowledgment Nanosil (yes/no/ Sinano)
The growth of small diameter silicon nanowires to nanotrees	P Gentile, T David, F Dhalluin, D Buttard, N Pauc, M Den Hertog, P Ferret and T Baron	FMNT-LTM, CEA	2.4	Nanotechnology 19 (2008) 125608	Published	
Monte Carlo study of apparent magnetoresistance mobility in nanometer scale metal oxyde semiconductor field effect transistors	K. Huet, D. Querlioz, W. Chaisantikulwat, J. Saint-Martin, A. Bournel, M. Mpuis, P. Dollfus	UPS, INPG-IMEP	4.3	Journal of Applied Physics, vol.104, no.4, pp. 044504-1-7. (15 Aug. 2008)	Published	Yes
Monte-Carlo simulation of MOSFETs with band-offsets in the source and drain	M. Braccioli, P. Palestri, M. Mouis, T. Poiroux, M. Vinet, G. Le Carval, C. Fiegna, E. Sangiorgi, S. Deleonibus	IUNET, INPG-IMEP, CEA-LETI	4.3	Solid-State Electronics, Vol. 52, pp. 506-513	Published	SINANO
Extraction of η parameter characterizing μeff vs Eeff curves in strained Si nMOS devices.	K. Bennamane, M. DeMichielis, G. Ghibaudo, D. Esseni	INPG-IMEP, IUNET	4.3	Electronics Letters, 44, 1219 (2008)	Published	Yes
A capacitor-less 1T-DRAM on SOI based on double gate operation.	M. Bawedin, S. Cristoloveanu, D. Flandre	INPG-IMEP, UCL	1	IEEE Electron Device Letters, Vol. 29, n°7, 795-798 (2008)	Published	No
The Quantization Impact of Accumulated Carriers in Silicide-Gated MOSFETs	N. Rodriguez, F. Gámiz, L. Donetti, R. Clerc, G. Ghibaudo, S. Cristoloveanu	INPG-IMEP, URV-UGR	4.3	IEEE Electron Device Letters, Vol. 29, p. 628-631 (June 2008)	Published	No
On the Electron Mobility Enhancement in biaxially strained Si MOSFETs	F.Driussi, D.Esseni, L.Selmi, P.-E.Hellström, G.Malm, J.Hallstedt, M.Östling, T.J.Grasby, D.R.Leadley and X.Mescot	Udine, KTH, Warwick	1	Solid State Electronics 52 498–505 (2008)	Published	SINANO
High-frequency performance of Schottky Source/Drain	J.-P.Raskin, D.J.Pearman, G.Paillonc y,	UCL, Warwick	1, 3 & 4	IEEE Electronic Device Letters	Published	No

Silicon pMOS devices	J.M.Larson, J.Snyder, D.R.Leadley and T. E. Whall			29, 396-398 (2008)		
Silicon-based nanostructures and nanodevices for long-term nanoelectronics applications	F. Balestra, E. Parker, D. Leadley, S. Mantl, E. Dubois, O. Engstrom, R. Clerc, S. Cristoloveanu, H. Kurz, J.P. Raskin, M. Lemme, A. Ionescu, K.E. Moselund, K. Boucart, E. Kasper, A. Karmous, M. Baus, B. Spangenberg, M. Ostling, E. Sangiorgi, G. Ghibaudo, D. Flandre	ALL	ALL	Materials Science in Semiconductor Processing	In press	Yes
Fabrication and characterisation of strained Si heterojunction bipolar transistors on virtual substrates	S. Persson, M. Fjer, E. Escobedo-Cousin, G. Malm, Y.-B. Wang, P.-E. Hellström, M. Östling, E.H.C. Parker, L.J. Nash, P. Majhi, S.H. Olsen, A.G. O'Neill	Newcastle Unversity KTH	1 and 3	International Electron Device Meeting (IEDM) 2008 pp735-738	Published	Yes
Carrier mobility in undoped triple-gate FinFET structures and limitations of its description in terms of top and sidewall channel mobilities	T. Rudenko, V. Kilchytska, N. Collaert, M. Jurczak, A. Nazarov, D. Flandre,	UCL, IMEC	4	IEEE Trans. on Electron Devices, vol. 55, No. 12, 2008, p. 3532-3541.	published	YES
Characterization of ultrathin SOI film and application to short channel MOSFETs	X.H. Tang, N. Reckinger, G. Larrieu, et al.	UCL, IMEN-ISEN	1, 4	Nanotechnology, Vol. 19, No. 16, 2008	published	No
Low Schottky barrier height for ErSi2−x /n-Si contacts formed with a Ti cap	N. Reckinger, X. Tang, V. Bayot, D.A. Yarekha, E. Dubois, S. Godey, X. Wallart, G. Larrieu, A. Łaszcz, J. Ratajczak, P.J. Jacques, J.P. Raskin	UCL IEMN	1	J. Appl. Physics 104, 2008	published	No
Impact of channel doping on Schottky barrier height and investigation on p-SB MOSFETs performance	G. Larrieu, E. Dubois, D. Yarekha, N. Breil, N. Reckinger, X. Tang, J. Ratajczak, A. Laszcz	IEMN-ISEN, UCL	1	Materials Science and Engineering B	published	No
Amorphous to crystalline transition of Er silicide upon thermal annealing and impact on the Schottky barrier height	N. Reckinger, X. Tang, V. Bayot, D. A. Yarekha, E. Dubois, S. Godey, X. Wallart, G. Larrieu, A. Laszcz, J. Ratajczak, P. J. Jacques, and J.-P. Raskin	UCL, IEMN-ISEN	1	Applied Physics Letters	submitted	Yes
RF small signal analysis of Schottky-Barrier p-MOSFET	R. Valentin, E. Dubois, J.-P. Raskin, G. Larrieu, G. Dambrine, Tao Chuan Lim, N. Breil and F. Danneville,	UCL, IEMN-ISEN	1	IEEE TED, vol. 55, no. 5, pp. 1192-1202, May 2008.	published	No
High Frequency Noise Performance of 60 nm gate length FinFETs	J.-P. Raskin, G. Pailloncy, D. Lederer, F. Danneville, G. Dambrine, S. Decoutere, A. Mercha,	UCL, IEMN-ISEN, IMEC	4	IEEE TED, vol. 55, no. 10, pp. 2718-2727, October 2008.	published	No

	B. Parvais					
Experimental and Theoretical Analysis of Hole Transport in Uniaxially Strained pMOSFETs	K. Huet, M. Feraille, D. Rideau, R. Delamare V. Aubry-Fortuna, M. Kasbari, S. Blayac, C. Rivero, A. Bournel, C. Tavernier, P. Dollfus, H. Jaouen	UPS, STM	4	Proc. ESSDERC 2008, Institute of Physics (2008) 234-237	published	Yes
Leakage current effects on C-V plots of high-k MOS capacitors	Y. Lu, S. Hall, L. Z. Tan, I. Z. Mitrovic, W. M. Davey, B. Raeissi, O. Engstrom, K. Cherkaoui, S. Monaghan, P. K. Hurley, H.D.B. Gottlob, and M. C. Lemme	LIVUNI, Chalmers, AMO, Tyndall	1	JVST Jan 2009	accepted	Yes
Sensitivity of trigate MOSFETs to random dopant induced threshold voltage fluctuations	Ran Yan, Danny Lynch, Thibault Cayron, Dimitri Lederer, Aryan Afzalian, Chi-Woo Lee, Nima Dehdashti, J.P. Colinge,	INPG Tyndall	4	Solid-State Electronics, Vol. 52, No. 12, pp. 1872-1876, 2008	Published	No
A quasi two-dimensional compact drain current model for undoped symmetric double gate MOSFETs including short-channel effects	F. Lime, B.Iñiguez and O. Moldovan	URV, INPG	4	IEEE Trans. on Electron Devices, vol. 55, no. 6, pp. 1441-1448, June 2008	published	Yes
Conduction mechanisms of silicon oxide/titanium oxide MOS stack structures	J.C. Tinoco, M. Estrada, B. Iñiguez and A. Cerdeira	URV, UCL	1	Micro-electronics Reliability, Vol. 48, No 3, pp. 370-381, 2008	published	No
Threshold voltage model for bulk strained-silicon NMOSFETs	J C Tinoco, R Garcia, B Iñiguez, A Cerdeira and M Estrada	URV, UCL	1, 4	Semiconductor Science & Technology, 23 (2008) 035017	published	SINANO
Accurate prediction of the volume inversion impact on undoped Double-Gate MOSFET capacitances	O. Moldovan, F. A. Chaves, D. Jiménez, J. P. Raskin and B. Iñiguez	URV, UCL	4	International Journal of Numerical Modelling:Electronic Networks, Devices and Fields	submitted	Yes
Interface defects in HfO_2, $LaSiO_x$, and Gd_2O_3 high-k/metal-gate structures on silicon: energy distribution and passivation,	P. K. Hurley, K. Cherkaoui, E. O'Connor, A.W. Groenland, M. C. Lemme, H. D. B. Gottlob, M. Schmidt, S. Hall, Y. Lu, O. Buiu, B. Raeissi, J. Piscator and O. Engström	Tyndall, AMO, Liverpool, Chalmers	1.3	J. Electrochem. Soc. 155, G13 (2008)	Published	No
High-k-oxide/silicon interfaces characterized by capacitance frequency spectroscopy	B.Raeissi, J.Piscator, O. Engström, S.Hall, O. Buiu, M.C.Lemme, H.D.B.Gottlob, P.K.Hurley, K.Charkaoui and H.J.Osten	Chalmers, Liverpool, AMO, Tyndall	1.3	Solid State Electronics, 52, 1274 (2008)	Published	No
Gd silicate: A High-k	H.D.B. Gottlob1,, A.	AMO,	1.3	J. Vacum. Sci.	Accepted	No

Dielectric Compatible with High Temperature Annealing	Stefani, M. Schmidt, M.C. Lemme, H. Kurz, I.Z. Mitrovic, M. Werner3, W.M. Davey, S. Hall, P.R. Chalker, K. Cherkaoui, P.K. Hurley, J. Piscator, O. Engström, S.B. Newcomb	Tyndall, Liverpool, Chalmers, Glebe		Tech.		
Deep level transient spectroscopy in quantum dot characterization.	O. Engström, M. Kaniewska	Chalmers, ITE	2.4	Nanotech. Res. Lett. 3,179 (2008)	Published	No
Thermal instability of electron traps in InAs/GaAs quantum dot structures	M. Kaniewska, O. Engström, M. Kaczmarczyk and G. Zaremba	ITE, Chalmers	2.4	Mater. Sci.: Mater. Electron. 19, S101 (2008)	Published	No
Electrical study of InAs/GaAs quantum dots with two different environments	M. Kaniewska, O. Engström, M. Kaczmarczyk, B. Surma, W. Jung and G. Zaremba	ITE, Chalmers	2.4	Phys. Stat. Sol. (c), 5, 2926 (2008)	Published	No
The high-mobility bended channel silicon nanowire transistor	K. E. Moselund, P. Dobrosz*, S. Olsen*, A. O'Neill*, D. Bouvet, L. De Michielis, V. Pott, D. Tsamados and A. M. Ionescu	EPFL UNEW	2	IEEE TED	Submitted, in revision To appear 2009	Yes
Determination of electron effective mass and electron affinity in HfO2 using MOS and MOSFET structures	S. Monaghan, P. K. Hurley, K. Cherkaoui, M. A. Negara, and A. Schenk	ETHZ, Tyndall	1, 2, 4	Solid State Electronics	In Press	No
Si-SiO2 interface band-gap transition – effects on MOS inversion layer	S. Markov, P. V. Sushko, S. Roy, C. Fiegha, E. Sangiorgi, A. L. Shliger, and A. Asenov	GU IUNET	4	Physika Status Solidi a Vol 205, pp 1290-1295 (2008)	Published	No
Analysis of Self-Heating Effects in Ultra-Thin Body SOI MOSFETs by Device Simulation	Claudio Fiegna1, Yang Yang, Enrico Sangiorgi1, Anthony G. O'Neill	UNEW, IUNET	4	IEEE Trans Electron Dev, Vol55, No.1, p233, 2008	Published (invited paper)	No
Strained Si/SiGe MOS technology: improving gate dielectric integrity	SH Olsen, L Yan, R Agaiby, E Escobedo-Cousin, AG O'Neill, P-E Hellström, M Östling, K Lyutovich, E Kasper, C Claeys and EHC Parker	UNEW, KTH, USTUTT, IMEC, Warwick	4	Microelectronics Engineering, 2008	Published (invited paper)	Yes
Reduced self-heating by strained silicon substrate engineering	A O'Neill, S Olsen, Y Yang, R Agaiby, P-E Hellstrom, M Ostling, K Lyutovich, E Kasper, G Eneman, P Verheyen, R Loo, C Claeys, C Fiegna and E Sangiorgi	UNEW, IUNET, USTUTT, KTH, IMEC	4	Applied Surface Science Vol 254 p6182 (2008)	Published (invited paper)	Yes
Nanoscale strain characterisation for ultimate CMOS and beyond	SH Olsen, P Dobrosz, RMB Agaiby, YL Tsang, O Alatise, SJ Bull, AG O'Neill, KE	UNEW, EPFL, FZJ	4	Materials Science in Semiconductor Processing	Accepted (invited paper)	Yes

	Moselund, AM Ionescu, P Majhi, D Buca, S Mantl and H Coulson					
Insight into the aggravated lifetime reliability in advanced MOSFETs with strained Si channels on SiGe strain relaxed buffers due to self-heating	R Agaiby, AG O'Neill, SH Olsen, G Eneman, P Verheyen, R Loo and C Claeys	UNEW, IMEC	4	IEEE Transactions on Electron Devices, vol. 55, pp. 1568-1573, 2008	published	SINANO

Presentation at the Conferences and Workshops (emphasize if invited lectures)

Title	Author(s)	Nanosil partners	Conference /Workshop	WP	Date & Location	Type of presenta-tion	Status
SOI as a platform for transition from micro to nano	F. Balestra	INPG-IMEP	215th ECS Meeting Symposium E9: SOI Device Technology	6	May 24-29, 2009, San Francisco, (USA)	Invited	Accepte d
What is the killing advantage of multiple-gate SOI MOSFET?	F. Balestra	INPG-IMEP)	5th EUROSOI Workshop	6	Goteborg, Sweden, January 2009	Invited, panel session	Accepte d
Status and trends in Nanoscale Si-based devices and materials	F. Balestra	Coordi-nator	9th International Conference on Solid-State and Integrated-Circuit Technology	6	Beijing, China (October 20-23, 2008)	Invitedr	Done
New semiconductor Nanodevices	F. Balestra	Coordi-nator	International School on the Physics of Semiconducti ng Compounds 2008	6	Jaszowiec, Poland, June 2008	Invited	Done
NANOSIL Network of Excellence: Silicon-based nanostructures and nanodevices for long-term nanoelectronic s applications.	F. Balestra, E. Parker, D. Leadley, S. Mantl, E. Dubois, O. Engstrom, R. Clerc, S. Cristoloveanu, H. Kurz, J.P. Raskin, M. Lemme, A. Ionescu, E. Kasper, A. Karmous, M. Baus, B. Spangenberg, M. Ostling, E. Sangiogi, G. Ghibaudo, D. Flandre	All	European Materials Research Society (E-MRS 2008), Symposium J	6	Strasbourg, France (26-30 Mai 2008)	Invited	Done
Mobility of strained and unstrained short channel MOSFETs: New insight by magnetoresist	M. Cassé, F. Rochette, N. Bhouri, F. Andrieu, K. Romanjek, D.K. Maude, M. Mouis, G. Reimbold, F.	CEA/LETI, INPG-IMEP	Symposium on VLSI Technology (VLSI 2008), Proceedings IEEE. pp. 170-1.	4.3	June 17-20, 2008, Honolulu, Hawaï (USA)	Oral	Done

ance	Boulanger		Piscataway, NJ, USA				
Emerging nanotechnology	T. Baron, B. Salem, F. Dhalluin, P. Gentile, N. Pauc, M. Den Hertog, J.L. Rouvière, P. Mur, B. De Salvo, P. Ferret, J. Dufourcq, S. Bodnar	FMNT-LTM, CEA	38th European Solid-State Device Research Conference (ESSDERC)		Edinburgh, UK (15-19 Sept 2008)	Invited	Done
The Ge condensation technique: a solution for planar SOI/GeOI co-integration for advanced CMOS technologies?	B. Vincent, J.F. Damlencourt, Y. Morand, A. Pouydebasque, C. Le Royer, L. Clavelier, N. Dechoux, P. Rivallini, T. Nguyen, S. Cristoloveanu, Y. Campidelli, D. Rouchon, M. Mermoux, S. Deleonibus, D. Bensahel, T. Billon	STM, CEA-LETI, INPG-IMEP	European Materials Research Society (E-MRS 2008), Symposium J. Proceedings in Materials Science in Semiconductor Processing, Elsevier	1.1	Strasbourg, France (May 26-30, 2008)	Invited	Done
A Mobility Extraction Method for 3D Multichannel Devices	C. Dupré, T. Ernst, E. Bernard, B. Guillaumot, N. Vulliet, P. Coronel, T. Skotnicki, S. Cristoloveanu, G. Ghibaudo and S. Deleonibus	CEA/LETI, STM, INPG-IMEP	38th European Solid-State Device Research Conference (ESSDERC'08)	4.3	Edinburgh, UK (15-19 Sept 2008)	Oral	Done
Characterization methods for nanodevices.	S. Cristoloveanu	INPG-IMEP	38th European Solid-State Device Research Conference ESSDERC'08	4.3	Edinburgh, UK (15-19 Sept 2008)	Invited	Done
Introduction of diamond into advanced FDSOI CMOS	J-P. Mazellier, O. Faynot, F. Andrieu, S. Cristoloveanu, S. Deleonibus	CEA-LETI, INPG-IMEP	4th EUROSOI Workshop	1.1	Cork, Ireland (23-25 janvier 2008)	Oral	Done
Ge diffusion during Ge-condensation process	C.S. Beer, R.J.H. Morris, T.E. Whall, E.H.C. Parker and D.R. Leadley	Warwick	ISTDM	1	Taiwan, (May, 2008)	Poster	Done
Ge-On-Insulator substrates formed by Ge condensation technique: fabrication, modeling and characterization.	J.F. Damlencourt, B. Vincent, C. Le Royer, P. Rivallin, E. Martinez, M.C. Roure, Y. Campidelli, D. Rouchon, T. Nguyen, S. Cristoloveanu, Y. Morand, S. Descombes, L. Clavelier	Grenoble INP	International Conference of Electronic Materials, sponsored by Int. Union of Materials Research Society (ICEM-IUMRS 2008)	1.1	Sydney, Australia (28 juillet - 1 août 2008)	Invited	Done

Quantum transport in nanowire metal-oxide-semiconductor transistors: influence of dielectric confinement	M. Bescond, M. Lannoo, F. Michelini, N. Cavassilas, M. G. Pala	INPG, CNRS	ICPS	2.4, 4.3	Rio de Janeiro, July 27-August 1, 2008	Poster	done
Full 3D Real-Space NEGF Simulation of Transport and Magnetotransport in Si-Nanowire FETs	C. Buran, M. G. Pala, M. Bescond and M. Mouis	INPG, CNRS	ESSDERC	2.4, 4.3	Rio de Janeiro, July 27-August 1, 2008	Poster	done
Reverse graded SiGe/Ge/Si heterostructures for high-composition virtual substrates.	V.A.Shah, D.R.Leadley, D.Fulgoni, J.Parsons, E.H.C.Parker	Warwick	E-MRS	1	Strasbourg (May 2008)	Oral	Done
Channel Backscattering Characteristics of High Performance Germanium pMOSFETs	A. Dobbie, B. De Jaeger, M. Meuris, T.E. Whall, E.H.C. Parker and D.R. Leadley	Warwick, IMEC	ULIS	1	Udine, Italy (March, 2008)	Oral	Done
Anomalous Ge diffusion effects during Ge-condensation	C.S. Beer, T.E. Whall, R.J.H. Morris, E.H.C. Parker and D.R. Leadley	Warwick	ULIS	1	Udine, Italy (March, 2008)	Poster	Done
The role of interface states in the low temperature mobility of hafnium-oxide gated Ge-pMOSFETs and the effect of a hydrogen anneal	C.S. Beer, T.E. Whall, E.H.C. Parker, D.R. Leadley, B. De Jaeger, G. Nicholas, P. Zimmerman and M. Meuris	Warwick, IMEC	ULIS	1	Udine, Italy (March, 2008)	Oral	Done
Relaxation of Strained Silicon on $Si_{0.5}Ge_{0.5}$ Virtual Substrates	J. Parsons, R.J.H. Morris, D.R. Leadley and E.H.C. Parker	Warwick	ULIS	1	Udine, Italy (March, 2008)	Poster	Done
Confinement and Transport in Silicon Based Quantum Structures	B. Berghoff, R. Rölver, B. Spangenberg, D. Bätzner, H. Kurz, A. Dimyati. A. Sologubenkoo, J. Mayer	RWTH	33rd IEEE Photovoltaic Specialists Conference,	2 2.4	San Diego, 11.05-16.05. (2008)	oral	done
Towards Schottky-Barrier Source/Drain MOSFETs	M. Östling, V. Gudmundsson, P.-E. Hellström, B.G. Malm, Z. Zhang, S.-L.	KTH	2008 9TH International Conference on Solid-State and	1 and 3	October 20-23, Beijing, China	Invited presentation	Done

	Zhang		Integrated-Circuit Technology				
Substrate impact on sub-32 nm Ultra Thin SOI MOSFETs with Thin Buried Oxide	S. Burignat, D. Flandre, V. Kilchytska, F. Andrieux, O. Faynot and J.-P. Raskin	UCL, CEA	EuroSOI 2009	4	Jan. 2009 Gothenburg	oral	accepted
Transconductance and Mobility Behaviors in UTB SOI MOSFETs with Standard and Thin BOX	T. Rudenko, V. Kilchytska, S. Burignat, J.–P. Raskin, F. Andrieu, O. Faynot, A. Nazarov, V.S. Lysenko and D. Flandre	UCL, CEA	EuroSOI 2009	4	Jan. 2009 Gothenburg	oral	accepted
Impact of channel doping on Schottky barrier height and investigation on p-SB MOSFETs performance	G. Larrieu, E. Dubois, D. Yarekha, N. Breil, N. Reckinger, X. Tang, J. Ratajczak, A. Laszcz	IEMN UCL	e-MRS Spring Meeting	1	26-30 May 2008 Strasbourg	Oral	done
Selective etching of implanted silicon-dioxide in hydrofluoric acid	V. Passi, A. Lecestre, E. Dubois, J.P. Raskin	UCL IEMN	34th Conference on Micro and Nano Technology	2	September 15-18, 2008, Athens	Oral	done
Investigation on the Platinum Silicide Schottky Barrier Height Modulation using a Dopant Segregation Approach	N. Breil, A. Halimaoui, E. Dubois, E. Lampin, Ludovic Godet, George Papasouliotis, Guilhem Larrieu	IEMN	MRS-Spring Meeting, Mater. Res. Soc	1	24-28 April 2008 San Francisco	oral	done
Impact of channel doping on Schottky barrier height and investigation on p-SB MOSFETs performance	G. Larrieu, E. Dubois, D. Yarekha, N. Breil, N. Reckinger, X. Tang, J. Ratajczak, A. Laszcz	IEMN UCL	e-MRS Spring Meeting	1	26-30 May 2008 Strasbourg	Oral	done
Selective etching of implanted silicon-dioxide in hydrofluoric acid	V. Passi, A. Lecestre, E. Dubois, J.P. Raskin	UCL IEMN	34th Conference on Micro and Nano Technology	2	September 15-18, 2008, Athens	Oral	done
DC and RF characteristics of a 60 nm FinFET for a wide temperature	J. C. Tinoco, B. Parvais, A. Mercha, S. Decoutere, J-P Raskin	UCL, IMEC	EUROSOI – 2008	4	Tyndall January 23-25, 2008	Oral	done

range							
Revised RF extraction methods for deep submicron MOSFETs"	J. C. Tinoco and J.-P. Raskin,	UCL	38th European Microwave Week 2008	4	Amsterdam, October 28-31, 2008, pp. 127-130.	Oral	done
RF-extraction methods for MOSFET series resistances: a fair comparison	J. C. Tinoco and J.-P. Raskin,	UCL	Seventh International Caribbean Conference on Devices, Circuits and Systems	4	Cancun, Mexico, April 28-30, 2008, paper 64, pp. 1-6.	Oral	done
Optimizing FinFET Geometry and Parasitics for RF applications	A. Kranti, J.-P. Raskin and G. A. Armstrong,	UCL	IEEE International SOI Conference, SOI'2008,		New York, USA, October 6-9, 2008, pp. 123-124.	Oral	done
Impact of temperature reduction and channel engineering on the linearity of FD SOI nMOSFETs	M. de Souza1, D. Flandre, J. A. Martino, E. Simoen, C. Claeys, M. A. Pavanello;	UCL, IMEC	EuroSOI 2009	4	Jan. 2009, Gothenburg,	Oral	done
Experimental and Theoretical Analysis of Hole Transport in Uniaxially Strained pMOSFETs	K. Huet, M. Feraille, D. Rideau, R. Delamare V. Aubry-Fortuna, M. Kasbari, S. Blayac, C. Rivero, A. Bournel, C. Tavernier, P. Dollfus, H. Jaouen	UPS, STM	ESSDERC 2008	4	15-19 Sept., Edinburgh, UK	oral	done
Wigner Monte Carlo approach to quantum transport in nanodevices	P. Dollfus, D. Querlioz, J. Saint-Martin, V. Nam Do, A. Bournel	UPS	SISPAD 2008	4	9-11 Sept., Hakone Japan	invited	done
On the Wigner Formalism of Quantum Transport in Semi-conductor Nanodevices	P. Dollfus, D. Querlioz, J. Saint-Martin, V. Nam Do, A. Bournel	UPS	AMSN 2008	4	15-21 Sept., Nha Trang, Viet Nam	invited	done
Electron-phonon interaction in silicon quantum dots	A. Valentin, J. Sée, S. Galdin-Retailleau, P. Dollfus	UPS	ULIS 2008	2	13-14 March, Udine, Italy	oral	done
Particle Monte Carlo approach to semi-classical and quantum transport in CNTFET within a multiscale	P. Dollfus, S. Galdin-Retailleau, H. Cazin d'Honincthun, H. Nha Nguyen, D. Querlioz, A. Bournel	UPS	CCTN 08	2	28 June, Mont-pellier, France	invited	done

simulation framework from atoms to circuit							
Static and dynamic performance of CNTFETs using particle Monte Carlo simulation	H. Nha Nguyen, H. Cazin d'Honincthun, P. Dollfus, A. Bournel, S. Galdin-Retailleau	UPS	NT 08	2	29 Jun. - 4 Jul., Montpellier, France	poster	done
Electronic transport and spin polarization effects in single graphene barrier structures	V. Nam Do, V. Hung Nguyen, P. Dollfus, A. Bournel	UPS	NT 08	2	29 Jun. - 4 Jul., Montpellier, France	poster	done
Effect of edge disorder on the bandgap of graphene nanoribbons	D. Querlioz, Y. Apertet, A. Valentin, K. Huet, A. Bournel, S. Galdin-Retailleau, P. Dollfus	UPS	NT 08	2	29 Jun. - 4 Jul., Montpellier, France	poster	done
Platforms for planar & non-planar ultrathin silicon	M. Schmidt, H.D.B. Gottlob, J. Bolten, T. Wahlbrink, T. Mollenhauer, M. Bückins, T.E. Weirich, F. Dorn, J. Mayer, H. Kurz	AMO	EUROSOI 2009	2	19.01.2009 Gotenburg, Sweden	oral	done
Leakage current effects on C-V plots of high-k MOS capacitors	Y. Lu, S. Hall, L. Z. Tan, I. Z. Mitrovic, W. M. Davey, B. Raeissi, O. Engstrom, K. Cherkaoui, S. Monaghan, P. K. Hurley, H.D.B. Gottlob, and M. C. Lemme	LIVUNI, Chalmers, AMO, Tyndall	Workshop on Dielectrics in Microelectronics WoDiM 2008	1	June 23 – 25, 2008 in Bad Saarow (Berlin), Germany	poster	done
Quest for an Optimal Gadolinium Silicate Gate Dielectric Stack	I.Z. Mitrovic, M. Werner, W.M. Davey, S. Hall, P.R. Chalker, H.D.B. Gottlob, M.C. Lemme, O. Engstrom, K. Cherkaoui and P.K. Hurley	LIVUNI, Chalmers, AMO, Tyndall	39th IEEE Semiconductor Interface Specialists Conference SISC 2009	1	December 11-13, 2008 San Diego, (CA), USA	poster	accepted
Small-Signal Compact Modelling of Multi-Gate MOSFETs	B. Iñiguez	URV	IEEE EDS Mini-Colloquium on Advanced Electron Devices Technology & Modeling	4, 2	Cambridge (UK), September 12 2008	Invited lecture	Done
Porous anodic alumina thin films on Si as	A. G. Nassiopoulou, V. Gianneta, F.	IMEL	1st IC4N-2008: International	2.4	Halkidiki, Greece, 16-18 June	Invited	done

masking layers for silicon surface nanostructuring and as templates for nanostructure growth	Zacharatos, M. Kokonou, M. Hauffman		Conference from Nanoparticles and Nanomaterials to Nanodevices and Nanosystems		2008		
Structural, chemical and light emission properties of very thin anodic silicon films fabricated by short single current pulses	S. Gardelis, A. G. Nassiopoulou, F. Petraki, S. Kennou, I. Tsiaoussis, N. Frangis	IMEL	XXIV Panhellenic Conference on Solid State Physics and Materials Science	2.4	Heraklion, Crete, September 21-24, 2008	Invited	done
Advanced compact modeling techniques of nanoscale Multi-Gate MOSFETs	B. Iñiguez, A. Lázaro, O. Moldovan, B. Nae, A. Cerdeira	URV	IEEE Lester Eastman Conference	4, 2	Newark (Delaware, USA), August 5-7 2008	Invited lecture	Done
Compact Modeling Techniques in Thin Film SOI MOSFETs	B. Iñiguez, D. Flandre	URV, UCL	MOS-AK Workshop	4	Edinburgh (UK), September 19 2008	Invited lecture	Done
Finite element Simulations of parasitic capacitances related to multiple-gate field-effect transistors Architectures	O. Moldovan, D. Lederer, B. Iñiguez, J. P. Raskin	URV, Tyndall, UCL	8th IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF 2008)	4	Orlando (FL, USA), January 23-25 2008	Poster	Done
Compact Charge and Capacitance Modeling of Undoped Ultra-Thin-Body SOI MOSETs	O. Moldovan, F. A. Chaves, D. Jimenez, B. Iñiguez	URV	EUROSOI 2008 Workshop	4	Cork (Ireland), January 23-25 2008	Poster	Done
DC, RF and Noise Compact Model for FinFETs Including Quantum Effects	B. Nae, A. Lázaro, B. Iñiguez, F. García, M. Tienda-Luna, A. Godoy	URV, UGR	Conference on Design of Circuits and Integrated Systems (DCIS)	4	Grenoble (France), November 12-14 2008	Oral	Done
Study of Ballisticity in SOI Nano-MOSFETs at Very Low Drain Bias	C. Sampedro, F. Gámiz, A. Godoy, S. Cristoloveanu and I. M. Tienda-Luna	UGR, INPG	EUROSOI 2008 Workshop	4	Cork (Ireland), January 23-25 2008	Oral presentation	Done
Equivalent Oxide Thickness of SOI-GAA devices	F. J. García Ruiz, I.M. Tienda-Luna, L.Donetti, A.Godoy, F. Gámiz	UGR	EUROSOI 2008 Workshop	1, 4	Cork (Ireland), January 23-25 2008	Poster	Done

In-depth characterization of quantum effects in SOI MOSFETs for modeling purposes	J. B. Roldán, M. Balaguer, A. Godoy, F. G. Ruiz, F. Gámiz	UGR	EUROSOI 2008 Workshop	4	Cork (Ireland), January 23-25 2008	Poster	Done
Impact of the top surface density of states on the characteristics of ultrathin SOI pseudo-MOSFETs	N. Rodriguez, S. Cristoloveanu, T. Nguyen, F. Gámiz	UGR, INPG	EUROSOI 2008 Workshop	4	Cork (Ireland), January 23-25 2008	Poster	Done
Enhanced Electron Transport by Carrier Overshoot in Ultrascaled Double Gate MOSFETs	N. Rodriguez, L.Donetti, C.Sampedro, F.Martinez-Carricondo, F.Gamiz	UGR, INPG	ULIS-2008, The 9th International Conference On Ultimate Integration On Silicon	4	Udine (Italy), March 12-14 2008	Poster	Done
Fully self-consistent k p solver and Monte Carlo simulator for hole inversion layers	L.Donetti, F.Gamiz, A.Godoy, N.Rodriguez	UGR, INPG	ESSDERC-2008, European Solid State Device Research Conference	4	Edinburgh (UK), September 15-19	Oral	Done
Simulation of CMOS inverters based on the novel Surrounding Gate Transistors. A Verilog-A implementation	A.Roldán, J.B.Roldán, F.Gamiz	UGR	MOS-AK Workshop	4	Edinburgh (UK), September 19	Poster	Done
A Revisited Pseudo-MOSFET Model for Ultrathin SOI Films	N.Rodriguez, S.Cristoloveanu, F.Gamiz	UGR, INPG	2008 IEEE International SOI Conference	4	New Palz, NY (USA), October 6-9	Poster	Done
Gd silicate: A High-k Dielectric Compatible with High Temperature Annealing,	H.D.B. Gottlob, M. Schmidt, M.C. Lemme, H. Kurz, I.Z. Mitrovic, M. Werner, W.M. Davey, S. Hall, P.R. Chalker, K. Cherkaoui, P.K. Hurley, B. Raeissi, O. Engström, and S.B. Newcomb	AMO, Liverpool, Tyndall, Chalmers	Workshop on Dielectrics in Microelectronics (WoDiM 2008)	1.3	June 23 – 25, 2008 in Bad Saarow (Berlin), Germany	Oral	Done
A generalized methodology for oxide leakage current metric,	O. Engström, J. Piscator, B. Raeissi, P. K. Hurley, K. Charkaoui, S,Hall, M.C.Lemme and H.D.B. Gottlob	Chalmers, Tyndall, Liverpool, AMO	Ultimate Integration on Silicon Conference (ULIS08),	1.3	March 2008, Udine	Poster	Done
Comprehensive study of	M. Kaczmarczyk, O. Engström, J.	ITE, Chalmers	9th Exmatec,	2.4	June 2008, Lodz	Poster	Done

InAs/GaAs quantum dots by means of complementary methods	Piscator, M. Kaniewska, B. Surma, S. Lin and A. R. Peaker,						
Method for identifying confined electron states in quantum dot structures	M. Kaczmarczyk, O. Engström and M. Kaniewska	ITE, Chalmers	9th Exmatec	2.4	June 2008, Lodz	Poster	Done
Metastable behaviorof 1 eV trap in InAs/GaAs quantum dot structures	G. Zaremba, O. Engström, M. Kaniewska and M. Kaczmarczyk	ITE, Chalmers	9th Exmatec,	2.4	June, 2008, Lodz	Poster	Done
Characterization of deep elvels and quantum confined energy levels in InAs/ GaAs quantum dot structures by electrical methods	M. Kaniewska, O. Engström, M. Kaczmarczyk and G. Zaremba	ITE, Chalmers	ICCE 16, Kunming, China	2.4	July 2008	Oral	Done
Deep level transient spectroscopy in quantum dot characterization,	O. Engström and M. Kaniewska	Chalmers, ITE	Villa Conference on Interaction among Nanostructures	2.4	February 2008, Orlando, Florida	Oral	Done
Multiphonon capture of electrons at high-k-silicon interfaces	O. Engström, B. Raeissi and J. Piscator	Chalmers	Gordon Conference	1.3	August,2008 New London, New Hampshire	Poster	Done
Electron traps at HfO_2/SiO_x interfaces	B. Raeissi, Y. Y. Chen, J. Piscator, Z. H. Lai and O. Engström	Chalmers	ESSDERC 2008	1.3	September 2008, Edinburgh	Oral	Done
Future high-k gate stack materials	O. Engström	Chalmers	Tutorial given at ESSDERC 08.	1.3	September 2008, Edinburgh	Invited	Done
High-k dielectrics and metal gates	O. Engström	Chalmers	MIGAS'08,	1.3	July, 2008, Autrans, France	Invited	Done
Small slope switches	A.M. Ionescu	EPFL	Nanosil workshop @ ESDERC 2008	2.3	September 18th, Edinburg	oral	done
Determination of Physical Parameters for HfO2/SiOx/TiN MOSFET Gate Stacks by Electrical Characterization and Reverse Modeling	S. Monaghan, P. K. Hurley, K. Cherkaoui, M. A. Negara, and A. Schenk	ETHZ, Tyndall	ULIS'2008	1, 2, 4	Udine, Italy, 12 - 14 March 2008	oral	done
Advanced simulation of statistical	A. Asenov, S. Roy, A. R. Brown, G. Roy, C.	GU	IEDM	4	15 Dec San Francisco	Invited	done

variability and reliability in nano CMOS transistors	Alexander, C. Riddet, C. Millar, B. Cheng, A. Martinez, N. Seoane, D. Reid, M. F. Bukhori, X. Wang, U. Kovac						
Fabrication and characterisation of strained Si heterojunction bipolar transistors on virtual substrates	S. Persson, M. Fjer, E. Escobedo-Cousin, G. Malm, Y.-B. Wang, P.-E. Hellström, M. Östling, E. Parker, S.H. Olsen and A.G. O'Neill	UNEW, KTH, Warwick	IEDM	1, 4	Dec 08, San Francisco		done
Piezomobility Description of Strain-Induced Mobility	A. O'Neill, Y. L. Tsang, B. J. Gallacher, S.H. Olsen	UNEW	ICSICT	1, 4	Oct 08, Beijing	Invited paper	done
Strain engineering for high mobility channels	S Olsen, ZA Tarawneh, J Varzgar, E Escobedo-Cousin, R Agaiby, P Dobrosz, A O'Neill, P-E Hellström, M Östling, E Parker, R Loo and C Claeys	UNEW, KTH, Warwick, IMEC	ICST	1, 4	March 08, Shanghai	Invited paper	done
Nanoscale strain characterisation for ultimate CMOS and post-CMOS devices	SH Olsen, P Dobrosz, RMB Agaiby, YL Tsang, O Alatise, SJ Bull, AG O'Neill, KE Moselund, AM Ionescu, P Majhi, D Buca, S Mantl and H Coulson	UNEW, EPFL, FZJ	EMRS	4	May 08, Strasbourg	Invited paper	done
Gate leakage in high mobility substrates: correlating macroscopic leakage with nanoscale measurements	SH Olsen et al	UNEW, IMEC	MRS Spring Meeting	4	April 09, San Francisco	Invited paper	
Nanoscale strain characterisation in patterned SSOI structures	P Dobrosz, SH Olsen, SJ Bull, YL Tsang, RMB Agaiby, AG O'Neill, D Buca, S Mantl, B Ghyselen	UNEW, FZJ,	EMRS	4	May 08, Strasbourg		done
Nanometer scale strain profiling through Si/SiGe heterolayers	RMB Agaiby, SH Olsen, P Dobrosz, H Coulson, SJ Bull and AG O'Neill	UNEW	EMC	4	June 08, Santa Barbara		done
Improved analog performance of strained Si n-MOSFETs on thin SiGe	O Alatise, KSK Kwa, S Olsen and A O'Neill	UNEW	ESSDERC	1, 4	Sept 08, Edinburgh		done

strain relaxed buffers							
Investigation of strain profile optimization in gate-all-around suspended silicon nanowire FET	M Najmzadeh, K Moselund, A Ionescu, P Dobrosz, S Olsen and A O'Neill	EPFL, UNEW	ESSDERC	1, 2, 4	Sept 08, Edinburgh		done
Top down and Bottom-up routes to nanoscale electronic components	A Houlton, BR Horrocks, NG Wright, S Olsen and A O'Neill	UNEW	Intel European Research and Innovation Conference		Sept 08, Dublin	Invited paper	done
Source-drain Engineering for Channel-limited PMOS Device Performance: Advances in Understanding of Amor-phization-Based Implant Techniques	NEB Cowern	UNEW	MRS Spring Meeting		April 08, San Francisco	Invited paper	done
Schottky source-drain contacts	E. Dubois	IEMN-ISEN	MIGAS'08,	1	International Summer School on Advanced Microelectronics, 28.06 – 4.07. 2008	Invited	done

Appendix 1.

Summary on the "screening of national projects of relevance" *(as at the beginning of 2008)***.**

UK 17 projects

Project title	**Renaissance Ge**
Acronym/number	
Duration (from-to)	May 2008 to Oct 2011
Participants (inside NANOSIL)	Warwick, Glasgow, IMEC
Participants (beyond NANOSIL)	Sheffield
Coordinator (with contact details)	Dr David Leadley, Dept. of Physics, University of Warwick, Coventry CV4 7AL, UK d.r.leadley@warwick.ac.uk
Funding source	EPSRC (UK Research Council)
Indicative budget	2.5 million GBP

Project title	**On-chip millikelvin electronic refrigerator for astronomical and quantum device applications**
Acronym/number	Cooltronics
Duration (from-to)	Oct 2008 to Oct 2012
Participants (inside NANOSIL)	Warwick
Participants (beyond NANOSIL)	VTT, Helsinki University of Technology, University of Leicester, Royal Holloway University of London, University of Cardiff
Coordinator (with contact details)	Dr David Leadley, Dept. of Physics, University of Warwick, Coventry CV4 7AL, UK d.r.leadley@warwick.ac.uk
Funding source	EPSRC (UK Research Council)
Indicative budget	2.8 million GBP

Project title	**Feasibility of Novel Deca-Nanometer Vertical MOSFETs for Low-cost Radio Frequency Circuit Application**
Acronym/number	EP/C515803/1
Duration (from-to)	January 2007 December 2010
Participants (inside NANOSIL)	LIVUNI
Participants (beyond NANOSIL)	University of Southampton
Coordinator (with contact details)	S.Hall
Funding source	Engineering & Physical Sciences Research Council
Indicative budget	£640k

Project title	**A Biologically Plausible Spiking Neuron in Hardware**
Acronym/number	EP/F05551X/1
Duration (from-to)	September 2008 August 2011
Participants (inside NANOSIL)	LIVUNI
Participants (beyond NANOSIL)	University of Ulster
Coordinator (with contact details)	S.Hall
Funding source	Engineering & Physical Sciences Research Council
Indicative budget	£435k

Project title	Performance, degradation and defect structure of MOS devices using high-k materials as gate dielectrics
Acronym/number	EP/C003071/1
Duration (from-to)	August 2005 July 2008
Participants (inside NANOSIL)	LIVUNI, IMEC, Tyndall
Participants (beyond NANOSIL)	University of Manchester, Liverpool John Moores University
Coordinator (with contact details)	S.Hall
Funding source	Engineering & Physical Sciences Research Council
Indicative budget	£195k

Project title	Precision Passive Component Design & Manufacture in Micro-Module Electronics: PPM2
Acronym/number	TP/8/ADM/6/I/Q2030K
Duration (from-to)	June 2008 May 20011
Participants (inside NANOSIL)	LIVUNI
Participants (beyond NANOSIL)	TWI, Zarlink Semiconductor, University of Leeds, JLS Designs Ltd, Qudos Technology, Flomerics
Coordinator (with contact details)	David Pedder, TWI
Funding source	Engineering & Physical Sciences Research Council / Technology Strategy Board
Indicative budget	£350k

Project title	**PLATFORM GRANT Strained Si/SiGe: Materials, Technology and Design**
Acronym/number	EP/D036682
Duration (from-to)	2005-2010
Participants (inside NANOSIL)	NEWCASTLE UNIVERSITY
Participants (beyond NANOSIL)	
Coordinator (with contact details)	ANTHONY O'NEILL , anthony.oneill@ncl.ac.uk, tel: +44 (0)191 222 7328
Funding source	EPSRC
Indicative budget	

Project title	**Nanometre Strain Evaluation for Future and Emerging Technologies**
Acronym/number	EP/D06113X
Duration (from-to)	2006-2008
Participants (inside NANOSIL)	NEWCASTLE UNIVERSITY
Participants (beyond NANOSIL)	
Coordinator (with contact details)	S. OLSEN , sarah.olsen@ncl.ac.uk, tel: +44 (0)191 222 8552
Funding source	EPSRC
Indicative budget	

Project title	**Nanoscale Strain Measurements and Modeling of Short Channel Planar and Non Planar Devices**
Acronym/number	FEPI004
Duration (from-to)	2008-2009
Participants (inside NANOSIL)	NEWCASTLE UNIVERSITY
Participants (beyond NANOSIL)	
Coordinator (with contact details)	S. OLSEN , sarah.olsen@ncl.ac.uk, tel: +44 (0)191 222 8552
Funding source	SEMATECH
Indicative budget	

Project title	**Strained Si Tip Enhanced Raman Spectroscopy**
Acronym/number	
Duration (from-to)	2007-2009
Participants (inside NANOSIL)	NEWCASTLE UNIVERSITY
Participants (beyond NANOSIL)	
Coordinator (with contact details)	S. OLSEN , sarah.olsen@ncl.ac.uk, tel: +44 (0)191 222 8552
Funding source	HORIBA JOBIN YVON; Scanwel
Indicative budget	

Project title	**Nanoelectronics Laboratory**
Acronym/number	
Duration (from-to)	2007-2009
Participants (inside NANOSIL)	NEWCASTLE UNIVERSITY
Participants (beyond NANOSIL)	Cenamps
Coordinator (with contact details)	ANTHONY O'NEILL , anthony.oneill@ncl.ac.uk, tel: +44 (0)191 222 7328

Funding source	Cenamps
Indicative budget	

Project title	**Nanoelectronics Characterisation**
Acronym/number	
Duration (from-to)	2007
Participants (inside NANOSIL)	NEWCASTLE UNIVERSITY
Participants (beyond NANOSIL)	
Coordinator (with contact details)	ANTHONY O'NEILL , anthony.oneill@ncl.ac.uk, tel: +44 (0)191 222 7328
Funding source	One North East
Indicative budget	

Project title	**Physical Electronics**
Acronym/number	
Duration (from-to)	2006-2008
Participants (inside NANOSIL)	NEWCASTLE UNIVERSITY
Participants (beyond NANOSIL)	
Coordinator (with contact details)	ANTHONY O'NEILL , anthony.oneill@ncl.ac.uk, tel: +44 (0)191 222 7328
Funding source	SRIF3
Indicative budget	

TOTAL BUDGET UNEW = £4.752M

Project title	**Novel Time-Resolved Thermal Imaging: AlGaN/GaN**
Acronym/number	EP/D04698X/1
Duration (from-to)	04/06 04/10
Participants (inside NANOSIL)	GU
Participants (beyond NANOSIL)	Quinetic, University of Bristol
Coordinator (with contact details)	A. Asenov
Funding source	EPSRC
Indicative budget	€111,029

Project title	**Meeting the Design Challenges of the Nano-CMOS electronics**
Acronym/number	EP/E003125/1
Duration (from-to)	10/06 09/10
Participants (inside NANOSIL)	GU, Synopsys
Participants (beyond NANOSIL)	ARM, Fujitsu, National semiconductors, Freescale
Coordinator (with contact details)	A. Asenov

Funding source	EPSRC
Indicative budget	€2,560,000

Project title	**III-V MOSFETs for ultimate CMOS**
Acronym/number	EP/F002610/1
Duration (from-to)	05/07 04/10
Participants (inside NANOSIL)	GU
Participants (beyond NANOSIL)	Freescale
Coordinator (with contact details)	A. Asenov
Funding source	EPSRC
Indicative budget	€455,000

Project title	**Atomic Scale Simulation of Nanoelectronics Devices**
Acronym/number	GR/E038344/1
Duration (from-to)	10/07 10/12
Participants (inside NANOSIL)	GU, Synopsis
Participants (beyond NANOSIL)	
Coordinator (with contact details)	A. Asenov
Funding source	EPSRC
Indicative budget	€1,583,931

IRELAND 4 projects

Project title	**Semiconductor & Molecular Wire Simulation for Technology Design**
Acronym/number	
Duration (from-to)	2007-2010
Participants (inside NANOSIL)	Tyndall
Participants (beyond NANOSIL)	
Coordinator (with contact details)	Jim Greer jim.greer@tyndall.ie
Funding source	Science Foundation Ireland
Indicative budget	

Project title	**Functional Oxides and Related Materials for Electronics**
Acronym/number	FORME
Duration (from-to)	2007-2011
Participants (inside NANOSIL)	Tyndall
Participants (beyond NANOSIL)	
Coordinator (with contact details	Martyn Pemble martyn.pemble@tyndall.ie
Funding source	Science Foundation Ireland
Indicative budget	

Project title	**Advanced Scalable Silicon-on-Insulator Devices for "Beyond-End-of-Roadmap" Semiconductor Technology**
Acronym/number	
Duration (from-to)	2006-2010
Participants (inside NANOSIL)	Tyndall
Participants (beyond NANOSIL)	
Coordinator (with contact details	JP Colinge jean-pierre.colinge@tyndall.ie
Funding source	Science Foundation Ireland
Indicative budget	

Project title	**High dielectric constant materials for future ICT**
Acronym/number	
Duration (from-to)	2005-2009
Participants (inside NANOSIL)	Tyndall
Participants (beyond NANOSIL)	Dublin City University and Trinity College Dublin
Coordinator (with contact details)	Paul Hurley paul.hurley@tyndall.ie
Funding source	Science Foundation Ireland
Indicative budget	

SWITZERLAND 1 project

Project title	**Improvement of Dopant Diffusion and Activation Models in Strained Silicon by Ab Initio Simulations on the Atomic Scale**
Acronym/number	ATOMDIFF
Duration (from-to)	May 06 - April 09
Participants (inside NANOSIL)	ETHZ, SNPS
Participants (beyond NANOSIL)	
Coordinator (with contact details)	Prof. W. Fichtner (fw@iis.ee.ethz.ch)
Funding source	Swiss Commission for Technology and Innovation
Indicative budget	1374911 CHF

SPAIN 8 projects

Project title	**Techniques of characterization and modeling of nanoscale MOSFETs in RF and microwave applications**
Acronym/number	TEC2005-06297/MIC
Duration (from-to)	01/01/2006-31/12/2008
Participants (inside NANOSIL)	URV
Participants (beyond NANOSIL)	
Coordinator (with contact details)	Antonio Lázaro, URV, Tel: +629024907, E-mail: antonioramon.lazaro@urv.cat
Funding source	Spanish Ministry of Science
Indicative budget	120000 Euro

Project title	**Characterization and modeling of nanoscale MOSFETs**
Acronym/number	
Duration (from-to)	01/01/2004-30/09/2008
Participants (inside NANOSIL)	URV
Participants (beyond NANOSIL)	
Coordinator (with contact details)	Benjamin Iñiguez, URV, Tel: +34977558521
Funding source	Catalan Government
Indicative budget	140000 Euro

Project title	**Characterization and modeling of nanoscale Ultrathin Body (UTB) SOI MOSFETs valid for DC y RF analysis**
Acronym/number	
Duration (from-to)	01/01/2008-31/12/2009
Participants (inside NANOSIL)	URV
Participants (beyond NANOSIL)	Université de Montpellier 2 (France)
Coordinator (with contact details)	Benjamin Iñiguez, Tel: +34977558521
Funding source	Spanish Ministry of Science / French Ministry of Science
Indicative budget	22000 Euro

Project title	**Development of a platform for the study of the viability of SOI technology in Information and Communication applications.**
Acronym/number	P05-TIC-0831/P06-TIC-1899
Duration (from-to)	01-04-2006/30-03-2010
Participants (inside NANOSIL)	UGR, IMEP(FR), CEA-LETI(FR)
Participants (beyond NANOSIL)	Universidad Autonoma Barcelona (ES), Universidad Santiago Compostela (ES)
Coordinator (with contact details)	Francisco Gamiz, fgamiz@ugr.es
Funding source	Junta de Andalucia
Indicative budget	236000 €

Project title	**Study of the electron transport in semiconductor inversion layers. Desing of nanoelectrónico devices for very high frecuency applications FIS 2005-6832.**
Acronym/number	FIS 2005-6832
Duration (from-to)	01-01-2005/31-12-2008
Participants (inside NANOSIL)	UGR
Participants (beyond NANOSIL)	
Coordinator (with contact details)	Andres Godoy, agodoy@ugr.es
Funding source	Spanish Goverment
Indicative budget	32000 €

Project title	**Development of SPICE models and circuit simulation in emerging technologies (strained silicon, SiGe, SOI, GeOI)**
Acronym/number	TEC 2005-1948
Duration (from-to)	01-01-2005/31-12-2008
Participants (inside NANOSIL)	UGR
Participants (beyond NANOSIL)	
Coordinator (with contact details)	Juan Roldán, jroldan@ugr.es
Funding source	Spanish Goverment
Indicative budget	43900 €

Project title	**Characterization, simulation and modelling of ultimate CMOS nanotransistors for RF and UWB applications**
Acronym/number	MAGNUM-1
Duration (from-to)	01-01-2009/31-12-2011
Participants (inside NANOSIL)	UGR, URV
Participants (beyond NANOSIL)	University of Vigo
Coordinator (with contact details)	Francisco Gamiz, fgamiz@ugr.es
Funding source	Spanish Government
Indicative budget	368000 €

Project title	**Laboratory for Nanoelectronics**
Acronym/number	NANOLAB
Duration (from-to)	01-01-2008/31-12-2009
Participants (inside NANOSIL)	UGR
Participants (beyond NANOSIL)	
Coordinator (with contact details)	Francisco Gamiz, fgamiz@ugr.es
Funding source	Spanish Government
Indicative budget	1414000 €

GERMANY 7 projects

Project title	**Investigation of Silicon-Nanowire-MOSFETs (accepted)**
Acronym/number	Ku 540/51-1
Duration (from-to)	07/2008 – 06/2011
Participants (inside NANOSIL)	AMICA AMO-GmbH
Participants (beyond NANOSIL)	Technical University Ilmenau
Coordinator (with contact details)	Prof. Dr. Heinrich Kurz and Dr. Bernd Spangenberg, IHT, RWTH Aachen
Funding source	Deutsche Forschungsgemeinschaft (DFG)
Indicative budget	230 k€

Project title	**Silicon-based photonic devices for telecommunication and optical interconnect applications: Development of lasers and electro-optical modulators fabricated on SOI platform (submitted)**
Acronym/number	01BL0800, MISTRAL
Duration (from-to)	10/008– 092011
Participants (inside NANOSIL)	AMICA AMO-GmbH
Participants (beyond NANOSIL)	University Karlsruhe, Leibniz University Hannover, University Heidelberg, Coreoptics GmbH, IBM Deutschland Entwicklung GmbH
Coordinator (with contact details)	Prof. Dr. Heinrich Kurz and Dr. Michael Först, IHT, RWTH Aachen
Funding source	Deutsches Zentrum für Luft- und Raumfahrt e.V. (DLR - BMBF)
Indicative budget	410 k€

Project title	**Silicon-based thin film materials for future solar cells, (submitted)**
Acronym/number	GIN-SF-109, SINOVA
Duration (from-to)	10/2008 – 09/2011
Participants (inside NANOSIL)	
Participants (beyond NANOSIL)	HMI-Berlin, IZM-Halle University, IFTO-Jena University, Joint Laboratory Institut für innovative Mikroelektronik (IHP) Frankfurt (Oder) and BTU-Cottbus, FZ-Juelich (IEF-5 and ER-C) and GfE RWTH Aachen
Coordinator (with contact details)	Prof. Dr. Heinrich Kurz and Dr. Bernd Spangenberg, IHT, RWTH Aachen
Funding source	BMBF-PTJ-Juelich
Indicative budget	423 k€

Project title	**Alternative Werkstoffe für die Nanoelektronik: Graphen**
Acronym/number	ALEGRA
Duration (from-to)	01.11.2006 – 31.12.2010
Participants (inside NANOSIL)	AMO

Participants (beyond NANOSIL)	-
Coordinator (with contact details)	AMO, (contact: Prof. Dr. Heinrich Kurz, kurz@amo.de, +49 241-8867-200)
Funding source	BMBF
Indicative budget	1.7 Mio€

Project title	**Metall-Gate-Elektroden und epitaktische Oxide als Gate-Stacks für zukünftige CMOS-Logik- und Speichergenerationen**
Acronym/number	MEGAEPOS
Duration (from-to)	01.03.2007 bis 28.02.2010
Participants (inside NANOSIL)	AMO
Participants (beyond NANOSIL)	Advanced Micro Devices (AMD) Fab 36 LLC & Co KG, NaMLab gGmbH, Paul-Drude-Institut für Festkörperelektronik, Technische Universität Darmstadt, Leibniz Universität Hannover, Innovations for High Performance Microelectronics (IHP) GmbH
Coordinator (with contact details)	AMO, (contact: Dr. Heinrich Gottlob, gottlob@amo.de, +49 241-8867-223)
Funding source	BMBF
Indicative budget	5.5 Mio€

Project title	**Device & Circuit performance boosted through silicon material fabrication**
Acronym/number	DECISIF 2T104 (Medea Project)
Duration (from-to)	01.06.2008 – 31.05.2011
Participants (inside NANOSIL)	FZJ
Participants (beyond NANOSIL)	AMD, Siltronic, Aixtron, STM, Soitec, LETI, MPI Halle
Coordinator (with contact details)	Gilles Thomas (STM); national coordinator: Siegfried Mantl
Funding source	BMBF
Indicative budget	

Project title	**Positioning of single nanostructures - Single quantum devices**
Acronym/number	FOR730
Duration (from-to)	04.2006 to 04.2009
Participants (inside NANOSIL)	Universitaet Stuttgart (USTUTT)
Participants (beyond NANOSIL)	Max-Planck Institut für Festkörperforschung, Stuttgart
Coordinator (with contact details)	Prof. Dr. Peter Michler (Universität Stuttgart) E-mail: p.michler@ihfg.uni-stuttgart.de
Funding source	Deutsche Forschungsgesellschaft (DFG)
Indicative budget	

FRANCE 16 projects

Project title	**Pompe à électrons silicium intégrée**
Acronym/number	POESI
Duration (from-to)	2007-2009
Participants (inside NANOSIL)	X. Jehl, M. Sanquer, M. Vinet (partner 9)
Participants (beyond NANOSIL)	N. Feltin , L. Devoille (LNE, Trappes France)
Coordinator (with contact details)	Dr. X. Jehl LaTEQS CEA-Grenoble +33 4 38 78 90 45 email: xavier.jehl@cea.fr
Funding source	ANR P'NANO 2006
Indicative budget	Total budget (full cost) about 800keuros

Project title	**Modelling of Electron Devices in Nanometer Regime**
Acronym/number	MODERN
Duration (from-to)	December 2005 – November 2008
Participants (inside NANOSIL)	UPS (IEF), INPG (IMEP), CEA (LETI), STMicroelectronics
Participants (beyond NANOSIL)	IM2NP, INL
Coordinator (with contact details)	Philippe Dollfus (UPS-IEF) philippe.dollfus@ief.u-psud.fr +33 1 69 15 72 83
Funding source	Agence Nationale de la Recherche
Indicative budget	870 k€

Project title	**Carbon Nanotube-based nanodevices for multi-GHz applications**
Acronym/number	HF-CNT
Duration (from-to)	December 2005 – November 2008
Participants (inside NANOSIL)	UPS (IEF)
Participants (beyond NANOSIL)	CEA (LEM), IEMN, ENS (LPA)
Coordinator (with contact details)	Jean-Philippe Bourgoin CEA (LEM) jean-philippe.bourgoin@cea.fr +33 1 69 08 55 65
Funding source	Agence Nationale de la Recherche
Indicative budget	350 k€

Project title	**Multigate devices**
Acronym/number	MULTIGRILLE
Duration (from-to)	
Participants (inside NANOSIL)	IMEP-FMNT, LETI
Participants (beyond NANOSIL)	L2MP, ISEP, ECL
Coordinator (with contact details)	Olivier Rozeau, LETI, olivier.rozeau@cea.fr

Funding source	French ANR
Indicative budget	

Project title	**Quantum and atomistic modelling of nanodevices**
Acronym/number	QUANTAMONDE
Duration (from-to)	
Participants (inside NANOSIL)	IMEP-FMNT, CEA-INAC, IEMN, ST
Participants (beyond NANOSIL)	Néel Institute
Coordinator (with contact details	Marco Pala, IMEP, pala@minatec.inpg.fr
Funding source	French ANR
Indicative budget	

Project title	**Scanning gate microscopy for measurements of local electrical properties**
Acronym/number	MICATEC
Duration (from-to)	
Participants (inside NANOSIL)	IMEP-FMNT, IEMN
Participants (beyond NANOSIL)	Néel Institute
Coordinator (with contact details)	Serge Huant, Institut Néel, contact : pala@minatec.inpg.fr
Funding source	French ANR
Indicative budget	

Project title	**Graphene : from material to test devices**
Acronym/number	DISPOGRAPH
Duration (from-to)	
Participants (inside NANOSIL)	IMEP/LMGP-FMNT, CEA
Participants (beyond NANOSIL)	Néel Institute, LCMI
Coordinator (with contact details	Laurence Magaud, Institut Néel, contact : mouis@minatec.inpg.fr
Funding source	RTRA
Indicative budget	

Project title	**Top-down Nanowires**
Acronym/number	CORE
Duration (from-to)	
Participants (inside NANOSIL)	IMEP-FMNT, LETI
Participants (beyond NANOSIL)	
Coordinator (with contact detail)	Mireille Mouis, IMEP, mouis@minatec.inpg.fr
Funding source	RTRA
Indicative budget	

Project title	**Tunnel FETs**
Acronym/number	TunFET
Duration (from-to)	
Participants (inside NANOSIL)	IMEP-FMNT, LETI
Participants (beyond NANOSIL)	
Coordinator (with contact details)	Sorin Cristoloveanu, IMEP, sorin@minatec.inpg.fr
Funding source	RTRA
Indicative budget	

Project title	**Multi-scale Simulation of Carbon Nanotube Transistors**
Acronym/number	ACCENT
Duration (from-to)	January 2007 – December 2009
Participants (inside NANOSIL)	CEA (LETI), UPS (IEF)
Participants (beyond NANOSIL)	LPMCN, IMS, Silvaco
Coordinator (with contact details)	François Triozon (CEA-LETI) francois.triozon@cea.fr +33 4 38 78 18 48
Funding source	Agence Nationale de la Recherche
Indicative budget	550 k€

Project title	**Matériaux piézoELectriqUeS ultra-fins pour applicatioNs microsystèmEs**
Acronym/number	MELUSINE
Duration (from-to)	03/12/2007 – 02/12/2009
Participants (inside NANOSIL)	CEA-LETI; FEMTO-ST (UMR6174), IEMN
Participants (beyond NANOSIL)	LAAS (UPR8001) SPMS (UMR8580)
Coordinator (with contact details)	
Funding source	Agence Nationale de la Recherche
Indicative budget	101088 (IEMN)

Project title	**Propriétés électroniques d'assemblage auto-organisés à base de nanofils**
Acronym/number	PREAANS
Duration (from-to)	28/02/2007 – 30/03/2010
Participants (inside NANOSIL)	CEA STMicroelectronics, IEMN
Participants (beyond NANOSIL)	LTM - UMR5129, CEMES-UPR8011
Coordinator (with contact details)	
Funding source	Agence Nationale de la Recherche
Indicative budget	44523 (IEMN)

Project title	**Ingénierie quantique du transport électronique dans les hétérostructures de nitrures**
Acronym/number	TRANSNIT
Duration (from-to)	06/11/2006 – 05/11/2009
Participants (inside NANOSIL)	CEA, IEMN
Participants (beyond NANOSIL)	IEF- UMR8622, CRHEA- UPR010
Coordinator (with contact details)	
Funding source	Agence Nationale de la Recherche Blanc
Indicative budget	72838 (IEMN)

Project title	**Synthèse et caractérisation de nanofils**
Acronym/number	NANOFILOUS
Duration (from-to)	01/12/2005 – 30/11/2008
Participants (inside NANOSIL)	IEMN
Participants (beyond NANOSIL)	
Coordinator (with contact details)	
Funding source	Agence Nationale de la Recherche Jeune chercheur
Indicative budget	150000

Project title	**Développement d'une mémoire moléculaire compatible CMOS**
Acronym/number	MEMO
Duration (from-to)	01/12/2005 – 30/11/2008
Participants (inside NANOSIL)	CEA-Grenoble, CEA-Saclay, CEA-LETI, L2MP, STMicroelectronics, IEMN
Participants (beyond NANOSIL)	
Coordinator (with contact details)	
Funding source	Agence Nationale de la Recherche PNANO
Indicative budget	244400 (IEMN)

Project title	**Antimoine pour TBH THz optimisé pour une ElectroNique Analogique**
Acronym/number	ATTHENA
Duration (from-to)	01/12/2005 – 30/11/2008
Participants (inside NANOSIL)	IEMN
Participants (beyond NANOSIL)	Alcatel Thales III-V Lab, Picogiga international, Courtaboeuf, LPN-CNRS, Marcoussis, LPM-CNRS, Lyon, IRCOM-CNRS, Limoges,
Coordinator (with contact details)	
Funding source	Agence Nationale de la Recherche PNANO
Indicative budget	3120 (IEMN)

SWEDEN 1 project

Project title	**MC2SOI**
Acronym/number	MC2SOI
Duration (from-to)	January 2008 – December 2008
Participants (inside NANOSIL)	Olof Engström, Bahman Raeissi, Johan Piscator
Participants (beyond NANOSIL)	
Coordinator (with contact details)	Olof Engström
Funding source	Chalmers
Indicative budget	130 kEURO

BELGIUM 3 projects

Project title	**Multilayered thermo-chemically driven Nano-Electro-Mechanical Systems**
Acronym/number	ARC 05/10 – 330
Duration (from-to)	From October 2005 – October 2010
Participants (inside NANOSIL)	UCL
Participants (beyond NANOSIL)	none
Coordinator (with contact details)	UCL (jean-pierre.raskin@uclouvain.be)
Funding source	Communauté française de Belgique
Indicative budget	900 kEuros

Project title	**Design of a wideband detector for submillimeter-waves imagery**
Acronym/number	
Duration (from-to)	April 2005 – March 2009 (with possible prolongation for 1 year)
Participants (inside NANOSIL)	UCL
Participants (beyond NANOSIL)	VUB/LAMI, RUG/INTEC, IMEC, KUL/TELEMIC
Coordinator (with contact details)	UCL (jean-pierre.raskin@uclouvain.be)
Funding source	IWT (Flemish Governoment)
Indicative budget	369 kEuros

Project title	**Nano-Bio-ICT convergence**
Acronym/number	NANOTIC
Duration (from-to)	From November 2005 – October 2010
Participants (inside NANOSIL)	UCL
Participants (beyond NANOSIL)	none
Coordinator (with contact details)	UCL (denis.flandre@uclouvain.be)
Funding source	Région Wallonne Ministry, Belgium
Indicative budget	1750 kEuros

GREECE 1 project

Project title	**Micro- and Nanofabrication for elctronics and MEMS within AKMON**
Acronym/number	AKMON-IMEL
Duration (from-to)	1/3/2006-30/6/2008
Participants (inside NANOSIL)	IMEL/NCSR Demokritos
Participants (beyond NANOSIL)	
Coordinator (with contact details)	Androula G. Nassiopoulou, e-mail:A.Nassiopoulou@imel.demokritos.gr
Funding source	General Secretariat for Research and Technology-Greece
Indicative budget	580.000 Euros or IMEL

POLAND 3 projects

Project title	**Modeling of silicon structures with low-dimensional electron gas**
Acronym/number	N51504132/3248
Duration (from-to)	From 29.05.2007 to 28.05.2010
Participants (inside NANOSIL)	WUT
Participants (beyond NANOSIL)	
Coordinator (with contact details)	Jakub Walczak, WUT, j.walczak@imio.pw.edu.pl
Funding source	Polish Ministry of Science and Higher Education
Indicative budget	€100 000

Project title	**Modeling and characterization of multigate SOI MOS structures**
Acronym/number	N515 4449 33
Duration (from-to)	From July 1st, 2007 to June 30th 2009
Participants (inside NANOSIL)	WUT, ITE
Participants (beyond NANOSIL)	
Coordinator (with contact details)	Andrzej Jakubowski, WUT, a.jakubowski@imio.pw.edu.pl
Funding source	Polish Ministry of Science and Higher Education
Indicative budget	€180 000

Project title	**Charge pumping as a tool for characterization of electrophysical parameters of new generation MOS devices**
Acronym/number	
Duration (from-to)	From May 17th, 2005 to May 16th 2008
Participants (inside NANOSIL)	WUT
Participants (beyond NANOSIL)	
Coordinator (with contact details)	Lidia Łukasiak, WUT, l.lukasiak@imio.pw.edu.pl
Funding source	Polish Ministry of Science and Higher Education
Indicative budget	€120 000