Newsletter July 2012

Modeling CMOS devices

One of the main goals of the COSMIC project is the development of a device model for CMOS devices that must be able to predict the electrical characteristics of both p- and n-type

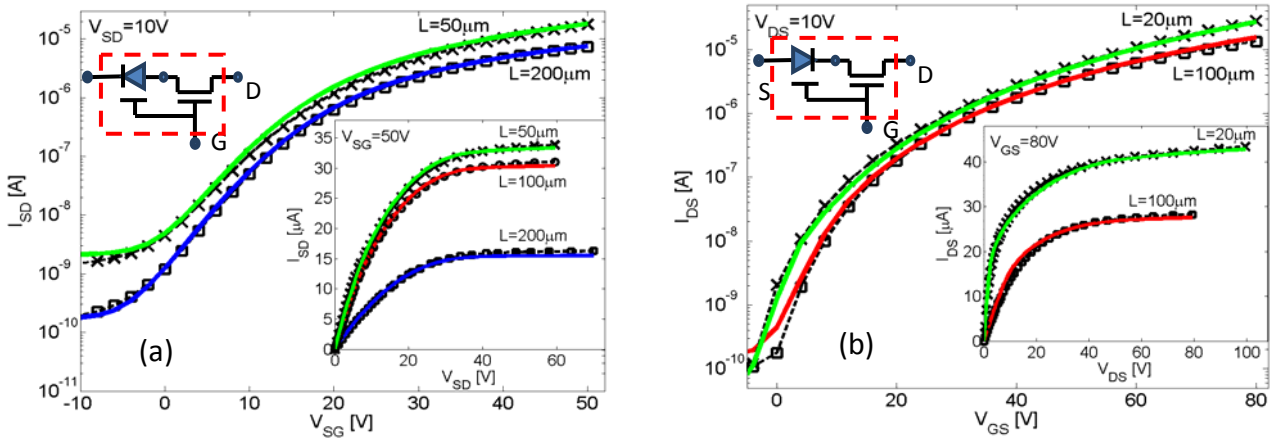


Fig. 1. Experimental (symbols) and simulated (lines) electrical characteristics of p- (a) and n-channel (b) printed staggered OTFTs with different channel lengths.

OTFTs as well as their scaling behaviour, allowing an accurate design of CMOS circuits. Starting from the experimental characteristics of devices made by CEA-LITEN (see newsletter 12/2011), CNR, TUE and ST-Microelectronics have developed a physically based analytical model able to accurately describe both n- and p-type staggered OTFTs. The measured electrical characteristics of high mobility staggered OTFTs are affected by contacts effects that become increasingly evident as the channel length is scaled down and as $|V_{ds}|$ is increased, whereas they are negligible in long channel devices (L>100μm). We found that the transistor current is mainly limited by the Schottky barrier at the source contact [1,2], which is reverse biased in the normal operating conditions, and the experimental characteristics are well reproduced considering barrier lowering induced by high electric field at the contact for high V_{ds}[1]. A detailed analysis performed by two dimensional numerical simulations [2], showed that the output characteristics of the staggered OTFTs are deeply affected by contact resistance at the source electrode up to a drain voltage, $V_{dsat}=(V_{gs}-V_T)$, when pinch-off occurs at the drain end of the channel and the transistor takes control of the current.Based on previous analysis, the electrical characteristics of the staggered OTFTs have been modelled as the series of an “ideal transistor” and a reverse biased Schottky diode (source contact region) (see insets in fig.1) [3]. The ideal transistor is modelled assuming a distribution of traps in the semiconductor. In the on-regime the drain current follows a power-law dependence on the gate voltage and it is modelled as suggested in [4], while in the subthreshold regime current increases exponentially with the gate voltage. The two regimes are combined according to the interpolation function presented in [5]. The parameters of the channel and the contact are extracted by considering the electrical characteristics of the

longest and shortest channel transistor, respectively. The model accurately fits the electrical characteristics of transistors with different channel widths and lengths with a single set of physical parameters (one for p-OTFTs and another for n-OTFTs) (fig,1).The model has been implemented in a circuit simulator.

1) A.Valletta et al., “Contact effects in high performance fully printed p-channel Organic Thin Film Transistors “, Appl. Phys. Lett. 99 (2011) 233309
2) M. Rapisarda et al., “Analysis of contact effects in fully printed p-channel Organic Thin Film Transistors”, Org. Electr. 2012 (accepted, DOI: 10.1016/j.orgel.2012.06.003
3) F. Torricelli et al. “Physically-based compact model of staggered p- and n-type Organic Thin-Film Transistors”, 8th International Thin-Film Transistors Conference, ITC2012 (30-31 Jan. 2012, Lisbon, Portugal).
4) E. Calvetti et al., Solid-State Electronics, **49**, 567 (2005).
5) O. Marinov, IEEE Trans. Electron Devices **56**, 2952 (2009).

For more information see
www.project-cosmic.eu

COSMIC Summerschool & Workshop 2012

The announced summer school had to be postponed. The new event date is 19./20. November 2012 in Munich at the Fraunhofer Institute EMFT.

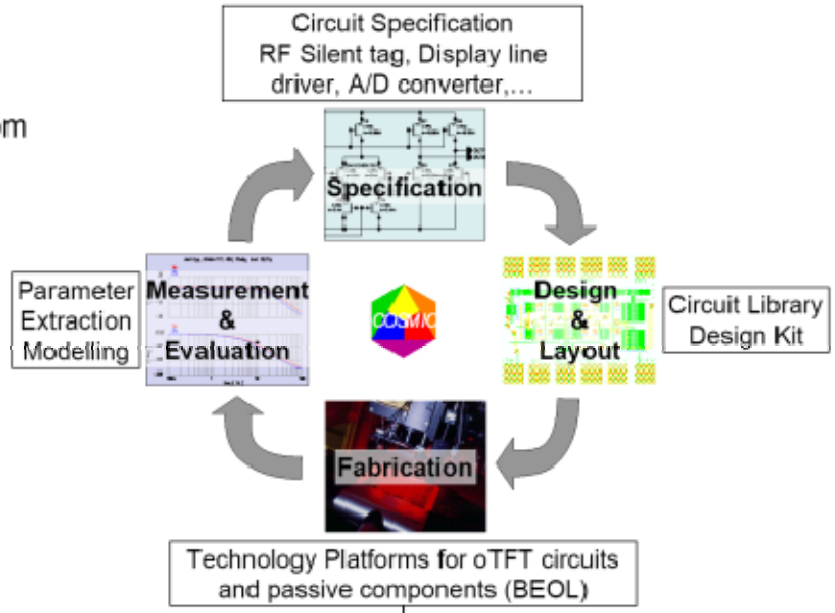
The event is a cooperation of 4 EU projects: Interflex, Polaric, Smart-EC and COSMIC. It will offer presentations with current processes in the field of printed electronics and targets engineers active in organic and large area electronics as well as students interested in this field.

Supporting EU projects:

SMART-EC **Interflex** COSMIC POLARIC

The collaborative project COSMIC

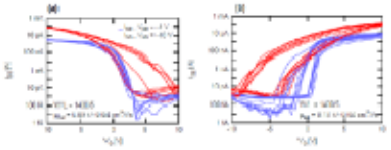
- generates a technology platform for organic electronics
- covers organic electronic applications from flexible complex, large-area to low-cost circuits
- targets complementary organic thin film transistor logic with p- and n-type oTFTs
- addresses the chain from design to manufacturing level
- optimizes process robustness to increase integration density
- sets up circuit modelling and design libraries
- includes digital and analog circuits as well as passive components
- will demonstrate technology with major lead applications



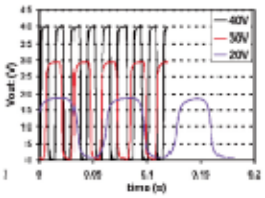
Foil on Carrier (W2W)
Ø150 mm foil on carrier
Clean room
Complex organic circuits

Sheet to Sheet (S2S)
320x380 mm sheets
Printing processes
Large area circuits

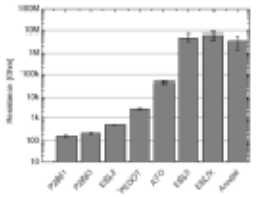
Roll to Roll (R2R)
210mm web
inline processes
Low-cost circuits



Statistics on p- and n-type oTFTs



Oscillation of ring oscillator with complementary inverters



Resistors printed with different carbon pastes

Project partners:
Fraunhofer EMFT (D)
CEA (F)
ST Microelectronics (I)
TNO (NL)
TU Eindhoven (NL)
IMEC (B)
Università di Catania (I)
CNR (I)
TU Berlin (D)
Friendly Technologies Ltd. (UK)
Flexink Ltd. (UK)
PolymerVision B.V. (NL)

Duration:
1.1.2010 - 31.12.2013

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