Recently developed n-type semiconductor and its availability in large quantities opens opportunities in organic electronics for a complementary logic that offers high process robustness and low power consumption. But integration of p- and n-type thin film transistors towards complex integrated organic circuits is challenges process technology because of the high requirements for a reproducible, stable and reliable fabrication process. Development of this fabrication has been started on transistor and simple device level with the target to get continuously improvements in device characteristics and reduce performance variation to a minimum.

After development of the device fabrication on transistor level COSMIC has now succeeded to show the next integration level with analog and digital circuits in complementary technology. TNO and IMEC showed working flip-flops circuits that can be used to build line driver applications for flexible or rollable display applications. These devices have been processed in carrier based approach for plastic film processing with transistors channel of few microns. These miniaturized patterns have been manufactured in a clean-room micro systems technology environment and can be further integrated to large and complex circuits.

Based on printed solutions, CEA-Liten has advanced its organic electronic technology towards complementary circuit integration with a very stable process flow. In meantime they reached the level of circuit building blocks for different application like RFId or A/D conversion. A highlighted development is a working 4 bit analog to digital converter with comparator, counter, and D/A converter. But also other applications will get possible on CEA's sheet-to-sheet printing technology platform PICTIC.

Fraunhofer EMFT has re-focused its roll-to-roll technology towards applications with a cost structure that are compliant with a low-cost large-volume application. For this the development targets on an RF system that facilitates a sensor readout by modulation of the carrier frequency.

Major facilitators of these developments are design, layout, characterization and modeling developed in collaboration between TU Eindhoven, University of Catania, CNR Rome and STMicroelectronics. Design has extensively worked in innovative circuit design of digital and analog building blocks, which are considering design solutions adapted to organic material limitations and processing variations. Modeling provided a thorough analysis of the contact effects in staggered and coplanar (W2W technology) OTFTs. From these experimental results new model parameters were extracted and included in the new design kit.

Reliability under bias stress has been extensively studied with oTFTs from CEA technology by CNR. The results are explained considering that the instability is related to the combination of two mechanisms: VT-variations by "mobile ion"-like mechanism and charge-trapping, showing different dependence on stress bias and temperature. From the temperature dependence self–heating plays a considerable role in determining the effects of bias stress.

In view of the planned demonstrators the industrial partners have worked out the system architecture for the planned circuits. To verify the correct functionality either of every lead application or of the mixed application, dedicate hardware platforms have been built that will allow to measure the electrical performance of the different lead applications and to reference them to conventional electronic solutions.

Overall the technological basis has improved so far that the development phase for circuit integration has reached an excellent basis to enable the ambitious applications selected for demonstration of the technology.

For more information see the project website www.project-cosmic.eu

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