Annex to Deliverable 2.2: Fabrication Process specification for Junctionless MOSFET.

JP Colinge, Tyndall national Institute – 24/11/2020

The following graphs describe the variation of threshold voltage, I_{on} and I_{off} in long-channel (n-channel) junctionless transistors as a function of silicon nanowire width and thickness.

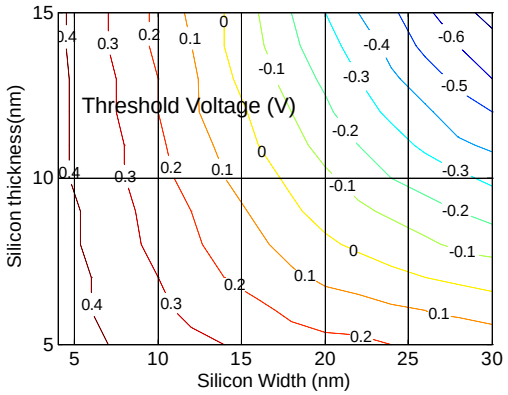
The threshold voltage is extracted from the maximum value of dg_m/dV_G plotted as a function of V_G using 2D simulations.
The I_{on} and I_{off} are expressed in arbitrary units (AU) because the channel length, the mobility and the drain voltage are not specified, but the I_{on}/I_{off} ratios are correct. I_{on} is defined at V_G=1V and I_{off} at V_G=0V.

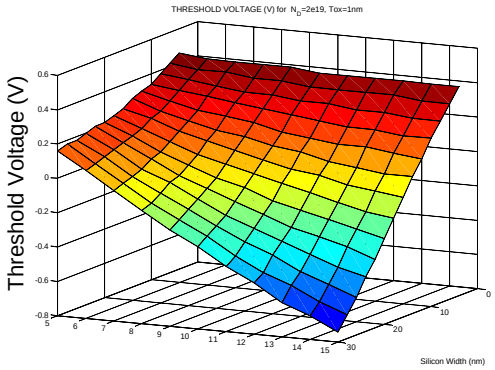
The gate material is a midgap metal ($E_{F\_metal}=E_{i\_silicon}$).

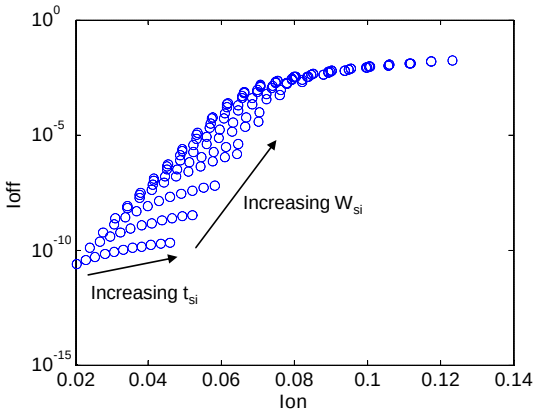
Four sets of graphs are presented, covering two channel doping concentrations and two equivalenyt oxide thickness (EOT) values.

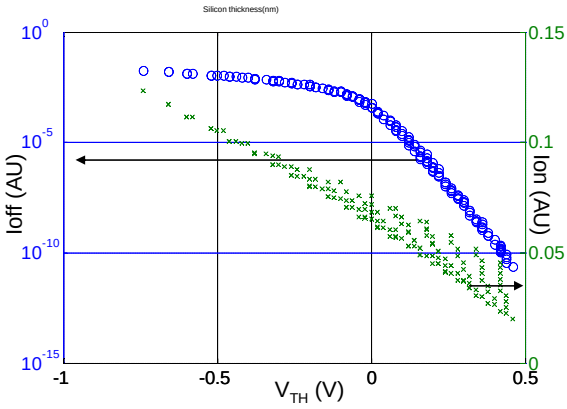
Ultimate Silicon Devices Group, Tyndall national Institute, Lee Maltings, Prospect Row, Cork, Ireland
Phone: +353 21 4904865; FAX: +353 21 4904297 e-mail: jean-pierre.colinge@tyndall.ie

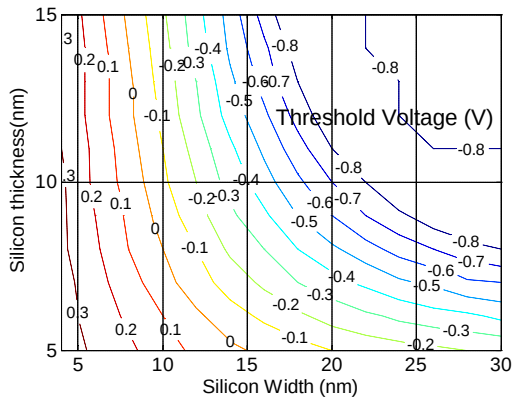
$N_D=1x10^{19}cm^{-3}$; EOT=1nm ; Midgap gate



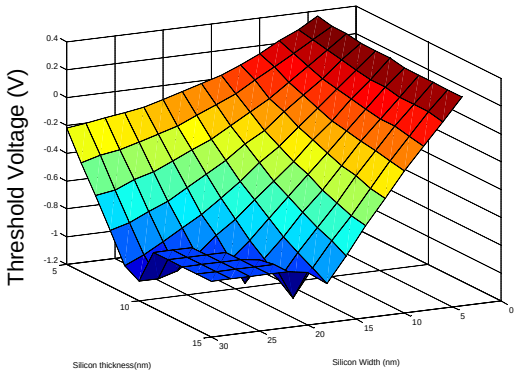


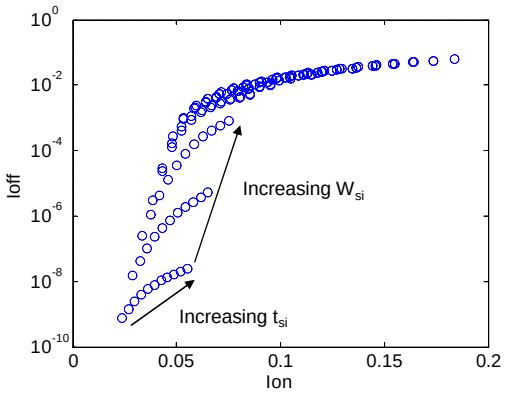


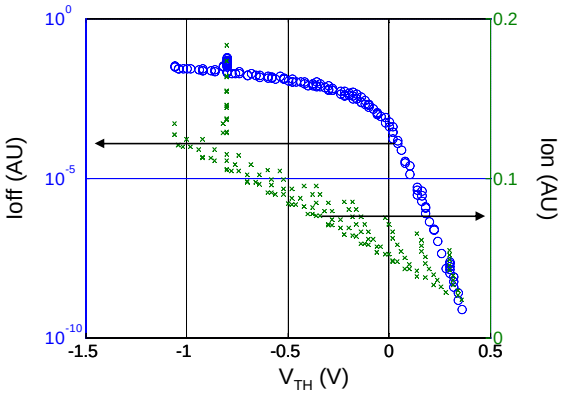




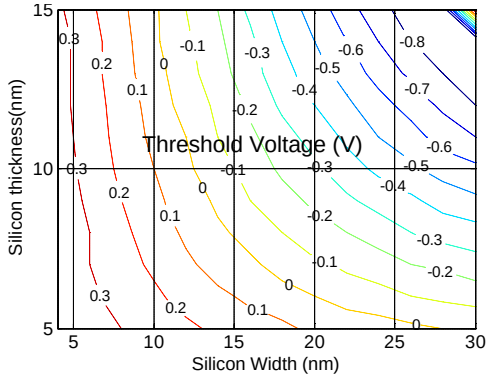
$N_D=2x10^{19}cm^{-3}$; EOT=1nm ; Midgap gate

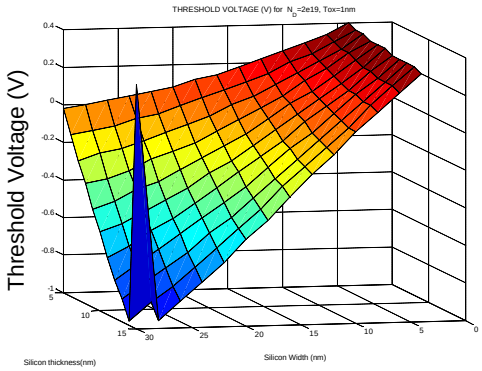


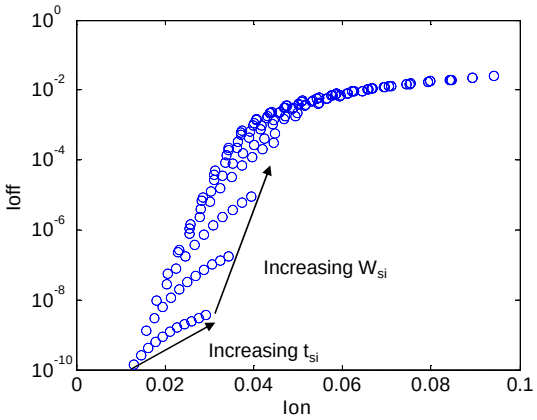


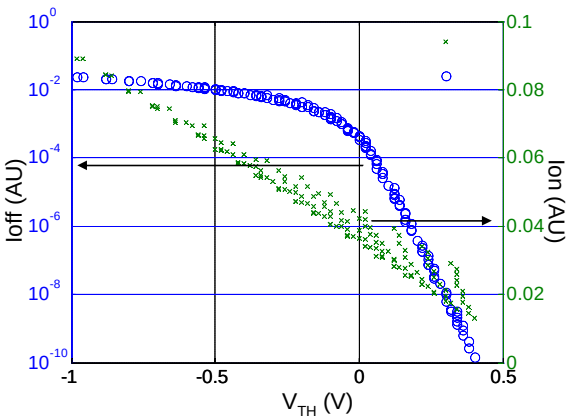


$N_D=1x10^{19}cm^{-3}$; EOT=2nm ; Midgap gate









$N_D=2x10^{19}cm^{-3}$; EOT=2nm ; Midgap gate