Deliverable 2.3: Process Specification for Variable Barrier Transistors

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Nanowire (NW) and Tri-gated Complementary Metal Oxide Semiconductor (CMOS) technology appear as an attractive option to overcome standard CMOS bulk technology limits in terms of scaling, performances and power consumption [1-3]. The electrostatic control over the channel is indeed improved in NWs, leading to a significant reduction of short channel effects [4] and thus leakage currents in the OFF state. Based on existing expertise in fabrication of FD-SOI nanowire devices, we will develop a fabrication route for n-channel and p-channel *Variable Barrier* nanowire transistor. We propose the fabrication of tri-gate nanowire transistors that include soft tunnel barriers which should strongly reduce source-to-drain tunneling and could even, in theory, achieve sub 60 mV/dec subthreshold slopes.

Existing mask set will be used, with the exception of the active area level which will have to be redrawn. The FD-SOI route will be adapted in order to target NW with width varying from $10nm \leq W \leq 20nm$, silicon thickness T_{SOI}=10nm and with a gate length $L_G < 30nm$.

I. INTRODUCTION

Steep subthreshold-slope or small subthreshold-swing devices are of great interest and significance in light of increasing subthreshold leakage current, which constitutes a major concern not only for power dissipation of digital integrated circuits but also for their energy efficiency. With the downscaling of MOSFETs devices, the phenomenon of subthreshold leakage becomes more significant because of short-channel effects and increasing parameter variations [5], as well as strong coupling between temperature and subthreshold leakage current [6]. In conventional MOSFET architectures, the lower limit for the subthreshold slope (*SS*) is $ln(10)\times kT/q$ or ≈60mV/dec at a temperature of 300K. Specifically, it is observed that most of CMOS-based transistors have subthreshold slope higher than 60mV/dec at room temperature for the shorter gate length. It is to note that among these MOSFET devices, the silicon nanowire field-effect transistor is one of the promising candidates for future ultra-scaled CMOS technology because it offers the best gate electrostatic control on short-channel-effects and then the lower subthreshold leakage current. Nevertheless, achieving steeper subthreshold slope transistors remains a key concern for further CMOS downscaling. Indeed, this increase in subthreshold swing as gate length is decreased marks a significant fundamental limitation of conventional FETs. Among the new generations of sub-kT/q transistors, Tunnel-FET devices appears as a promising device due to subthreshold swing smaller than 60 mV/dec and thus low OFF current [7-8]. However, it has also lower ON currents and higher threshold voltages compared with MOSFETs.

In this work, a new type of transistor is investigated. We propose the possibility of achieving sub-*kT/q* subthreshold slope by using a "boosted" CMOS transistor, modified to comprise tunnel barriers near the gate edges. The improvement in subthreshold slope results from a combination of relative motion between channel and tunnel barriers that modulates resonant tunneling states created by the longitudinal (transport direction) confinement in the different potential wells created between the different barriers.

The objective of this task (D2.3) is to propose an integration scheme for the fabrication of n-channel and p-channel *variable barrier transistors* on 300 mm wafers based on an adapted route from Tri-gated nanowire MOSFET devices developed at

CEA-Leti. The only difference being the formation of constrictions in the nanowire at the edges of the gate as illustrated in Fig. 1.

Existing mask sets will be used, with the exception of the active area level which will have to be redrawn. Particular emphasis will be placed on the control and reproducibility of the width of the nanowires as well as both constrictions.

II. OPERATING OF VARIABLE BARRIER TUNNELING TRANSISTOR: A THEORETICAL POINT OF VIEW

Recently, A. Afzalian *et al.* from Tyndall-UCC have demonstrated (using simulations) that the formation of soft tunnel barriers near the source/drain junctions can yield an improvement of subthreshold slope and even break the 60 mV/decade barrier [9-12]. This technique yields perfectly symmetrical MOS transistors.

This novel devices has been investigated using a fast coupled mode-space self-consistent 3D NEGF quantum simulator based on a effective mass Hamiltonian including a non-parabolic correction for the transport. A schematic representation of the simulated rectangular Gate-All-Around nanowire (with constrictions) is represented in Fig. 1.

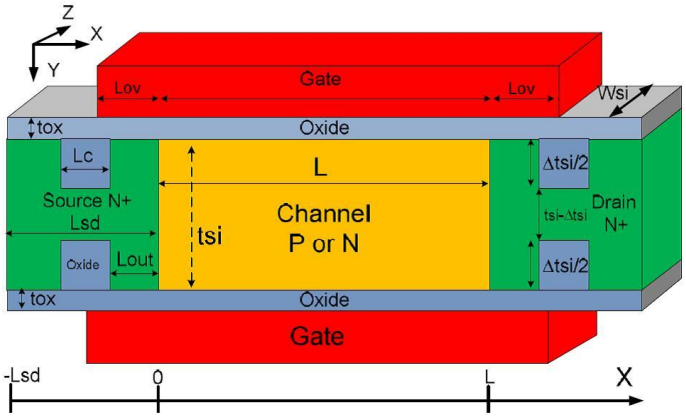


Figure 1: Rectangular GAA SOI nanowire with constrictions. T_{Si}=W=2nm, $L_{channel}$=10nm, L_{sd}=5nm. Data from Ref. [10].

In Fig. 2, the drain current and the s*ubthreshold slope (versus V_{GS})* of devices including tunnel barriers (TBs) with different parameters and different values of *Lout* and *Lov* are shown and compared to those of an identical classical "reference" nanowire transistor without barrier (Tref). Different regimes can be found:

1) The tunnel barrier transistor (TBT) characteristics are identical for a given V_{GS} range to those of Tref (*i.e.* for TBT with *Lout*=1nm and *Lov*=0 and V_{GS}<0.1V).

2) The TBT current is reduced and the *subthreshold slope* can be i) identical, ii) improved and below the *kT/q* limit of 60mV/dec, or iii) degraded. In Fig. 2.A, it is also shown the current ratio, *IR*, as a function of V_{GS} which is a convenient way to assess the impact of subthreshold slope variations on the current.

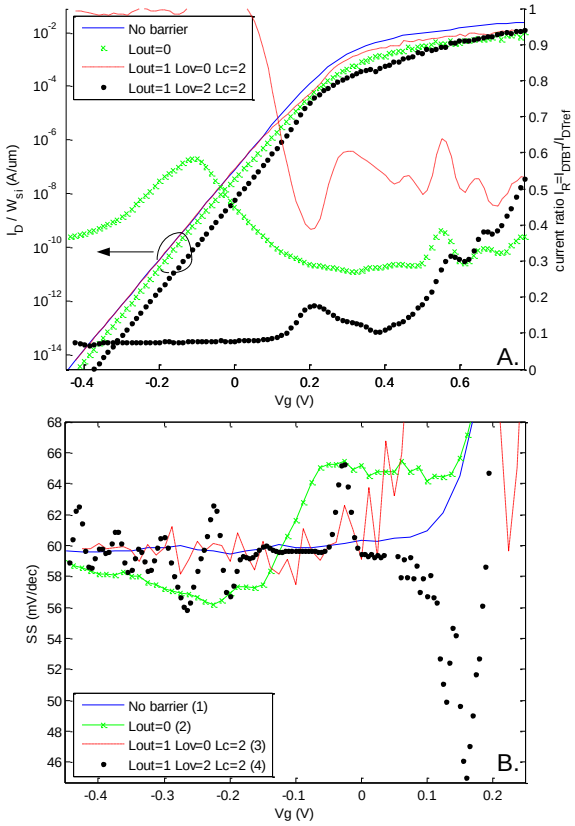


Figure 2: $I_{DS}(V_{GS})$ and $SS(V_{GS})$ curves of the nanowire without (1) and with constrictions with Lout=0, and Lc=1nm TB_S=0.26eV, TB_D=0.46eV (2), L_{out}=1nm, L_C=2nm, TB_S=0.2eV, TB_D=0.36eV L_{ov}=0 (3) and same as (3) but L_{ov}=2nm (4). Vd=1V. L=10nm. Data from Ref. [10]

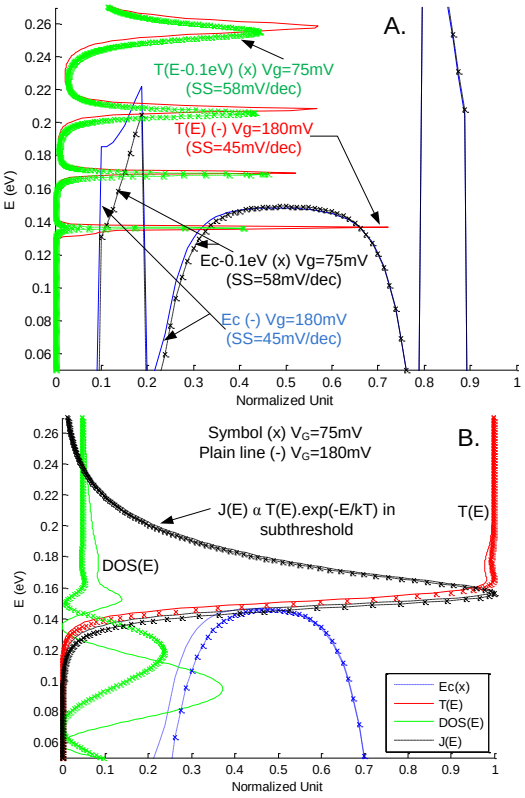


Figure 3: E_C vs. normalized x, and T (non normalized) vs. energy at V_{GS}=75 and 180mV (the curves for V_{GS}=75mV have been shifted down in energy by 102mV for comparison) for A) TBT with Lout=1 and Lov=2nm and B) Tref. In this case, the normalized spectral current density, J(E) is also shown. Data from Ref. [10]

Fig. 3.A shows the conduction band (E_C) and the transmission (T) of the TBT with *Lout*=1nm and *Lov*=2nm at V_{GS}=0.075V, where *SS* is 58mV/dec and at V_{GS}=0.18V where SS=45mV/dec (Fig. 2).

Fig. 3.B shows the same quantity for "standard" nanowire transistor (without barrier). The transmission of the device with constrictions is quite different from that without constrictions and shows very sharp peaks. This is the signature of resonant tunneling

states. When the height of the TBs become typically comparable to that of the channel barrier, they can induce resonant energy states in the quantum wells formed between tunnel-channel and/or tunnel-tunnel barriers. This decreases the current, compared to the reference transistor. In addition, it is explained in [10] that the TBs can locally move differently than the top of the channel barrier through 3D electrostatics effects at the gate edges and mixed influence between gate/source and gate/drain voltages (Fig. 3.A). A change in the relative shape of the wells with V_{GS} (*i.e.* a non translational invariant movement) can induce modifications in energy levels and their broadening (γ) which influence the density of state (DOS), transmission, current, and subthreshold slope. A reduction of *SS* below *kT/q* can be observed by this mean even if the transparency of the TBs decreases relatively compared to the channel barrier because the electron concentration is increasing faster than the Fermi-Dirac distribution of carriers with energy due to the strong non-linear change of DOS (and therefore transmission) with V_{GS}. As a result, one can achieve a lower tunneling probability when the device is turned off than when it is turned on. This increase of barrier transparency with gate voltage makes it possible to improve the subthreshold slope and even to drive it below 60 mV/decade.

This process modification (the local formation of local constrictions) can be applied to "regular" (i.e. *npn*) nanowire transistors. In the next section, the process specifications for variable barrier tunneling are described.

III. PROCESS SPECIFICATION FOR VARIABLE BARRIER TUNNELING TRANSISTOR

The main difference between conventional and variable barrier tunneling MOSFET transistors is the formation of constrictions at the edges of the gate.

III.1. NANOWIRE ELABORATION ON 300 MM WAFERS FROM DUV193NM LITHOGRAPHY

Silicon-on-Insulator (SOI) structures with silicon layers of 12 nm in thickness are used. The key for the fabrication of variable barrier tunneling MOSFET transistors is the formation and the control of both constrictions at the edges of the gate. The silicon layer will be patterned to create the silicon nanowires by a mesa isolation technique. The active stack used in this work will be consisted of a 10nm undoped Si, 2.5nm

SiO_2 dielectric layer and an organic bottom anti-reflective coating (BARC) layer of around 24nm patterned using 193nm ArF resist. The thickness of the photoresist is around 160nm. The active zone (i.e. nanowire feature) will be carried out using the trimmed resist/BARC as a mask. Obviously, the final linewidth of nanowires will be determined mainly by the amount of trimmed resist.

The good electrostatic control being based on low dimensions of nanowire width (or diameter), shorter wavelengths are required for lithography. As a result, an alternative method to *e-beam* lithography is proposed in this study to achieve sub-15nm nanowire width in order to lower the manufacturing cost and shorten the development time.
Today's most advanced lithography uses 193nm wave-length for the production of integrated circuits devices. Following the same philosophy than for the gate patterning, we proposed to develop an approach based on resist trimming by dry plasma etching to elaborate our silicon nanowires. This approach has the advantage of reducing the dimensions without increasing the complexity of the lithography requirements. A schematic of the process flow of this trimming method is summarized in Fig. 4.

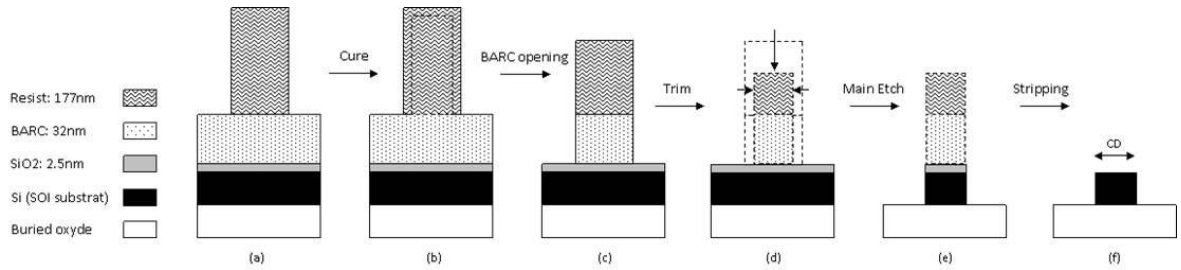


Figure 4: Schematic of the process flow for patterning the silicon nanowire

First of all, HBr plasma curing process was performed in order to harden the 193nm ArF resist for better etching resistance. Then, the BARC opening is done using CF_4 chemistry. This chemistry will be used in order to ensure vertical resist/BARC profile and correct linewidth roughness [13]. Moreover, this sequence consuming a lot of photoresist, the thin thickness of the BARC layer is well suited to minimize the resist budget during the process. Then, the BARC/resist trimming process is performed just before the main etch to selectively pattern the silicon on the buried oxide. Trimming resist is performed to achieve nanowire structures as small as **15nm in width** using the HBr/O_2 plasma. In order to smooth the resist patterns and then reduce the linewidth roughness, a curing step will be performed just before the trimming.

The investigated structures after the photolithography are shown in Fig. 5. They comprised isolated lines (NW) and arrays of lines with long and short dimensions. The arrays of lines with long dimensions will be used to extract the capacitance and the carrier mobility.

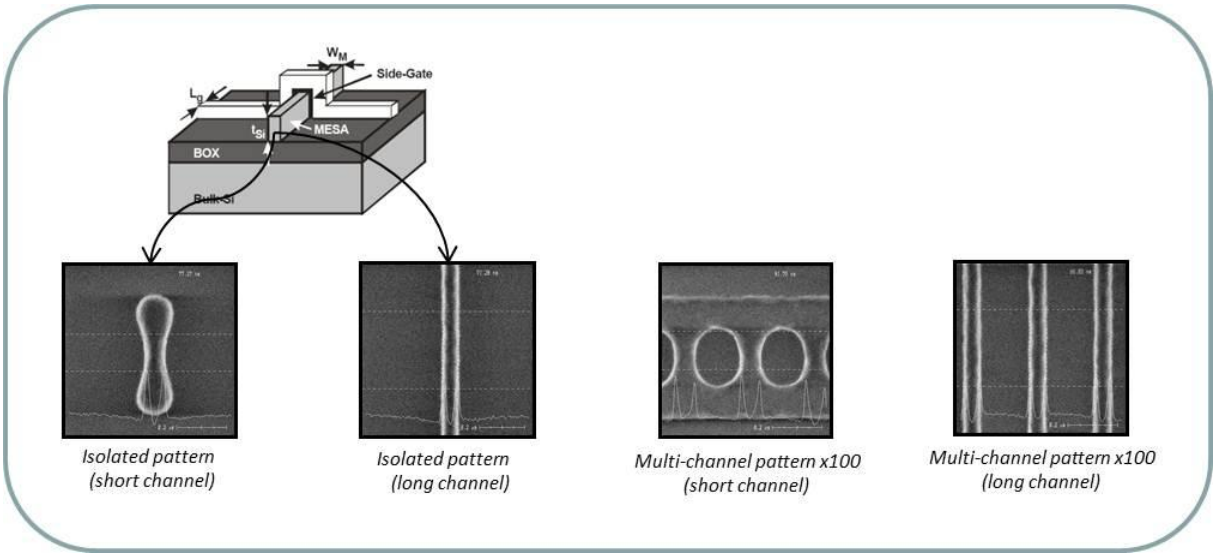


Figure 5: SEM pictures of the devices observed on various chips of the 300mm wafers after the photo-lithography. Long and short isolated devices with long and short arrays of devices (x100 fingers)

All the critical dimension (CD) measurements (after photolithography and after active patterning) will be done using in-line field-emission-scanning electron microscope (SEM).

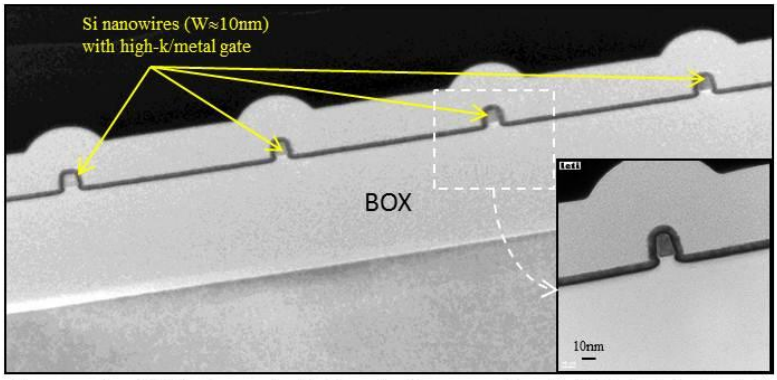
The linewidth before etching –referred to as developed inspection critical dimension- is around 80nm. After etching, the reduction of the silicon nanowire width induces by the trimming is targeted to 65 nm in order to have nanowire width of around 15nm. Due to the dispersions induce by the photolithography, the NW width after etching is expected to vary between 10nm and 20nm.

III.2. GATE STACK DEPOSITION AND CHANNEL LENGTH

The gate stack used will be composed of high-κ/metal gate. 2.3nm chemical vapour deposition (CVD) HfSiON with 5nm CVD TiN and Poly-Silicon (50nm) layers will be deposited. This corresponds to an equivalent oxide thickness (**EOT) of around 1.1nm**.

A HRTEM picture of the nanowire cross-section will be performed in order to reveal the good conformal gate stack deposition surrounding the nanowire and to evaluate

the nanowire width. Fig. 6 shows a cross-sectional TEM micrograph of a conventional triple-gate silicon nanowire with high-κ/metal gate stack (isolated devices).



Cross-sectional TEM micrograph of triple-gate silicon nanowire with high-k/metal gate stack

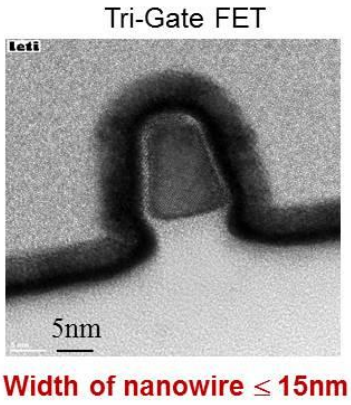


Figure 6: Cross-sectional TEM micrograph of a conventional triple-gate silicon nanowire with high-κ/metal gate stack

As for the active patterning, 193nm lithography tool will be used with a resist trimming in order to address **gate lengths down to 20nm**. First results obtained on regular Tri-gated nanowire are shown in Fig. 7.

III.3. FORMATION OF CONSTRICTIONS AT THE EDGES OF THE GATE

The both constrictions are fabricated after the gate etching (Fig. 8). A over-etch of the silicon film will be done in order to reduce the thickness. Then, we propose to do a deposition of thin spacer (nitride) to create the barrier between the source-drain and the channel. After the thin spacer etching, an epitaxial undoped silicon growth will be realized to recover the barrier and to form the both constrictions. Afterwards, a nitride spacer thickness of around 20nm will be formed on the silicon source-drain. Then, low parasitic resistance will be realized by **epitaxial doped silicon growth on the**

source-drain (ΔT_{SI}=18nm). Then, a second spacer will be deposited and etched before the source-drain doping.

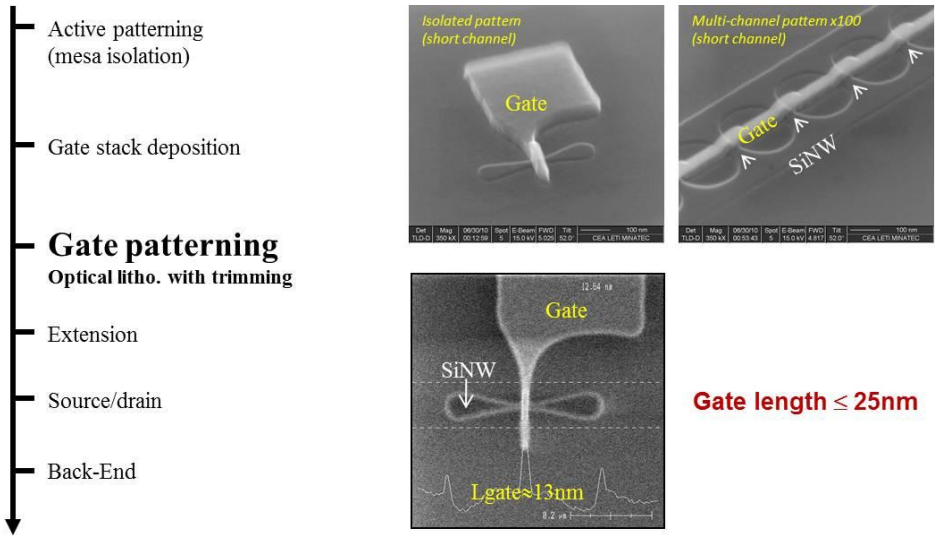


Figure 7: SEM picture of the gate after etching and trimming on regular Tri-gated nanowire transistors. Gate lengths below 25nm are obtained.

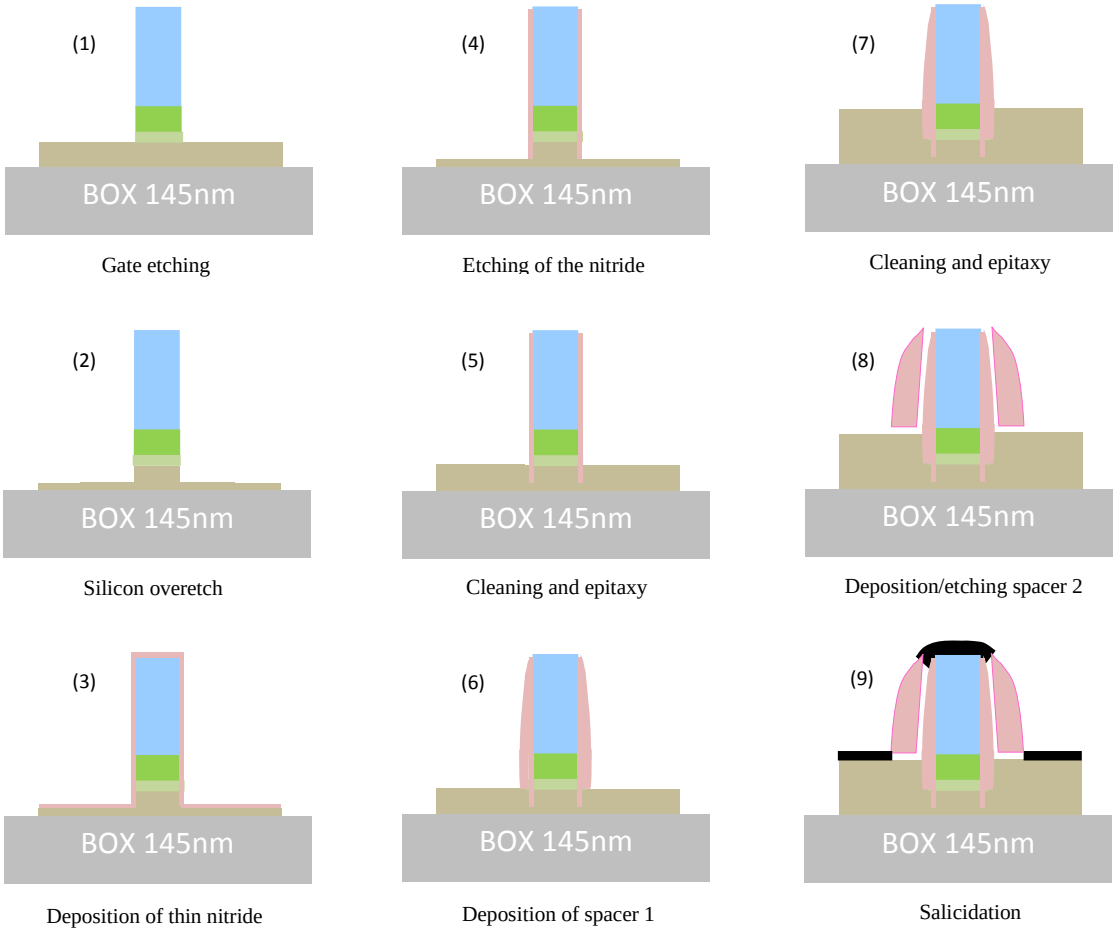
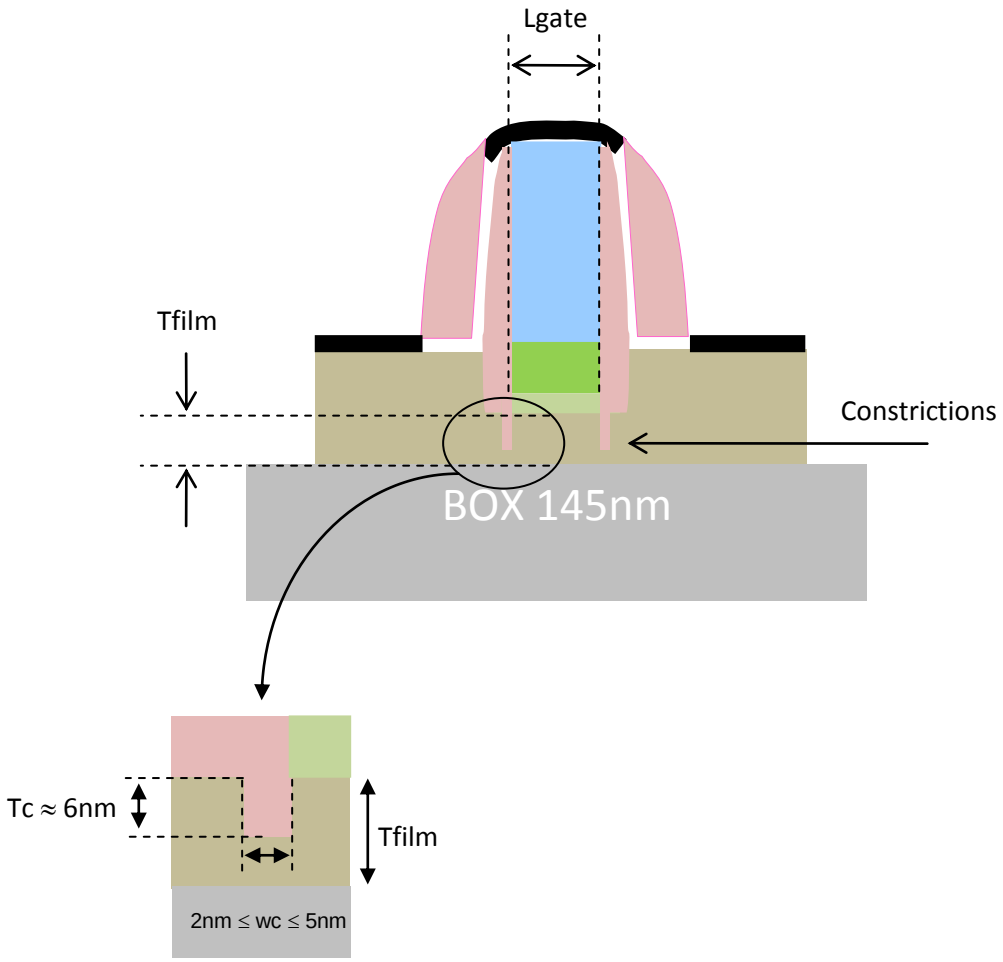


Figure 8: Simplified flow-chart for the fabrication of variable barrier tunnelling transistors.

Different splits on the thin nitride spacer will be done in order to obtain after etching a constriction of width varying from 5nm down to 2nm. Finally, the main process specifications for the fabrication of junctionless MOSFET are the following:



Width of nanowire W:	10nm ≤ W ≤ 20nm
Gate length L_g:	20nm ≤ L_g ≤ 10µm
Silicon thickness	T_{film}=12nm
Gate stack:	0.8nm SiO_2 / 2.3nm HfSiON / 5nm TiN / 50nm Poly-Si
CD spacer:	20nm
Elevated source/drain:	18nm
Width of constrictions:	2nm ≤ wc ≤ 5nm
Thickness of constrictions:	Tc≈6nm

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