Deliverable 4.2: TEM cross sections on prototyped Gated Resistors

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Abbreviation list

D: drain

FIB: focused ion-beam

HRTEM: high resolution TEM

S: source

SEM: scanning electron microscopy

SOI : Silicon-On-Insulator

TEM: transmission electron microscopy

Abstract

IPLS has performed the TEM cross sections on prototype devices made at TNI-UCC. This is going to help us to develop a protocol for the nanovisualisation of the nanowires to accurately measure their thickness and width, which will feed back to task 3.2.

Sample experiment

The prototype samples delivered to IPLS consist of a half 4-inch SOI wafer with 7 fields containing 198 devices each. These devices are junctionless transistors with

single or multiple fingers and different gate lengths and nanowire dimensions. The gate oxide is 10 nm thick, covered by a 50 nm polysilicon gate.

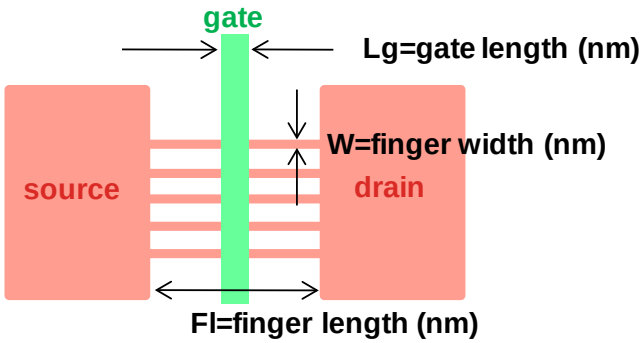

Fig. 1 Top-down of the devices with critical dimensions.

TEM characterization

For the analysis of nanowires with TEM the sample preparation is very critical in order to obtain excellent analysis results. This is done using an in-situ lift out technique on a dual-beam FEI Strata 400 focused ion-beam (FIB). The lift-out procedure consists on locating the area of interest using the FIB microscope capabilities. Then a layer of FIB-deposited Pt is placed over the area of interest to prevent milling or surface damaging. Using a large beam current two trenches are created on either side of the Pt strap. A smaller beam current is used to thin the central part between the trenches and three cuts are made to frame the area of interest. The omniprobe is inserted and positioned on the membrane and is pasted to it by depositing Pt. Then the membrane is lifted and brought to a premounted grid where is pasted. At this point, the omniprobe can be cut from the sample. Finally, once the sample is seated on the grid, it is thinned to a thickness of approx 100nm suitable for TEM imaging.

The transmission electron microscopy (TEM) analysis was performed on a FEI Technai G20 LaB6 operating at an accelerating voltage of 200 kV.

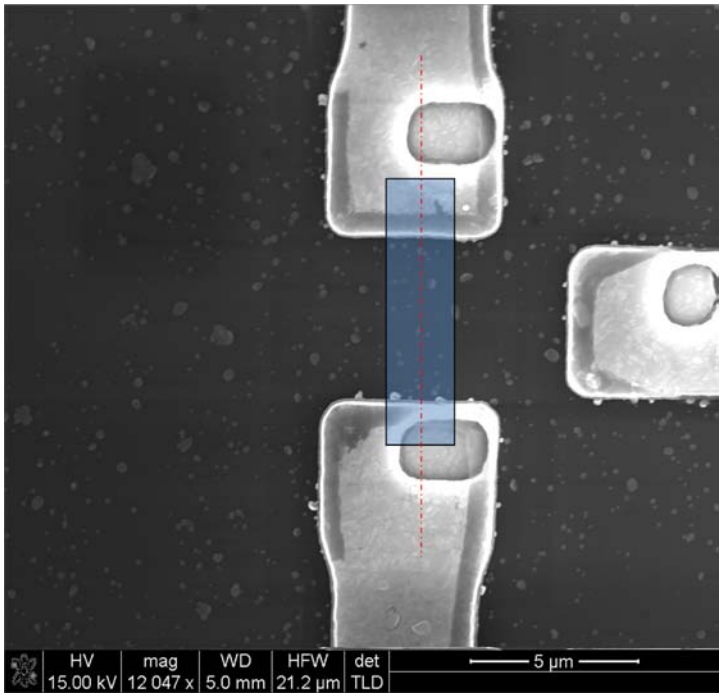

Fig. 2 Top down SEM overview with Pt location and section direction.

Results and discussion

The first TEM analysis was done on a wide single nanowire transistor along the nanowire length in order to check the Silicon thickness, the effective gate length and quantify the gate undercut.

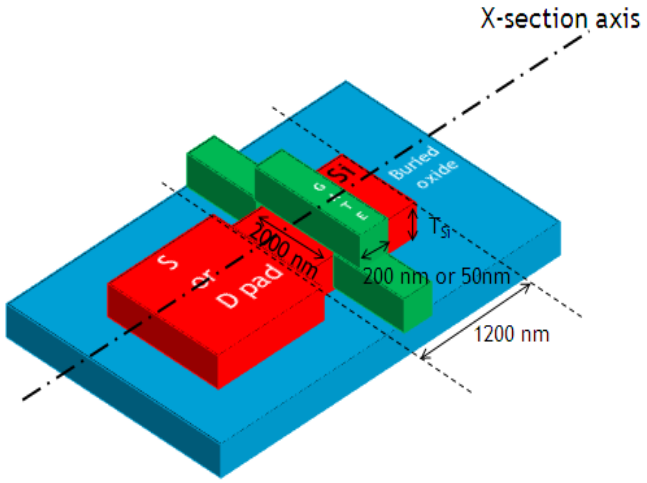

Fig. 3 Schematic of the nanowire transistor structure used for the first TEM analysis and the cross section axis.

In Fig. 4 it can be seen that the gate hasn't been fully etched, still remaining around 8nm of polysilicon. Tyndall is currently running a few test to optimise the gate etch sequence (breakthrough and softlanding times).

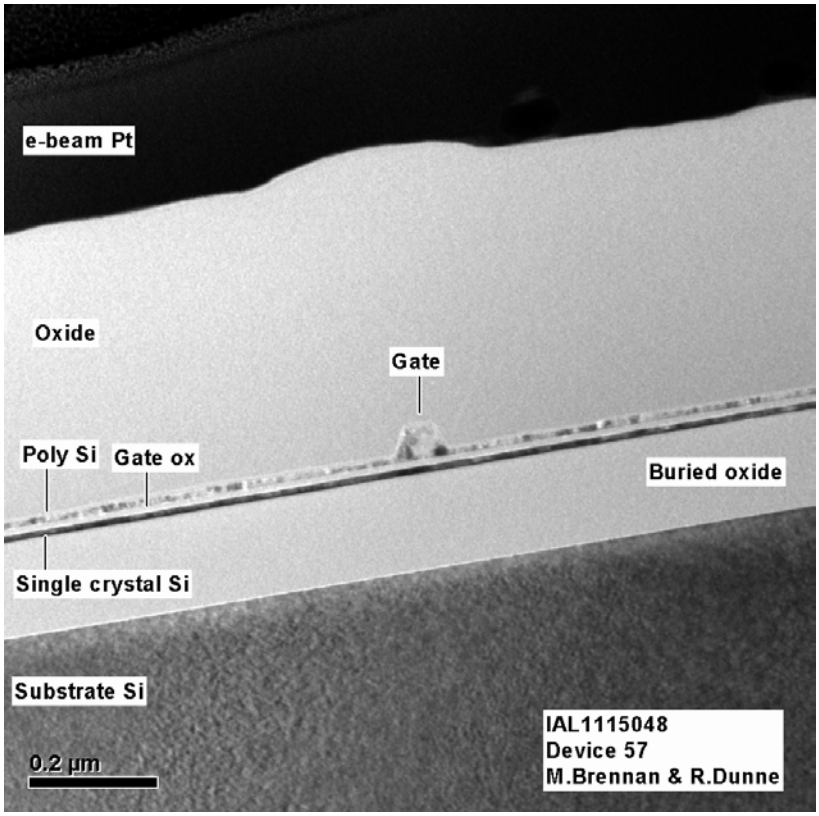

Fig. 4 TEM cross section along the nanowire showing the incomplete etching of the polysilicon gate.

The nominal gate length for the 2 devices analysed was 50 and 200nm. The resulted gates as shown in Fig 5 have a length at the base of 80 and 223nm respectively, which corresponds to 30 and 23 nm differences between the layout and the printed length respectively. The poly gate is also not showing a straight vertical profile, with a significant sidewall inclination, which would suggest an excessive polymerizing gas flow during the dry etch.

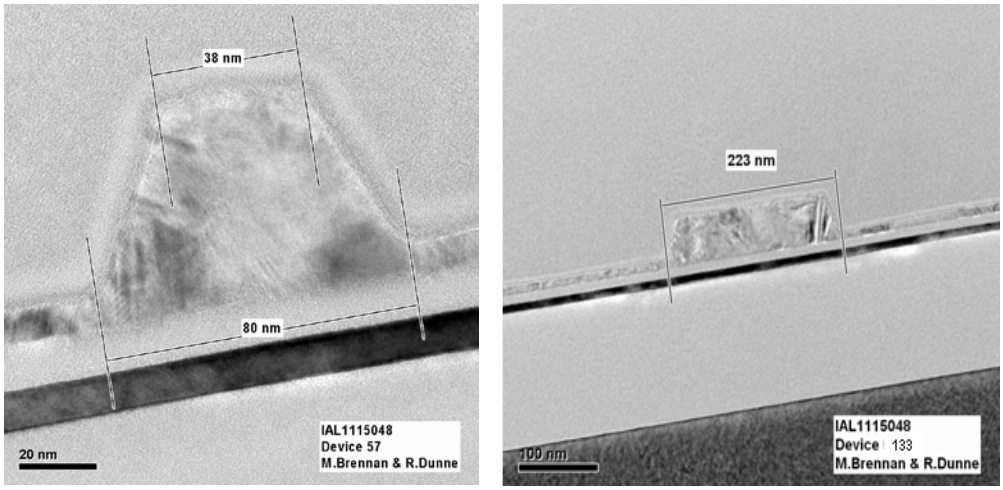

Fig. 5 HRTEM of the polysilicon gate showing the effective gate length measurements.

The second TEM analysis was done on a multiple finger transistor and cutting along the gate to measure the nanowire dimensions (Fig. 6). The structure analysed consists of 20 fingers which are 50nm wide with an expected Si thickness between 5 and 10 nm.

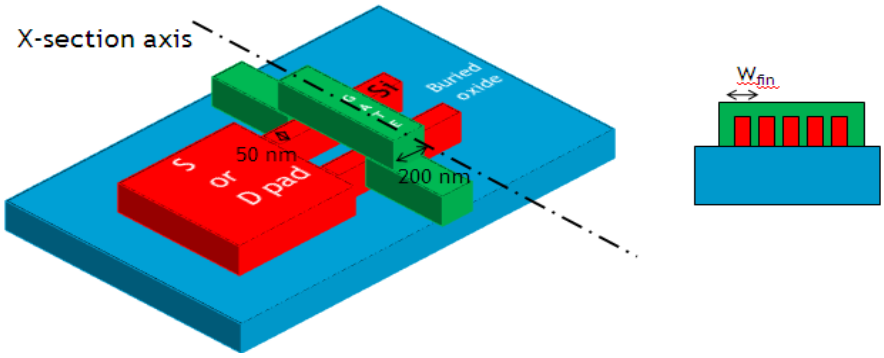

Fig. 6 Schematic of the nanowire transistor structure used for the second TEM analysis and the cross section axis.

Fig 7 shows the TEM cross section of 3 consecutive fingers. They have a dog bone type of shape (thinner in the middle), a width of 40nm and a Si thickness between 4.8 and 6.5 nm (Fig 8). The width of the rest of nanowires in the structure hasn't been measured but it was consistently uniform across the structure.

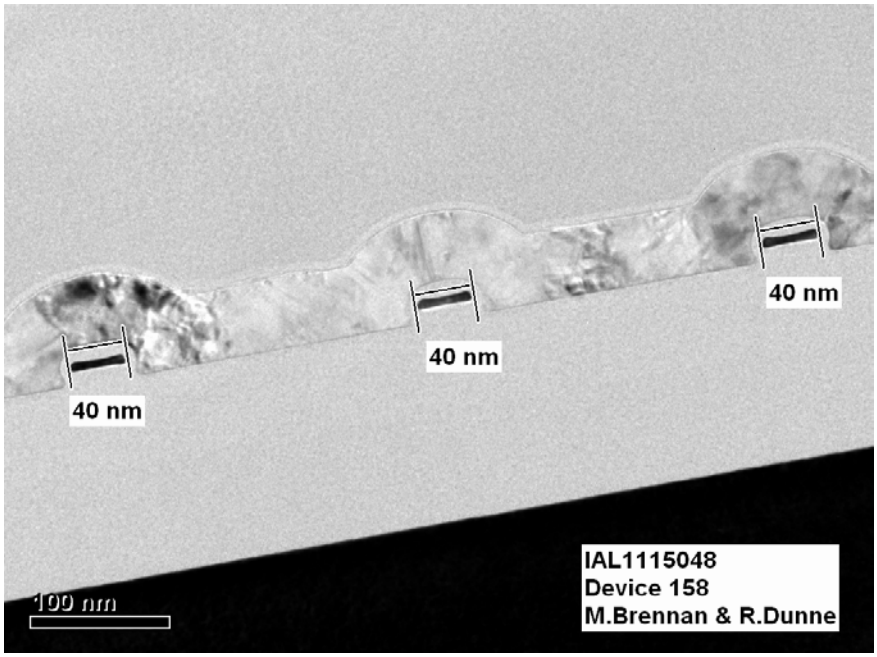

Fig. 7 TEM cross section along the gate showing 3 adjacent nanowires.

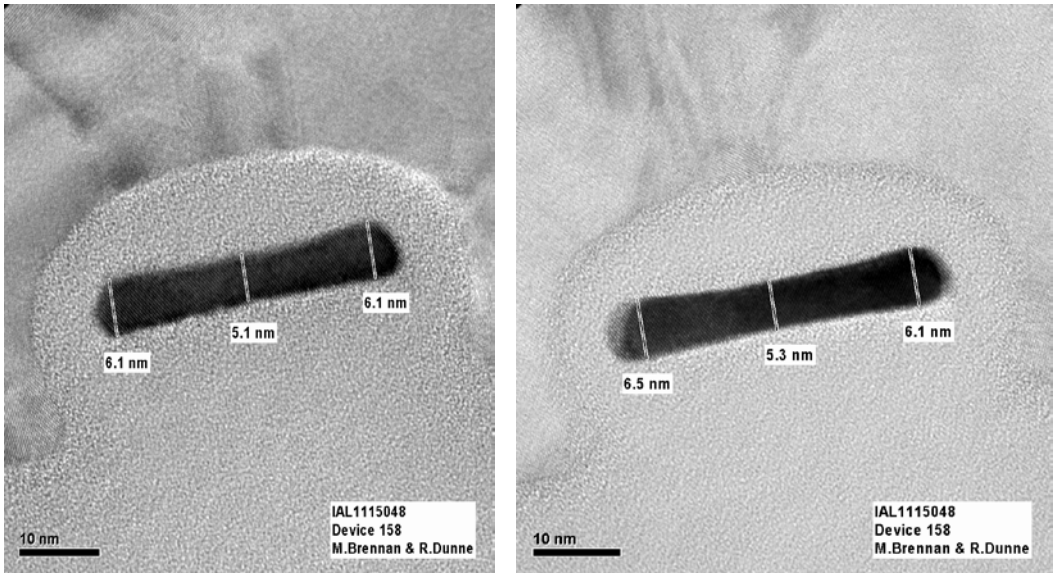

Fig. 8 HRTEM image showing the nanowire Si thickness for 2 adjacent fingers.

The polysilicon gate thickness is around 48 nm and the gate oxide thickness varies from 5.7 nm (at the edge, where is thinner) to 10.5 nm (at the centre, where is thicker) as seen in Fig 9.

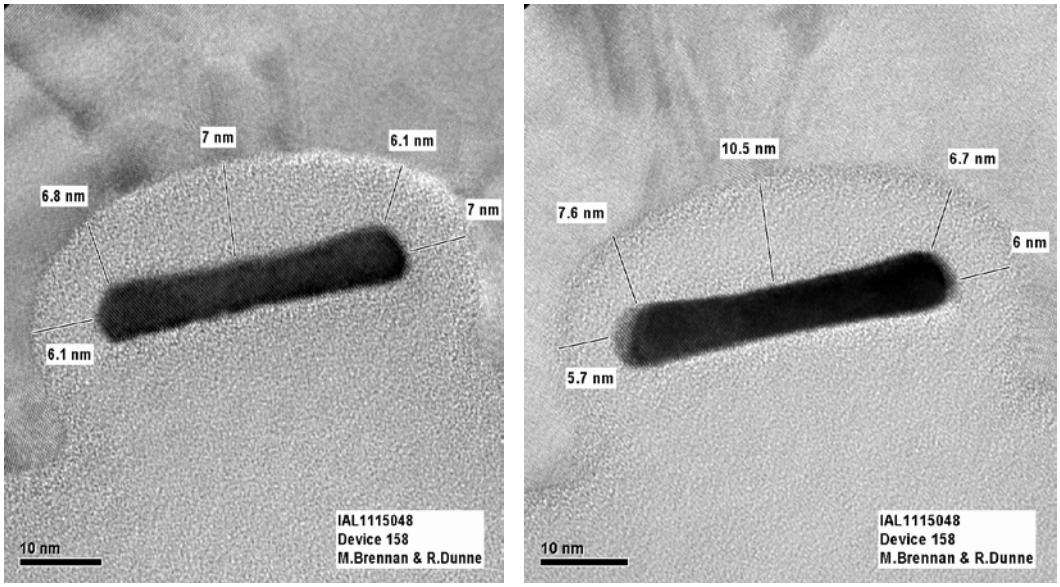

Fig. 9 HRTEM image showing the gate oxide thickness measurements.

Conclusions

In conclusion, TEM has proof to be an excellent analysis technique to accurately measure the thickness and width of the nanowires and assess the influence of processing on the nanowire geometry and quality.