3.1 Publishable summary

Summary description of project context and objectives

- SQWIRE (Silicon Quantum Wire Transistors) aimed at demonstrating the competitiveness of two novel advanced CMOS devices, the gated resistor (also referred to as 'junctionless nanowire transistor' or 'pinch-off transistor') and the variable barrier transistor (VBT). Both devices are seen as replacement candidates for the conventional inversion-mode field effect transistor for beyond the 22nm technology nodes, as they have proved to enable further MOSFET scaling. They do not require the formation of ultra-shallow junctions and have the capability to bring the sub-threshold slope below the thermo-dynamical limit of 60mV/decade (room temperature).

- Both device concepts have been recently patented by Prof. Jean-Pierre Colinge, the initial coordinator of the project. Within SQWIRE, the consortium carried out device modelling, fabrication and characterisation of gated resistors and variable barrier transistors in advanced research environments and state-of-the art semiconductor industry-compliant facilities.

- **Main objectives of SQWIRE are the following:**
  - Elaboration of quantum-mechanical models dedicated to the electronic transport in gated resistors and variable barrier transistors, and the integration of such models in a commercial and existing 3D simulation tool;
  - Use of the aforementioned simulation tool to predict key electrical properties in gated resistors and variable barrier transistors;
  - Development of a dedicated compact model for gated resistors and its validation by measurement data and simulations
  - Fabrication and delivery of ultra-thin 300mm silicon-on-insulator substrate (SOI) with high uniformity across the wafer (<0.35nm).
  - Fabrication of gated resistors and variable transistors on such high-uniformity SOI wafers, in a 300mm state-of-the art semiconductor processing facility.
  - Parametric testing of gated-resistors and variable barrier transistors fabricated on high-uniformity SOI wafers, to assess their variability at wafer level and demonstrate their suitability/viability for high-volume manufacturing.
  - Communicate to the semiconductor industry on the competitiveness of the gated resistors and variable barrier transistors.

- SQWIRE brings together a range of industrial partners, SME and representatives from the academic and research fields. By involving major semiconductor companies in the consortium, namely INTEL Learning Performance Solutions Ltd and SOITEC, SQWIRE was in a position to deliver industry-aware design specifications to meet the semiconductor industry's requirements in terms of performance and variability. Academic partners and research institutes involved in SQWIRE include: Tyndall National Institute-UCC (Ireland), CEA-LETI (France), IMEP-Institut Polytechnique de Grenoble (France), IMEC (Belgium) and Universitat Rovira I Virgili (Spain). MAGWEL is an SME within the SQWIRE consortium which brings expertise in the integration of models generated by research-oriented partners into a user-friendly and computational efficient simulation tool.

Achievements and highlights

The project objectives for the second reporting period (M18-M36) can be defined as follows:

- Modelling of carrier transport and development of compact models for multi-gate junctionless nanowire transistors.
- Implementation of the Non-Equilibrium Green's Function formalism in a commercial quantum simulation package.
- Provision of the second batch of junctionless and variable barrier transistors.
- Nanometrology protocol put in place for advanced physical characterisation of Variable Barrier Transistors.
- Advanced electrical Characterisation of junctionless nanowires.
- Evaluation of statistical parameter variability and its effect of Manufacturability of the SQWIRE architecture.

The simulation of the Variable-Barrier Transistor (VBT) was carried out using 3D quantum mechanical simulator based on the Non-Equilibrium Green's function formalism. The presence of variable tunnel barriers either side of the gate enabled this novel transistor to achieve a subthreshold slope lower than kT/q log(10). Subthreshold slope values as low as 45mV/dec can be predicted for optimised 10nm-long VBT transistors.
Modelling of carrier transport demonstrated that the mobility in junctionless nanowire transistor is dominated by ionised impurity scattering due to the high doping densities required. For nanowires with radii ranging between 2nm and 5nm, surface roughness is the dominant scattering mechanism, while ionised impurity scattering still significantly contribute to the overall mobility.
A compact model for junctionless long-channel double gate MOSFETs was developed as well as an analytical scalable 2D electrostatic model including short channel effects. These models showed excellent agreement with numerical TCAD simulations.
The non-equilibrium Green function formalism has been successfully implemented into MAGWEL's commercial device simulation software.
Highly uniform 300 mm SOI wafers with a top Si thickness standard deviation of 0.15 nm were fabricated and delivered for device fabrication. Junctionless nanowire transistors were successfully fabricated on the SOI wafers using optical (DUV) lithography and resist trimming process. In order to achieve 10nm wide by 10nm long Nanowire structures, two wafer batches were processed. The second batch presented an improved process flow i.e. thinner spacer to reduce the access resistance, and new mask set including larger number of device geometries. The novel variable barrier transistor was also successfully fabricated down to a gate length of 9nm. Two wafer batches were processed for the VBT process development.
The electrical performance of aggressively scaled junctionless Trigate nanowire transistors with high-κ/metal gate stack and epitaxially grown raised S/D has been investigated. The subthreshold slope and DIBL showed a slight improvement for the junctionless transistor when compared to the conventional inversion mode transistor for gate lengths lower than 15nm. At a gate length of 13nm and gate width of 7nm, the juctionless device exhibits near ideal subthreshold slope (SS=68mV/dec) and extremely low leakage current. Respectable drive current (500μA/μm) was achieved for an I_{OFF}=3nA/μm and V_{DD}=0.9V.
During the project, the main sources of variability of the transistor electrical characteristics were also explored. The variation across the wafer of threshold voltage (Vt) was measured and compared to nanowire width and thickness variation measured using transmission electron microscopy on multiple sites across the wafer. It was found that the width and thickness variation account for 30% and 20% of the overall Vt variability, respectively. Random dopant fluctuation and metal gate work function variability are the other main sources of variability of the electrical characteristics of the Junctionless transistor. The compact model developed by URV was integrated into an optimization tool in order to evaluate the impact of variability of some technology parameters on a circuit (SRAM Cell) and assess the manufacturability of junctionless transistor circuits.

Address of the project public website

A website has been created, www.sqwire.eu, which is dedicated to the project and its coordination