GRAND

Graphene-based Nanoelectronic Devices

Small or medium-scale focused research project

WP2 Fabrication & Material Characterization

Deliverable 2.3 “Report on graphene FETs and Interconnects”

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Deliverable Summary

In this deliverable we report on the fabrication and characterization of top-gated mono- and bilayer graphene nanoribbon (GNR) FETs. This topic belongs to task 2.6 in the DoW of the GRAND project.

The presented fabrication process for top-gated GNR FETs consists of 4 individual electron beam lithography steps and several steps of metal and dielectric evaporation followed by a lift-off, allowing the reliable realization of top-gated GNR FETs with a channel width below 30 nm.

The finished devices show a variety of effects presented and analyzed in detail in the chapter *electrical characterization*. Although the investigated monolayer GNR FET does not show a band gap at room temperature due to the insufficient small width of 30 nm, the top-gated bilayer GNR FET allows the direct observation of a tunable band gap even at room temperature (295 K). In bilayer graphene a perpendicular electric field introduces a band gap of up to 300 meV. Although already proved by infrared spectroscopy there are no transport studies available confirming the presence of a gap in double-gated bilayer graphene at RT to this date. The reason for this is most likely the presence of inter-gap states, leading to a non vanishing conductance when Fermi's energy is located inside the band gap. In the presented device we could reduce these inter-gap states by an advanced cleaning procedure and by reducing the width of the channel to 50 nm significantly so that a band gap of up to 50 meV could be observed by electrical measurements. The presented device shows an on/off ratio of 80 and a mobility of 1000 cm^2/Vs and outperform monolayer GNR FETs presented in literature [2,7]. We will end this chapter with prospects for the device performance reachable using the presented FET-design until the end of the GRAND project (12/2010), underlining the large potential of graphene FETs based on double gated bilayer ribbons. In the *Annex* a paper draft submitted to Applied Physics Letters is attached [11].

A brief summary of the work on graphene interconnects will be given in the last chapter.

Introduction

One of the major objectives of the GRAND project is the realization and investigation of graphene based field-effect-transistors (FET) working at room temperature. The main advantage of graphene as channel material in FETs is the enormous mobility of charge carriers reaching values up to 100.000 cm²/Vs (measured at RT in suspended graphene flakes [1]). For comparison the mobility in conventional silicon based FETs is typically of order 100 cm²/Vs. Hence even if during processing the outstanding mobility of graphene is reduced to typical values reached in state of the art devices (1.000 to 10.000 cm²/Vs), graphene FETs will surpass silicon FETs in speed and find possible application in high-speed logic and RF-devices. However as graphene is a semi-metal without a native band gap, the on/off ratio due to electric field modulation is rather poor (typically <10 in graphene monolayers with top-gate control) and not sufficient for most applications. The main requirements and challenges for a successful realization of graphene based FET are the opening of a band gap in the density of states and the top-gate control of channel conductance, both ideally achieved with only a minimal reduction of the charge carrier mobility. In the following chapter we will present a fabrication process and electrical characterization of top-gated graphene FETs showing on/off ratios of up 80 and carrier mobility of 1.000 cm²/Vs, both measured at room temperature. These FETs are based on double gated bilayer graphene and exceed monolayer graphene nanoribbon FETs in mobility.
Another exceptional characteristic of graphene is the high current capabilities reaching values 100 times larger than copper. Therefore the use of graphene as on chip interconnects is a possible application. In the last chapter we will briefly summarize our investigations on graphene interconnects.

FETs based on bilayer graphene and graphene nanoribbons

Fabrication process for top-gated mono- and bilayer graphene FETs

The fabricating process for top-gated graphene nanoribbons starts with the definition of source and drain electrodes and etching of the graphene nanoribbon as illustrated in figure 1A and 1B. These fabrication steps are based on PMMA resist as was previously described in deliverable D2.2 (Report on fabrication methods for graphene crystallites and graphene nanoribbons). This process allows the reproducible fabrication of nanoribbons with a width down to ~20 nm. In the first step source and drain electrodes are defined by electron-beam lithography and thermal evaporation of 20 nm nickel and a lift-off process. The fabrication of the nickel electrodes is followed by patterning a PMMA etching mask for the definition of the nanoribbons. The etching is performed using oxygen plasma. Using PMMA resist as etching mask for the graphene nanoribbons has compared to HSQ resist the advantage, that PMMA can be removed from the graphene quite easily using organic solvents like acetone. An uncovered ribbon is needed for further processing of the device, i.e. depositing the top-gate dielectric directly on top of the graphene. In Figure 2C a SEM picture of a contacted graphene nanoribbon having a width of ~25 nm and a length of 250 nm is displayed.

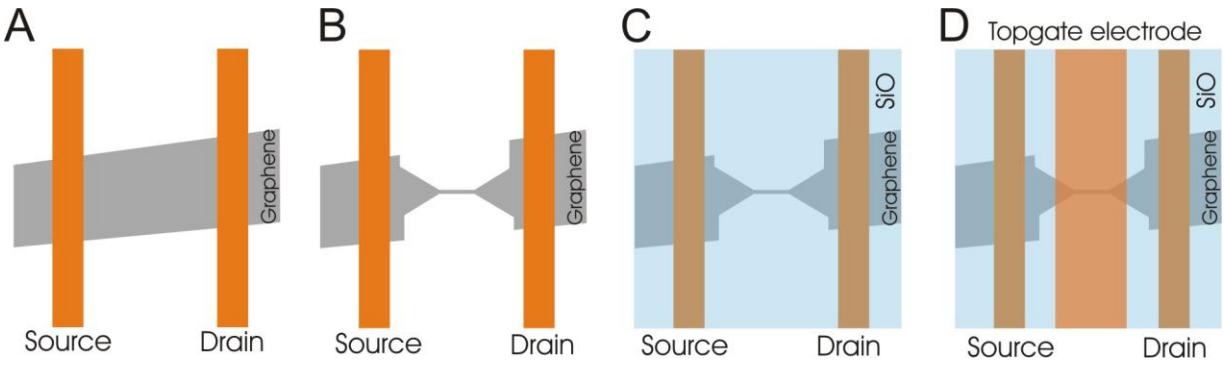

Fig. 1: Schematic of the fabrication process for top-gated graphene nanoribbon FETs. A) The first step is defining the source and drain contact electrodes. B) In the second step the nanoribbon is patterned. C) The top-gate dielectric (here SiO_x) is deposited in the third step. D) In the last step the top gate electrode is defined.

After defining the graphene nanoribbons the top-gate dielectric is deposited locally (see figure 1C and 2A). In the devices shown in this deliverable the deposition of the top-gate dielectric was done by thermal evaporation of SiO_2 followed by a lift-off process. During the evaporation process a decomposition of SiO_2 into SiO_x takes place [9], when no additional oxygen is introduced into the evaporation chamber. Hence our top gate dielectric consists of a 25 nm thick SiO_x layer with a dielectric constant of ~6.5±0.4. The dielectric constant was measured in a different experiment using a standard MOS-capacitor geometry with the used SiO_x and is in excellent agreement with the values reported in literature. The last step of the fabrication process is the deposition of the top-gate electrode. This is done similar to the deposition of the source and drain contacts by thermal evaporation of 40 nm nickel and a lift-off-process.

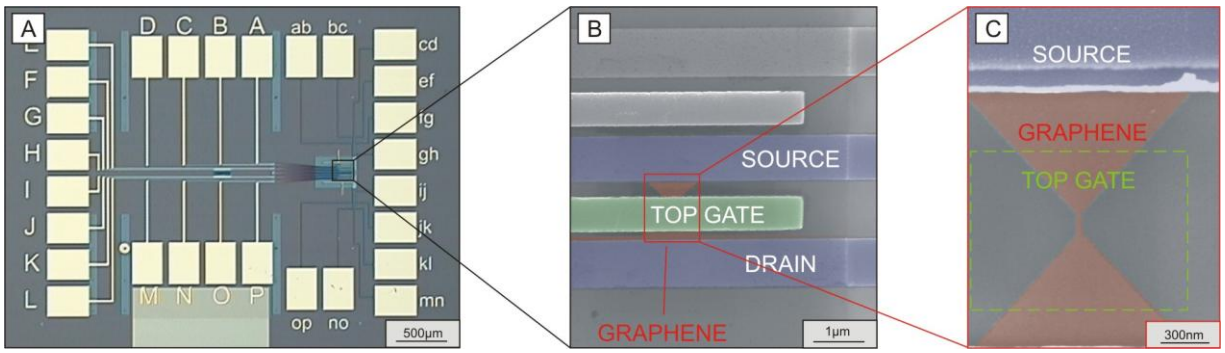

Fig. 2: Images of a completed top-gated graphene nanoribbon device. A) Optical image of the whole sample consisting of 12 individual bilayer nanoribbons (width = 50 nm, length = 250 nm) with top-gates. The source and drain contacts are labeled from **A** *to* **P**, *the top-gate electrodes are labeled from* **ab** *to* **op**. *The SiO_x top gate dielectric is lighter blue. B) Electron micrograph (false colors) of one top-gated bilayer nanoribbon shown in A). C) Electron micrograph of a graphene nanoribbon (false color) without a top-gate dielectric and electrode for illustration of the geometry.*

An optical image of a finished device is displayed in figure 2A. This device consists of 12 individual bilayer nanoribbons having a top-gate. For the fabrication of this device four electron beam lithography

steps, three lift-off steps, two steps of nickel evaporation and one step for SiO_x evaporation and plasma etching are necessary. Although all individual steps are well controlled and highly reproducible the fabrication of top-gated graphene nanoribbon devices is a time consuming procedure, as it takes more than one week for fabrication.

Detailed views on one device are displayed in figure 2B, 2C and 3. In figure 2B an electron micrograph of a top gated bilayer graphene nanoribbon is displayed. The nanoribbon itself (width 50 nm, length 250 nm) is not visible in this picture, as it is located below the top-gate electrode. A similar graphene nanoribbon is displayed in figure 2C for illustration. In figure 3 an electron micrograph (false color) of a top-gated graphene nanoribbon taken under an angle of 50° is displayed. Here source and drain electrodes, located below the SiO_x dielectric, are visible. The graphene nanoribbon, not visible in this SEM image, is marked yellow. As the SiO_x is nearly transparent for the used thickness of 25 nm not only in an optical image but also in a SEM picture the top-gate electrode seems to levitate above the nanoribbon.

In summary the presented process allows the fabrication of top-gated graphene mono- and bilayer nanoribbons having a width down to ~20 nm in a highly reproducible but time consuming manner. The electrical characterization of top-gated GNR FETs will be presented in the following chapter.

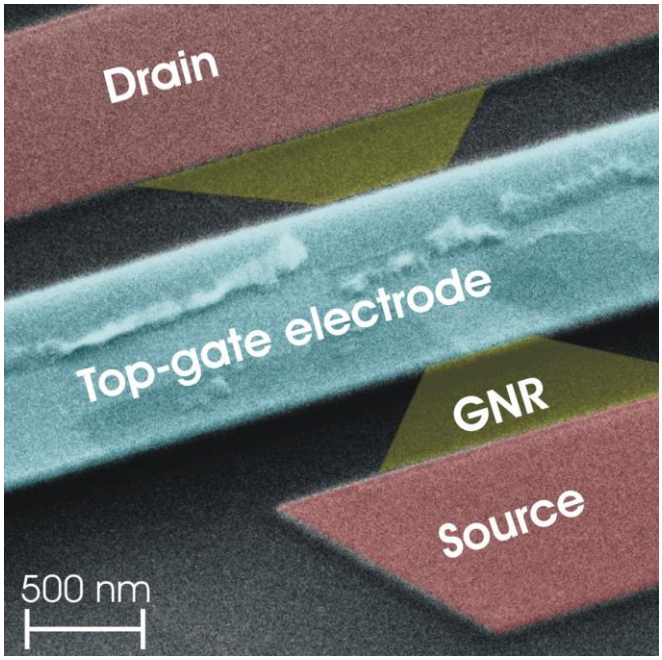

Fig. 3: Electron micrograph (false color) of a top-gated bilayer graphene FET. The top-gate electrode is located on top of SiO_x*, not visible in this SEM picture.*

Electrical characterization of top-gated mono- and bilayer graphene nanoribbons

In order to characterize the fabricated GNR FETs electrical measurements of the devices were performed. The main focus of the electrical investigations was on the measurement of the transfer characteristics in order to verify the existence and size of an energy gap in the density of states,

necessary for FET operation. A comparison with state of the art GNRs from literature is given to evaluate the performance of the devices.

The top-gate transfer characteristics of a monolayer graphene nanoribbon having a width of 30 ± 5 nm and a length of 100 nm is shown in figure 4a) for different back-gate voltages. The measurements were performed at room temperature (295 K) in nitrogen atmosphere at a fixed source-drain voltage of 10 mV. At zero back-gate voltage the transfer characteristics of the device show a monotonic decrease and no Dirac point in the investigated voltage range from -6 V to 6 V suggesting that the ribbon is highly p-doped. Increasing the back-gate voltage to +20 V and +30 V a smeared Dirac point emerges at ~3 V and ~1.5 V respectively. This behavior is expected since a positive back-gate voltage compensates the p-doping of the graphene by introducing electrons. The pronounced asymmetry of the transfer characteristics between p-conductance (left side) and n-conductance (right side) is also attributed to the high doping level of the graphene.

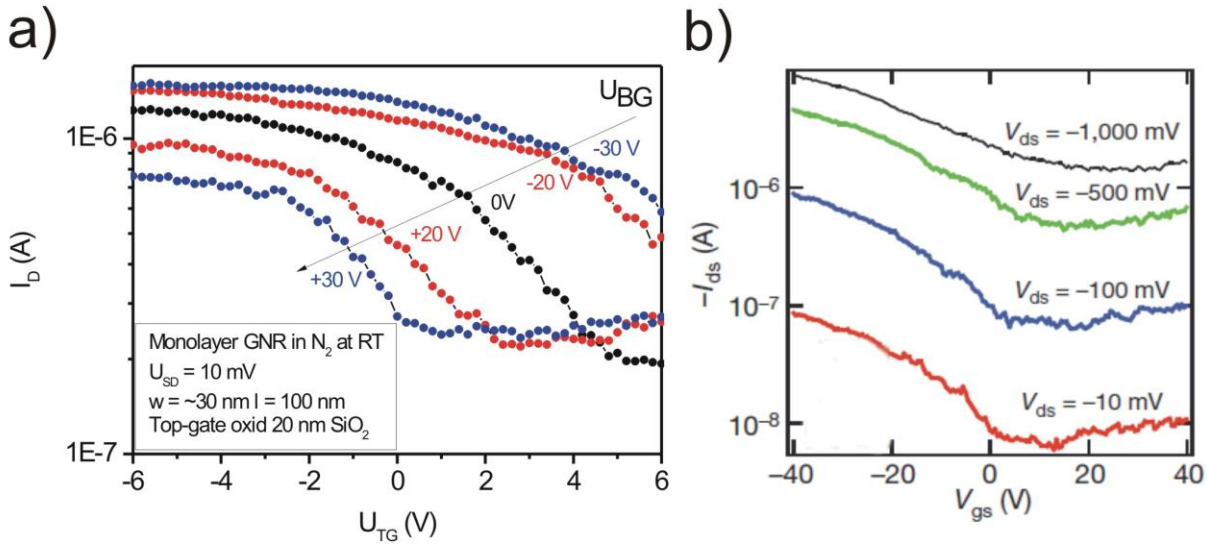

Fig. 4: a) Top-gate transfer characteristics of a monolayer graphene nanoribbon (w = ~30 nm, l = 100 nm) for different back-gate voltages measured at room temperature in N_2 atmosphere. b) For comparison: Back-gate transfer characteristics of a state of the art 7 nm wide monolayer GNR at different source drain voltages measured in air at room temperature [2].

The on/off ratio of this device is ~8 at zero back-gate voltage decreasing slightly with increasing back-gate voltage to ~3 at +30 V. These low on/off ratios show that there is no gap present in the density of states of the investigated device. For a comparison the transfer characteristics of a 7 nm wide graphene monolayer ribbon, taken from literature [2], is shown in figure 4b) for different source-drain voltages at room temperature. The investigated 7 nm wide ribbon was fabricated by cutting carbon nanotubes to wires. Nanoribbons fabricated by this technique outperform lithographically fabricated GNRs by a factor of 2…3 in minimal width (here the current state of the art is ~16 nm [3]) by simultaneously having much smoother edges. Therefore these GNRs will guide as state of the art reference for graphene based FETs in this deliverable. As shown in figure 4b) the 7 nm wide GNR shows an on/off ratio of up to ~12 increasing with decreasing source-drain voltage. This behavior shows that a gap, although quite small, is observable even at room temperature and that ~7 nm is the

upper limit for graphene FETs based on monolayer GNRs operating at RT. With state of the art lithography such small line widths of < 7 nm are hardly achievable and hence simply reducing the width of GNRs for creating a gap is from the present point of view not a promising route.

A quite different approach for creating a gap in the density of states in graphene is using bilayer graphene and applying a perpendicular electric field. The applied electric field breaks the symmetry of the two layers and modifies the density of states in such a way, that a band gap at the Dirac point opens. The induced band gap scales with the applied electric field and can reach values of up to ~300 meV, which would be sufficient for room temperature FET operation. However, in micron-scale graphene bilayers a gap was not yet observed at room temperature using electrical measurements. The reason for this is that inhomogeneities in the doping level of the graphene, intrinsic or introduced by adhesive matter, create a random potential variation and electrical transport takes place via variable range hopping when a gap is introduced [4]. The approach of the GRAND consortium to suppress conductance in bilayer graphene is to confine bilayer graphene below the typical inhomogeneity size (typically ~20 nm, measured by STM [5]) to inhibit variable range hopping.

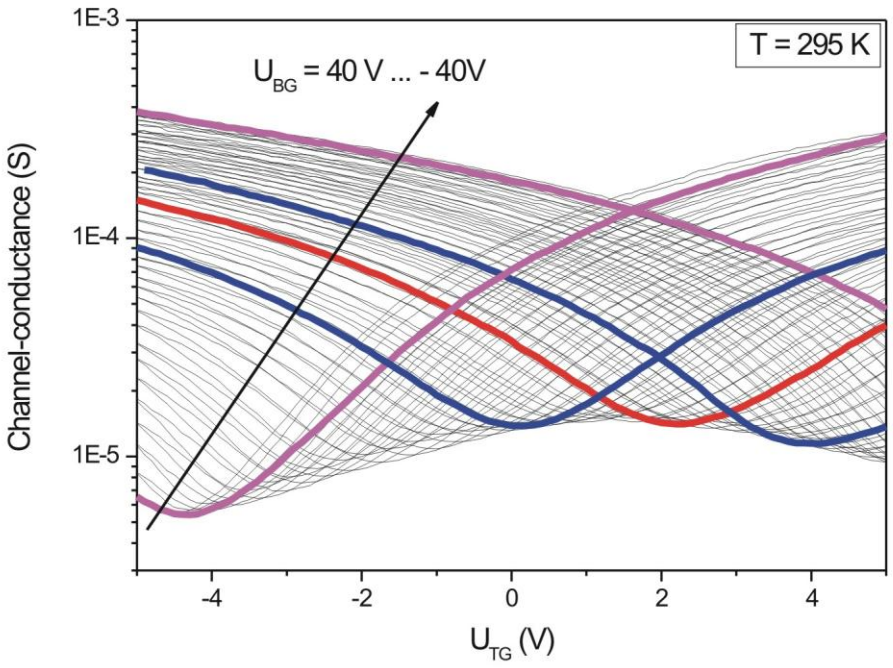

Fig. 5: Transfer characteristic of the top gated bilayer GNR FET Wolpertinger 1.2 at different back-gate voltages from -40 V to 40 V. The transfer characteristics at U_{BG} 0 V (red line), ±10 V (blue lines) and ±40 V (magenta lines) are highlighted for clarity. The measurement was performed at room temperature (295 K) under nitrogen atmosphere at a constant source drain voltage of 50 mV.

The transfer characteristics of a top gated bilayer graphene nanoribbon (internal codename *Wolpertinger*) are shown in figure 5 for different back gate voltages from -40 V to 40 V. The device is identical to the device shown in figure 2 and 3 having a wire width of 50 nm and a wire length of 250 nm. For the top-gate dielectric 25 nm evaporated SiO_x was used. All measurements were performed at

room temperature (295 K) in nitrogen atmosphere. The channel conductance plotted in figure 5 corresponds to the conductance of the active region below the top gate electrode. This conductance was derived by subtracting the resistance of the nickel and graphene interconnects (here 12 kΩ; an estimation of the individual resistances contributing to the device is given in the chapter *graphene interconnects*) from the measured 2 point resistance. At zero back gate voltage (red line in figure 5) the transfer characteristics shows the typical behavior for graphene with an on/off ratio of ~8. This on/off ratio is typical for bilayer graphene. The mobility of the device is 1000 ± 200 V/cm² at a carrier concentration of $1*10^{13}$ /cm² decreasing with decreasing carrier concentration as recently shown in reference [8]. By applying a back gate voltage of ±10 V (blue lines in figure 5) not only the Dirac-point shifts due to the additional introduced carriers, but also the on-current increases and the off-current decreases slightly. The increased on-current is related to the increased carrier concentration, while the decreased off-current manifests the opening of a gap. A further increase of the applied back gate voltage to ±40 V (magenta lines in figure 5) leads to a decrease of the off-current by a factor of ~3 compared to zero back gate voltage. Hence the electrical measurement shown in figure 5 provides direct evidence that a perpendicular electric field opens a gap in the density of states in bilayer graphene visible in transport at room temperature.

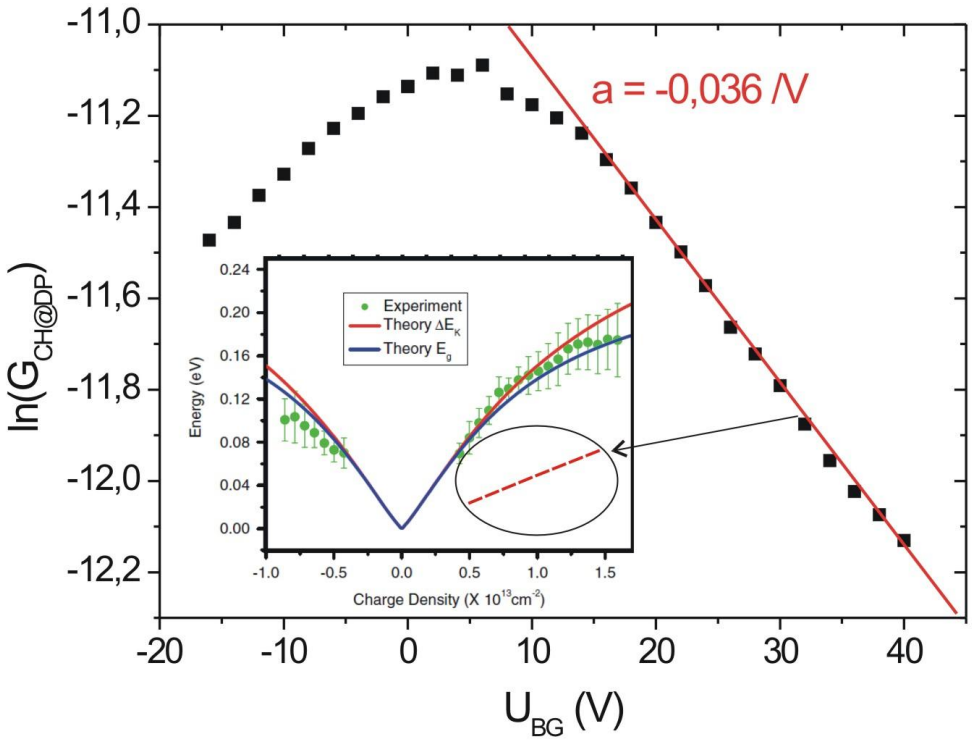

Fig. 6: Logarithm of the channel conductance $G_{CH@DP}$ of the bilayer GNR-FET Wolpertinger 1.2 measured at the Dirac-point as a function of the applied back gate voltage U_{BG}. From the slope (a = -0.036 /V) the energy gap can be estimated. The inset shows the energy gap measured by infrared spectroscopy and calculated in bilayer graphene [6] as a function of carrier concentration. The red dotted line gives the energy gap observed in the bilayer GNR-FET Wolpertinger 1.2.

To determine the size of the introduced band gap, we plotted the channel conductance at the Dirac point $G_{CH@DP}$ as a function of the applied back gate voltage (figure 6). In a semiconductor the conductance *G* is proportional to $\exp(-E_G/2k_BT)$, when Fermi's energy is located in the middle of the band gap (here at the Dirac-point). Hence the band gap energy at U_{BG}=40 V can be estimated using: $E_G=\ln(G_{CH@DP}(4V)-\ln(G_{CH@DP}(40V)$, assuming that the band gap vanishes when $G_{CH@DP}$ is minimal; here at U_{BG}=4V. This leads to a band gap energy of ~50 meV. In the inset of figure 5 the calculations for the band gap in bilayer graphene as a function of the applied electric field respectively carrier concentration are shown (straight red and blue lines) [6]. The green symbols correspond to measurements of the band gap using infrared absorption spectroscopy [6]. The band gap measured in the top gated bilayer GNR FET Wolpertinger 1.2 by electrical measurements is indicated by the red dotted line. Although optical measurements show a nice agreement with calculations our electrical measurements fail by a factor of 4. The reasons are most likely states inside the band gap leading to an effectively smaller band gap in transport experiments. These states are randomly distributed and hence don't lead to sharp absorption peaks in infrared spectroscopy experiments as band edges do. By measuring the band gap using infrared spectroscopy the value of the real band gap is observed, while electric measurements deliver the electrical effective band gap determined by inter-gap states.
The characteristic parameters at room temperature of the top-gated bilayer GNR FET Wolpertinger 1.2 are shown in table 1. The device shows a band gap of 50 meV, an on/off ratio of 80, a mobility of 1000 cm²/Vs and a slope of 2 V/dec. Up to now 6 similar devices, made of different bilayer flakes were measured showing all comparable parameters (within ~30% deviation), indicating that the process is highly reproducible. For comparison the characteristic parameters of a 7 nm, a 6 nm and a 2 nm wide nanoribbon FET are listed [2,7]. These nanoribbons were fabricated by cutting carbon nanotubes to graphene nanoribbons (7 nm and 6 nm) [2] or chemically derived from graphite (2 nm) [7] and are the state of the art, surpassing lithographically fabricated graphene nanowires in minimal width and edge roughness. However these nanoribbon FETs only provide a back gate control of the conductance. Top-gated nanoribbon FETs with a suitable switching at room temperature (on/off ratio > 10) have not yet been demonstrated.

	Wolpertinger 1.2	7 nm GNR [2]	6 nm GNR [2]	2 nm GNR [7]	Target cons.	Target opti.
Band gap (meV)	50	?	?	?	>100	>200
On/Off ratio	80	12	~150	10^b	> 120	> 1000
Mobility (cm²/Vs)	1000	1000	~120	~50	>1200	>2000
Slope (V/dec)	2	40	~10	0.2	< 0.5	< 0.1

Table 1: Characteristic parameters of the top-gated bilayer GNR-FET Wolpertinger 1.2. For comparison state of the art monolayer FETs (6 nm, 7 nm wide) derived from cutting CNT are listed [2] and a 2 nm wide ribbon chemically derived [7]. In the last two columns prospects for the device performance reachable until 12/2010 are given for a conservative and an optimistic estimation.

As shown in table 1 the bilayer GNR FET Wolpertinger 1.2 outperforms the 7 nm wide monolayer GNR FET in all listed parameters. Compared to the 6 nm wide monolayer FET the Wolpertinger 1.2 shows much better mobility, but with an on/off ratio smaller by a factor of two. In graphene nanoribbons the band gap increases with decreasing width. However, as theoretical calculations performed by the

GRAND partner IUNET show, the reduced wire width leads to a dramatic mobility reduction; this is an intrinsic behavior of graphene related to phonon scattering and therefore cannot be avoided by e.g. an advanced fabrication process. Hence in graphene nanoribbon FETs an increase in the band gap, which results in an increased on/off ratio always causes a reduction of the mobility to values also achieved in conventional CMOS devices. Consequently Wolpertinger 1.2 has a mobility larger by a factor of 8 than the 6 nm wide nanoribbon FET and by a factor of 20 larger compared to 2 nm wide GNR FET.

In the rearmost two columns we listed the targets for the parameters reachable till the end of the GRAND project (12/2010) for a conservative and an optimistic estimation. The plan for increasing the band gap is to reduce the inter-gap states by an advanced cleaning procedure, optimization of the top-gate dielectric and a further reduction of the active channel width. This increase in the band gap energy will automatically lead to an reduced off current. For an increase in mobility we do not see large space for further optimization, as the already reached values of 1000 cm^2/Vs are state of the art for bilayer graphene [8]. For decreasing the slope we will optimize the top gate dielectric. In the presented device Wolpertinger 1.2 25 nm of SiO_x was used. Hence there is large potential to decrease the slope by reducing the thickness of the dielectric and changing the material to high-k dielectrics like Al_2O_3, HfO_2 or Ta_2O_5.

Graphene interconnects

Due to its high current capability, reaching values of $1*10^9$ A/cm^2, the use of graphene as on chip interconnects represents another point for possible application. The main advantage of graphene as interconnect material compared to conventional copper based interconnects would be a smaller capacitance and consequently lower charging energies, as graphene interconnects could be design significant smaller due to the much higher current capability (a factor of 100 larger as copper). Additionally carbon is in contrast to copper compatible to standard CMOS technology and does therefore not require additional diffusion barriers. An additional advantage of graphene for the use of interconnects is the perfect integration into graphene based FETs. Hence on a graphene based chip the FET channel material and the on chip interconnects could be made out of the same material, as graphene combines two contrary properties: High current capability (low resistance) and band gap (high resistance). Additionally graphene has the advantage compared to nickel or palladium interconnects, that no Schottky-barrier forms between the interconnects and the active graphene channel. E.g. the chemically derived back-gated nanoribbon FETs shown in reference [7] are directly contacted by palladium contacts. As the palladium couples only to the valence band a Schottky-barrier forms and the ambipolar character of graphene is lost, so that the graphene ribbon shows only p-type conductance. This Schottky barrier is also contributing to the large on/off ratio of 10^6 reported in [7].

In the Wolpertinger 1.2 device presented in the previous chapter the active region below the top-gate is already connected to the larger nickel contacts by graphene interconnects. In the following we will give an estimation of the resistances contributing to the whole device, namely the resistance of the active FET region below the top gate, the resistance of the graphene interconnects, the contact resistance

between the graphene interconnects and the nickel interconnects and the resistance of the nickel leads: The two point resistance between two contact pads of the Wolpertinger device 1.2 ranges between 14 kΩ and 210 kΩ. Therein the relatively long nickel leads (each 1.4 mm long) contribute a constant value of ~10 ± 1 kΩ. This resistance was determined on a nickel reference structure with identical thickness and fabrication process (20 nm of sputtered nickel) leading to a specific resistivity of 2.2 10^{-5} Ωcm, which is in good agreement with the values for sputtered nickel reported in literature (2 10^{-5} Ωcm [10]). The resistance of the active FET channel ranges from 2.5 kΩ to 200 kΩ depending on the applied back gate and top-gate voltage and the resistance of the graphene interconnects is ~1..4 kΩ, depending on the applied back gate voltage. The contact resistance between graphene and nickel is smaller than 1 kΩ.

In summary the use of graphene as interconnect material is obvious especially for graphene FET devices, as the same material can be used for the active channel and the interconnects. Therefore in the presented FET Wolpertinger 1.2 graphene interconnects were already used. However the extended use of graphene interconnects still requires the availability of large area graphene layers with well defined thickness not available yet.

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Annex: Paper draft [11]

Electrical observation of a tunable band gap in bilayer graphene nanoribbons at room temperature

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(Dated: January 28, 2010)

We investigate the transport properties of double-gated bilayer graphene nanoribbons at room temperature. The devices were fabricated using conventional CMOS-compatible processes. By analyzing the dependence of the resistance at the charge neutrality point as a function of the electric field applied perpendicular to the graphene surface, we show that a band gap in the density of states opens, reaching an effective value of ~ 50 meV. This demonstrates the potential of bilayer graphene as FET channel material in a conventional CMOS environment.

The two dimensional arrangement of sp^2-bonded carbon atoms, known as graphene, has attracted enormous attention since the group of Geim pushed it into the spotlight of the solid state community in 2004 [1]. From a technological point of view the high mobility and the ampibolar character of charge carriers in graphene have attracted much interest and have led to investigations on using graphene as channel material for field-effect transistors (FET) [2, 3] and opto-electronic devices [4]. However, as a zero band gap material the intrinsic on/off ratio of graphene based FETs is rather poor and not suitable for most applications. Therefore a major focus of research is on the investigation of opening a band gap in the density of states to increase the on/off ratio of graphene based FETs.

In bilayer graphene a tunable band gap can be introduced by a perpendicularly applied electric field. The electric field breaks inversion symmetry and introduces a band gap at the Dirac point reaching values of up to 300 meV [5, 6]. Although such a band gap could be observed by infrared spectroscopy [7, 8], the electrical measurement of such a gap is more sophisticated. As reported by Oostinga *et al.* an insulating state occurs in double-gated bilayer graphene, but only at cryogenic temperatures revealing an effective band gap size below 10 meV [9]. They proposed that inter-gap states induced by inhomogeneities in the local doping lead to a transport mediated via variable range hopping. Very recently F. Xia *et al.* [10] managed to detect a band gap in double-gated graphene by transport measurements at room temperature. By depositing a 9 nm thick organic layer directly on top of the graphene they could minimize inhomogeneities in the doping and thus reduce inter-gap states in the graphene. Our approach for reducing inhomogeneities in the doping concentration is confining the graphene layer to a nanoribbon. As recently shown by scanning gate microscopy micronscale inhomogeneities in the local carrier concentration with $\Delta n > 10^{12}/\mathrm{cm}^2$ are present in graphene layers [11]. These inhomogeneities can be avoided by using nanoscale devices. In such small devices only smaller inhomogeneities with $\Delta n \sim 4 \times 10^{11}$ /cm^2 are expected on a length scale of typically 20 nm [12].

For investigating transport in bilayer graphene we fabricated double-gated graphene nanoribbons (GNRs) using standard CMOS-compatible processes. Bilayer graphene flakes were deposited by mechanical exfoliation from natural graphite on highly doped silicon substrates covered with 90 nm of thermal SiO_2. Bilayer flakes were identified by their optical contrast to the substrate [13]. As back-gate electrode the highly p-doped substrate was used. In the first lithography step metal contacts were defined by means of electron beam lithography, thermal evaporation of 20 nm nickel and a subsequent lift-off. In the next step an etching mask for the nanoribbons was defined using e-beam lithography and PMMA as resist. The graphene etching was performed with an oxygen plasma. With this technique we were able to define nanoribbons with a width down to 30 nm uncovered by a resist, as PMMA can be removed after etching. An electron micrograph (false color) of a GNR having a width of 30 nm and a length of 250 nm is shown in figure 1C. After patterning the GNR the top-gate dielectric was deposited by thermal evaporation of $t = 25$ nm SiO_x and lift-off. The dielectric constant of the evaporated SiO_x was measured using standard MOS-capacitors: $\epsilon_r = 6.5 \pm 0.4$. In the last step the top-gate electrodes were defined by e-beam lithography and thermal evaporation of 40 nm nickel followed by a lift-off process. A finished sample is depicted in figure 1 A-C. The top-gated bilayer GNRs presented in this paper have a width of 50 nm and a length of 250 nm. All measurements were performed at room temperature (295 K) in a needle probe station under nitrogen atmosphere. For probing a HP 4156B semiconductor parameter analyzer was used. Immediately before the measurement the sample was annealed for one hour in nitrogen atmosphere at 200 °C to minimize contamination.

To investigate the opening of a band gap in bilayer graphene, the resistance of top-gated bilayer GNRs was measured as a function of the applied back-gate and top-gate voltage at a fixed source-drain voltage of 50 mV. In figure 2 the channel resistance of a top-gated bilayer GNR is depicted as a function of the applied top-gate voltage

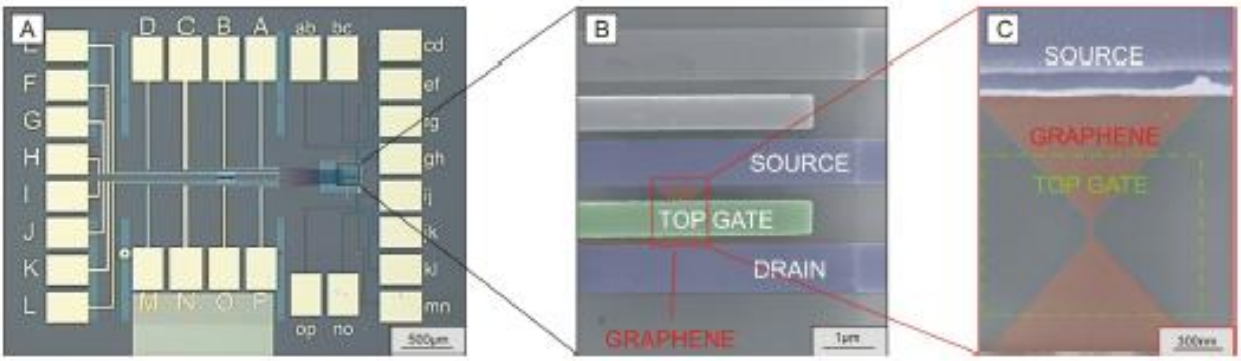

FIG. 1. Images of double-gated bilayer graphene nanoribbons. A) Optical image of a sample with a set of 12 individual double-gated bilayer GNR devices. The 16 source-drain contact pads are labeled from A to P. The 12 top-gate contact pads are labeled from ab to op. The SiO_x dielectric is light blue. B) Electron micrograph of one double-gated bilayer GNR (false color). The ribbon is located below the top-gate electrode. C) Electron micrograph of a similar bilayer GNR ($w = 30$ nm, $l = 250$ nm) before deposition of the top-gate dielectric and top-gate electrode for illustration of the used geometry (false color).

for different back-gate voltages ranging from −40 V to 40 V. The measured resistance, in the presented device ranging from 15 kΩ to 200 kΩ, consists of the resistance of the active channel below the top-gate electrode and the resistance of the leads. As only the resistance of the active region is required for an analysis we subtracted the resistance of the relatively long and narrow leads which is in our case 12 kΩ. This resistance was estimated using the lead geometry and the corresponding nickel resistivity and confirmed by a fit of the zero back-gate voltage transfer-trace similar to the one described in reference [14]. With this fit we also extracted a carrier mobility of 1000 cm^2/Vs. At zero back-gate voltage

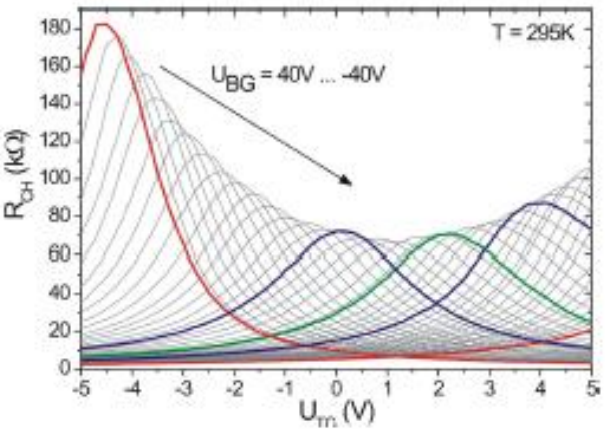

FIG. 2. Channel resistance of a double-gated bilayer GNR as function of the top-gate voltage for different back-gate voltages from -40 V to 40 V (2 V steps). The measurement was performed at room temperature (295 K) in nitrogen atmosphere at a fixed source-drain voltage of 50 mV. For clarity the transfer characteristics at 0 V (green trace), ±10 V (blue traces) and ±40 V (red traces) are highlighted.

(green trace in figure 2) the transfer characteristics show the typical behavior for bilayer graphene with an on/off ratio slightly below 10. The charge neutrality point is at a top-gate voltage of 2 V corresponding to a doping concentration of 2.5×10^{12} /cm^2. The resistance at the charge neutrality point is 71 kΩ, which translates into a sheet resistance of 6.2 kΩ $\sim h/4e^2$. With increasing back-gate voltage both, the resistance at the charge neutrality point and the on/off ratio increase, reaching values of ∼180 kΩ and ∼80 at $U_{BG} = 40$ V respectively. These increases reveal the opening of a band gap in the density of states. The top-gate voltage at the Dirac point is plotted as a function of the applied back-gate voltage in the inset of figure 3 showing a perfect linear behavior as expected. From the slope the SiO_x dielectric constant can be estimated to $\epsilon_r = 6.4$ which is in good agreement with the ϵ_r estimated by using MOS-capacitors. To analyze the opening of a band gap more quantitatively we plotted the logarithm of the channel resistance at the Dirac point $R_{CH@DP}$ as a function of the applied back-gate voltage in figure 3. In a semiconductor with the Fermi energy located inside the band gap the resistance R depends on the temperature T and the band gap energy E_G by $R \propto \exp(E_G/2k_BT)$. Assuming that the band gap vanishes when $R_{CH@DP}$ is minimal, the band gap energy at $U_{BG} = 40$ V can be estimated by: $E_G(40V) = \ln R_{CH@DP}(40V) - \ln R_{CH@DP}(4V) \sim 50$ meV. As indicated by the straight line in figure 3, the band gap energy scales roughly linearly for back-gate voltages from 15 V to 40 V, as one would expect for bilayer graphene at band gap energies smaller than 150 meV [7, 8]. The average vacuum displacement field at the charge neutrality point $D = (U_{BG} - U_{BG0}) \times \epsilon_{r(BG)}/t_{BG}$ is 1.6 V/nm for $U_{BG} - U_{BG0} = 36$ V; here U_{BG0} is the applied back gate voltage where $R_{CH@DP}$ is minimal. The estimated band gap energy is in fair agreement with the value re-

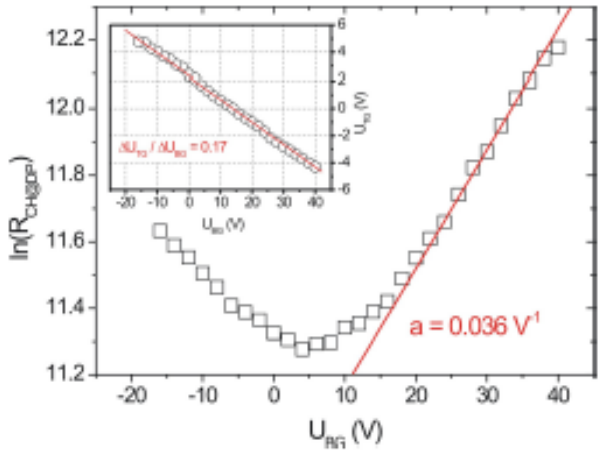

FIG. 3. Logarithmic channel resistance at the charge neutrality point of the double gated GNR shown in figure 2 as a function of the applied back-gate voltage. The straight line gives a slope of 0.036 V^{-1}. The inset shows the top-gate voltage of the charge neutrality point as a function of the applied back-gate voltage. The straight line is the best linear fit, having a slope of 0.17.

ported by F. Xia *et al.* (80 meV at $D = 1.3$ V/nm [10]), but by a factor of four smaller than measrued optically [8]. This difference can most likely be attributed to inter-gap states, which reduce the electric effective band gap, but do not alter the shape of the infrared spectroscopy signal. This explanation was already suggested by J.B. Oostinga *et al.* and confirmed by their analysis of the temperature dependency of the resistance at the charge neutrality point, showing an $\exp(1/T^{(1/3)})$ behavior at cryogenic temperatures, typical for variable range hopping [9]. We also investigated electric transport in two not-annealed top-gated bilayer GNRs having the same geometry as the device shown above. In these two devices the resistance at the charge neutrality point also increased with increasing back-gate voltage, but the effective band gap energy, estimated by the method shown in this paper, was only ~ 35 meV. This suggests that impurities removable by an annealing procedure are a major source of inter-gap states, which limit the effective band gap opening.

In summary, we have investigated transport in double gated bilayer graphene nanoribbons at room temperature. The resistance and on/off ratio of the investigated devices at the charge neutrality point increases with increasing displacement field showing that a band gap opens. The maximal achieved effective band gap energy was ~ 50 meV at $D = 1.6$ V/nm in reasonable agreement with recent results obtained by Xia *et al.* in a different environment [10], but four times smaller than calculated by theory and measured using infrared spectroscopy [8]. This deviation between electrical and optical measurements in combination with the enhancement of the effective gap size by annealing shows that transport is still limited by randomly distributed inter-gap states introduced by contamination. Further attempts to increase the bandgap requires accurate control of the individual process steps to reduce parasitic contamination.

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