SEVENTH FRAMEWORK PROGRAMME
THEME [ICT-1-3.1]
Next-Generation Nanoelectronics Components and Electronics Integration

Deliverable Report

Work Package 1 – IC power integrity model

Deliverable D1.1 – Report describing the modeling approach of both output and IC core power rails and their coupling effect. Models of proprietary and third party IC devices.

Contract no.: 216732
Project acronym: MOCHA
Project full title: MOdelling and CHAracterization for SiP Signal and Power Integrity Analysis
Start date of project: 1st January 2008
Duration: 2 years
Instrument: Small or medium-scale focused research project - STREP

Report responsible partner: Numonyx Italy Srl
Report preparation date: 27/02/2009
Dissemination level: PU

Project coordinator: Antonio Girardi
Project coordinator organization: Numonyx Italy Srl

Revision: 1.0
## Contents

1. Introduction .................................................................................................................. 3
2. Buffers power rails model .............................................................................................. 4
   2.1 EM Simulations ........................................................................................................... 5
      2.1.1 Analysis of Power Rail Modeling .................................................................... 8
      2.1.2 Results .............................................................................................................. 9
      2.1.3 Model structure and parameter estimation ..................................................... 11
2.2 Model generation from measurements ....................................................................... 15
   2.2.1 First test case (on-wafer measurements) ......................................................... 15
   2.2.2 First test case (on-board measurements) ........................................................... 18
   2.2.3 Second test case (Third parties device) .............................................................. 19
3. IC core power rails and coupling models ..................................................................... 22
   3.1 Model structure and parameter estimation ............................................................ 22
      3.1.2 First test case (on-wafer measurements) ......................................................... 23
      3.1.3 Computation of model parameters and results (first test case) .................. 25
      3.1.4 Second test case (on-wafer measurements) .................................................... 27
      3.1.5 Model accounting for the coupling effects ...................................................... 29
4. Additional results on a test-chip .................................................................................. 29
5. Simulation data validation ............................................................................................ 32
   5.1 First Test Case ......................................................................................................... 32
   5.2 Second Test Case ..................................................................................................... 34
   5.2 Third Test Case ....................................................................................................... 35
6. References ................................................................................................................... 37
Appendix .......................................................................................................................... 37
   List of Acronyms .......................................................................................................... 37
1. Introduction

Nowadays, shrinking device dimensions, faster switching frequencies and increasing power consumption in deep sub-micrometer technologies cause large switching currents to flow in the power and ground networks which degrade performance and reliability. This phenomenon is generally due to two main causes:

- the resistance of the interconnections constituting the network, that produces a voltage drop commonly referred to as the **IR-drop.**

- the inductance of interconnections (especially package leads) which causes a voltage drop at the pad locations due to the time varying current drawn by the devices on die. This voltage drop is referred to as the **di/dt-drop.**

In this way the voltage seen at the devices is the supply voltage minus the IR-drop and di/dt-drop. Excessive voltage drops in the power grid reduce switching speeds and noise margins of circuits, and inject noise which might lead to functional failures. Therefore, the challenge in the design of a power distribution network is in achieving excellent voltage regulation at the consumption points notwithstanding the wide fluctuations in power demand across the chip, and to build such a network using minimum area of the metal layers.

Capacitance between power and ground distribution networks, referred to as decoupling capacitors or **decaps,** acts as local charge storage and is helpful in mitigating the voltage drop at supply points. Parasitic capacitance between metal wires of supply lines, device capacitance of the switching and non-switching devices, and capacitance between N-well and substrate, occur as implicit decoupling capacitances in a power distribution network. Unfortunately, this implicit decoupling capacitance is sometimes not enough to constrain the voltage drop within safe bounds and designers often have to add intentional explicit decoupling capacitance structures on the die at strategic locations. These explicitly added decoupling capacitances are not free and increase the area and leakage power consumption of the chip. Moreover, it is worth noting that the decoupling capacitances and the RLC (Resistance, Inductance, and Capacitance) parasitic of package/IC interconnections form a complex circuit which has its own resonance frequency. If the resonance frequency lies close to the operating frequency of the design, large voltage drops can occur in the power grid.

Considering the current limits of simulations approaches to extract a reliable wide-frequency-range model of IC power supply networks, the main objective of WP1 is to develop a methodology for extrapolating such a model by measurements and then address the due enhancements to simulation’s methodology.
2. Buffers power rails model

In order to understand the most appropriate model structure of the power delivery rails, a set of preliminary EM simulations and measurements were defined, starting from the first internal Numonyx test case.

The chosen device is a 512Mb Numonyx NOR Flash memory in 90nm technology. In Fig.1 is reported its BSA (Build Sheet Assembly) with the related pads distribution information.

---

![Figure 1. BSA of the 512Mb Numonyx NOR Flash memory in 90nm technology](image-url)
As can be extrapolated from datasheet [2], the device, whose functional diagram is reported in Fig. 2, is supplied by two different power supply voltages:

- ✓ VDDQ for the Input/Output circuitry.
- ✓ VDD for the Core circuitry.

For both, the nominal supply voltage value is 1.8V.

In these hypotheses it was mandatory to characterize:

- the power networks that supply the input/output buffers section of the device (hereafter referred as VDDQ/VSSQ), which consist of a two coplanar rails with a uniformly distributed set of VDDQ and VSSQ pads. In the test case we worked on, there was one DQ pad for each couple of VDDQ/VSSQ pads;

- the power supply distribution structures of the internal circuitry (hereafter referred as VDD/VSS)

### 2.1 EM Simulations

In order to define a set of EM simulations based on a realistic structure that accurately represents the power rail on a real IC, Numonyx extracted their CAD description in a GDSII file format provided it to POLITO and IT). This extracted structure, because of its complexity, was not suitable to be imported at the beginning in any commercial EM solver so it was simplified considering the most important connections that composed the supply rail.

The electromagnetic CAD description of the VDDQ/VSSQ rail is shown in Fig. 3.
The first set of EM simulations were focused on the VDDQ/VSSQ rails and was devised to understand the general behavior of the structure of interest in order to select the most appropriate model representation. To this aim the following actions were arranged:

i. to focus on the elementary cell of the power rails (they have an almost periodic structure)

ii. to compute the set of network parameters and field distributions of the cell over the bandwidth [0-10GHz]

In order to comply with (i.), a simplified cell as a 4-port element composed of two metallic traces was defined, that mimics a couple of VDDQ-VSSQ pads and their rails, and of metallic patches representing the output pads. This simplified cell is shown in Fig. 4.

With the simplified cell, the complete rail can be generated by cascading identical replicas of the cell itself via ports 1 and 2, corresponding to the interfaces between the adjacent cells. Port 3 represents the couple of VSSQ and VDDQ pads that will be excited via the on-chip probing/measurements and port 4 corresponds to the position where the simplified equivalent capacitive impedances representing the I/O buffers will be connected.
The simplified cell can be effectively used in a 3D EM simulator for large number numerical experiments. Most important, the simplified cell allows a systematic analysis of the effects of material parameters (e.g. the conductivity of the substrate).

At present, a number of simulations were carried out as outlined below.

- computation of network parameters and field distribution for the simplified cell with homogeneous dielectric and no reference plane
- computation of network parameters and field distribution for the simplified cell with insulator and semiconductor layers
- computation of network parameters and field distribution for the simplified cell with insulator and semiconductor layers and reference plane

These simulations were aimed at

- getting the main port behavior of the simplified cell
- verifying the effect of the reference plane on the cell behavior (field distributions)
- verifying the consistence of port definitions (field distributions)
- defining a quasi-lumped model of the simplified cell

The results of this analysis were exploited for a further set of simulations, and in particular:

- computation of the responses of the supply rail from the quasi-lumped model
- validation of the responses with the EM simulation of the whole supply rail
- computation of the effect of the buffer loads on the supply rail
- simulation of possible measurement configuration aimed at estimating model parameters
- assessment of the effects of power supply bounding on the responses of the power rail structure
- assessment of the supply rail fluctuations due to buffer activity

For the VDD/VSS power distributions supplying the internal circuitry of the device, a lumped equivalent was assumed. These distribution networks have a limited number of external pads and, in addition, the internal structure of the power rails cannot be described in terms of a limited number of topologies, as for the VDDQ/VSSQ case, thus forcing a lumped characterization from S-parameter measurements, only.

The numerical experiments defined before have been carried out by using a commercial 3D field solver and the CAD description of Fig. 4. Different test cases have been considered to assess the effects of the different parameters and material properties possibly affecting the behavior of the EM structure.
2.1.1 Analysis of Power Rail Modeling

In the MOCHA internal report “IT_MOCHA_WP1_InternalReport_26Jun2008.pdf” produced by IT [3], an analysis was shown for the behavior of a general power rail structure, with dimensions similar to those of the test board provided by Numonyx, and for the frequency range of interest. The focus of this analysis was on the evaluation of the theoretical possibility of using a lumped parameters model to successfully simulate the behavior of power rail structures, and also to define a strategy for the determination of such lumped models. As detailed in such internal report and after analyzing the properties of the 3D structure provided by Numonyx (which, evidently, also apply to the structure of Fig.4), three basic assumptions were formulated on the electro-magnetic (EM) behavior they are subjected to, for the considered frequency range:

(I) All chip interconnect metal objects whose dimensions are less than a few tens of micron can be neglected, as they can be treated as uniform-potential lines, or lumped into a single circuit node.

(II) All chip interconnect metal objects whose width is smaller than a few tens of micron, but whose length is greater or equal than 100μm, or so, will propagate a TEM mode (or quasi-TEM mode if we consider that the dielectric is not homogeneous), and so they can be treated as conventional transmission lines with an effective characteristic impedance, \( Z_0 \), and propagation constant, \( \gamma \), (or attenuation per unit length, \( \alpha \), and phase constant \( \beta \)).

(III) Structures whose length and width are both on the order of 100μm or higher, should be simulated or measured as possible EM structures, and their two-port behavior obtained in the form of some multi-port scattering matrix.

These assumptions are the basis for a divide-to-conquer strategy which consists in dividing the complex power rail structure into simple blocks, where each block will be replaced by a simple simulation model based on lumped elements. To illustrate this strategy, Fig. 5 shows an example of a VDDQ-VSSQ structure that is divided, according to the above assumptions, into simple blocks (Fig. 6).

![Diagram of a typical power rail structure.](image-url)
The models for each simple block can consist of sequences of T or \( \pi \) RLC topologies, whose values are properly determined from transmission line and electro-magnetic analysis, using simulated and measured data. In [1], a simple structure was simulated by an EM software from which S parameters were determined. Then, a simple T-structure RLC model was determined and it was shown that it would have the capability to mimic the obtained S parameter behavior (on a frequency range from 100MHz to 20GHz).

The complete model of the power rail structure will then be composed of a series of simple lumped parameter models, connected in cascade or in parallel, according to the physical structure being analyzed.

### 2.1.2 Results

The simulation test cases that have been confirmed to provide the most useful information and that allow to address the generation of a rail model are:

1. Test #1: *the structure of Fig.4 is immersed in a homogeneous dielectric material (\( \varepsilon_r = 7 \)).*

2. Test #2: *a silicon substrate is placed on the bottom of the structure (the electrical and geometrical information of the substrate have been given by Numonyx).*

As an example, Fig. 7 shows the frequency-domain scattering parameters obtained for the two simulation test cases based on the structure of Fig. 4.
From the responses of Fig.7, the following comments hold:

- The silicon substrate placed under the conducting traces weakly modifies the responses of the cell in the high-bandwidth region only, i.e. within the range 1-10 GHz.

- The behavior of the different scattering functions is very smooth within all bandwidth of interests, i.e. up to 10GHz.

- The values of the scattering functions are very close to those that can be obtained for the ideal simplified structure of Fig. 8 and a small variation of the scattering parameters around the ideal values is observed.

$$S = \begin{bmatrix}
-0.5 & 0.5 & 0.5 & 0.5 \\
0.5 & -0.5 & 0.5 & 0.5 \\
0.5 & 0.5 & -0.5 & 0.5 \\
0.5 & 0.5 & 0.5 & -0.5 
\end{bmatrix}$$

Figure 8. Ideal structure representing the cell of Fig. 4 and the corresponding scattering matrix.
- The regular behavior of the scattering responses along with the geometrical dimensions of the structure of Fig. 4 confirms that a simple lumped equivalent can be effectively used to approximate the behavior of the cell of Fig. 7. No complex structures seem to be required.

### 2.1.3 Model structure and parameter estimation

This section defines a first power rail model structure and the procedure for the estimation of the model parameters. As an example, aimed at confirming the lumped assumption, the IdEM (Identification of Electrical Macromodels) tool has been used to process the scattering parameters and to generate a lumped model of the structure of second test case. IdEM is a modeling technique developed by the POLITO unit based on the estimation of a reduced order rational approximation reproducing the port behavior of a complex linear structure from their port responses (see the section “software” of [http://www.emc.polito.it/](http://www.emc.polito.it/)). The approximation is performed via the powerful and well-known Vector Fitting (VF) algorithm [4], with an a-posteriori correction to assure the passivity of the obtained rational model [5]. Figure 9 shows the comparison between a selection of the reference and the model scattering responses, thus highlighting the fairly good accuracy of a 4-th order model.

The previous analysis has been extremely useful to understand the behavior of the simplified cell and thus to define a lumped-equivalent of the cell. However, in order to allow an easy estimation of model parameters from real measured data, the lumped equivalent must be sufficiently simple, i.e. defined by a limited number of parameters.

To devise the most appropriate model structure, the scattering parameters of Fig. 7 have been converted into the impedance matrix $Z$ by means of

$$Z = R_o (I - S)^{-1} (S + I)$$

(1)

where $R_o=50\,\Omega$ is the reference impedance used to define the scattering waves. Figure 10 shows the different entries of the 4x4 impedance matrix $Z$.

The curves of Fig. 10 suggest a dominant capacitive behavior of all the matrix entries, with a small deviation in the high frequency region. From the phase diagram it is also clear that the deviation is due to an inductive behavior.

These observations suggest the simplified model structure of Fig. 11. For the sake of simplicity, the structure of Fig. 11 does not include the explicit definition of ports 3 and 4. Without loss of generality, all the comments hold for the complete structure. If needed, minor modifications of the structure of Fig. 11 and of the following equations allow handling the ports 3 and 4.
Figure 9. Selection of the scattering responses of the second test case (see the right panels of Fig. 7). Solid line: reference; dashed lines: IdEM model responses.
Figure 10. Entries of the impedance matrix $Z$ defined in (1). Left panel: magnitude, logarithmic scales; right panel: magnitude and phase, semilog scale.

Figure 11. Two-port model structure of the supply rail (for the sake of simplicity port 1 and 2 are included only) with the most relevant circuit elements.

The impedance matrix of the simplified two-port circuit element of Fig. 11 writes:

$$Z_m = \begin{bmatrix} (Z_S + Z_p) & Z_p \\ Z_p & (Z_S + Z_p) \end{bmatrix}$$

(2)

From the structure of the matrix defined by (2) and the reference curves of Fig. 10, it is clear that the effects of the series component $Z_S$ is negligible at low frequency since some effects appear for frequencies larger than 1 GHz only. Owing to this, the shunt impedance $Z_p$, i.e., the value of the capacitance can be estimated by fitting the $Z_{m12}$ entry of the matrix to the $Z_{11}$ frequency domain response of Fig. 10.

$$Z_p = 1/(j2\pi fC) \quad @ \quad f=1\text{GHz} = Z_{m12} \approx \text{Im}(Z_{11}) \to C=0.34\text{pF}$$

(3)

In a similar way, the estimation of the alternate parameters in $Z_S$, i.e. the series resistor and the inductor, can be effectively done via the admittance representation of the structure of Fig. 11 that highlights the effects of the series components. From the equation (2), the admittance matrix of the two-port element defined by the ports 1 and 2 (with the ports 3 and 4 left open) writes:
\[
Y_m = Z_m^{-1} = \begin{bmatrix} Y_{m11} & Y_{m12} \\ Y_{m21} & Y_{m22} \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_s(Z_s + 2Z_p)} & -Z_p \\ -Z_p & (Z_s + Z_p) \end{bmatrix}
\]  

(4)

As an example, Fig. 12 shows the entries of the reduced admittance matrix $Y_2$ obtained by inverting the matrix $Z_2 = [Z_{11}, Z_{12}; Z_{21}, Z_{22}]$, where $Z_{jk}$ are the corresponding curves of Fig. 10. As already done for $Z_p$ in (3), $Z_s$ is estimated by fitting $Y_{m11}$ in (4) to the corresponding curve of Fig. 12 (e.g. at a fixed frequency point). R and L can be thus estimated as follows

\[
Y_{m11} = \frac{(Z_s + Z_p)}{Z_s/(Z_s + 2Z_p)} \approx \frac{1}{2Z_s} @ f=1\text{GHz} \rightarrow R = 0.22\Omega; \ L = 0.13\text{nH}.
\]  

(5)

Figure 12. Entries of the reduced admittance matrix $Y_2$ obtained by inverting the matrix $Z_2 = [Z_{11}, Z_{12}; Z_{21}, Z_{22}]$. $Z_2$ is obtained by filling in the different entries of the matrix with the curves of Fig. 10. Left panel: magnitude, logarithmic scales; right panel: magnitude and phase, semilog scale.
2.2 Model generation from measurements

A set of measurements of the responses observable at the power rail pads were defined. The aim was to use these responses to estimate parameters of the model of the power rail structure as outlined in the previous Section, i.e. to obtain information of the transmission properties of the power rail by combining measured data and models developed from numerical analysis.

The measurements and the power rail model generation have been carried out for the first test case considered in Sec. 2 (i.e. the 512Mb NOR Flash memory in 90nm technology provided by Numonyx) and for a third party 512Mb DDR memory device in 70nm technology (referred as the second test case hereafter).

The measurements that have been considered for the estimation of model parameters and for model validation are:

1. Measurements on-wafer: e.g., 2-port S matrix between two couples of adjacent pads of the VDDQ-VSSQ net. Two Single Ended RF probes and DC probes were used. Biased and unbiased measurements were considered to understand the effect of device polarization.

2. Measurements on a die (on-board): to verify the effect of the polarization and of the states of the output buffers. For this latter test, the VDDQ-VSSQ nets were biased via RF probes. The VDD-VSS nets + chip_enable (+ possibly RP pad) were biased via dc probes.

The measurement sessions leading to the measured responses collected in this report have been held at the Philips - MiPlaza laboratory, Eindhoven for the first test case and at the research laboratory of IT for the second one. The next subsections collect the measurement results.

2.2.1 First test case (on-wafer measurements)

The setup used for the collection of the two-port S parameters of the VDDQ-VSSQ power supply structure of the first test case is shown in Fig. 13. In this setup, two RF probes are connected to the first and to the last couples of the VDDQ-VSSQ pads. Some DC probes are possibly connected to other pads to bias the device instead. The position of the DC probes depends on the specific device and its information is retrieved by the datasheet.

Figure 14 shows a selection of the scattering responses of the VDDQ-VSSQ structure that are collected for the case of biased and unbiased devices, thus confirming the same smooth behavior for the two different configurations. Also the responses of Fig. 14 suggest that the bandwidth of interests is certainly less than 10 GHz (the magnitude of S21 is ~60dB at 10GHz), being reasonable to limit the bandwidth to about 2GHz.

Figure 15 collects the same set of responses for the biased case (see the black curves) compared to the responses obtained by moving the position of the second RF probe P2 closer to the probe P1 (see the gray curves). This Figure highlights that very small differences are obtained, thus confirming the lumped behavior of the power supply rails for this first test case. Owing to this, lumped equivalents defined by the cascaded connection of lumped cells can be effectively used for the power delivery structures we are interested in (see Fig. 16, where each basic cell is a lumped equivalent defined by a RLC cell like the one of Fig. 11). As a first simplification, the ZP element is neglected since the parasitic capacitance of the supply rails is much less than the typical values of the buffer capacitance. From the measured response it is expected that the contribution of the buffer behavior dominates. As a further simplification, the possible substrate contributions have not been considered.
Figure 13. Setup for the collection of the two-port S parameters of the VDDQ-VSSQ power supply structure of the example device from on-die measurements.

Figure 14. Selection of scattering responses of the VDDQ-VSSQ structure. Solid line: S11; Dashed line: S21; Red: measurements carried out with DC bias (biased case); Blue: measurements carried out with DC bias (unbiased case).

Figure 15. Selection of scattering responses VDDQ-VSSQ structure obtained by moving the position of the second RF probe P2 (biased case). Black curves: reference responses of Fig. 14; Gray curves: responses obtained by moving P2 closer to P1.

In order to estimate the model parameters of the structure of Fig. 16, the following procedure is applied:

1. **Estimation of the shunt (parallel) element CB.** The scattering responses are converted into the frequency-domain impedance matrix $Z$ (see Fig. 17). From the low frequency behavior of the curves of Fig. 17, the total contribution of the CB capacitors is estimated. It is worth noting that at f=10 MHz, the impedance $Z_{11}$ behaves as a capacitor (the phase is -90 deg).

   @ f=10 MHz, $|Z_{11}|$ dB $=43.4$ dB

   $Z_{11} = 1/j\omega C_{\text{TOT}} \rightarrow C_{\text{TOT}} = 0.1\text{nF (biased case)}$ (140 pF for the unbiased case)

   $C_{B} = C_{\text{TOT}}$/number of I/Os (16 in the first test case) $\approx 6.3$ pF

2. **Estimation of the series element $Z_{S}$.** Similarly, the scattering responses are converted into the frequency-domain admittance matrix $Y$ (see Fig. 18). From the low frequency behavior of the curves of Fig. 18, the total contribution of the different $Z_{S}$ is estimated. Within the range 10-
100MHz, the phase of the Y11 network function is approximately zero, thus allowing the computation of the R value (in this frequency range, the effects of the inductance can be certainly neglected).

@ 10 MHz, \( R_{TOT} = 36.5 \text{ Ohm (biased case)} \) (37 Ohm for the unbiased case)

16 basic cells \( \rightarrow R \) (single cell) \( \approx 1.6 \Omega \)

For the additional inductance \( L \) and shunt capacitance \( C \), the values obtained from the EM simulations can be used as an initial guess when they are available. As an alternative, their value will be considered zero.

As an example, Fig. 19 collects the comparison between the measured scattering responses (for biased case) of Fig. 14 and the responses obtained by a simple SPICE simulation of the structure of Fig. 16 with the values of the parameters estimated as outlined above. From this first comparison, the good accuracy of the predicted responses is verified. If needed, improved results can be obtained via the fine tuning of the structure / model parameters (\( L \), substrate,...). This can be effectively done via possible optimization features embedded in commercial EDA tools like the Agilent ADS.

---

**Figure 16.** Model structure assumed for the VDDQ-VSSQ power supply rail. \( Z_s = R + sL; \ Z_T = 1/sC; \ C_B = I/O \) (buffer) capacitance.

**Figure 17.** Selection of the entries of the network functions defined by the impedance matrix \( Z \) obtained by converting the scattering responses of Fig. 14 for the biased case.
2.2.2 First test case (on-board measurements)

In order to verify the effects of the different states of the I/O buffers on the power rails model, a second set of measurements were carried out on the first test case. This second set was done by using an existing test board, developed by Numonyx, where the die is mounted on a memory module on top of the board (see Fig. 20). More details on the board are collected in the Deliverable D1.2 Report. As already done in the previous sections, two RF probes were used for the measurement of the 2-port scattering responses along the VDDQ-VSSQ networks. Of course, no DC probes were needed in this case because the power supply and the memory configuration were provided by the board itself.

Figure 18. Selection of the entries of the network functions defined by the admittance matrix \( Y \) obtained by converting the scattering responses of Fig. 15 for the biased case

Figure 19. Comparison between the measurements and the simulation of the model structure of Fig. 17 for the specific values of the parameters estimated for the first test case.

Figure 20. Test board used for the on-board measurements.

Figure 21. Selection of scattering responses of the VDDQ-VSSQ structure. Solid line: S11; Dashed line: S21; Blue: measurements carried out via the on-wafer measurements. 1. Gray curves: on-board measurements carried out by forcing the buffers in different stats (e.g., all the I/Os in high state, low state)
Figure 21 shows a selection of the scattering responses, obtained for different configurations of the buffers states. The curves in this Figure highlight that the low frequency behavior of the scattering responses collected via the on-wafer measurements are corrupted by the board itself (and in particular by the voltage regulators and the circuitry on the board that are connected to the power pads via the bonding wires). Owing to this, the modeling procedure can be hardly applied.

2.2.3 Second test case (Third parties device)

As previously anticipated, the second test case considered for extracting the power network model is a third party 512Mb DDR Mobile RAM in 70nm technology, with a data bus x16 and working at 133MHz [6].

This device operates with a 133 MHz clock, but it uses both the edges of the clock cycle. Hence, it produces data at an equivalent clock rate of 266 MHz, in fact it is a Double Data Rate (DDR) RAM memory. Although the output data have a double data rate throughput the internal core circuitries operates at only the 133 MHz clock rate.

In such a device the VDDQ/VSSQ pads are distributed on a unique side, at a reciprocal distance of 80μm, while the VDD/VSS pads are on both sides (figure 22). The VDD and VDDQ supply voltage values are equal to 1.8V.

The measurements have been mainly concentrated on-wafer (both unbiased and biased) (see Fig.23 (a) and (b)). In these figures it is worth observing that the behavior of scattering responses changes moving the reciprocal positions of RF probes. As a result, the lumped assumption is less valid than the first test case. In addition, considering the higher working frequency of DDR device, it is mandatory to get an accurate distributed model. Nevertheless, it is a third parties device and usually the external supplier provides only the equivalent capacitance, which cannot be enough at all to carry out reliable signal integrity analysis. This result confirms once again the importance of MOCHA project, aimed at overcoming such limitations through the identification of a methodology for extracting by measurements a most accurate model.

Besides, the same modeling procedure of Sec. 2.2.1 is applied to build the model of the VDDQ-VSSQ structure. In details:

1. **Estimation of the shunt (parallel) element CB.** The black scattering responses of Fig. 23 are converted into the frequency-domain impedance matrix \( \mathbf{Z} \) (see Fig. 24). From the low frequency behavior of the curves of Fig. 24, the total contribution of the CB capacitors is estimated. Also in this case, at \( f=10\text{MHz} \), the impedance \( Z_{11} \) nearly behaves as a capacitor (the phase is \( \sim -90 \text{deg} \)).

   @ \( f=10\text{MHz} \), \(|Z_{11}|\text{dB}=43.4\text{ dB}\)

   \[ Z_{11} = \frac{1}{j\omega C_{\text{TOT}}} \rightarrow C_{\text{TOT}} = 0.32\text{nF (unbiased case)} \]

   \[ C_{\text{B}} = C_{\text{TOT}}/\text{number of I/Os (16 in the second test case)} \approx 20\text{pF} \]
2. *Estimation of the series element* $Z_S$. Similarly, the scattering responses are converted into the frequency-domain admittance matrix $Y$ (see Fig. 25). From the low frequency behavior of the curves of Fig.25, the total contribution of the different $Z_S$ is estimated.

@ 10 MHz, $R_{TOT} = 42.34 \text{ Ohm}$

8 basic cells $\rightarrow R \text{ (single cell)} \approx 5.3 \ \Omega \text{(unbiased case)}$

It is worth noting that the total series resistance (the $R_{TOT}$ parameter above) can be used to define a first rough model for the VDDQ-VSSQ network that consists of the cascaded connection of 8 identical cells, thus leading to a basic cell of Fig. 16 with $Z_s = R_s + sL$ where $R_s = 5.3 \ \Omega$. However, if needed (and this is what is done in this study), a more refined model can be obtained by defining different values of the series resistance of each cell that account for the real length of the rails within two adjacent pairs of the power supply pads. The information on the length (that is used to distribute the value of $R_{TOT}$ in the different cells) can be obtained from the BSA scheme like the one of Fig. 22.

In this case, the initial guess of L and C of the structure of Fig. 16 is zero. No detailed information on the physical structure of the rails was available for this test case.

Figure 26 collects the comparison between the measured scattering responses (for the unbiased case) of Fig. 23 (a) and the responses obtained by a simple SPICE simulation of the structure of Fig. 16 with the values of the parameters estimated as outlined above. From this second comparison, the
accuracy of the predicted responses is confirmed. Again, if needed, improved results can be obtained via the fine tuning of the structure / model parameters.

The same procedure has been applied to the biased curves of Fig. 23 (b), leading to the following parameters: $R_{TOT}= 27.7 \, \Omega$; $C_{TOT}= 0.56nF$. It is worth noting that the different values of the parameters come from: (i) the biasing of the chip and (ii) the use of a different set of measured response. The measured responses that have been used are those obtained with the probes P1 on the pad #7 (first couple of VDDQ/VSSQ in figure 22) and P2 on the pad #54 (for some mechanical constraints the position of the second probe on the last pair of supply pads, i.e., on the pad #66, was not possible).

![Graph A](image1)

**Figure 23 (a).** Selection of scattering responses VDDQ-VSSQ structure obtained by moving the position of the first RF probe P1 (unbiased case). Black curves: reference responses with P1 = pad #7 and P2= pad #66; Gray curves: responses obtained by moving P1 closer to P2.

![Graph B](image2)

**Figure 23 (b).** Selection of scattering responses VDDQ-VSSQ structure obtained by moving the position of the first RF probe P1 (biased case). Black curves: reference responses with P1 = pad #7 and P2= pad #54 (for mechanical constraints pad #66 was not accessible); Gray curves: responses obtained by moving P1 closer to P2.

![Graph C](image3)

**Figure 24.** Selection of the entries of the network functions defined by the impedance matrix $Z$ obtained by converting the black scattering responses of Fig. 23 (a).
3. IC core power rails and coupling models

The modeling approach that is proposed for the generation of the IC core power delivery network model, as well as of its coupling one with the I/O network, can be briefly summarized into the following steps:

- Assume the most suitable model structure for the different power delivery subsystems;
- Collect the measured scattering responses of the IC power delivery structure;
- Compute model parameters by fitting the measured and the model responses.

The following subsections collect a detailed description of the above three steps and of the obtained results for the first and second test case.

3.1 Model structure and parameter estimation

As described above, for the VDD/VSS power distributions supplying the internal circuitry of the device, a lumped equivalent was assumed. These distribution networks have a limited number of external pads and, in addition, the internal structure of the power rails cannot be described in terms of a limited number of topologies, as for the VDDQ/VSSQ case. Thus forcing a lumped characterization from S-parameter measurements, only.

Moreover, the EM simulations and the measurements results have confirmed that a lumped behavior holds and that lumped equivalents can be effectively used for the power delivery structures we are interested in.

It is worth to remark that the power network of a digital IC consists of different weakly-coupled structures. For the example of the study, the different structures are the VDD-VSS network, which supplies the core circuitry, and the VDDQ-VSSQ power rail, which supplies the I/O buffers. All these parts have been designed to be uncoupled, so that their characterization as separate parts is allowed.
For this example, under the assumption of weakly coupled networks, we concentrated on the separate two-port characterization/modeling of the two networks and on the possible coupling effects among VDD-VSS and VDDQ-VSSQ.

The model structures assumed for the modeling of the core power networks are either simplified T or Y equivalent circuits or purely black-box equivalents based on real rational approximations (see Fig. 27 for the classification). Details on the estimation of the model parameters will be given in Sec. 3.1.3. These different model structures are considered to assess their possible strengths and limitations for the problem at hand and to provide the users with a selection of models with different complexity and accuracy levels.

(i) T equivalent

\[
Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_1(s) + Z_3(s) & Z_3(s) \\ Z_3(s) & Z_2(s) + Z_3(s) \end{bmatrix}
\]

(ii) Y equivalent

\[
Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_1(s) + Y_3(s) & -Y_3(s) \\ -Y_3(s) & Y_2(s) + Y_3(s) \end{bmatrix}
\]

(iii) Black-box

\[
S(s) = \sum_n \frac{R_n}{s - p_n}
\]

Figure 27. Simplified equivalent structures assumed for the different supply distribution networks and the corresponding two port matrix representations: (i) T lumped equivalent and its Z representation, (ii) Y lumped equivalent and its Y representation and (iii) black-box element defined by a real rational scattering matrix.

For the modeling of the core power delivery network, ports P1 and P2 of the structures of Fig. 27 are the two couples of VDD-VSS pads. Finally, coupling effects are modeled by defining P1 and P2 as couples of pads of different power delivery networks: VDDQ-VSSQ and VDD-VSS, respectively.

3.1.2 First test case (on-wafer measurements)

As outlined in the previous Section, two-port scattering responses have been considered. The different measurements collected in this report have been carried out via RF probing on different dies on a wafer.

As an example, Fig. 28 shows the setup used in the Miplaza lab for the measurement of the 2-port scattering responses of the VDD-VSS network. The Figure highlights the RF probes connected to the two pairs of pads (i.e., the ports P1 and P2 of the model structures of Fig. 27) and the DC probes used to bias the device (the configuration/position of the DC probes must be adapted to the proper...
specifications of each device being measured, which must be provided by the device designer/manufacturer).

Figure 29 shows a selection of scattering responses measured by the setup of Fig. 28 for different dies. The gray curves represent five sets of measurements on different biased dies and the blue curves are instead the measurements on unbiased dies (in this case, the DC probes shown in Fig. 28 were disconnected). It is worth noticing that the differences between the curves for the biased and the unbiased case at low frequency are very small (on the order of 2-3 dBs).

![Figure 28. Setup for the collection of the two-port S parameters of the VDD-VSS power supply structure of the first test chip from on-die measurements.](image)

Figure 29. Selection of the scattering responses of the VDD-VSS network. Solid lines: S11; dashed lines: S21. The gray and the blue curves represent measurements on different biased and unbiased dies, respectively (see text for details).

Finally, Figure 30 shows the scattering responses measured by setting ports P1 and P2 on different power delivery networks: VDDQ-VSSQ and VDD-VSS, respectively. These measurements will be possibly used to understand the behavior of the coupling effects among the different supply networks.
Figure 30. Selection of the scattering responses for the coupling of the VDDQ-VSSQ (Port P1) and of the VDD-VSS (Port P2) structures. Solid lines: S11; dashed lines: S21. Port P1 is defined by the VDDQ-VSSQ couple of pads surrounding the DQ11.

3.1.3 Computation of model parameters and results (first test case)

This Section summarizes the results on the generation of the models of the power structures outlined in Sec. 3.1.2.

As a first set of modeling experiments, the measured 2-port scattering responses of the VDD-VSS network have been used to generate possible alternative models with different accuracy and complexity.

Figure 31. Selection of the scattering responses of the VDD-VSS structure. Solid lines: reference measured responses; dashed lines: responses of the model defined by the structure on the right (C=1.4nF).
The qualitative behavior of the responses of Fig. 29 suggests that the VDD-VSS structure has a dominant capacitive behavior. The simplest model we considered is therefore a shunt capacitor only (this model structure belongs to the class (i) of Fig. 27 where $Z_1$ and $Z_2$ are short circuits and $Z_3 = 1/sC$). $C$ can be estimated by fitting the reference and the model responses in a low frequency region (e.g., at $f=10$MHz). Figure 31 compares the reference and the model responses for this simple case, thus highlighting the qualitative behavior of the measured responses is reproduced well and that the accuracy is very good in the low frequency region only.

In order to improve the accuracy of the first rough model, a second model defined by a structure belonging to the class (ii) has been considered. As in the first case, the circuit elements have been selected on the basis of the physical interpretation of the qualitative behavior of the measured responses ($Z_1 = 1/sC$, $Z_2 = 1/sC$ and $Z_3 = R_8$). The curves of Figure 32, that shows the comparison between the reference and the model responses for the latter assumption, confirms that a very good accuracy can be obtained via refined physically-based models.

![Figure 32. Selection of the scattering responses of the VDD-VSS structure. Solid lines: reference measured responses; dashed lines: responses of the model defined by the structure on the right ($C=1.4nF$, $R_8=4\Omega$).](image)

If needed, a black-box approach is always available for the generation of black-box models belonging to the class (iii) of Fig. 27. The key resource in this step is the application of the state-of-the-art techniques for the generation of a reduced order rational approximation, reproducing the port behavior of a complex linear structure from its port responses. This approximation is performed via the powerful and well-known Vector Fitting (VF) algorithm [4], with an a-posteriori correction to enforce the passivity of the obtained rational model [5], as explained in Section 2.1.3.

As an example, a black-box model defined by a rational function with 12 poles has been generated via the IdEM tool. Figure 33 shows the comparison between the reference and the black-box model responses for this example test, thus highlighting the very good accuracy achieved by this latter black-box approach. However, the increased accuracy and complexity is not justified for the specific case of the VDD-VSS structure for which the physics-based models offer a simpler solution with a reasonable accuracy.
3.1.4 Second test case (on-wafer measurements)

As already done in the previous Sections, on-wafer measurements have been carried out on the second test case. All the measurements have been done for the unbiased and biased cases.

Figures 34 and 35 show, respectively, the comparison between the measurements and the simulations of the (i) and (ii) possible models of Fig. 27 for the VDD-VSS structure of this test case. The approach followed for estimating the C and Rs values has been exactly the same described in the before section. It is worth noticing in figure 34 (b) for biased case the excellent agreement with an equivalent model with a lumped capacitor. In this case the model (i) of fig.27 is sufficient to achieve a good accuracy and no additional improvement is obtained extracting the model (ii).

Figure 34 (a). Selection of the scattering responses of the VDD-VSS structure in unbiased case. Solid lines: reference measured responses; dashed lines: responses of the model defined by the structure on the right (C=0.45nF).
Figure 34 (b). Selection of the scattering responses of the VDD-VSS structure in biased case. Solid lines: reference measured responses; dashed lines: responses of the model defined by the structure on the right (C=6.5nF).

Figure 35. Selection of the scattering responses of the VDD-VSS structure in unbiased case. Solid lines: reference measured responses; dashed lines: responses of the model defined by the structure on the right (C=0.45nF, \( R_s = 0.9\Omega \)).

Finally, Figure 36 shows a selection of the 2-port scattering responses carried out between a VDD-VSS and a VDDQ-VSSQ couple of pads. The figure highlights that the coupling effects between the core and I/O power distribution networks is negligible and does not need to be taken into account.
3.1.5 Model accounting for the coupling effects

For the two test cases considered in this study, the coupling among the different supply subsystems is extremely low and does not justify the generation of specific models accounting for this effect.

In fact, the S21 scattering parameters of both the first test case (Fig.30) and the second one (Fig.36) are less than -50dB in the upper range of frequencies. Considering that the coupling effects have an influence especially at higher frequency, the obtained results confirm that they could be neglected for the analyzed test cases.

However, if needed, a pure black-box approach can be effectively used (and it is recommended) to generate the most suitable coupling model. The scattering responses could be effectively processed as done for the latter example of Sec. 3.1.3.

4. Additional results on a test-chip

As an additional set of experiments, the same on-wafer measurements have been carried out on a new test chip designed by Nromyx in 90nm technology, with a Low Power DDR interface for I/O buffers and a clock frequency of 166MHz. This innovative test chip includes only I/O buffers circuitry, so only the VDDQ-VSSQ power rails has been considered. In the figure 37 the layout of the I/O circuitry has been reported.
This device shows 9 signals, everyone surrounded by a couple of VDDQ-VSSQ. The VDDQ supply voltage value is equal to 1.8V.

It is worth noting that this test case has been considered as an additional chip that were not required in the original MOCHA work plan. It has been included to stress the proposed methodology as well as to possibly contribute to the inclusion of a larger number of devices of interest. The additional efforts that are going to be spent for this additional example will allow the researchers involved in this activity to tune the proposed model structures and modeling methodology.

Figure 39 shows a selection of the scattering responses of the VDDQ-VSSQ structure of this device carried out as in the first two test cases. Two RF probes are connected to two VDDQ-VSSQ couple of pads of the power rail (Fig.38). Once again the target is to collect the responses for both unbiased and biased cases, even though the only unbiased data are reported in this report because it has been delivered while the biased ones were still in progress. The measurements compare the scattering responses obtained by moving the position of the two probes. The black curves collect the measurements with the two RF probes connected to the first and the last couple of pads as reported in the figure 38.

![Figure 38. Setup for the collection of the two-port S parameters of the VDDQ-VSSQ power supply structure](image)

The gray curves collect the responses obtained by moving the second probe closer to the first one instead. Again, the smooth and lumped behavior of the responses of this power delivery structure is confirmed.

![Figure 39. Selection of unbiased scattering responses of VDDQ-VSSQ structure obtained by moving the position of the second RF probe closer to the first one (see text for details). Black curves: reference responses; Gray curves: responses obtained by moving the two probes closer.](image)
The same modeling procedure of Sec. 2.2.1 is applied:

1. *Estimation of the shunt (parallel) element CB.* The black scattering responses of Fig. 40 are converted into the frequency-domain impedance matrix \( Z \) (see Fig. 40). From the low frequency behavior of the curves of Fig. 40, the total contribution of the CB capacitors is estimated. Also in this case, at \( f=10\) MHz, the impedance \( Z_{11} \) nearly behaves as a capacitor (the phase is \( \sim -90\) deg).

   \[ @ \ f=10 \ \text{MHz}, \ |Z_{11}| dB = 32.2 \ \text{dB} \]

   \[ Z_{11} = \frac{1}{j\omega C_{\text{TOT}}} \rightarrow C_{\text{TOT}} = 0.39\ \text{nF} \]

   \[ C_B = C_{\text{TOT}}/\text{number of I/Os (9 in the test chip)} \approx 43.3 \ \text{pF} \]

2. *Estimation of the series element \( Z_S.\)* Similarly, the scattering responses are converted into the frequency-domain admittance matrix \( Y \) (see Fig. 41). From the low frequency behavior of the curves of Fig. 41, the total contribution of the different \( Z_S \) is estimated.

   \[ @ \ 10 \ \text{MHz}, \ R_{\text{TOT}} = 3.34 \ \text{Ohm} \]

   \( 9 \) basic cells \( \rightarrow R \) (single cell) \( \approx 0.37 \ \Omega \)

In this case, the initial guess of \( L \) and \( C \) of the structure of Fig. 17 is zero.

Figure 42 collects the comparison between the measured scattering responses (for the unbiased case) of Fig. 39 and the responses obtained by a simple SPICE simulation of the structure of Fig. 16 with the values of the parameters estimated as outlined above. From this additional comparison, the accuracy of the predicted responses of \( S_{11} \) is confirmed within all the bandwidth of interest. On the other hand, some improvements on the \( S_{21} \) function in the high frequency can be further considered via the fine tuning of the structure / model parameters.

![Figure 40](image1.png)

**Figure 40.** Selection of the entries of the network functions defined by the admittance matrix \( Z \) obtained by converting the black scattering responses of Fig. 39.

![Figure 41](image2.png)

**Figure 41.** Selection of the entries of the network functions defined by the admittance matrix \( Y \) obtained by converting the black scattering responses of Fig. 39.
5. Simulation data validation

In order to validate the procedure for extracting equivalent impedance for power rail by simulation, a comparison with the results obtained by measurements is reported for every test case considered in the previous sections.

5.1 First Test Case

For the internal test case, equivalent impedance for I/O power rail was extrapolated via a detailed full-chip simulation, including in the netlist both parasitic diodes and resistance-capacitance values of rail (the so called back-annotated netlist). In the figure 43 the comparison between equivalent impedance from measurement and simulation is reported for the first test case in biased case. The good agreement up medium frequencies, on one side demonstrates the good accuracy of the used methodology and, on the other side, confirms its limitation to extrapolate a reliable wide-frequency-range model.
Figure 43. Comparison between the measurements and the simulation for first test case I/O power rail in biased case

Moreover, in the Table I is reported the comparison between the total capacitance value of I/O power rails extracted by simulation and measurement. They confirm once again the good agreement at low frequency.

<table>
<thead>
<tr>
<th></th>
<th>C_{TOT} (Biased)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Meas.</td>
<td>100 pF</td>
</tr>
<tr>
<td>Sim.</td>
<td>110 pF</td>
</tr>
</tbody>
</table>

Table I

About the core power rail model, moreover a comparison has been carried out between the estimated total capacitance $C_{TOT}$ obtained from the measurements and the values obtained via a simplified full-chip simulation for biased case. Some differences are noticed in biased case and they will be addressed. Fig. 44 shows the S21 measured scattering response of the VDD-VSS network superimposed to the curve obtained by simulation. It is worth noting that for the VDD-VSS network, the comparison concentrates on the scattering responses to avoid the conversion of the measurements into the Z parameters in a frequency range where S11 is nearly constant and equal to 1.

![Figure 44](image-url)

Figure 44. Comparison between the measurements and the simulation for first test case core power rail in biased case

The Table II reports the comparison between the estimated total capacitance values from measurements and simulations.

<table>
<thead>
<tr>
<th></th>
<th>C_{TOT} (Biased)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Meas.</td>
<td>2 nF</td>
</tr>
<tr>
<td>Sim.</td>
<td>900 pF</td>
</tr>
</tbody>
</table>

Table II

Page 33 of 37
5.2 Second Test Case

For external test case generally only a capacitance value or impedance for I/O power rail is provided by supplier. This unique value is not sufficient to perform reliable signal integrity simulations especially for devices that work with high working frequency as seen in Section 2.2.3. This is confirmed by figure 45 that reports the comparison in biased case between measurement and simulation that includes the only equivalent capacitance calculated by external supplier (blue curves).

![Graph showing comparison between measurement and simulation](image)

Figure 45. Comparison between the measurements and the simulation for external test case I/O power rail in biased case

The Table III reports the comparison between the estimated total capacitance obtained from the measurements and the value of capacitance provided by external supplier for I/O power rail.

<table>
<thead>
<tr>
<th></th>
<th>C&lt;sub&gt;TOT&lt;/sub&gt; (Biased)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Meas.</td>
<td>560 pF</td>
</tr>
<tr>
<td>Sim.</td>
<td>776 pF</td>
</tr>
</tbody>
</table>

Table III

Fig. 46 shows the S21 measured scattering response of the VDD-VSS network superimposed to the curve obtained by External supplier.
The Table IV reports the comparison between the estimated total capacitance obtained from the measurements and the value of capacitance provided by external supplier of the core power rail structure.

<table>
<thead>
<tr>
<th></th>
<th>C\text{TOT} (Biased)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Meas.</td>
<td>6.5 nF</td>
</tr>
<tr>
<td>Sim.</td>
<td>9.8 nF</td>
</tr>
</tbody>
</table>

Table IV

5.2 Third Test Case

At the end, through the same procedure used in the first test case, equivalent impedance for I/O power rail was extrapolated for test chip. In figure 47 the comparison between equivalent impedance extracted by simulation and measurement is reported for unbiased case. It is worth noticing the importance to extract an accurate impedance to perform reliable signal integrity, considering the higher working frequency of this device (333MHz).
Figure 47. Comparison between the measurements and the simulation for test chip I/O power rail in unbiased case

For the same test case the total capacitance value extracted by simulation and measurement is reported for unbiased values in the table V.

<table>
<thead>
<tr>
<th>$C_{TOT}$ (Unbiased)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Meas.</td>
<td>390 pF</td>
</tr>
<tr>
<td>Sim.</td>
<td>500 pF</td>
</tr>
</tbody>
</table>

Table V
6. References


Appendix

List of Acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BSA</td>
<td>Build Sheet Assembly</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer Aided Design</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
</tr>
<tr>
<td>EM</td>
<td>Electro Magnetic</td>
</tr>
<tr>
<td>FFIB</td>
<td>Fast Flash Interface Board</td>
</tr>
<tr>
<td>GDSII</td>
<td>Graphic Data System II</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
</tbody>
</table>