SEVENTH FRAMEWORK PROGRAMME
THEME [ICT-1-3.1]
Next-Generation Nanoelectronics Components and Electronics Integration

Deliverable Report

Work Package 1 – IC power integrity model

Deliverable D1.2 - Report describing the simulation and measurement approach for extracting the IC core "switching activity" model. Models of proprietary and third party IC devices.

Contract no.: 216732
Project acronym: MOCHA
Project full title: MOdelling and CHAracterization for SiP Signal and Power Integrity Analysis
Start date of project: 1st January 2008
Duration: 2 years

Instrument: Small or medium-scale focused research project - STREP

Report responsible partner: Numonyx Italy Srl
Report preparation date: 27/02/2009
Dissemination level: PU

Project coordinator: Antonio Girardi
Project coordinator organization: Numonyx Italy Srl

Revision: 1.0

Content

1. Introduction....3
2. Core Switching Activity Model Proposed by IEC 3
3. IC core “switching activity” model by simulation for proprietary device....4
4. IC core “switching activity” model by simulation for third parties device 9
5. Measurement of “core switching activity” current....11
5.1 Supply Current Characterization....13
5.2 Buffer Characterization....14
5.3 Board design 15
6. References 16
Appendix....16
List of Acronyms....16

1. Introduction

Nowadays, with increasing of IC performances, clock speed and faster transition time, Integrated Circuits (ICs) are ever more generating EMC (Electro Magnetic Compatibility) and EMI (Electro Magnetic Interference) problems in the modern electronic equipment and systems. The capability to predict by simulations EMC/EMI issues is becoming a topical demand for both IC manufactures and end-users. At this aim, IEC (International Electro technical Commission) proposes a standard model called ICEM (Integrated Circuit Electrical Model) [1] [2], registered as IEC 62014-3, for simulating conducted and radiated emission of the integrated circuits on printed circuit boards. This model is based on the knowledge of the current flowing in the overall power supply networks of IC+package+PCB.

Since the EMI/EMC issues are strictly related to the power integrity ones, it has been considered appropriate to start from ICEM for developing the power integrity model inside the MOCHA project. In fact, in such a way, the final model may be used for both applications.

The objective of Task 1.2 of WP1 is just to extract a simulation model, based on standard ICEM, which describes the internal switching activity of IC core for power integrity analysis.

In this derivable both approaches based on simulation and on measurement to extract IC "core switching activity" current will be described for proprietary and third parties devices.

2. Core Switching Activity Model Proposed by IEC

To model IC core switching activity, which represents the current flowing through all the IC core gates (Ivdd and Ivss) during high to low or low to high transitions (Fig.1), the standard ICEM proposes an equivalent current generator. It is represented by Ib generator in Fig. 2, where is reported the ICEM model related to an IC whose core and I/O buffers are supplied by two different rails (VDD Core and VDD I/O).

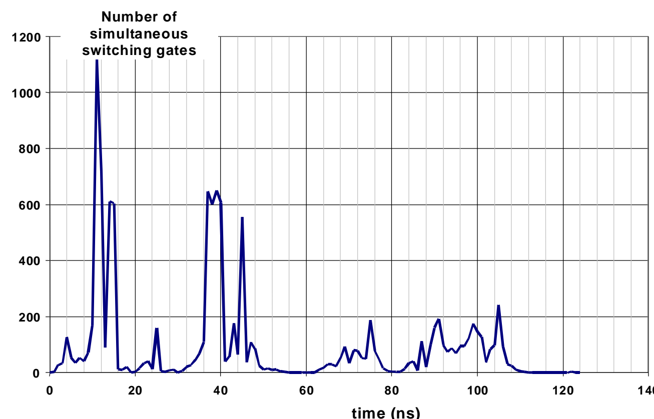

Fig.1 - Number of switching gates versus time

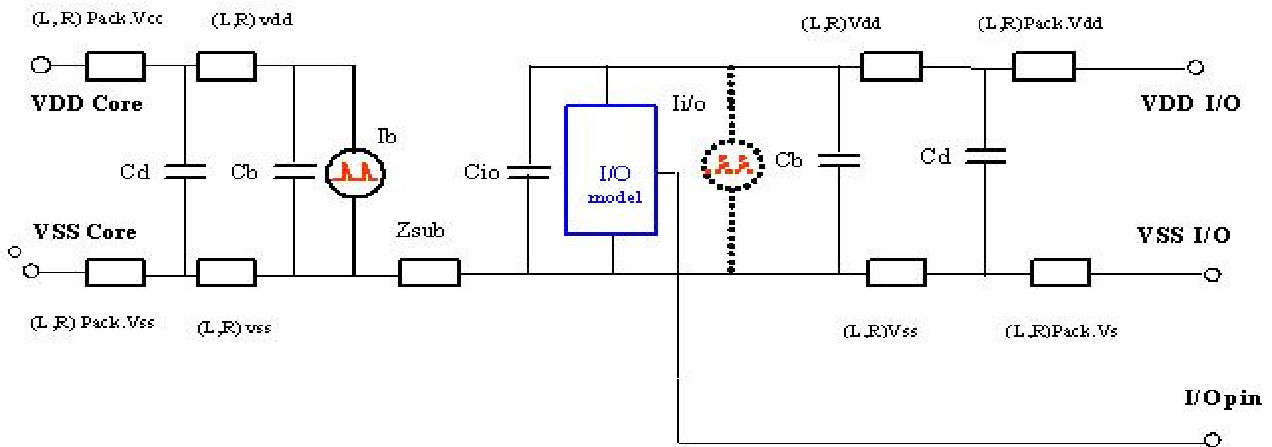

Fig.2 - Model of the IC supply lines suggested by ICEM

I/O buffers can be modeled in three different ways (PWL generators, IBIS models and SPICE models), while the "switching activity" of IC core can be modeled only by a PWL current generator due to the complexity of IC core circuitry.

3. IC core "switching activity" model by simulation for proprietary device

The first test case considered for extracting switching activity model is a 512Mb Numonyx NOR Flash memory in 90nm technology, whose pads distribution, even called BSA (Build Sheet Assembly), is reported in Fig.3.
As can be extrapolated from datasheet [3], the device, whose functional diagram is reported in fig.4, is supplied by two different power supply:

- ✓ VDDQ for the Input/Output pins.
- ✓ VDD for the Core circuitry.

For both, the nominal supply voltage value is 1.8V.

As a result, for VDD power rail an equivalent current generator should be extracted to take into account the overall switching activity of the device's core circuitry.
The memory may be erased electrically at Block level and programmed using VDD supply for the core circuitry and VDDQ for the Input/Output circuitry. It has a symmetrical Block architecture and is based on a Multi level cell technology. Moreover, it is composed by an array of 256 blocks and it is divided into 64Mbits banks.

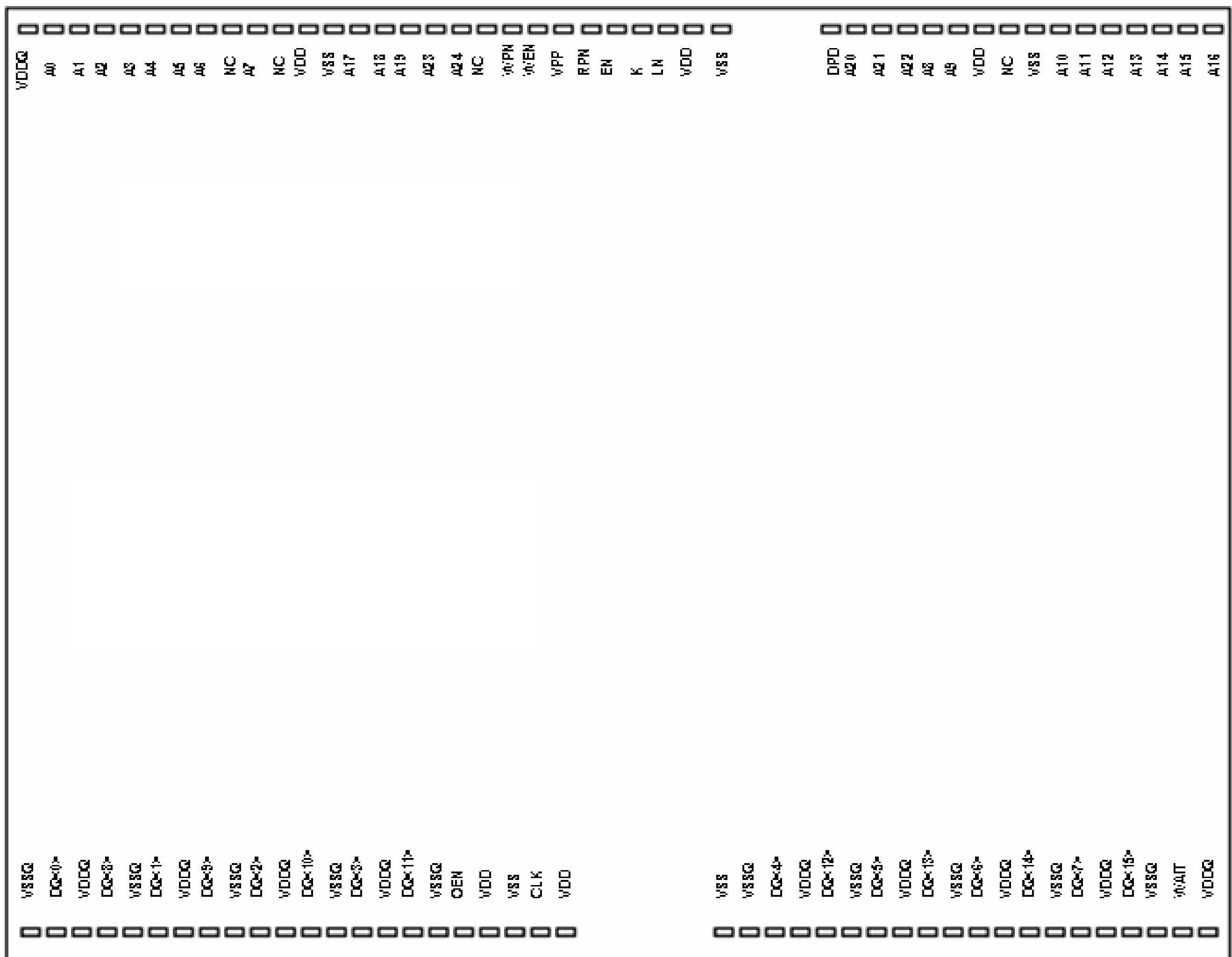

Fig.3 – BSA of the 512Mb Numonyx NOR Flash memory in 90nm technology

Besides erase and program operations, the device supports Synchronous Burst Read and Asynchronous Read from all blocks of memory. Burst mode read is a read operation synchronized with the rising or falling edge of clock (K in Fig.6). In this way the device offers improvements in speed and performance by reducing sequential read access time respect to asynchronous read. Unfortunately this operation requires extra-pins as latch (L#), clock (K) and WAIT . In synchronous burst read mode, the number of clock cycles, called latency, from when the address is valid up to when the first data become available, can be set by user (Fig.5). In this way the data is output on each clock cycle at frequencies of up to 108MHz. As data output, a byte (x8 burst length) or a word (x16 burst length) can be obtained. In fig.6 is reported a burst synchronous read timing with latency (X-latency).
Burst read synchronous operation is more critical in terms of core switching activity Vdd current.
Considering that the device carries out different operations (Burst Read, Erase and Program), it was decided to extrapolate an equivalent “switching activity” current generator for each one.

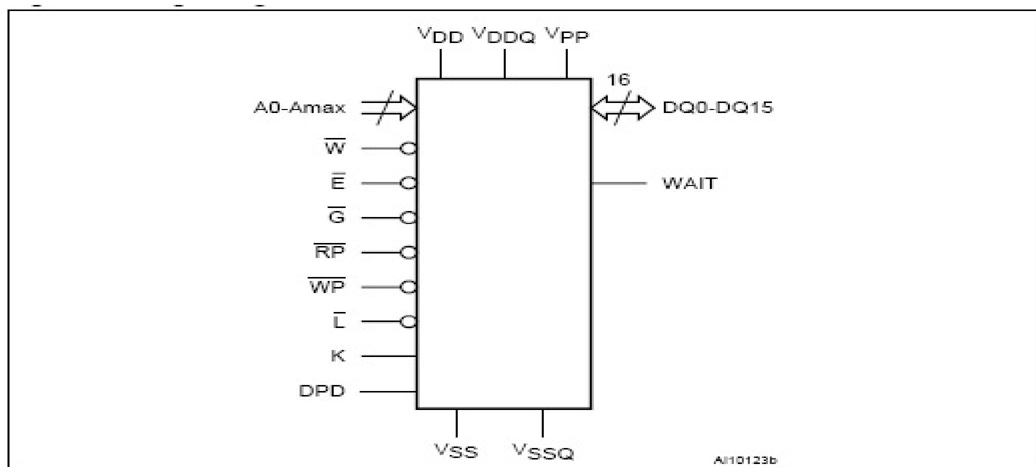

Fig.4 – Functional Diagram

f_{max}	t_{Kmin}	X-Latency
40MHz	25ns	4
54MHz	19ns	5
66MHz	15ns	6
108MHz	9ns	10

Fig.5 – X-Latency setting

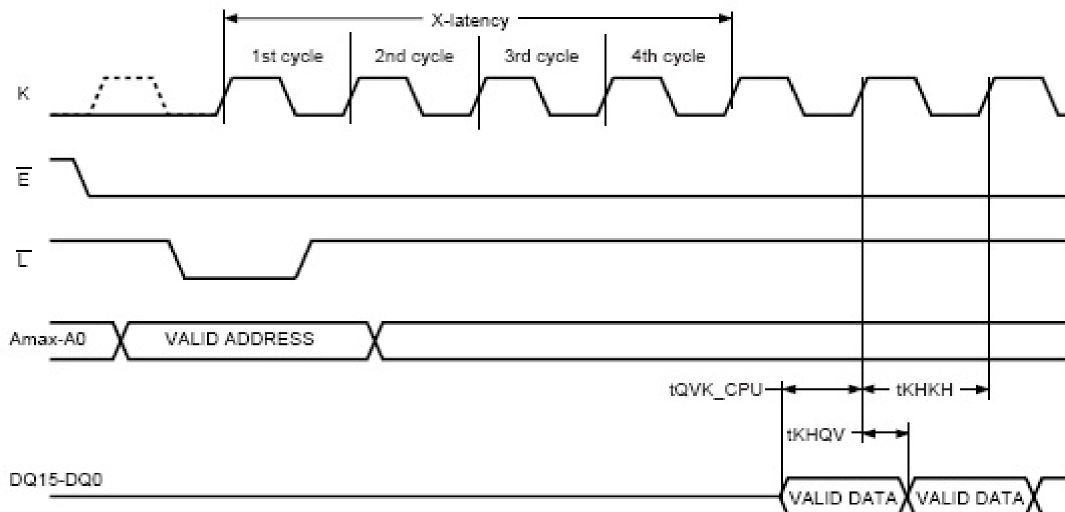

Fig.6 – Burst read timing

Since more ground and power pads are distributed along the VDD/VSS rails, it was difficult to estimate the unique resistance value advised in the ICEM model reported in Fig.2. As a result, it was decided to extrapolate a distributed model of resistances, keeping the VDD and VSS ports close with the actual pad distribution. Moreover, considering that the core circuitry is composed of different macro-blocks that together contribute to the total switching activity current, it was also decided to explode the current generator in more ones related to the main macro-blocks.

As a result, the switching activity model extracted for each operation is composed of a distributed model of resistances and of a group of macro-block equivalent current generators (Fig.7).

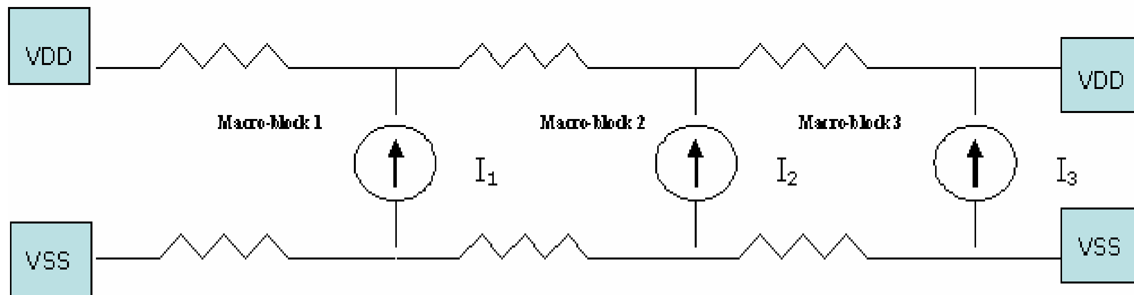

Fig.7 – Switching activity model for a specific operation

Therefore, the overall model will be composed of all current generators and the specific operation (erase, program and burst) is activated by turning on some switches (Fig.8).

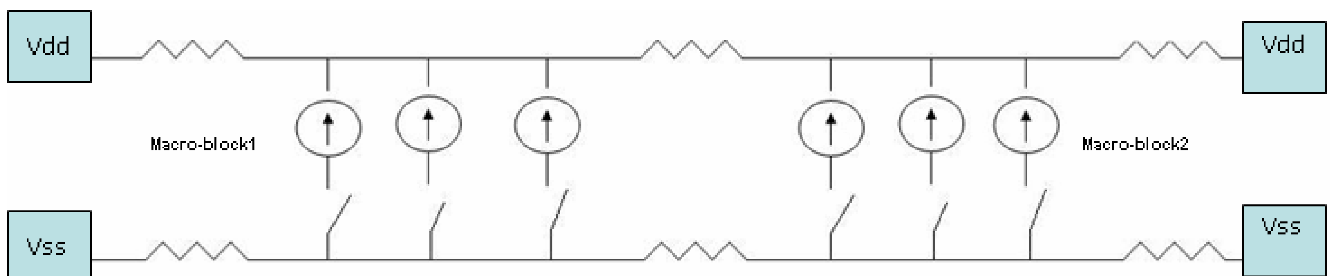

Fig.8 – Switching activity model for all operations

The inductance values of power rails were not included in the extracted model, because of the absence of a dedicated tool to extract them in a reliable way. For future measurement correlation, they might be estimated with an empirical value equal to 0.6nH/mm.

The simulations were carried out on full-chip netlists, inclusive of layout parasitic elements as capacitances, by a commercial fast-spice simulator.

In the following figures, are reported the simulation results of the global switching activity current for every working operation.

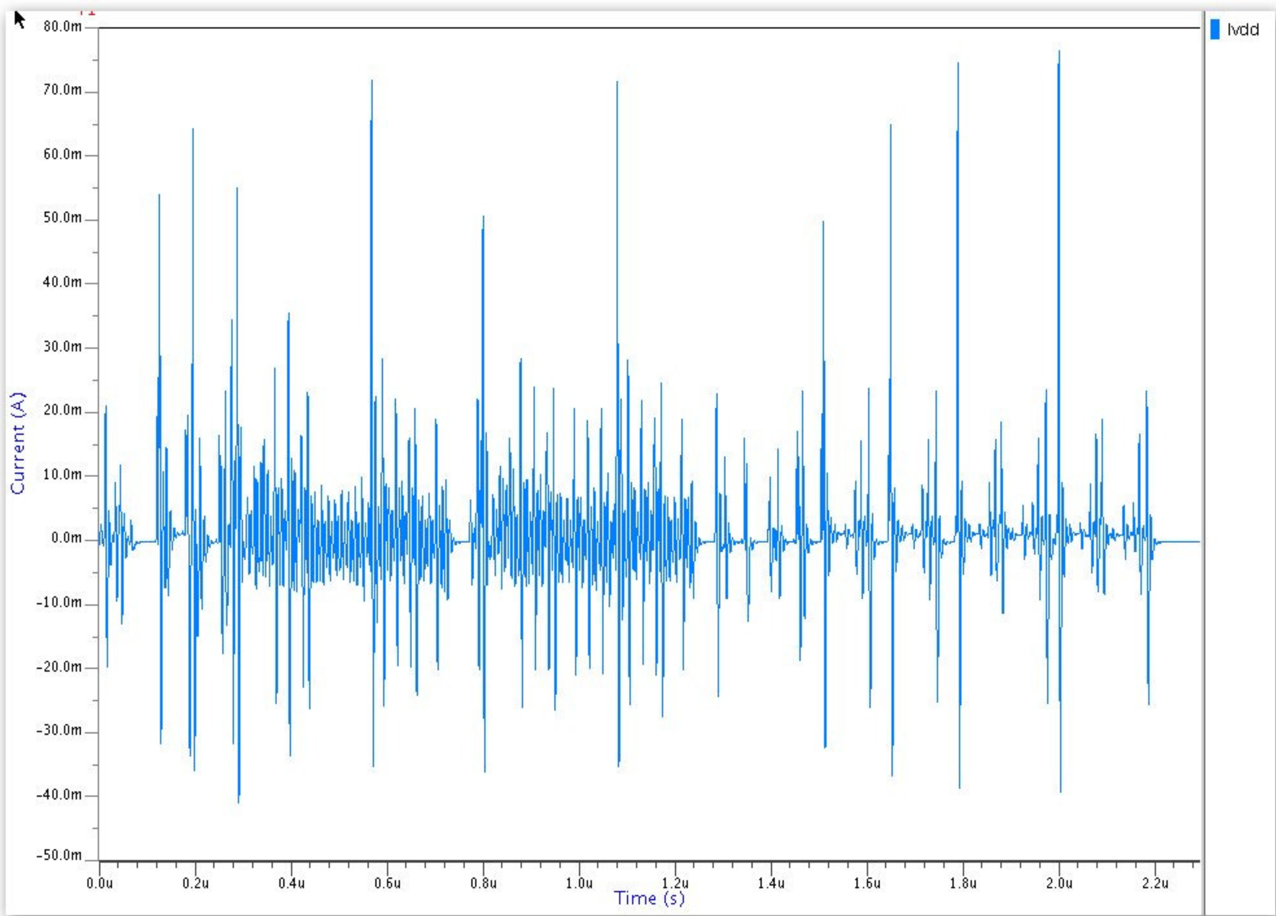

Fig.9 – Burst continuous-operation

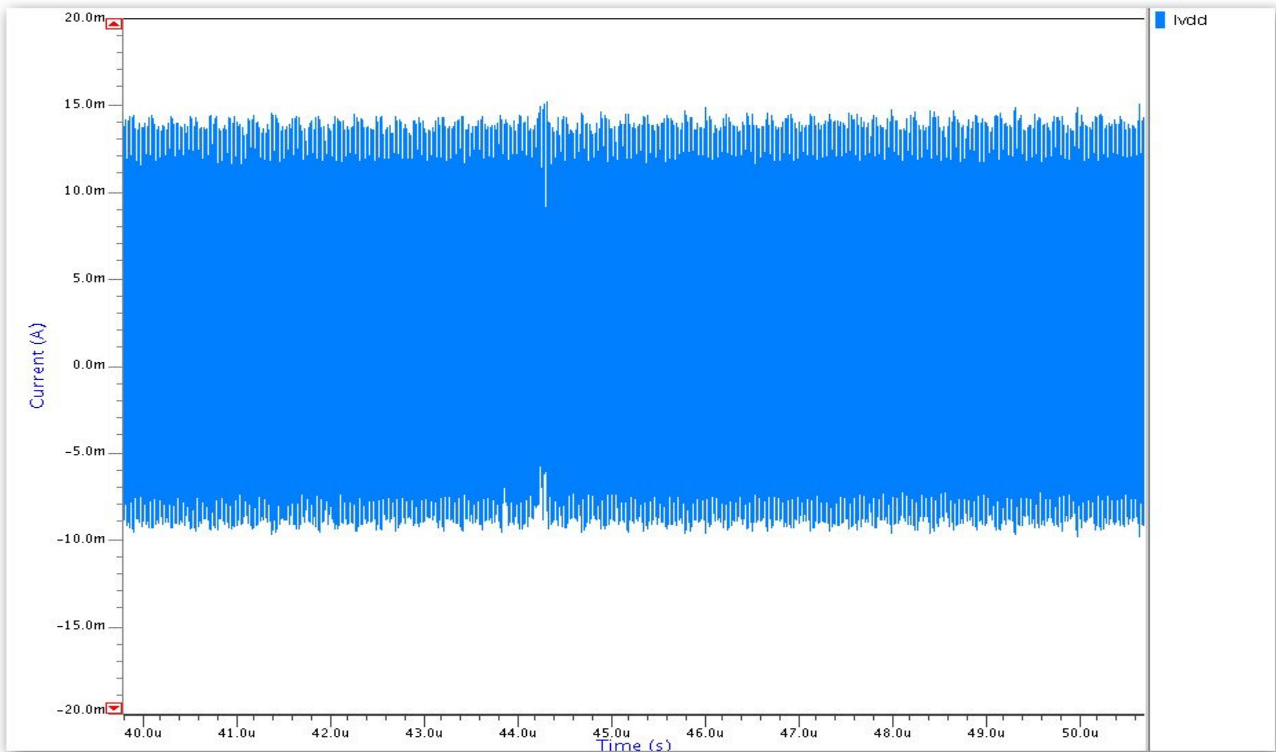

Fig.10 – Erase-operation

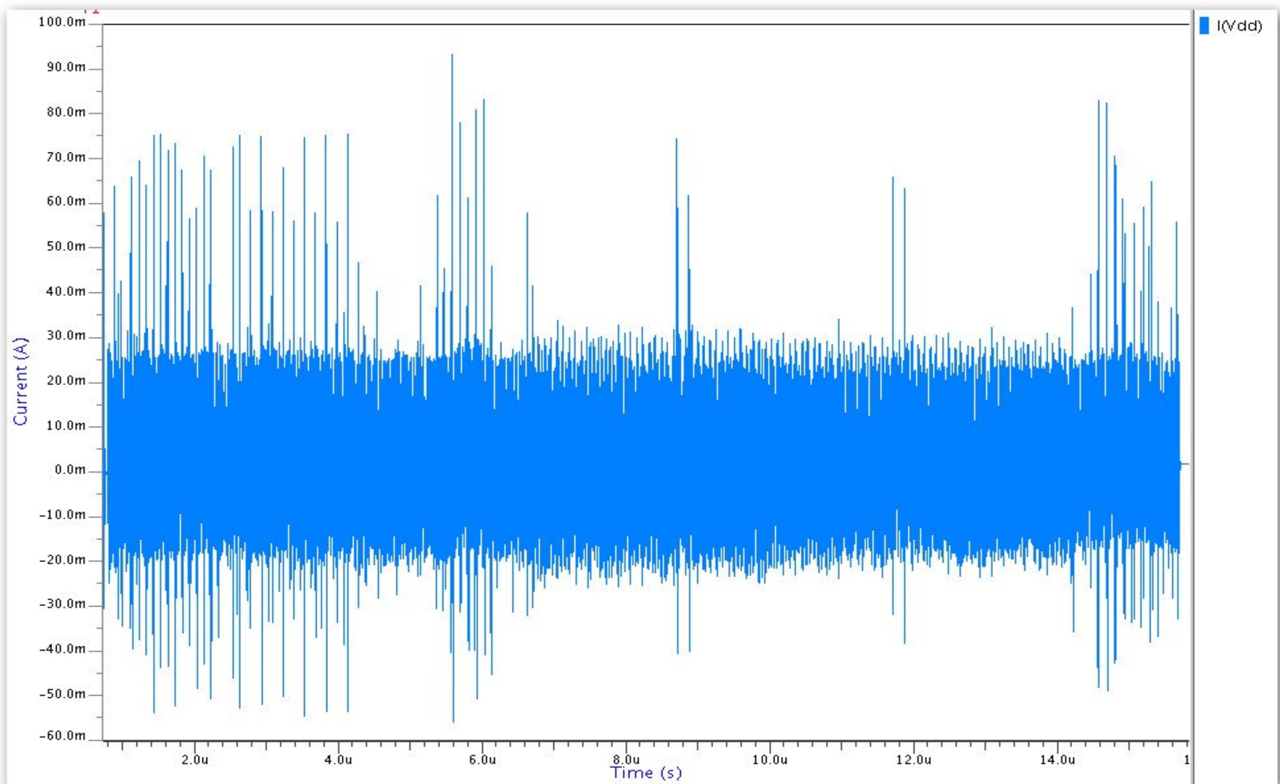

Fig.11 – Program-operation

The current waveforms were than converted in equivalent PWL generators.

4. IC core "switching activity" model by simulation for third parties device

The second testcase considered for extracting switching activity model is a third party 512Mb DDR Mobile RAM in 70nm technology at 133MHz x16 [3].

This device operates with a 133 MHz clock, but it uses both the edges of the clock cycle. Hence, it produces data at an equivalent clock rate of 266 MHz, in fact it is a Double Data Rate (DDR) RAM memory. Although the output data have a double data rate throughput the internal core circuitries operates at only the 133 MHz clock rate.

It is organized in memory pages that are divided into four sections, called banks. In order to perform a read or write operations, the bank must first be charged. A memory bank is usually pre charged to speed up read/write operations. Pre charging one memory bank can usually be overlapped with accessing a second memory bank.

Besides read and write working modes, refresh operation is provided by DDR device. In fact, since DRAM cells are capacitors, they must be periodically refreshed. A row must be refreshed periodically (often 64 ms) otherwise its cells loose their charge.

DDR allows to output data in bursts. The burst length is the length of sequential output data and it can be set to 2, 4, 8 or 16.

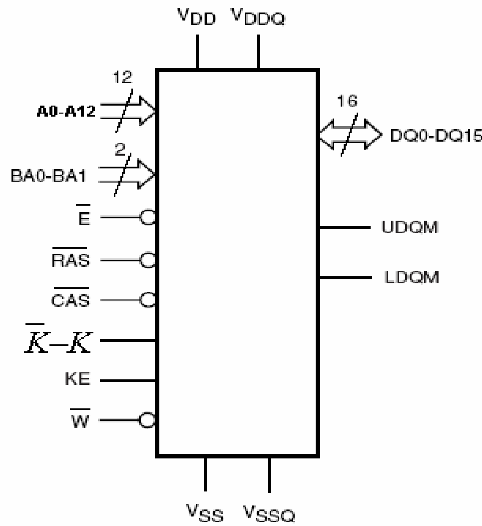

Fig.12 – Functional Diagram

DDR device is supplied by two different power supply voltage:

- ✓ VDDQ for the Input/Output pins
- ✓ VDD for the Core circuitry

The switching activity models for the main operations were provided by DDR supplier. Obviously, in such a case the macro-block approach were not applied and only one equivalent generator was provided for each working operation (Fig.13).

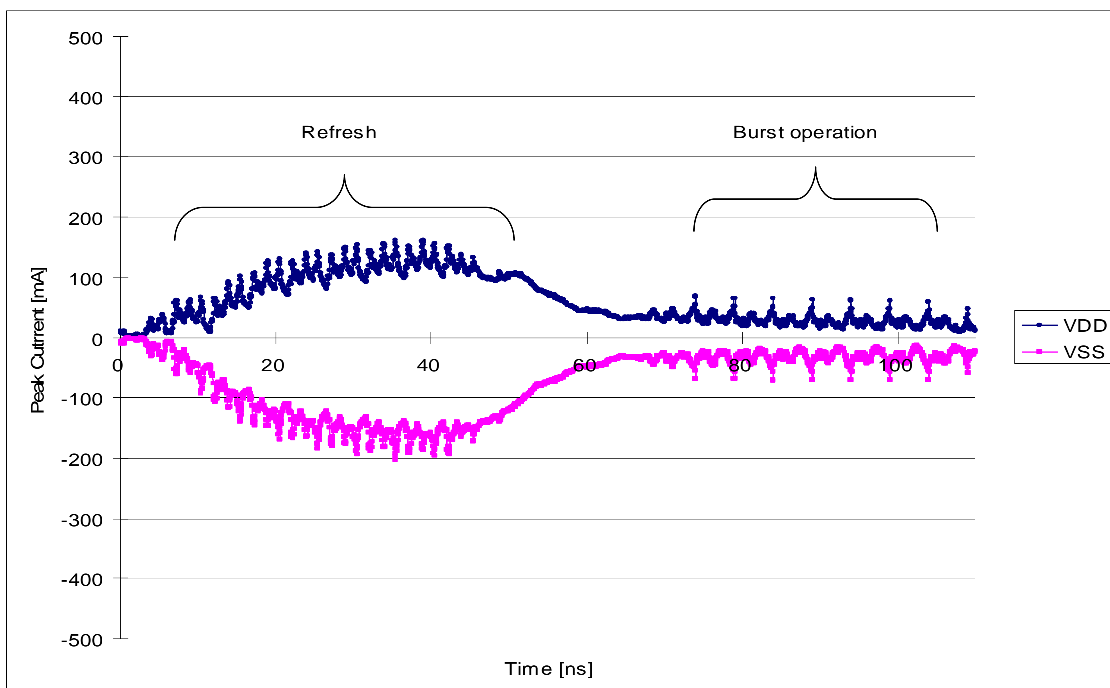

Fig.13 – DDR Switching activity current

5. Measurement of "core switching activity" current

In order to validate the core switching activity model described in the previous paragraphs, an innovative test board (hereafter referred to as EMC-board) and ad hoc probe cards have been designed and manufactured. . In fact, after having analyzed simulation results of first and second test cases and after having performed a deep search about the state-of-the-art of commercial current probes, Numonyx and POLITO concluded that it was essential to design specific solutions (probes and optimized boards) to ensure accurate measurements of core switching activity.

As a first attempt of design optimization, the features required by the I/O buffer characterization and modeling have been considered and implemented in the current board design, thus anticipating the future characterization board that will be finalized during the activities of Task 2.3.

This additional effort has been decided upon with the other partners involved in the project to start a preliminary study of the optimization of the possible different boards that are going to be manufactured within the MOCHA project. The outcome of this design will be certainly used to improve the future board design.

Therefore the objectives to be fulfilled with the EMC-board are basically two:

1. Core switching activity model validation by means of time-domain power supply current measurement (with the possibility of a frequency-domain one by using a spectrum analyzer). In fact, the most convenient way of measuring a supply current is by probing the current flowing out of the ground pin(s), instead of into the power supply one(s).

2. I/O buffer model validation by means of time-domain output voltage and current measurements: the former is the output voltage referred to the buffer ground; the latter is the sourced or sunk output current.

The design of the EMC-board is based on an already existing test board, developed by Numonyx (fig. 15).

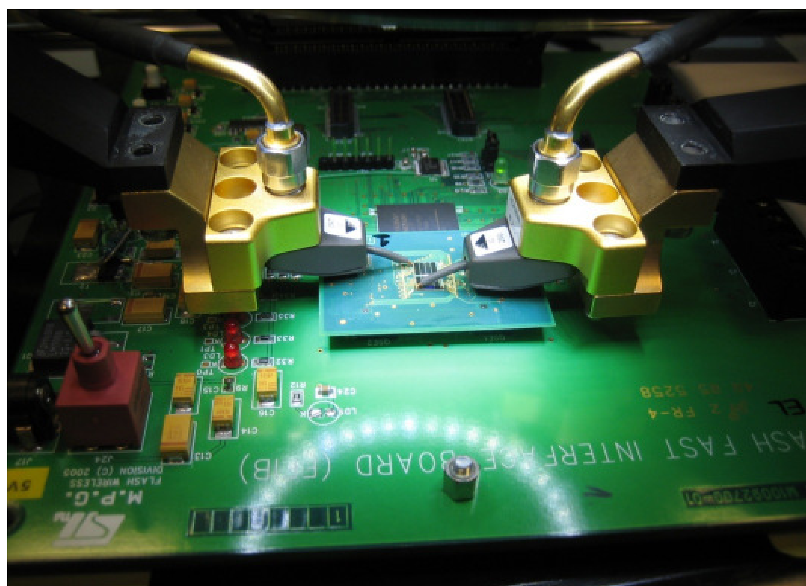

Figure 15. Numonyx's Flash Fast Interface Board (FFIB)

The pre-existing board, named Flash Fast Interface Board (FFIB), is in fact a general purpose test board that does not host directly the device under test (DUT), but provides a pair of 40-pin QTE connectors. These connectors are used to plug a smaller board (the so called Memory Module) that hosts the DUT. The FFIB basically hosts a flash memory controller, designed and implemented with a small Xilinx FPGA. This architecture allows a flexible testing of any device by manufacturing a very simple and cheap board (if compared with a full custom design), hosting only the DUT.

It was therefore decided, for reasons of convenience, to base the EMC-board project on the already existing FFIB, by reusing it as it is, and re-designing the small DUT board only [4].

There are several benefits with this approach:

- Backward compatibility
- FFIB (expensive and with a time-consuming design) reuse, as well as controller's design
- Easy and quick implementation (and re-implementation, if ever required) of the EMC-board
- Low cost.

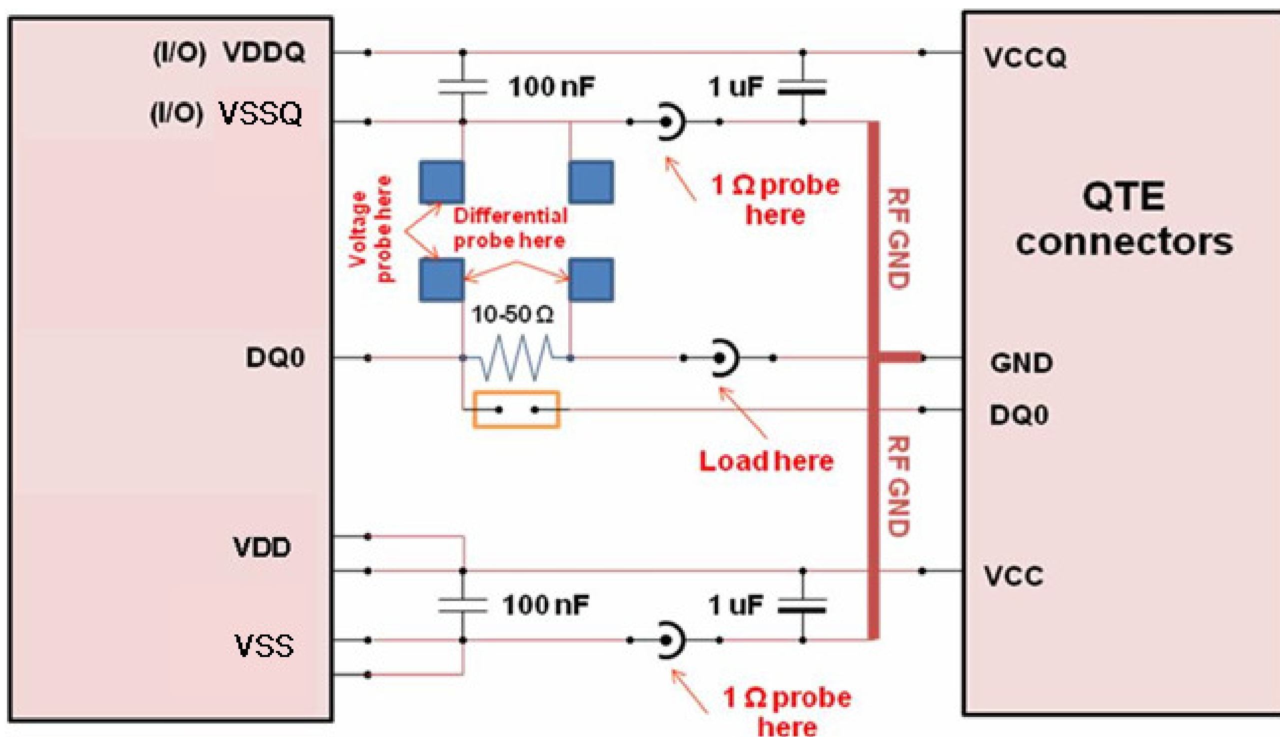

Figure 16. EMC-board high level architecture

There are of course a few drawbacks, due to the fact that the FFIB interface is already defined and cannot be modified:

- QTE connectors positions cannot be changed
- Memory interface signals are already defined on both connectors (as well as power supplies and grounds), constraining therefore signal routing

- The DUT cannot be easily moved in a different position, due to routing constraints.

As DUT for this first small board to design is the 512Mb Numonyx NOR Flash memory in 90nm technology.

The overall EMC-board architecture is outlined in fig.16.

5.1 Supply Current Characterization

Core switching activity characterization, as defined in the previous sections, requires a time-domain acquisition of the supply current. For reason of convenience and simplicity, it is advisable to acquire the current flowing out of the VSS pin(s). When a simple resistor is used as probe element, the advantage is that one of the two terminals is grounded, and that simplifies a lot the acquisition, since it is not needed to use a differential probe.

In the literature several methods are considered when measuring electromagnetic emissions:

- direct method (onboard resistor + oscilloscope voltage probe)
- 1 Ω current probe method (defined in the IEC 61967-4 Standard)
- Magnetic probe (defined in the IEC 61967-6 Standard)
- TEM cell conducted emission.

The 1 Ω current probe method has been found to be the most convenient choice for this task. It is simple and can be effectively used up to 1 GHz [5]. The IEC 61967-4 Standard defines it for the purpose of measuring the power spectrum of the supply current, but the probe can be used to acquire a time domain signal, too. The advantage over the direct method is that the probe can be characterized separately with a network analyzer, which is not possible if the 1 Ω resistor is soldered on the DUT board.

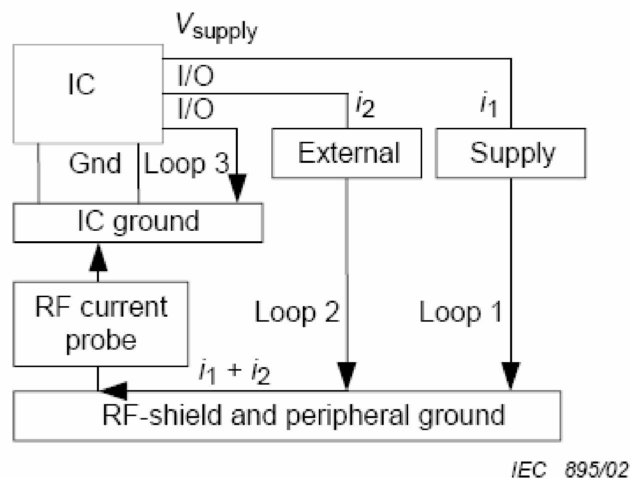

Figure 17. 1 Ω current probe method as defined in the IEC 61967-4 Standard.

Fig.17 shows the measurement principle related to such a probe, as described in the IEC 61967-4 Standard. The probe must be inserted between the IC ground and the real reference ground (called peripheral ground in the figure), reducing as much as possible any capacitive coupling between the two.

The probe itself is accurately specified in the standard. Fig. 18 shows its architecture. An SMA connector will be used as probe tip, in order to easily couple it with the board.

Probe manufacturing and characterization will be an integral part of the task. Characterization through a VNA is required mainly when acquiring the power spectrum of the signal, but it is significant for a time-domain acquisition, too.

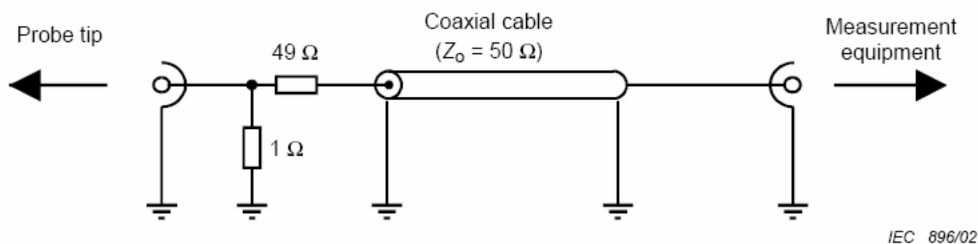

Figure 18. 1 Ω current probe as defined in the IEC 61967-4 Standard.

From a system point of view, it is considered as 'core' all the analog and digital circuitry. Output buffers are considered separately. In proprietary NOR flash memory, there are five pads of VSS paired with five VDD supply pads, as can be noted by the BSA scheme of Fig.5.

Ten VSSQ pads are used as ground references for the output buffers (paired with nine VDDQ supply pads). As shown in fig. 16, two test points for a 1-Ω probe will be inserted in the board: one for VSS pads and one for VSSQ pads.

5.2 Buffer Characterization

As already stated above, output buffer characterization requires the simultaneous time-domain measurements of the output voltage and the output current of a buffer. The output voltage is referred to buffer ground (there are ten VSSQ pins, each one connected to a couple of output buffers, except one). The output current is measured by picking the voltage across a resistor in series with the output pin (Fig.16).

An SMA connector is provided in order to plug a suitable load (an open, a short, 50 Ω, a transmission line…) that can help the modeling task (for example, by generating a high number of reflections, and therefore harmonics).

Actually it is the voltage across the resistor that is measured. Two pairs of test points are therefore provided, in order to create the contact areas for a couple of Z_0-probes, or (better) for a differential voltage probe (that can measure the voltage across the resistor directly). The inner test point pair is used for probing the output buffer voltage, too.

A more detailed discussion of the features required for the buffer characterization and the possible modifications based on this preliminary design will be considered during the WP2 – Task 2.3 activities.

5.3 Board design

In Fig. 19 the Gerber view of top layer of the manufactured PCB is shown.

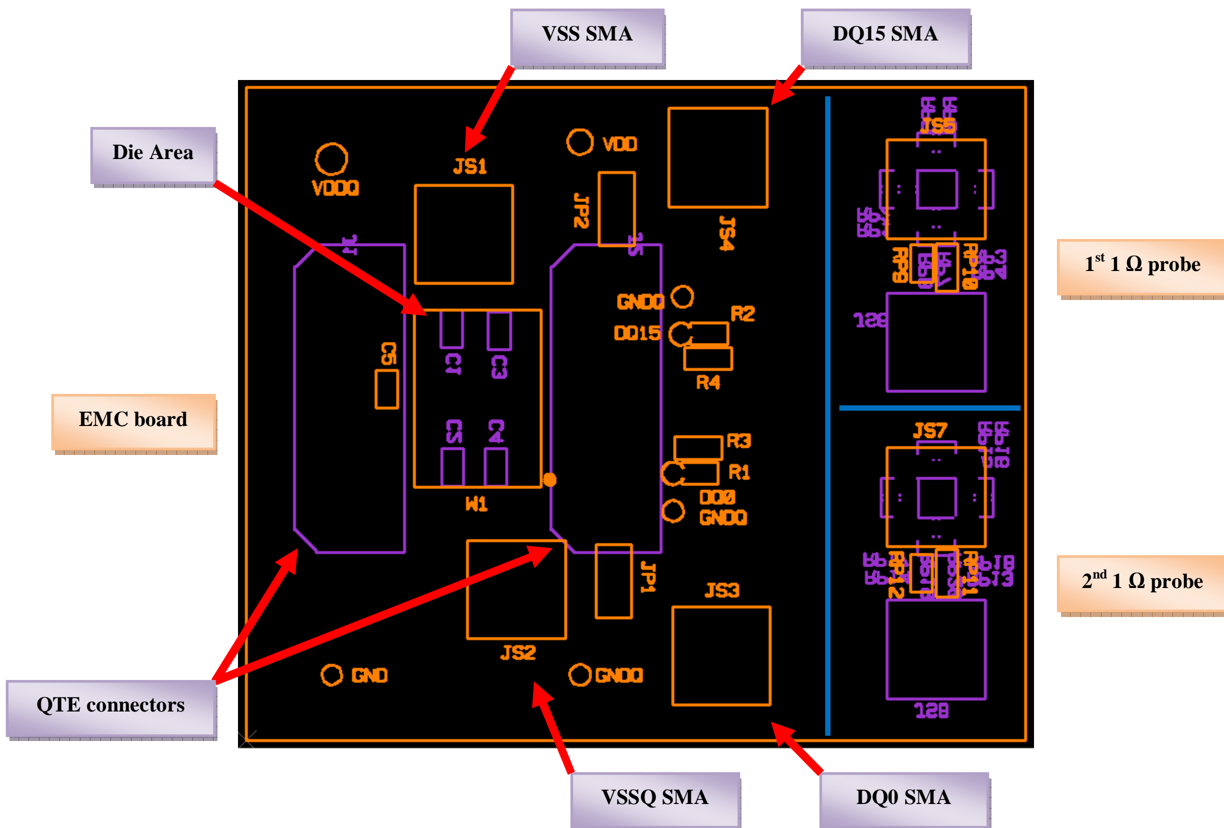

Figure 19. EMC board. Silkscreen Top and Bottom Layers.

The main components, visible in the silkscreen layers, are:

- two QTE connectors (J1 and J2), to plug the board into the FFIB;
- two SMA connectors (JS1 and JS2) to plug the 1 Ω-probe, one for VSS, the other for VSSQ;
- two SMA connectors (JS3 and JS4) to insert a load on DQ0 and DQ15 in series with the current measurement resistors (R1 and R2). It was decided to allow the characterization of two buffers instead of one in order to make a comparison between the two.

It is important to highlight again that this first designed board, for the validation of the first test case, implements a first solution for both the measurement of the switching activity of the chip and the circuitry for the characterization of the buffers. The design of the second test board, devoted to the validation of the second test case is in progress in order to include possible improvements based on the gained experience in the first board and to create a design that will be in part reused in the next tasks of the project.

6. References

[1] J-L Levant, Mramdani, R.Perdriau *“ICEM modeling of microcontroller current activity”,* Microelectronics Journal 35 (2004) 501-507.

[2] Calvet, C.Huet, J.Levant, C.Marot, J.Perrin, E.Sicard “*Integrated Circuit Electromagnetic Model (ICEM)”* -Cookbook – Release 1.c, 19 September 2001

[3] *M58PRxxxJ* Numonyx Datasheet

[4] *M65KGxxxAJ* Numonyx Datasheet

[5] L.Rigazio, I.S.Stievano, I.A.Maio, F.G.Canavero, *“Test board for supply current measurements and device characterization”,* MOCHA Internal Presentation (EMC Memory Module ver2.pdf), September 2008.

[6] IEC 61967, *"Integrated circuits — Measurement of electromagnetic emissions, 150 kHz to 1 GHz, Parts 1-7,"* International Electrotechnical Commission, Geneva, Switzerland.

Appendix

List of Acronyms

BSA	Build Sheet Assembly
DUT	Device Under Test
EMC	Electro Magnetic Compatibility
EMI	Electro Magnetic Interference
FFIB	Fast Flash Interface Board
IBIS	I/O Buffer Information Specification
IC	Integrated Circuit
ICEM	Integrated Circuit Electrical Model
IEC	International Electro technical Commission
PCB	Printed Circuit Board
PWL	Piecewise linear