PROJECT FINAL REPORT

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1. Final publishable summary report

Executive summary

The HELIOS project was a large and successful project in silicon photonics, aiming at building a whole **design and fabrication chain** enabling the integration of a **photonic layer** with a **CMOS circuit**, using **microelectronics fabrication processes**.

The task on Design Environment has led to the implementation of a complete design flow, integrating both silicon photonics device design and electronic/photonic system design in an EDA-compatible framework.

The development of building blocks leads to results exceeding the original specifications, positioning the partners at the leading edge of the state of the art in the field:

- High performance passive devices were obtained and introduced in the demonstrators.
- The wafer-level integration of laser by III-V/Si bonding led to the demonstration of single mode operation with 3dBm output power, 30dB SMSR, Ith < 35mA in CW. More advanced devices like tunable or multi-wavelength lasers as well as DFB lasers were also obtained. These hybrid lasers exhibited a good stability (compared to standard InP lasers) under extensive robustness tests.
- 40G carrier depletion Si modulators were demonstrated in MZI, Ring, slow wave, interdigitated modulators configuration using two technologies. On PIPIN diodes, the main result was the demonstration of a 40 Gbit/s MZI modulator exhibiting simultaneously 6.6 dB extinction ratio and 6 dB optical loss. With self-aligned PN diode, an MZI with 1mm phase shifters was tested at 50Gbit/s with ER around 3dB, and a total loss of 7.4dB. On 500µm long slow wave PN modulators , a high contrast 40 Gbit/s operation was demonstrated with an on-chip insertion loss of 6 dB.
- Photodetector activity has been addressed either with the hybrid approach (bonded devices) or monolithic one (pure Ge). Both showed high responsivity (1A/W) and low dark current (<100nA at RT @-1V). With Ge lateral photodiodes, the bandwidth topped at 130GHz and a 40GBit/s data transmission without bias voltage was demonstrated. A 16x10 Gbit/s receiver was produced with Ge photodiodes, 2D grating couplers and 2 AWG.

Three wafer-level Electronic/Photonic integration schemes have been explored:

- Wafer bonding of the photonic wafer either on the front side or on the backside of the electronic wafer,
- Front End Of Line (FEOL) co-integration of photonics with electronics

The combination of these building blocks in order to make complex demonstrators led to the following achievements:

- FEOL integrated modulators + BiCMOS driver, operating at 10Gb/s with dynamic extinction ratio of 5.5dB.
- An integrated tunable laser–Mach-Zehnder modulator (ITLMZ) was characterized at 10Gb/s with a BER of 10^{-9} for received power levels lower than -25 dBm.
- First chips integrating lasers, modulators, photodiodes and AWG have been fabricated and tested.
- A photonic QAM Modulator composed of a DEMUX, two I-Q MZM, Microheaters and monitoring Ge photodiodes exhibited open eye-diagram of the modulated DPSK signal at 5Gbps. A Photonic QAM Demodulator including a TO tunable MZI power splitter to actively control the input power to the Mach-Zehnder Delay Interferometer (MZDI) and two balanced Ge photo diodes (BPD) showed also a well opened eye-diagram of the demodulated signal for 2x5Gbps operation.

Generic packaging techniques have also been studied, with the design and fabrication of metal housing, silicon submount, DC and RF ceramic PVB.

With the work on innovative devices, amorphous silicon modulator exhibited performances far beyond the original expectations. Even if lasing with Si nanocrystals has not been achieved, guided electroluminescence from slot waveguides and micro-ring resonators has been observed. CMOS-compatible 2.5D III-V/Si VCSELs were highly-efficient optically-pumped and lasing with electrical pumping will be soon demonstrated. Moreover experimental demonstration of optical coupling of these VCSEL with silicon micro-guides has been achieved.

Last but not least, the work of the HELIOS consortium led to more 170 publications and communications in peer-review journals and international conference

Summary description of project context and objectives

Photonics is a rapidly growing sector in the global economy. Optical communications, optical storage, imaging, lighting, optical sensors or security are just a few examples. Even if photonics could bring new functionalities to electronic components as low propagation losses, high bandwidth, wavelength multiplexing and immunity to electromagnetic noise, the high cost of photonic components and there assembly is a major obstacle to their deployment in most of application fields. Just like in micro-electronics, many applications can be realized in a much more compact and cost-effective way by integrating the required functionality in a single chip.

Silicon photonics (or more precisely CMOS Photonics) is a way to tackle the problem by developing a small number of generic integration technologies with a level of functionality that can address a broad range of applications. Such technologies, which should be made accessible via foundries, can address markets that are sufficiently large to pay back the development costs.
Functional demonstration of basic building blocks such as a µlaser, a detector, coupling, and link has been realized in previous research projects. As a next step the HELIOS project proposes to integrate photonics components with integrated circuits as a joint effort of major players of the European CMOS Photonics community, in order to enable an integrated design and fabrication chain that can be transferred to EU manufacturers.
The objective of the project HELIOS is to combine a photonic layer with a CMOS circuit by different innovative means, using microelectronics fabrication processes.

- Development of high performance generic building blocks that can be used for a broad range of applications: WDM sources by III-V/Si heterogeneous integration, fast modulators and detectors, passive circuits and packaging
- Building and optimization of the whole “food chain” to fabricate complex functional devices. Photonics/electronics convergence will be addressed at the process level and also at the design level since HELIOS will contribute to the development of an adequate design environment
- Demonstrating the power of this proposed “food chain” by realizing several complex photonic IC’s addressing different industrial needs, including a 40Gb/s modulator, a 16x10 Gb/s transceiver, a Photonic QAM-10Gb/s wireless transmission system and a mixed analog and digital transceiver module for multifunction antennas..
- Investigation of more promising but challenging alternative approaches These concepts offer clear advantages in terms of integration on CMOS for the next generation of CMOS Photonics devices
- Road mapping, dissemination and training, to strengthen the European research and industry in this field and to raise awareness of new users about the interest of CMOS Photonics.

Context and rationale

Photonics is a rapidly growing sector in the global economy. Optical communications, optical storage, imaging, lighting, optical sensors or security are just a few examples. Even if photonics could bring new functionalities to electronic components as low propagation losses, high bandwidth, wavelength multiplexing and immunity to electromagnetic noise, the high cost of photonic components and there assembly is a major obstacle to their deployment in most of application fields. Just like in micro-electronics, many applications can be realized in a much more compact and cost-effective way by integrating the required functionality in a single chip.

So far, the progress in photonic integration technology has been hampered by the large variety in photonic devices and technologies, and the fact that most integration technologies are specific for the applications for which they have been developed. As a result the market for integrated photonics is too fragmented to justify the investments for developing an integration technology to a level that really leads to substantial cost reductions, and this, in turn, prevents rapid growth of the applications.
Silicon photonics (or more precisely CMOS Photonics) is a way to tackle the problem by developing a small number of generic integration technologies with a level of functionality that can address a broad range of applications. Such technologies, which should be made accessible via foundries, can address markets that are sufficiently large to pay back the development costs.
As in microelectronics, the key for the success of integration in photonics is to realize a broad range of optical functionalities with a small set of elementary components, and to develop a generic wafer-scale technology for integration. This generic technology will most likely not wipe away more specialized custom technologies but will create new opportunities for a much larger deployment of photonic ICs. Since the single device (e.g. laser/modulator/etc...) will have an insignificant cost, the designers will concentrate on the way to achieve the desired functions by using as many components as needed.
Moreover, by co-integrating optics and electronics on the same chip, high functionality, high performance and highly integrated devices can be fabricated, while using well mastered microelectronics fabrication process. Another advantage of CMOS photonics is that its success will move the emphasis from the component to the architecture. In other words, industrial and RTD efforts could be focused on new products or new functionalities rather than on the technology level.

However, there are many challenges and issues to be addressed before bringing Photonics on CMOS at a mature industrial level. Several requirements need to be fulfilled before it can become a reality:

- Performance of optical functions must meet the application needs
- Both photonic and electronic components cost structure must be similar (ie packaging cost lower than chip cost)
- Photonics integration must be straightforward for IC designers and manufacturers. That means that CMOS compatibility is mandatory, as well as the creation of design tools and libraries compatible with IC standards

At this moment, these conditions have been fulfilled neither through research laboratory demonstrations nor through industrial realisations.
Proof of concept or functional demonstrations of major building blocks have been made in previous research projects (laser, modulator, detector, coupling, and link). As an example, the FP6 project PICMOS (of which several partners are in HELIOS) demonstrated a full optical link on a chip. However, even though the results obtained were considered as a major breakthrough, major efforts are still needed to improve the performance in terms of functionality, bandwidth or power. To go one step further, the European CMOS Photonics community must demonstrate the integration of photonics with electronics and **make available an integrated design and fabrication chain** with standard and generic processes that could be transferred to foundries.

Objectives of the project

The objectives of HELIOS are manifold:

- Development of high performance generic building blocks that can be used for a broad range of applications: WDM sources by III-V/Si heterogeneous integration, fast modulators and detectors, passive circuits and packaging
- Building and optimization of the whole “food chain” to fabricate complex functional devices. Photonics/electronics convergence will be addressed at the process level and also at the

design level since HELIOS will contribute to the development of an adequate design environment
- Demonstrating the power of this proposed "food chain" by realizing several complex photonic IC's addressing different industrial needs, including a 40Gb/s modulator, a 16x10 Gb/s transceiver, a Photonic QAM-10Gb/s wireless transmission system and a mixed analog and digital transceiver module for multifunction antennas..
- Investigation of more promising but challenging alternative approaches These concepts offer clear advantages in terms of integration on CMOS for the next generation of CMOS Photonics devices
- Road mapping, dissemination and training, to strengthen the European research and industry in this field and to raise awareness of new users about the interest of CMOS Photonics.

Several major breakthroughs are foreseen in HELIOS:
- The integration of photonic active and passives functions with CMOS circuitry, to achieve a high level of functional integration and again an overall cost and size reduction. This integration will be made by using 200mm CMOS pilot lines operated by the partners.
- Demonstration of highly integrated circuits addressing industrial needs. These components will be fabricated on 200mm CMOS pilot lines operated by the partners.

HELIOS will tackle the remaining difficult building blocks which are hot topics, as sources (Silicon-based and heterogeneous integration of III-V on silicon), fast modulators and packaging. It will go beyond the demonstration of building blocks by demonstrating several devices with complex functions for various industrial needs. Even if the primary targeted applications are in the communication domain, the results of HELIOS will pave the way for applications of CMOS photonics for other fields, eg sensors or optical processing.

The objective of the project HELIOS is to combine a photonic layer with a CMOS circuit by different innovative means, using microelectronics fabrication processes. HELIOS will make integration technologies accessible for a broad circle of users in a foundry-like, fabless way

In the long term, IC manufacturers will use photonics libraries and IP blocks and integrate them in their circuit design.

Relevance of the project

The project HELIOS will contribute to the emergence of highly-functional and cost-efficient components through the convergence of electronics and photonics. This will enable Europe's industry to stay at the forefront of electronics developments and applications.
First, HELIOS aims at developing a generic integration and manufacturing technology for high density and high performance components and circuits involving passive and active photonic functions. This approach exhibits several advantages:
- The components (active and/or passive) and circuits will be fabricated by means of CMOS-oriented technologies, leading to potential cost and size reduction as well as improved manufacturability and testability
- The photonic functions will be integrated with electronic CMOS circuitry. This will allow a high level of functional integration and again an overall cost and size reduction.
- The "Above IC" integration scheme which will be investigated in depth in HELIOS allows the heterogeneous integration of silicon with other photonic materials as III-V (InP, GaAs) or any kind material system. This opens a wide range of possibilities, in particular for achieving high performance active functions.

HELIOS will investigate new design methodologies and tools. It will strive for developing a coherent design methodology and flow for the integration of photonics on CMOS covering all design and tool aspects, from virtual fab to system level. The project will also facilitate the electronic/photonic convergence at the design level, by developing an interface strategy for the integration of photonic design tools with EDA tools.

HELIOS will not only make available the "toolbox" for manufacturing photonic devices, since it will demonstrate several components that address directly industrial needs. HELIOS will allow a reduction in size, cost per Gbps and power consumption to enable higher performance photonic networks. Thanks to photonic integration, advanced modulation schemes, advanced metropolitan network architectures for bitrates of 100Gb/s and above will be available.
The wireless transmission system that will be demonstrated in WP10 will enable the fabrication of scalable, future-proof and economic components for broadband access and local area networks. In particular, radical cost reduction at component level through breakthroughs in device design, materials, packaging or integration is expected. Monolithic integration will improve cost-effectiveness of network elements and realize new functionality.

Progress beyond the state of the art (as defined at the beginning of HELIOS)

A set of target specifications has been defined in the table hereafter.

State of the art / baseline of the project	HELIOS Objectives
Laser on Si (Intel)(Ith= 175mA, 29mW power in SOI WG 1% global efficiency, multimode operation) µlaser (PICMOS) (Ith= 500µA, 50µW Pulsed power in SOI WG, 1% global efficiency)	Laser **3dBm** (ie 2 mW) output power, **single mode operation** with 30dB mode suppression ratio, threshold current <35mA CW laser operation at 65°C
Si vertical modulator (INTEL) (40Gbit/s modulators with 1 dB active modulation depth, 7 dB insertion loss) Si lateral modulator (LUXTERA) (10Gbit/s modulators, 3dB insertion loss)	40Gbit/s modulators array with **2 dB** active modulation depth, **6dB insertion loss integrated** with a PD on a **SiGe EIC**
Ge PD (IEF) (BW= 25 GHz, R>0.8 A/W, Id <100mA/cm²) InGaAs PD (Intel ,IMEC) (R=1.1 A/W, Id <1mA/cm²)	Ge or InGaAs Photodetector BW= 30 GHz, R>0.8 A/W, Id <50mA/cm², Wavelength range 1.5µm – 1.58µm integrated on EIC with specific TIA.
No integration of complex functions with EIC	Integration of complex photonic functions with EIC using standard CMOS compatible processes
LiNbO3 Modulator 40 Gb/s 35 x 2 mm with external PD	Si Modulator 40 Gb/s 5 x 1 mm with integrated PD on SiGe EIC
4 x10Gb/s transceiver with flip-chipped InP source	Fully integrated 16x10Gb/s transceiver
Wireless System with OOK up to 10Gbps @ 35 to 120 GHz (Lumera and NTT). 16QAM Modulator @ 3.6 Gb/s at 39 GHz (NTC & DAS Photonics).	Integrated (D)QPSK -10Gbps at mm-wave frequencies system on silicon

Description of the main S&T results/foregrounds

The HELIOS project was a large and successful project in silicon photonics. The development of building blocks leads to results exceeding the original specifications and moreover positioning the laboratories at the leading edge of the state of the art in the field. Even if it has been challenging to assemble these buildings blocks to fabricate demonstrators as the technology was more complex, advanced transceivers have been obtained. Three different ways of integration the photonic devices with electronic devices on a wafer to wafer basis were pushed with some success. With the work on innovative devices, amorphous silicon modulator exhibited performances far beyond the original expectations. Even lasing with Si nanocrystals has not been achieved, guided electroluminescence from slot waveguides
and micro-ring resonators has been observed. CMOS-compatible 2.5D III-V/Si VCSELs were highly-efficient optically-pumped and lasing with electrical pumping will be soon demonstrated. Moreover experimental demonstration of optical coupling of these VCSEL with silicon micro-guides has been achieved.
The report is divided in the different parts addressed by HELIOS.

Design environment

The implementation of a complete design flow, integrating both silicon photonics device design and electronic/photonic system design using these devices in an EDA-compatible framework was demonstrated. The flow distinguishes between the major use models (device design and system design) and by offering a clear interface in the form of model libraries, allows cooperation without significantly upsetting traditional design techniques specific to each domain. The flow not only allows simulation of an electronics/photonics system but also design space exploration (thus going beyond initial plans). We examined several possible approaches to address the synthesis of a wavelength-selective optical link reference case considering various types of model and design strategies:

- Library and model generation
    - Generation of a component library of passive photonic devices sweeping critical geometric parameters and temperature, in the form of s-matrix files for Verilog simulation
    - Point generation of specific component using an analytical model
    - Performance model generation using a specific design of experiments strategy (here exhaustive, based on the library sweep) and interpolation from the nearest models in the library to the specified performance requirements
- System simulation and exploration
    - Exploring exhaustively feasible combinations of building blocks with the Component Matching Search method
    - Exploring feasible design space using optimization based methods

The results of this design flow were shown to arrive at a complete design with performance metrics as specified by requirements.

Hybrid laser activity

The goal of WP2 is to develop a single longitudinal mode laser hybridly integrated on the silicon platform. The target performance was:

- 3dBm output power, 30dB SMSR, Ith < 35mA, CW operation

- -3dBm output power, 20dB SMSR, Ith <50mA, at 45°C

During the first year, the bonding process of III-V on silicon was address by three means: BCB bonding, direct bonding either with ITO or SiO2. High yield was obtained, but the focus was given on the first two means developed by imec and by CEA.

FP hybrid laser

During the year 1 & 2, a first generation of this device (GEN1), based on Fabry-Perot design, was implemented. Following first year's results, III-Vlab improved the metallization process of the devices and this resulted in laser operation. Both molecular bonded samples (delivered by CEA) and BCB bonded samples (delivered by *imec*) were processed. The device consists of a central gain section (light in III-V), a taper for coupling the light to the silicon (at both sides) and a short piece of silicon waveguide (at both sides). Some results are shown in the pictures below (CW operation). The minimum threshold was 50mA and the output varied from 1.5mW (for 500um long device) to 3mW (for 1100um long devices).

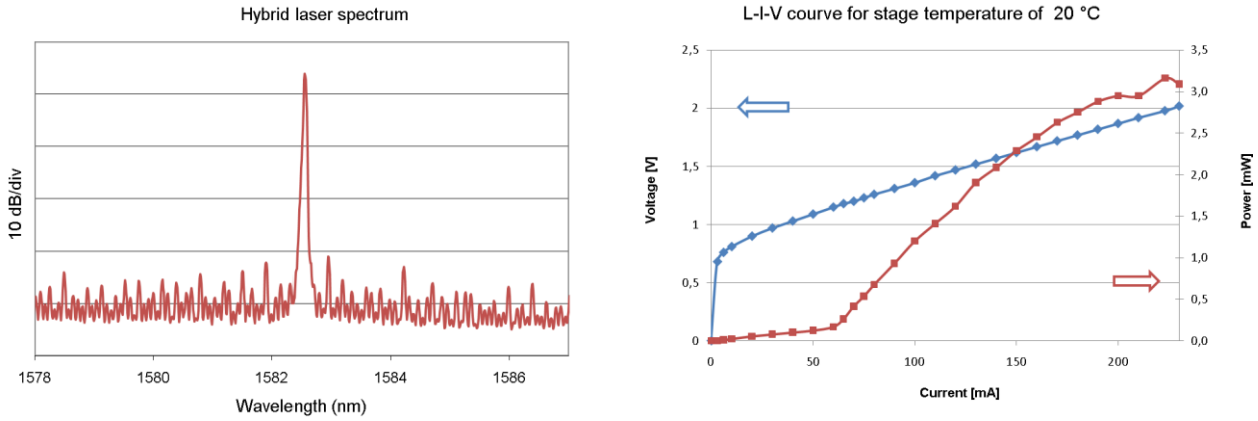

Figure 1: (Left) Optical spectrum of the laser driven at 55mA (Right) Laser power as a function of drive current (L-I curve) under CW operation at 20°C

Further fabrication and characterization of these InP on Si hybrid lasers needed deep ridge structures with 400nm InP taper tips. FP-type hybrid lasers showing <30mA threshold current at RT, have reached one of the main specifications for the laser.

Single mode hybrid lasers

With GEN2, the introduction of different designs with an optimized InP process conducted to various devices with in particular wavelength selective element. Figure 2 shows the principle of the laser. The gain section (purple) is fabricated in a III-V layer stack integrated on top of silicon waveguides using wafer bonding approaches. Light is coupled to the underlying silicon waveguides through adiabatic tapers at the front and back. The laser cavity is formed by two DBR mirrors etched in the silicon waveguides and contains a ring resonator to ensure single longitudinal mode operation. Figure 2b shows the LI curves at different environmental temperatures**. The threshold current for this device at RT is 35mA and the output power is beyond 4mW.** Even at 60C we still reach an output power of almost 1mW. Figure 3a shows the spectrum of the laser, when the ring resonator is thermally tuned (tuning power is indicated in graph). First of all we see a clear single mode operation, with SMSR certainly better than 30dB. Further we observe a broad tuning range over several nanometer.

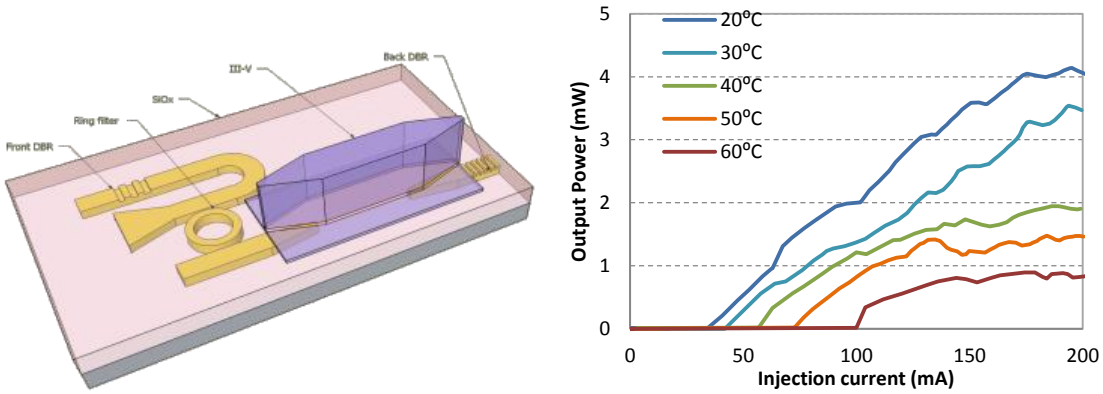

Figure 2 (a) Laser concept. (b) LI curves

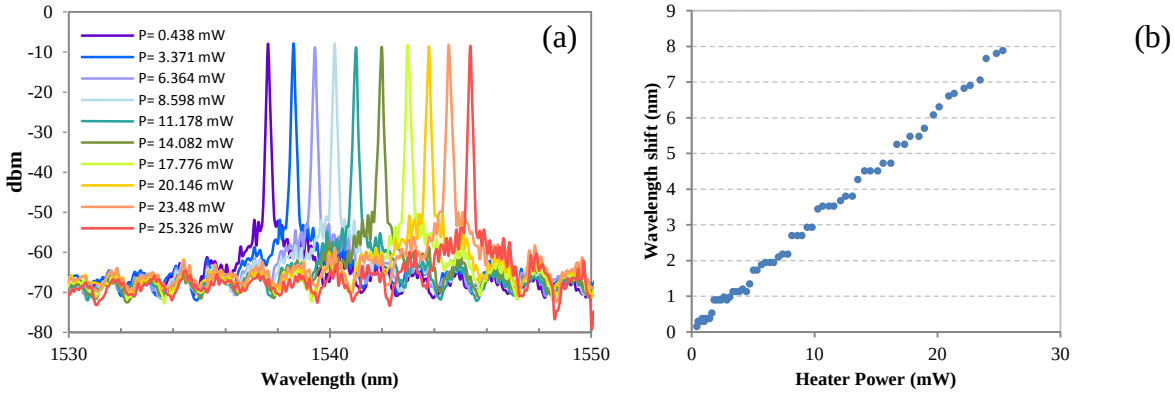

Figure 3 (a) Super-imposed laser spectra for several values of the heating power (b) laser wavelength as a function of the power dissipated in the heater, at 20°C and a laser injection current of 80 mA.

New laser devices

Using the same amplifier as the basic building block, several types of devices (DFB-lasers, multi-wavelength lasers using intracavity AWG or ring demultiplexers as the filter element, tunable lasers using new type of retro reflectors …) have been designed and characterized. The most important results are as follows:

- **Demonstration of a 4-channel AWG-based multi-wavelength laser. Threshold current <35mA, output power > -3dBm.**
- **Demonstration of a 4-channel multi-wavelength laser based on a ring resonator demultiplexer (presented at ACP 2012 as postdeadline paper)**
- **Demonstration of symmetric and asymmetric DFB-lasers**
- **Demonstration of new type of evanescently coupled active DBR laser (accepted for publication at OFC 2013)**

The fact that all these devices could be realized in a single fabrication run prove the versatility of the proposed hybrid III-V silicon integration process.

Robustness tests

3SP carried out extensive robustness tests on FP-type III-V on silicon lasers fabricated in the project. **This hybrid lasers exhibited a good stability (compared to standard InP lasers)** for Threshold current & Vf. It was observed a favourable increase of power, meaning that for a longer term qualification (& fabrication) of such lasers, a stabilization process will be needed.

Carrier depletion Si modulators

Two technologies of silicon carrier depletion modulators have been developed during the project. The first one is a self-aligned PN junction base on a thin SOI (200nm thickness). With this technology, MZI, Ring, and slow wave modulators were demonstrated. The second one is based on a thick SOI (400nm thickness) with a PIPIN junction. MZI, Ring, Interdigitated modulators are reported.

Thick modulator (UPS-CNRS):

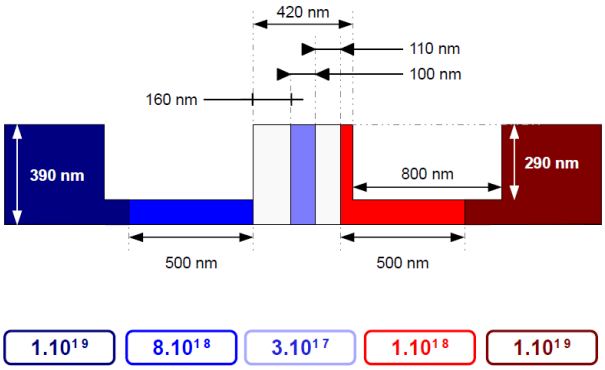

Figure 4: Active region cross-section of the optimized phase shifter. RC cut-off frequency is 35 GHz (40 Gbit/s optical modulator)

The typical phase shifting cross-section is illustrated on Figure 4. The 40 Gbit/s modulator has been designed and fabricated using a self-alignment method that has been developed to fabricate the PIPIN active region with a very good localisation of the central P doped region in the middle of the diode.
This structure was integrated in a 50 µm radius ring resonator, showing low optical loss and a 4.4 dB extinction ratio.
In addition, a new electrical structure to obtain intensity modulation has been demonstrated, based on interdigitated PN diodes. A ring modulator showing 4 dB extinction ratio at 10Gbit/s has been obtained.

The main result is the demonstration **of a 40 Gbit/s MZI modulator using a PIPIN diode showing simultaneously 6.6 dB extinction ratio and optical loss of 6 dB** as shown in Figure 5**Erreur ! Source du renvoi introuvable.**.

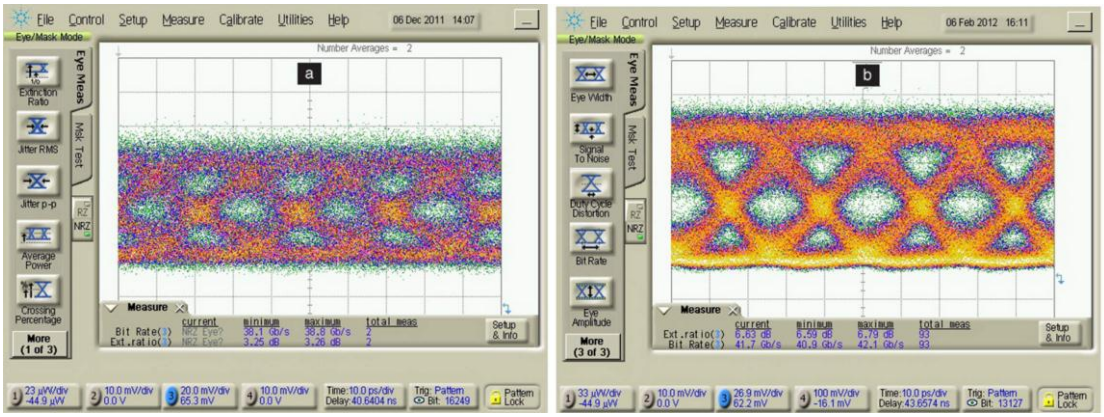

Figure 5: Optical eye diagrams at 40Gbit/s from the 0.95 mm-long phase shifter (left) and 4.7 mm long phase shifter (right).

Thin modulator (University of Southampton):

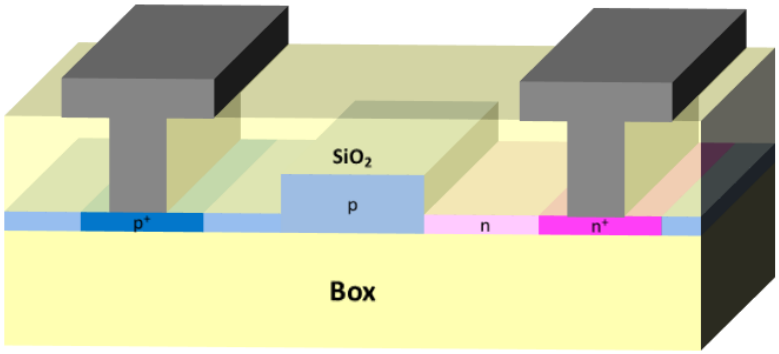

Figure 6 : Thin modulator cross-section

With thin Si design (PN diode), processing of thicker electrodes has resulted in a reduction in the electrode RF loss and the demonstration of 10Gbit/s modulation from devices of the first fabrication batch. Devices from the second fabrication batch have been characterised. 40Gbit/s modulation with a 10dB extinction ratio has been demonstrated from a 3.5mm long MZI although with a normalised optical loss of 15dB. 40Gbit/s modulation has also been demonstrated from a 1mm MZI with a modulation depth of 3.5dB and normalised optical loss of 5dB.

An MZI with 1mm phase shifters was tested **at 50Gbit/s.** An open eye diagram was achieved and the **extinction ratio (once the noise of the EDFA is accounted for) was calculated to be approximately 3dB, with the device biased with 3.2dB of** additional loss giving a total loss of **7.4dB**.

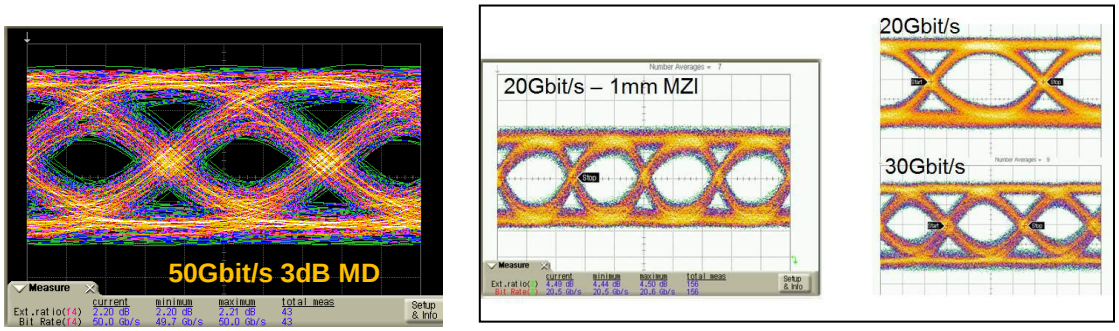

Figure 7 – Optical eye diagram at 50Gbit/s (left) and eye diagrams at 20Gbit/s and 30Gbit/s with low loss (right)

The DC and high speed performance of a ring resonator version of the device was tested. High speed operation up to 40Gbit/s was demonstrated.

Slow wave modulator (UPVLC):

The proposed slow wave structure consists of a deep-etched laterally corrugated waveguide with circular holes patterned onto its wide section. The addition of this perturbation in the periodic structure enables tailoring the dispersion relation in order to obtain a nearly flat band, i.e., a region inside the Brillouin zone where the group index is constant over a determined frequency range. Nearly constant group index as high as 13.5 over a wavelength range of ~14 nm was experimentally

demonstrated in a 50 µm long waveguide. A slow wave based thin modulator exhibited a $V_{\pi}.L_{\pi}$ ~1.27V·cm for a group index of 11 and as low as ~0.45V·cm when the group index increased up to ~22. Slow light enhancement was exploited for scaling the modulator length down to 500 µm (325 μm^2 footprint).

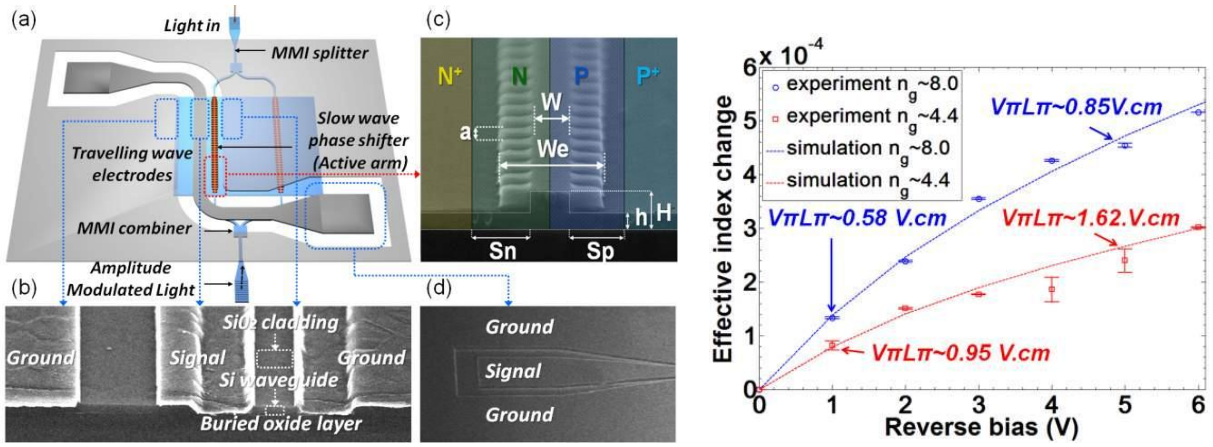

Figure 8- (a) Schematic of the slow wave modulator and SEM pictures of (b) the travelling wave coplanar electrodes, (c) the corrugated waveguide and (d) the contacting AlCu pads. (e) Effective index change versus reverse bias for group index values of ~4.4 (fast light, red) and ~8 (slow light, blue). Modulation efficiencies $V_{\pi}L_{\pi}$ are pointed by the arrows.

A high contrast 40 Gbit/s operation in a compact device was demonstrated with an on-chip insertion loss of only 6 dB, including the 1 dB loss of the two MMI structures.
With low drive voltages, transmission rates from 5 Gbit/s with 1 Vpp up to **25 Gbit/s with 3 Vpp with an insertion loss of ~12 dB were achieved on** a 1mm-long slow-light modulator.
A very efficient method of generating mixing products in the slow-light modulator has also been investigated. Minimum transmission point (MITB) was used to successfully demonstrate up-conversion from 1 GHz to 10.25 GHz with very low conversion losses ~7 dB and excellent quality of the received I/Q modulated QPSK signal with an error vector magnitude (EVM) of around 8%.

Passive devices

A large set of passive devices have been developed or optimized for the use in the different demonstrators.

- A transition between rib/strip waveguides has been designed and fabricated with less the 0.2dB measured losses.
- With respect to grating couplers, three techniques have been developed by *imec* to improve directionality and thus coupling efficiency: a bottom DBR mirror, a silicon overlay and non-uniform gratings. Out of these methods, the highest efficiency gratings that has been experimentally demonstrated showed 69% efficiency (-1.6dB loss). This has been the case for gratings with a bottom mirror and also for gratings with a silicon overlay. The low loss (<2dB) bandwidth is similar in both cases (~30nm). Polarization independent demultiplexing using AWGs and a novel approach to reduce the PDL below 1dB by incorporating a phase section in one of the arms of the circuit has been demonstrated by *imec*. 2D grating couplers with raised silicon overlay were developed but a higher than expected loss (5-6dB coupling efficiency) was measured. UPVLC fabricated and characterized the compact polarization splitters based on MMI structure. Extinction ratios better than 20dB were obtained for a

13.5µm long device. *imec* also developed a polarization rotator based on using symmetry breaking of an almost square waveguide. A polarization conversion efficiency of -0.5dB over a wavelength range of 80nm around 1550nm was measured.

- With respect to inverted taper based couplers, coupling losses below 1dB for a broad bandwidth of 100nm were demonstrated for the inverted taper approach embedded in a SiO_x rib waveguide. The coupler was optimised by CEA for coupling to standard single mode fibers by increasing the cross-section of the SiO_x rib waveguide. Coupling efficiency of 55 % (-2.6 dB) was demonstrated for a taper length of 200 µm. The direct butt coupling between a lensed fibre inserted in a V-groove etched in a silicon submount including a special notch allowing free space and epoxy free focusing of light from the fibre onto the inverted taper of a silicon wire waveguide was first demonstrated. Fibre to fibre insertion loss is in the range of –7dB. Thermal cycling (10x) between –40°C and +85°C gave 1dB of insertion loss variations.
- Two generations of AWG based demultiplexers, with variations in channel spacings and number of channels have been fabricated and tested by *imec*. For the 8 channel 400GHz device, crosstalk better than 20dB and losses lower than 1.5dB was demonstrated. For the 16 channel 200GHz device, losses of around 4dB for the central channel and crosstalk better than 15dB was demonstrated.
- A microring demultiplexer filter has been fabricated and characterised by UPVLC. Experimental results confirmed simulation results and demonstrated the target filtering performance of two optical carriers separated by 60GHz with extinction ratios above 20dB and insertion losses below 3dB.

Photodetection

Photodetector activity has been addressed either with the hybrid approach (bonded devices) or monolithic one (pure Ge).

The InGaAs MSM-detectors integrated on silicon waveguides integrated on vertically emitting grating couplers showed high responsivity (1A/W) and low dark current (<100nA at room temperature). The bandwidth is more than 10 GHz.

Vertical and lateral pin pure germanium photodetectors exhibited low dark current (below 100nA@-1V), high responsivity (between 0.8 and 1A/W) and high bandwidths: 42GHz under -4V for the vertical pin diode and higher than 130GHz for the lateral diode have been obtained. A 40GBit/s data transmission without bias voltage was demonstrated.

Electronic/Photonic convergence

As the current developments on electronic-photonic assembly are based on die to wafer solutions (wire bonding, flip-chip or copper pillars), the alternative ways studied in the project are based on wafer solutions in order to get a more collective fabrication. One is a combined fabrication where electronic and photonic processing steps are combined for the production of a photonic-electronic integrated circuit (PEIC). The two other solutions are based on wafer to wafer bonding either on the front side of the electronic wafer, either on the backside.

Front Side Integration: CEA

This front side integration is based on the direct bonding of a front end photonic wafer (PIC) at the front side on the electronic wafer (EIC) in order to get a photonic-electronic wafer (PEIC).
On wafers delivered by austriamicrosystems which were stopped after structuring of top metal, CEA has performed a pre-bonding process such as covering with thick SiO2 the top metal, planarization of the surface with CMP. For assessing the technology, with one CMOS wafer and with a trial photonic wafer, we performed successfully the wafer bonding and the substrate removal down the box (Figure 9).

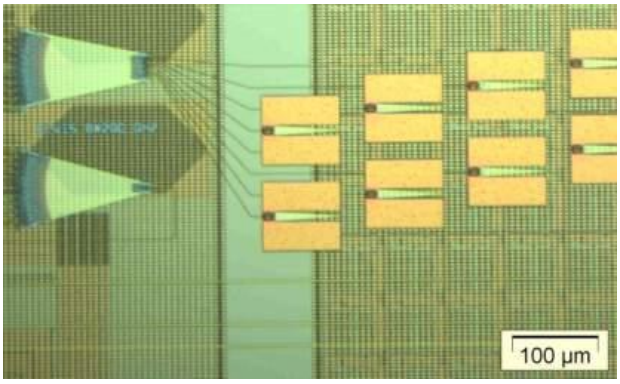

Figure 9: Photonic layer bonded on the top of a CMOS circuitry

For the PIC demonstrator , a receiver with Ge photodiodes was designed and fabricated at CEA with a 2D surface grating coupler, two identical 200GHz 16 channel AWGs, and 16 Ge photodiodes. The tests were performed on a 200mm wafer prober and good results were obtained such ~8dB coupling losses) at 1550nm with a 3dB bandwidth of 55nm for 2D grating coupler. The 16 channels AWG with 200GHz showed a crosstalk levels of -15 dB, and a minimum center-channel insertion losses around 2.8 dB. The Ge photodiode sensitivity is ~ 0.8 A/W with a dark current of the order of 100nA (-0.5V)

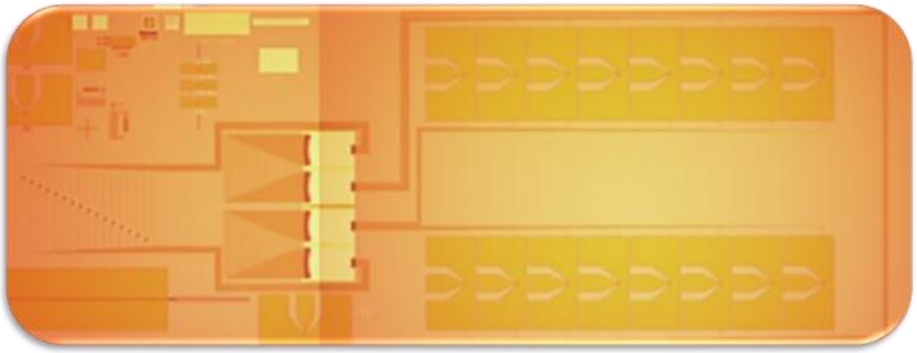

Figure 10: 16 channel receiver with Ge photodiode

After fabrication of EIC and PIC with planarized surface of oxide, the wafer to wafer bonding has been achieved. The remaining strain on the photonic wafer leads to incomplete bonding on the edges, but most of the surface has been transferred.

Front Side Integration: imec

3D integration route followed by imec involved fabrication of Cu/Sn micro-bumps at the backside of the photonic wafer (imec) and upside of bottom wafer (electronic wafer, made at ams). During

assembly, these bumps land on each other and are then fused together through transient liquid phase bonding

For a first demonstration, III-V photodetectors, were integrated on a 1 x 8 AWG, fabricated in a standard waveguide process. The response shown on Figure 11 includes the losses of the grating couplers at the input and the detector.

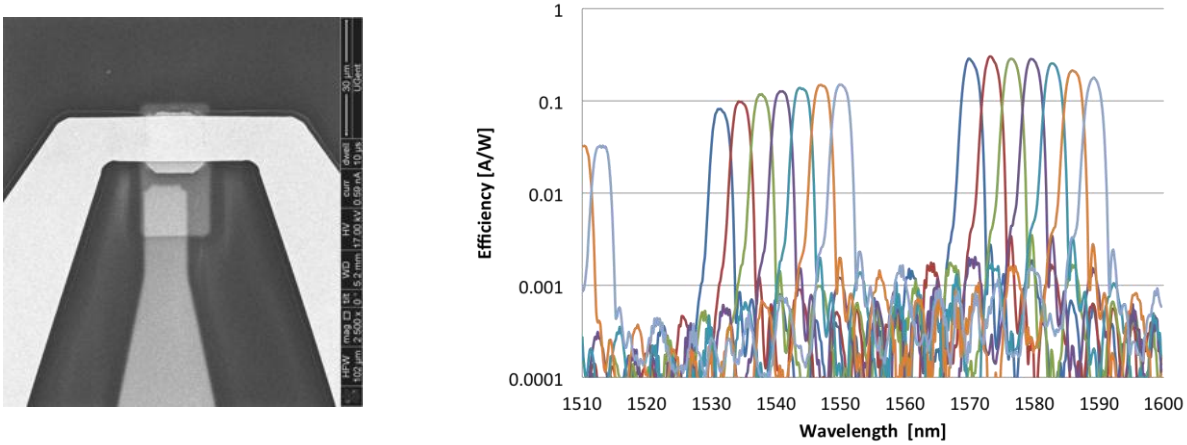

Figure 11: III-V photodetector on silicon grating and response of photodetectors integrated on top of 1x8 AWG, including losses from input grating coupler

To achieve the bonding, a process flow was conceived which basically included three steps:

1. Deposit blanket layer of a dielectric on the wafers.
2. Etch holes of same size and shape all over the wafer for 'dummy' micro-bumps (which connect to dummy TSVs) and 'functional' micro-bumps (which connect electronics devices of wafer with functional TSVs).
3. Fabricate micro-bumps on these holes through plating.

Back Side Integration: ams and CEA

This back side integration is based on the direct bonding of a front end photonic wafer (PIC) at the back side on the electronic wafer (EIC). Then formation of 250µm deep and 100µm diameter TSVs was realized in order to get an assembled photonic-electronic wafer (PEIC). The demonstrator was consisted of a thermally tuneable ring resonator connected to the electronic wafer.

The photonic wafer is based on 220nm SOI with fibre coupler, waveguides, 10µm radius ring resonators and 250nm Ti/TiN heater. Bonding of the two wafers, TSV and top metal processing have been performed by ams.

Below are the images of the results with front side and back side processed wafer, front side pads, back side with photonic layer, and ring resonator.

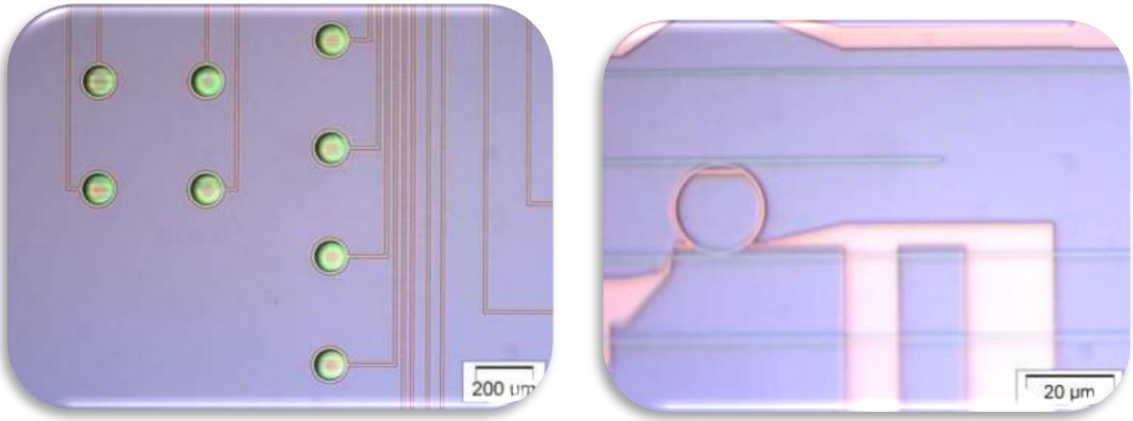

Figure 12: Images of the front side (TSV) and back side processed wafer (RR with heater)

The wafer has been diced in small samples and mounted on a PCB with holes for connecting the front side and testing the back side. The PCB was mounted on an optical bench with tilted fibers for injecting the light via the surface grating couplers. The FSR of the ring resonator is 7.7nm and the heater connected to the PCB by the front side has a tuning efficiency of 0.06nm/mW.

Integration with TIA: TUW

austriamicrosystems delivered two multi product wafer lots with the TIA designed by TUW for 10G operation for InGaAs or Ge photodetectors. The design demonstrates successful 10 Gbps data transmission even at low input currents. TUW constructed the measurement setups, characterised three 8-channel optical receivers experimentally and verified that heterogeneously integrated receivers can reach a sensitivity of -26dBm. CEA and IMEC provided 8-fold arrays of the Ge photodetector, respectively of the InP/InGaAs, photodetector - originally designed for heterogeneous integration on top of the CMOS wafer - with bond pads for conventional wire bonding. To characterise the CMOS chip these two photodiode types and a vertical Ge photodetector array, designed for wire bonding, were conventionally wire bonded to a receiver version equipped with external bond pads. Therefore three different receiver/photodiode combinations were available for characterisation.

The performance of the different receiver/photodiode combinations was determined by measuring the frequency response, the rise and fall times and the bit error rate using an optical PRBS31 data signal with a data rate of 10 Gbps. The two receiver versions with the wire bonded GePD and the InP/InGaAs photodiode arrays reached sensitivities of -12.65 dBm (CEA), respectively -12.60 dBm (IMEC). These sensitivities are the result of wire bonding photodiodes which were originally designed for heterogeneous integration on one hand and the detector responsivities of 0.15 A/W (CEA) and 0.14 A/W (IMEC) on the other hand.

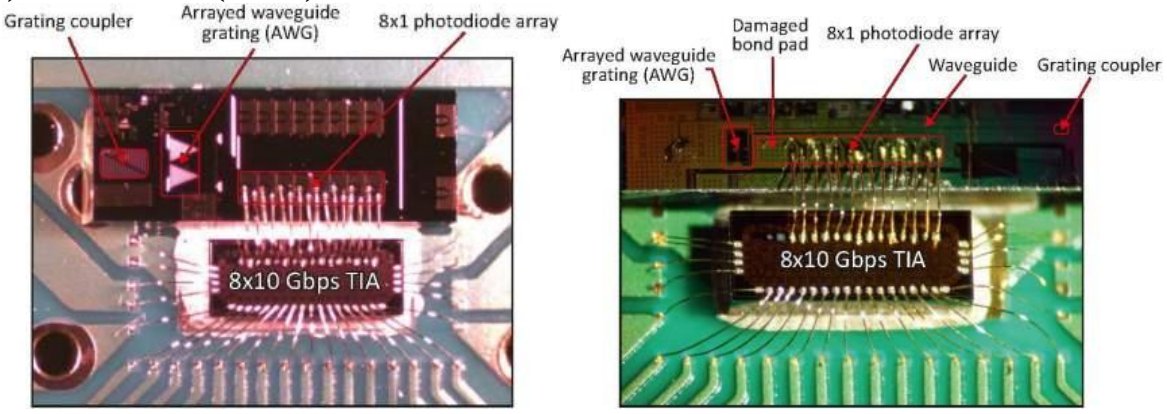

Figure 13: 8-channel receivers with 10Gb/s TIAs and 10E1 Ge photodiode array (left) and InP/InGaAs photodiode array (right) used for verification measurements

The receiver with the wire-bonded vertical Ge photodiode (R=0.5A/W) showed a measured sensitivity of -20dBm. Simulations showed that the heterogeneous integration of the photodiodes would increase the sensitivity by around -3 dBm due to the smaller parasitic capacitances between photodiode and amplifier input. Therefore sensitivities of around -26 dBm ($BER = 10^{-9}$) could be achieved by using heterogeneously integrated photodetectors with responsivities of around 1 A/W.

It can be concluded that the heterogeneous integration of the photonic chip on top of the CMOS chip is a promising way to improve the performance of optical receivers.

Modulator demonstrator with SiGe driver

Photonic SOI substrates as used to large extent in HELIOS are unfit for frontend of line co-integration of photonics with BiCMOS (i.e. realization of photonics and electronics next to each other on the same substrate). This is mainly for 2 reasons: incompatibility with collector fabrication and the higher thermal resistance compared to the bulk Si substrates normally used for high-performance BiCMOS or bipolar processes. To reconcile the different substrate requirements for photonic and electronic devices, IHP developed the so-called local-SOI approach for a novel photonic BiCMOS process. In this process, the electronics part used a SiGe bulk technology aside from a photonic part with a 2µm buried oxide.

TUW has designed modules of a >10Gb/s modulator driver in IHP SG25H3 technology by circuit simulation, layout and postlayout simulation. Each amplifier cell consists of a common-mode feedback circuit so that the amplifier works in an appropriate operation point. The driver uses two supply voltages to deal with the low collector-emitter breakdown voltage (2.3V) of HF-transistors (f_t max 110GHz).. The modulator driver has a power consumption of about 650mW.
A stand-alone modulator based on the thin modulator design was fabricated first and characterized. With the SiGe back-end technology, the electrode performances were sufficient to support 10Gbit/s and even 20Gb/s over the lengths used for the final demonstrator design. Good efficiency below 2V.cm was achieved with a total insertion loss from input fibre to output fibre, via 2 lensed fibre connected to grating couplers of 30dB.

A full combined modulator and SiGe driver (in SG25H3) demonstrator fabrication run was completed at the IHP foundry. The left part of Figure 14 of the dual drive modulator shows the two parallel coplanar electrodes with the two output RF tapers (top of the chip) and SiGe driver part at the bottom of the chip.

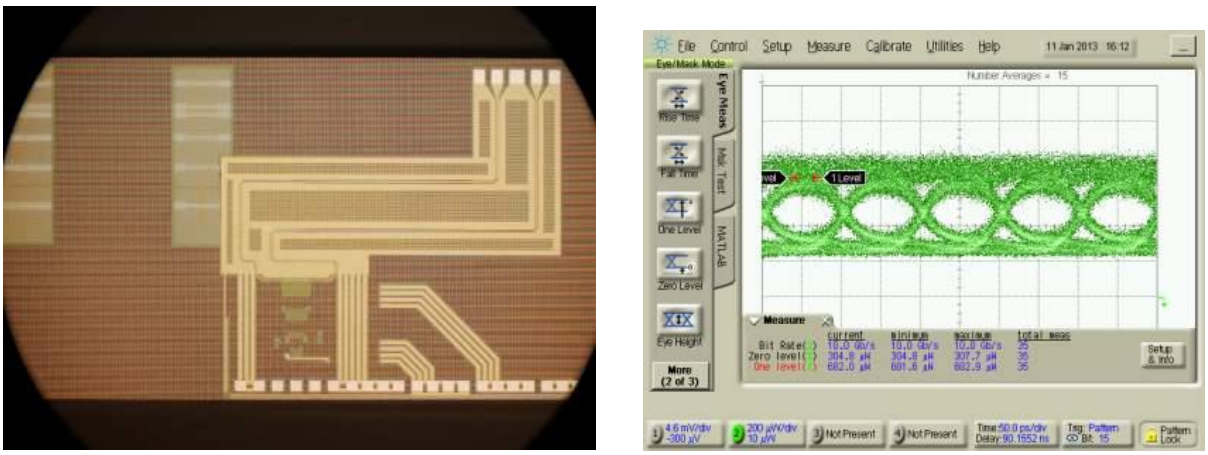

Figure 14: Microscope image of driver / modulator pair (left), eye diagram at 10Gb/s (right)

First test results obtained at University of Southampton of FEOL integrated modulators + driver devices indicate functional behaviour of the co-integrated devices up to 10Gb/s with dynamic extinction ratio of 5.5dB (Figure 14). **This is the first demonstration of full electronic-photonic integration in high-performance BiCMOS.**

16 x 10Gb/s transceivers

Integration of 16x10 Gbit/s receiver

The objective of this task was to realize polarization independent 16x10GBit/s receiver PIC, by combining silicon AWG based demultiplexer with integrated photodetectors. Polarization independence is obtained through a polarization diversity approach. For the detectors we chose heterogeneously integrated InGaAs detectors, bonded on top of silicon grating couplers. The rationale for this choice was twofold:

- This is a low temperature process (<400C) compatible with CMOS backend processing
- These detectors, bonded on III-V grating couplers are compatible with a thick bonding layer and hence put less restrictions on this bonding layer

The AWG based demultiplexer exhibited a low polarization dependant loss as seen on Figure 15, reaching a low PDL. However the yield for the InGasAs photodetectors was low despite a satisfactory bandwidth and sensitivity. The state-of-the-art on Ge-photodetectors such as CEA ones has improved a lot over the course of the HELIOS project. Therefore at this point it seemed no longer relevant to put effort in process development towards improving the yield of the grating coupled III-V detectors. However for application operating in other wavelength ranges (and in particular beyond 1600nm), III-V bonded photodetectors are still extremely relevant and the only practical choice available for the moment.

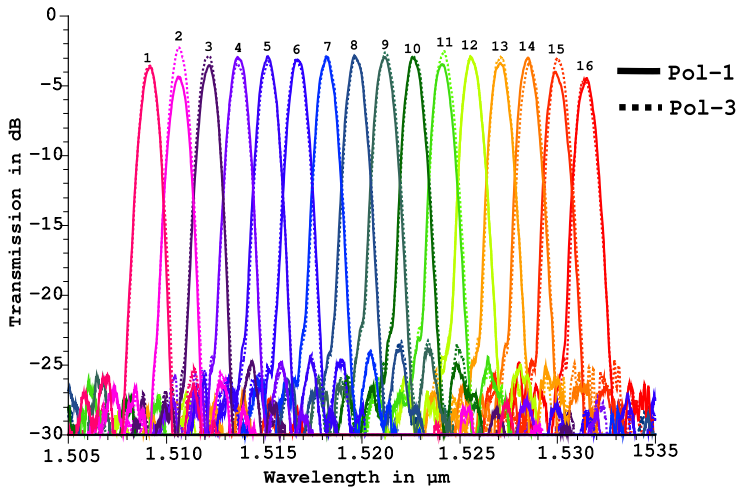

Figure 15: spectral response of the 16 channels 200GHz polarization diversity wavelength de-multiplexer circuit for two orthogonal polarizations.

Single channel III-V/SOI Tx at 10 Gbit/s

Single-channel III-V/SOI Tx design, fabrication and characterization were completed during the fourth year of the project. Figure 16 shows a schematic view (left) and a picture (right) of the integrated tunable laser – Mach-Zehnder modulator (ITLMZ). The ITLMZ chip consists of a single mode hybrid III-V/silicon laser, a silicon MZM and an optical output coupler. The single-mode hybrid laser includes an InP waveguide providing light amplification, and a ring resonator (RR) allowing single mode operation. Two Bragg reflectors etched on silicon waveguides close the laser cavity. The MZM allows modulation of the output light emitted by the hybrid laser.

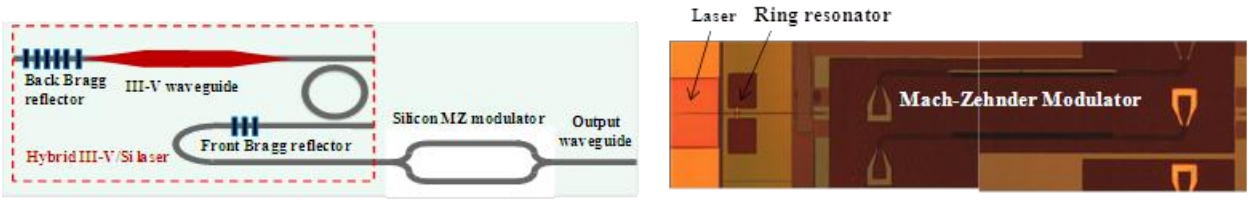

Figure 16: Schematic view (left), and picture (right) of the ITLMZ chip

The RR based hybrid laser exhibits a CW threshold current around 41 mA at 20°C and the output power coupled to the silicon waveguide is around 2.5 mW for an injection current of 100 mA. The maximum output power is around 6.5 mW at 20°C, and the output power is still higher than 1 mW at 60°C. Electrical current injection into the heater allows thermal tuning of the ring resonance wavelength. A typical tuning range of 9 nm is achieved in our transceivers. The heater resistance is in the range of 20-100 Ω, and the thermal tuning efficiency is in the range of 0.15–0.4 nm/mW.

The silicon modulator is a depletion type lateral pn junction modulator. The length of the modulated phase shifters is 3 mm. The arm length difference of the MZM is 150µm, resulting in a free spectral range of around 4.5 nm. The estimated VπLπ for the modulator is around 3 V cm. From the power level measurement from a laser alone with the same structure and from the output of the ITLMZ chip, the intrinsic losses of the MZM are estimated to be around 13 dB at its maximum transmission point. Dynamic measurements show that for a reverse bias Figure 17 larger than 2V, the 3 dB modulation bandwidth is larger than 13 GHz.
(left) shows the BER curves for all the wavelengths and also a reference curve for a directly modulated laser, measured using a high sensitivity receiver including an avalanche photodiode.. The ER of all those wavelengths varies from 6 to 10 dB, while the ER for the reference is only 4 dB. One can see that all channels have better BER performance than the reference for received power levels lower than -25 dBm, due to the higher ER of the ITLMZ compared to that of the reference.

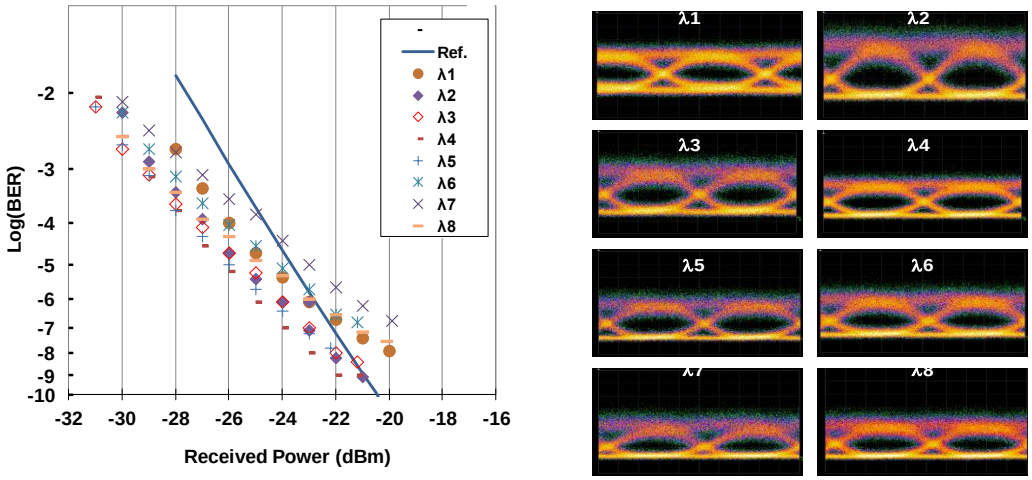

Figure 17: Bit error rate (left) and corresponding eye diagrams for different wavelengths (right)

Integration of a 16x10 Gbit/s transceivers (III-V Lab)

The same wafers as those for single channel Tx are used for the 16x10 Gb/s transceivers. As the lasers are designed to be tunable, they can be directly used in the 16x10 transceivers. The new element for this transceiver is the arrayed waveguide grating (AWG), which is also integrated and fabricated on those wafers. Figure 18 shows the transmission curves of an AWG with 16 channels

and 200 GHz channel spacing. AWG exhibits losses around 4 dB and channel cross-talk around 10 dB, which is perfectible.

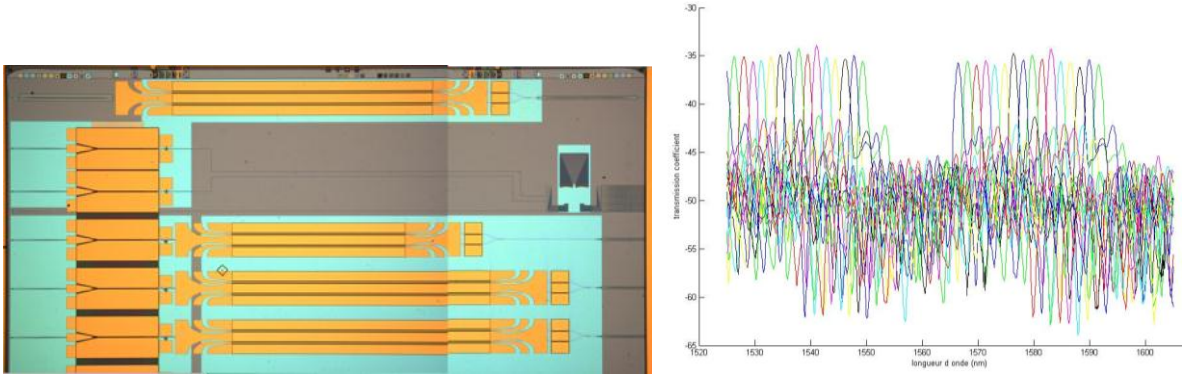

Figure 18: Transmission curves of an AWG with 16 channels

Transceiver modules for multi-function antennas

The transceiver modules for multi-function antennas include 4 WDM digital channels and one WDM analogue channel. Moreover, the transmitter and the receiver are integrated on the same chip which conducts to a complex technology.

Two technological runs have allowed to realize several multifunction transceivers. Several evaluations have been conducted:

- Hybrid lasers: Single mode operation with output power level around 0 dBm, SMSR > 30 dB, tuning range of 20 nm is achieved
- PIPIN modulators: the DC contrast was around 17 dB, with a 3 dB modulation bandwidth > 20 GHz.
- AWG: A cross-talk around 13 dB and the losses < 4 dB
- Ge photodiodes have demonstrated frequency response above the transceivers specifications.

It was the **first PIC chips integrating lasers, modulators, photodiodes and AWG.**

Photonic QAM receiver and modulator

Photonic QAM Modulator (DAS Photonics)

The QAM transmitter was fabricated at CEA and two critical building blocks are the DEMUX and the MZM based on the thin design of Southampton University. Microheaters and monitoring Ge photodiodes are also included in the fabrication.

Figure 19: Fabricated DQPQK transmitter

The measured eye-diagram of the modulated DPSK signal at 5Gbps, is shown in Figure 20. The noise is mainly due to the low driving voltage. For the best performance DPSK should be driven in

push pull with V_π driving voltage over each arm, summing up to a total of $2V_\pi$. The driver was limited to only 8V, reaching only 67% of the full driving power.

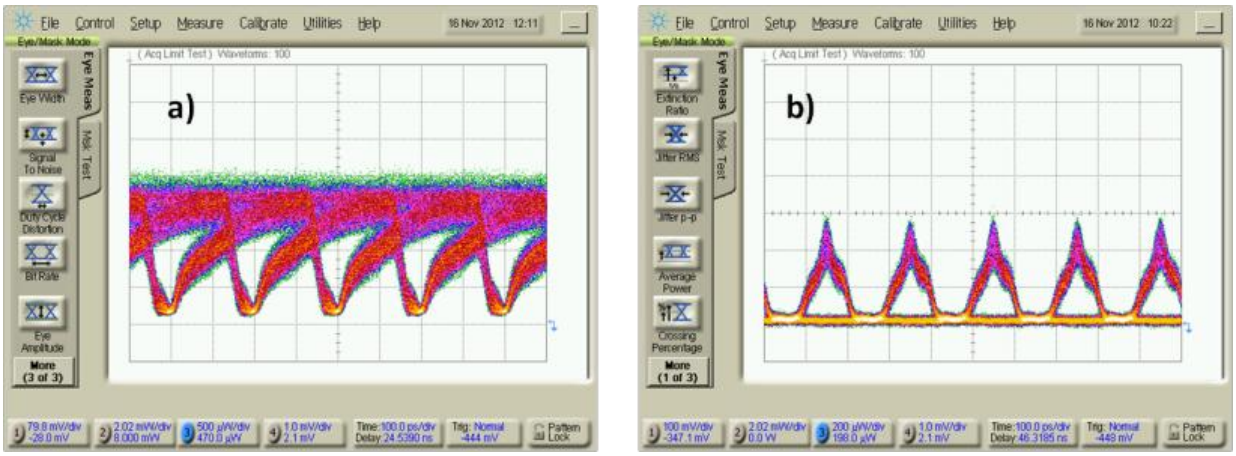

Figure 20: Eye-diagram of the modulated DPSK signal at 5Gbps

Photonic QAM Demodulator (DAS Photonics)

The receiver chip was fabricated at CEA including a thermo-optically tunable MZI power splitter to actively control the input power to the Mach-Zehnder Delay Interferometer (MZDI) ; MZDI that delays one bit with respect to its adjacent bit; and a 90 degree hybrid to recombine the I and Q signal. At the output the in-phase (I) and quadrature (Q) signals are detected using two balanced Ge photo diodes (BPD) in pinpin configuration.

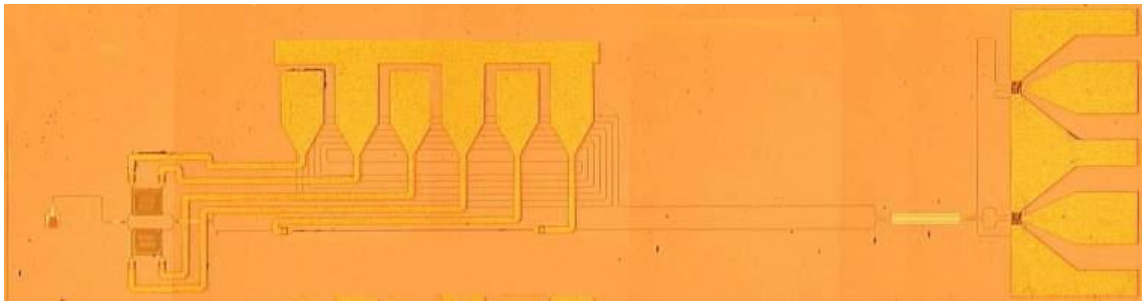

Figure 21: Fabricated DQPQK receiver

For an input power of 5.5dBm, a well opened eye-diagram of the demodulated signal for 2x5Gbps operation was obtained.

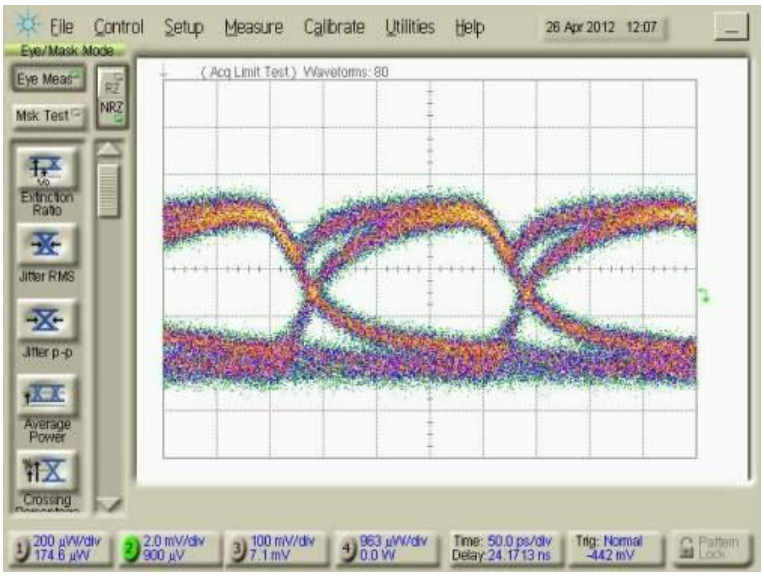

Figure 22: Eye diagram measured for the 2x5Gbps differential receiver

In order to validate the system, a set-up was build using commercial off-the-shelf components. The BER was measured at the output of the DPSK MZM. Results show a very good performance of the proposed differential phase modulated millimetre wave wireless system, considering that the results include fibre transmission and frequency up- and downconversion. Receiver sensitivity at the receiver CS of around -27.5 dBm was measured for a BER of 10^{-6}. Comparing with the B2B case, a penalty of 6 dB is observed. In the described measurements, just one RF amplifier is used, and a rough calculation of the power budget for a typical wireless link with high gain antennas and extra RF amplification stages indicates that transmission distance of a few hundreds of meters could be achieved with the obtained performance results.

Packaging

Targets of the packaging activity were the packaging and integration in metal housing of the 10Gbit/s wireless transmitter (Tx) and receiver (Rx) demonstrators and of the modulator and driver demonstrator with combined fabrication at IHP. All the metal housing, the silicon submount, DC and RF ceramic PVB were studied and designed in this frame, and fabricated. This work was conducted by Photline to make use of Photline's existing packaging technology portfolio for the packaging of the demonstrators. The essential feature of this technology is horizontal fiber coupling.

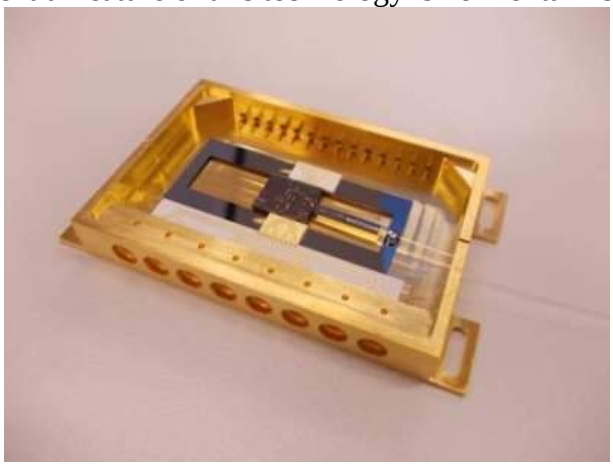

Figure 23: Assembly of the Rx model in the metal housing and connections to the primary RF ceramic PCB.

Amorphous Si modulator

The goal of the study was to evaluate the potentially of the fabrication of silicon modulator with a back-end technology (below 400°C)

A Mach-Zehnder Interferometer (MZI) based on the low temperature budget technology of hydrogenated amorphous silicon (a-Si:H) has been optimized with an efficient method for simulating the electrical and optical characteristics, in DC and transient conditions, of free carrier injection/depletion-based electro-optical active devices based on this semiconductor.

The Mach-Zehnder interferometers (MZI) based on an a-Si:H p-i-n structure have provided surprising results for low-temperature processed photonic devices (T<150°C), in particular very encouraging under the point of view of bandwidth. Switch-on and switch-off times of the order of 3 ns have been measured in fact, with a $V_\pi \times L_\pi$ figure of merit of ~20 V×cm.

The incorporation of the MZI into slow wave structures can offer advantages in both reduced device length and lower power consumption. Parametric simulations have been performed to design PCWs that are compatible with standard and low cost technologies. The best results were obtained assuming a refractive index n=3.58 for a-Si:H, a value that has been previously measured during the fabrication of the multistack waveguides where the electro-optical absorption effect has been characterized.
The refractive index change requested to get a full π-shift in mm-sized arms is consistent with the experimental results obtained on the experimental MZI. By using in fact the same $\Delta n/\Delta V$ experimentally verified for the a-Si:H MZI, characterised by an arm length of 13 mm, we can conclude that for the newly designed PhC device we could obtain a full π-shift in a 1.5 mm-long arm by applying the same driving signal (~30V), with a consequent reduction of the $V_\pi \times L_\pi$ figure of merit from 40 V×cm down to 4.6 V×cm.

Silicon nanocrystals for light emission and amplification

Silicon nanocrystals for light emission and amplification layers were designed, fabricated, and characterized. The main results are:

- Bipolar injection via direct tunnelling in nc-Si LED emitting in visible with power efficiency of 0.2% was demonstrated.

- LED Devices were fabricated: 0.1% of external quantum efficiency has been obtained. The LEDs physical principles have been understood and modelled.

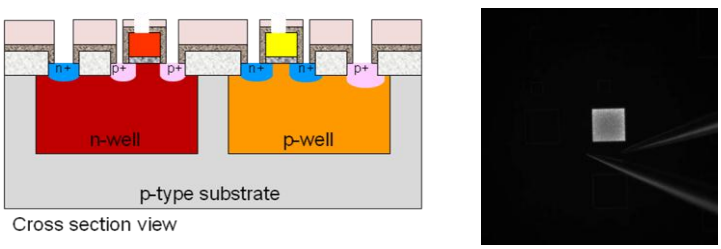

Figure 24: Schematic cross-section of the LED and a top-view image of emitting visible LED.

- Electrical and electroluminescence (EL) properties of Er-doped Si nanocrystals were studied in detail under both direct and alternating current excitation schemes in a broad range of

applied voltages and driving frequencies. Dependence of the Si-nc LED external power efficiency on the AC driving frequency is worked out, see Appl. Phys. Lett. 98, 201103 (2011).
We found that silicon oxide matrix (SRO) is much better for Er EL than silicon nitride (SRN), which is in contradiction with a raising consensus that SRN is much better than SRO for lasing (see, e.g., Si Laser MURI or KAIST publications). The high current in SRN is mostly leakage through conducting paths via defects.
Impact ionization is responsible for a great part of EL emission and we know what material is the best to maximize it. It is necessary at least 4-5 MV/cm to make most samples to emit and this is the threshold for the Fowler-Nordheim injection. Furthermore, we are able to saturate excitable Er in SRO by electrical pumping and we have checked that emission is comparable (within a factor 2, see below) to Er optically active in stoichiometric SiO_2. Even though results show that optically active Er is only 10-20% (see the preceding point 3) of the total Er concentration, we have to admit that those measurements and calculations were done by optical means with a strong pumping at 980 nm or 1480 nm and the uncertainty is large. So, being a factor of 2 less than Er in SiO_2 emission by electrical pumping is a very interesting result because it leaves great expectation on lasing in such system.

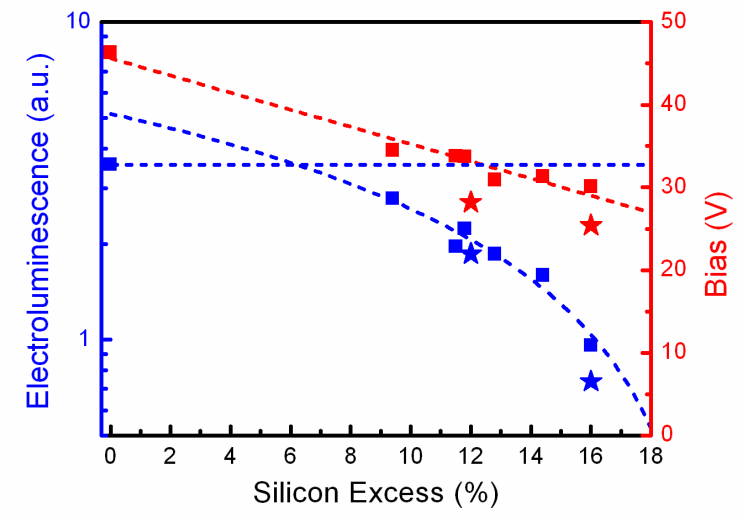

Figure 25: EL intensity at 1.54 µm (left axis, blue symbols) at a fixed injected current of 1 µA as a function of average content of silicon excess for a series of multilayer LEDs (squares) and single-layer LEDs (stars) and corresponding driving voltages (right ax

- Fabrication, layout, simulation and testing of the electrically driven horizontal slot waveguide amplifier devices with erbium-doped SiO_x have been performed during this last period. Although no gain is observed, the physics of the system has been investigated and many interesting results have been communicated. High propagation losses in the waveguide, charge accumulation in the slot region and low fraction of the Er ions coupled to Si-nc are identified as main reasons for the lack of amplification. The obtained results bring new understanding of the active material and new developments of the amplifier with Er coupled to Si-nc active material.

On injection slot ring-resonator laser cavity (Figure 26), clear whispering gallery mode resonances have been measured by transmission measurements. Guided electroluminescence from slot waveguides and the micro-ring resonators has been observed

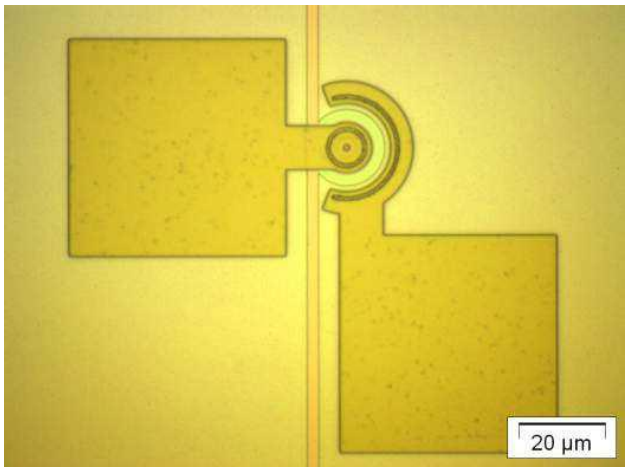

Figure 26: Injection slot ring-resonator

CMOS-compatible 2.5D VCSELs

This new concept brings a new class of photonic devices, combining VCSEL like technology and silicon photonics technology.

A broadband silicon photonic crystal based mirrors with a good tolerance to technological imperfections were designed and fabricated in the aim of getting compact 2.5D cavities with Q~10000 for III-V/Si microlaser and compact 2.5D cavity with Q~10000 for silicon-based light emitters.

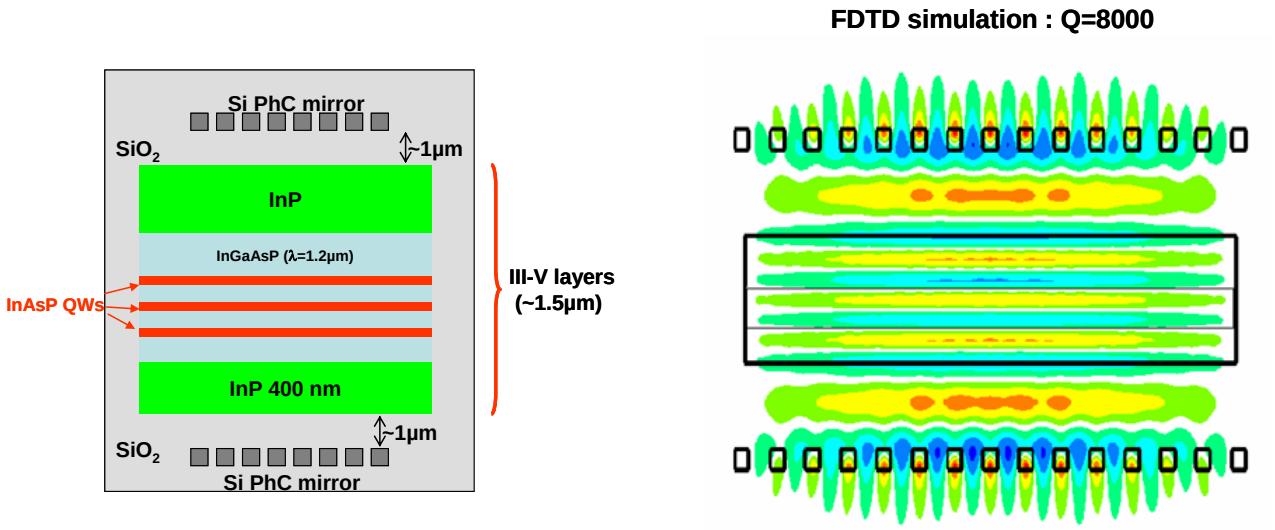

Figure 27: Schematic of a 2.5D VCSEL with III-V layers and corresponding electric field distribution

Optically pumped source

New generation of VCSEL devices have been fabricated onto 200-mm SOI wafer with 2-µm-thick buried oxide (BOX). Exemplifying schematic view of a double PCM-VCSEL structure is given in Figure 28. An embedded MOCVD-grown multiple-quantum-well active region is placed between two 900-nm-thick SiO_2 gaps. The structure is then vertically terminated by a top and bottom Si/SiO_2 1-D PCMs characterized with a 50% Si fill-factor, lattice period and membrane thickness equal, respectively, to 910 nm and 285 nm. In order to realize a better management of light losses in the

cavity, a photonic crystal heterostructure has been introduced in both PCMs through a step function of the silicon slits filling factor.

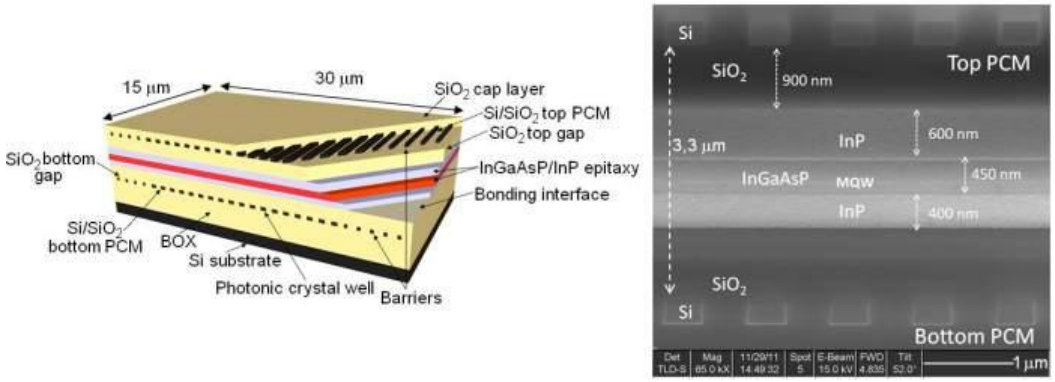

Figure 28: Schematic view (left) and cross-sectional view obtained by FIB (focused ion beam) milling (right) of double PCM-VCSEL structures.

With optical pumping, continuous-wave (CW) single-polarisation laser operation has been demonstrated with less than 500 µW threshold and up to 45°C under optical pumping. A full modal control of laser emission can be obtained in these VCSELs through the introduction of above mentioned heterostructures. Single (with side-mode suppression ratio larger than 26 dB) as well as multi-mode operation can be selectively addressed for each VCSEL device integrated on the SOI wafer by simply engineering the PCMs lithographic patterning of the silicon layer. Devices are endowed with enhanced lateral and vertical compactness (lateral size of 30 µm and 15 µm, respectively). Concerning maximum output power the devices, although very limited by the total available pumping power, exhibit CW output power levels around 0.4 mW.

Electrically pumped CMOS compatible 2.5D VCSELs

The fabrication of the devices has taken place at CEA during this last period and is illustrated below:

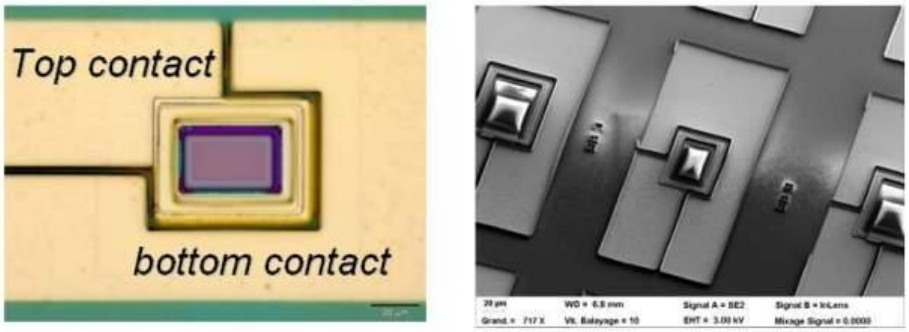

Figure 29: Optical (left) and scanning electron microscope (right) views of electrically-pumped 2.5D VCSEL devices.

Preliminary test of the devices have been performed. The control of the technology is further demonstrated by the electrical characteristics of the laser sources, which exhibit nearly ideal *pin* diode behavior, with negligible series resistances. Preliminary CW electroluminescence spectrum measurements, which were carried out on a limited number of devices, provide evidence of the presence of the expected optical modes of the 2.5D cavity. Stimulated emission is not yet clearly demonstrated, although not being far off (see Figure 30). A careful observation of the devices tested

so far indicate that the silicon filling factor of the top reflector is slightly too small, thus resulting in a reduced quality factor of the 2.5D hybrid cavity mode, as derived from the results of optical simulation.

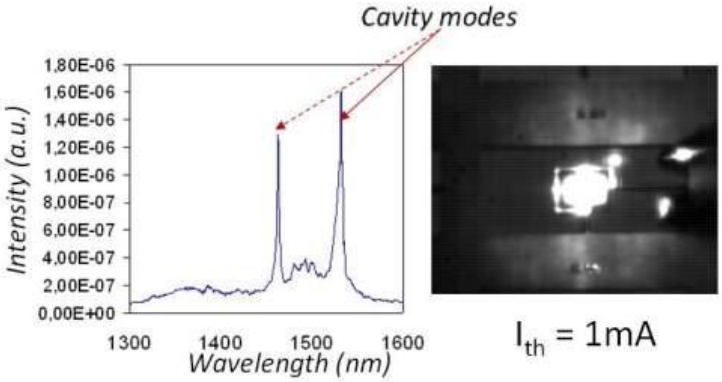

Figure 30: Electroluminescence spectrum and IR camera shot of the laser source under 1 mA of current injection (b)