Collaborative project

Small or medium-scale focused research project

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SEVENTH FRAMEWORK PROGRAMME

Table of Contents:

1. Executive summary

In recent years, flexible electronics technology has developed rapidly and is now on the verge of commercialization, promising new applications from smart food packaging to wearable health monitors. All these applications require programmable non-volatile memory (similar to the well-known Flash memory), and the more complex the application, the more memory it needs. However, flexible memory development hadn't kept pace with other areas of flexible electronics, limiting market opportunities. So the European Union launched the MOMA project in 2010 to develop low-cost, reprogrammable polymer memories and integrate them with thin-film transistors on flexible plastic substrates.

The MOMA consortium brings together commercial and research partners from across the memory value chain. These partners are chip maker STMicroelectronics, materials supplier Solvay Specialty Polymers, innovation centers imec and Holst Centre plus Catholic University of Louvain and University of Groningen.

The project focused on ferroelectric memories based on soluble ferroelectric polymers and organic and oxide semiconductors. It has successfully developed new grades of memory materials that can be tailored to specific applications and deposition techniques (including spin-coating, inkjet printing and imprinting). The project partners used these materials to develop memory arrays based on both transistors and diodes, optimizing production processes to deliver high yields and excellent memory performance.

With its 1-kbit (32x32) array, MOMA has delivered the largest flexible memory arrays to date and achieved production yields close to 100%. Furthermore, it has created the thin-film read-out electronics necessary for use in real applications. The partners have combined all these building blocks into fully functional memory arrays with the related read/write circuitry. At the end of the project, a well-elaborated application and technology roadmap is in place to ensure valorization of the project results. Part of the scientific work is published already in high-impact scientific journals as Advanced Materials and Nature Materials.

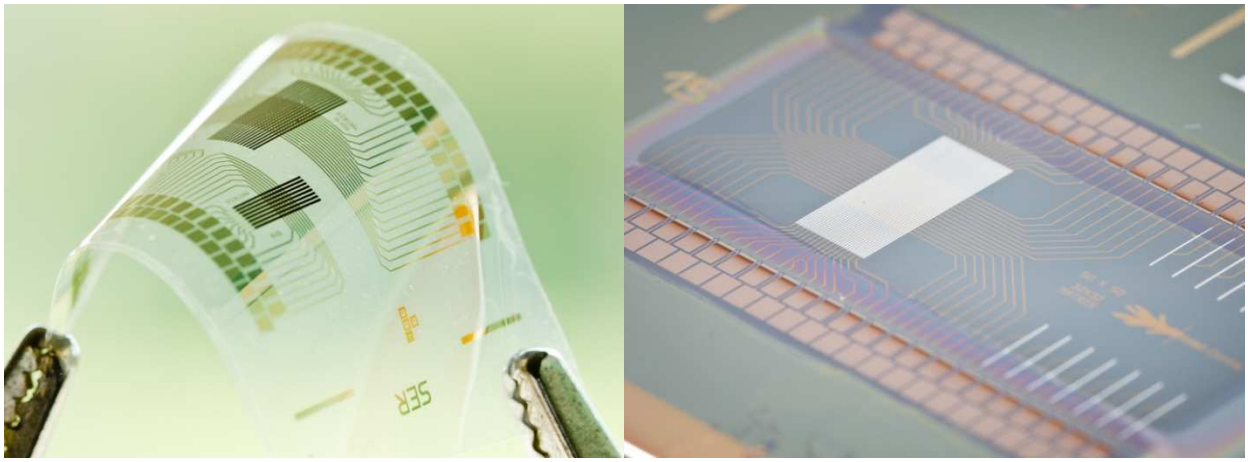


Figure 1: *Non-volatile memory arrays produced on flexible substrates: (left) 256-bit transistor based memory array, (right) 1 kbit diode based memory array.*

2. Summary description of project context and objectives

The proposed project intends to develop low-cost re-programmable polymer memories that are integrated with organic transistor circuitry on thin flexible, plastic substrates. To reach this goal we need to combine materials development, in particular with appropriate large area, low-cost manufacturing technologies that are in-line compatible and applicable to high volume production.

Advanced technologies in film deposition, device fabrication, device testing, memory structure and memory architecture will be researched and developed. A concrete focus on highly integrated memory demonstrators will be used to drive the research and technology forward. The above objectives are elaborated quantitatively, and in more detail, in section 2.1 (see Table 1).

2.1 The concept of embedded organic memory arrays: How?

The aim of this project is to develop the materials and processing technology to make polymer ferroelectric memory arrays on very thin plastic substrates. Key ingredients are:

Soluble ferroelectric polymers
We will use poly (vinylidene fluoride-trifluoro ethylene), P(VDF-TrFE), polymers as ferroelectric material. P(VDF-TrFE) has several advantageous properties including a large remanent polarization, excellent polarization stability, low leakage for high resistivity and switching times as short as 1 µs. Furthermore, it is intrinsically bistable, *i.e.,* it does not require a voltage to keep its polarization state. It can be processed from solution at **low temperatures**, opening the possibility of using a wide range of plastic substrates instead of glass – saving weight and making the final product thinner and virtually unbreakable. Moreover, since the **mechanical properties** of polymer materials are compatible with plastic substrates. It is therefore ideally suited for **next-generation organic electronics applications that require re-programmable, non-volatile memories.**

Film deposition and patterning
A range of technologies can be used for cost-effective solution-based deposition. Examples range from simple spin coating, reel (to-reel) coating or spray deposition for application of unstructured thin layers, to more advanced printing techniques such as inkjet and imprinting for direct application of patterned films. Since printing technologies and printing materials of today have to be considerably improved to enable fully printed smart objects in long-term perspective, the production technology for organic electronics and systems in near future will be most probably a heterogeneous integration process merging the different classical technologies with key additive deposition technologies to be developed in the next years. Traditional structurization like photolithographical processes will also play a role in future and may be also integrated in low-cost processing, in particular to achieve high-resolution patterns.
We will deposit and pattern these material using inkjet printing as well as direct photo-imaging of P(VDF-TrFE). Moreover, we will employ nanoimprinting to control the morphology with the aim to lower the programming voltage. Different grades of P(VDF-TrFE) will be synthesized with physico-chemical properties tailored to the requirements of the different process technologies (composition, molecular weight, solubility parameters, viscosity …).

Different devices
One of the simplest types of ferroelectric memory devices is the thin film capacitor. Information is stored by aligning the direction of the internal polarization either up or down with an applied field. It suffers however from the following drawbacks:

- destructive read-out. To retrieve the information one applies a switching voltage to obtain a high or a low charge displacement current response depending on whether the internal polarization was aligned or not with the direction of the applied field. Ferroelectric capacitors therefore have a so-called destructive read-out since a read operation can affect the stored information. If the polarization direction was changed during the read operation then a reset voltage needs to be applied afterwards.
- Scaling. The charge displacement response scales with the surface area of the capacitors. Downscaling of the lateral dimensions lowers the displacement currents and at some point they can no longer be detected reliably.

This device therefore requires complex addressing schemes. **We therefore focus on ferroelectric memory elements in which the programmed state is sensed as a change in resistivity without altering the state (non-destructive read-out).**

Transistor-based memories – We will work on the simplest layout of a ferroelectric memory transistor, i.e., a metal-ferroelectric-semiconductor layer stack, in which the ferroelectric layer serves as the gate dielectric. The polarization state of that ferroelectric regulates the flow of current through the transistor. Key to achieving good performance in these devices is the formation of well-defined, abrupt interfaces, especially between semiconductor and gate insulator. P(VDF-TrFE) polymers are semi-crystalline and thin layers therefore are relatively rough. A rough interface generally lowers the transistor performance. Furthermore, it is non-trivial when layers are processed from solution, *i.e.* by spincoating and/or inkjet printing, and requires a proper choice of solvents to prevent dissolution and swelling of the previously deposited films.
Using **nanoimprinting** of the P(VDF-TrFE) gate dielectric we vary the surface properties (e.g., roughness) and use that to study the relationship between the characteristics of the device and the nanostructure of the interface between the ferroelectric and semiconducting layers.

Diode-based memories – The concept behind this memory element is to combine two polymers that have distinct roles in its operation: a ferroelectric polymer provides the binary state and data retention whereas a semiconducting polymer provides the means to probe that state via an electrical signal. In the pioneering work of Asadi et al. a polymer blend is spread as a continuous film between the two electrode arrays. Although elegant in its simplicity, its operation mechanism is not understood. Hence, we also intend to work on a bi-layer concept in which the ferroelectric layer is deposited first and **nanoimprinted** after which the semiconductor is deposited. This task is divided in four sub-tasks, including the fabrication of suitable NIL molds with step profiles (upper row of Figure below), imprinting with step molds and structural characterization of the layer, fabrication of NIL moulds with sloped profiles and imprinting with sloped moulds and characterization of the imprinted layer.
This so-called bottom-up approach allows well-defined geometry, enables therefore good model systems for device physics and may also lead to improved memory devices.

Independent of the memory concept, a number of fundamental and technological hurdles need to be overcome: understanding and improvement of the device operation needs to be developed, as well as the printability and its influence on the nanoscale morphology of the blends/interface topology of the ferroelectric – semiconductor interface in transistors and diodes.

Memory arrays

Owing to its similar architecture, ferroelectric transistors can be 'simply' integrated into existing technology based on organic transistors. This compensates, we believe, for the larger footprint of this device. Ferroelectric diodes based on a combination of semiconducting and ferroelectric polymers allows for a simple crossbar array with the smallest foot print possible: the resistance of the memory switches, and hence the device offers the possibility for simple current read out.
Important aspects will be to study crosstalk, i.e. the influence of programming or reading on non-addressed bits. Although patent literature suggests that for P(VDF-TrFE) this issue is not severe as for other ferroelectric materials, it has not been confirmed, simply because no-one has made functional arrays yet. The relative importance of crosstalk becomes more important when scaling down the size of the bits. Scaling down on the other hand is economically attractive. We will study the effects of scaling down to ~100 bits/mm^2.

The memory elements are preferably made with the same, or similar, technology that is used to make the logic transistors. Here, IMEC and TNO will bring in their background in high-performance transistors, more specifically a 150-mm wafer process using pentacene as semiconductor. All layers are patterned using photolithography. This transistor technology will be used as a basis for integration of memory elements. Starting from a flexible substrate, the stack of layers that needs to be integrated to arrive at a circuit with embedded memory array is schematically represented in Figure 1.

Two transistor geometries will be developed:

- **Bottom-gate ferroelectric transistors** by incorporating ferroelectric polymer dielectric at pre-selected places to create memory transistors at these places in a circuit. Because many of the layers of the logic and memory transistor can be defined using the same mask step, this offers a route to low-mask count. Challenges are the compatibility of materials and processes. Key steps to be developed are a patterning process for the P(VDF-TrFE) gate dielectric, and a photolithographic process to make the source-drain contacts on top of the P(VDF-TrFE) laye.
- **Top-gate ferroelectric transistors**. In this case the memory transistors are made on top of a substrate containing already the fully processed (and functional) logic circuits, using low-cost additive inkjet printing methods. This allows maximum flexibility in choice of materials and processes, provided the performance of the logic transistors is not negatively impacted. Key steps to be developed are a inkjet printing process for the semiconductor (most likely a polymer), P(VDF-TrFE) gate dielectric, and applying a top gate electrode (initially shadow masker, later inkjet printing). In addition, extra wiring is needed to contact the top gate metal to the logic circuitry.

Also in the case of the diodes, these diodes are made on top of a substrate containing already the fully processed (and functional) logic circuits, using low-cost additive inkjet printing methods. It seems logical to define the bottom electrode of the diode in the same mask that is used to define the source-drain or gate electrode of the logic circuit, most likely we will use gold. The upper electrode of the diode will be made of silver. At first, evaporated using a shadow mask, but at a later phase we will also opt for direct deposition **(and curing of) inkjet printed Ag nanoparticles.**

The challenging combination of the elements above has not been shown in the state of the art.

Embedded memory arrays with logic circuitry

As the primary cost of a small array is likely to be in the drive electronics, the greater the number of word and bit lines, the lower will be the cost per bit as more bits are defined on a given area. Organic transistors are a potentially low cost technology. Moreover, they are highly compatible

with plastic substrates, because of its low processing temperatures and similarity in thermal expansion coefficients. Furthermore, Europe is frontrunner in this new technology. This is in contrast with amorphous silicon and oxide transistors, which is dominated by the Far East.

2.2 Detailed and Quantifiable objectives

The progress reported thus far for transistors and diodes is restricted to a single element, not an array. A great deal of research and development must take place between the researchers' demonstration of a stable state change for 1 bit in a laboratory and the production of a large-scale, manufacturable, memory array with acceptable retention, durability, and speed, and integrated read-out electronics. We intend to address all these areas in its project. The ambition of MOMA is to go far beyond the state of the art and to research and develop the difficult materials and process development challenges that will enable flexible circuits with embedded re-programmable memory for next-generation organic circuitry applications.

Table 1: *Summary of state of the art, and advance over the state of the art.*

Main MOMA Goals	**State of the Art**	**Advance over the State of the Art**
Materials and processes	► Ferroelectric materials are not optimized with respect to process. ► Non-patterned PVDF-TrFE) layers	► Different polymer grades of P(VDF-TrFE) will be made with physico-chemical properties tailored specifically towards inkjet printing, photo-imaging and nano-imprinting. ► PVDF-TrFE) patterned with optimized inkjet printing, photo-imaging process.
Development of single bit memory diode array on plastic	► Lab-scale prototypes of ferroelectric transistors and diodes	► Development of a commercially viable 150-mm wafer scale manufacturing process for memory elements on thin plastic substrates with known yield, parameter spread etc. ► Rational diode design based on scientific data. ► imprinted/inkjet printed functional layers
Development of multi bit memory diode array on plastic.	► Only ferroelectric capacitors demonstrated. ► Operational stability not explored.	► 1 kbit array of memory transistors/diodes ► Flexible ► Scaling studies
Demonstration of OTFT circuit with embedded re-programmable memories	► OTFT circuits with ROM or WORM	► Advanced OTFT circuitry ► Integration with re-programmable memories

3. Main S&T results/foregrounds

3.1 Synthesis of ferroelectric polymers with improved performance

The goal was to synthesize tailored ferroelectric P(VDF-TRFE) copolymers resulting in improved performance and formulations for photo-patterning, inkjet printing and nano imprinting. The mode of operation towards these improved materials and formulations is depicted in Figure 2.

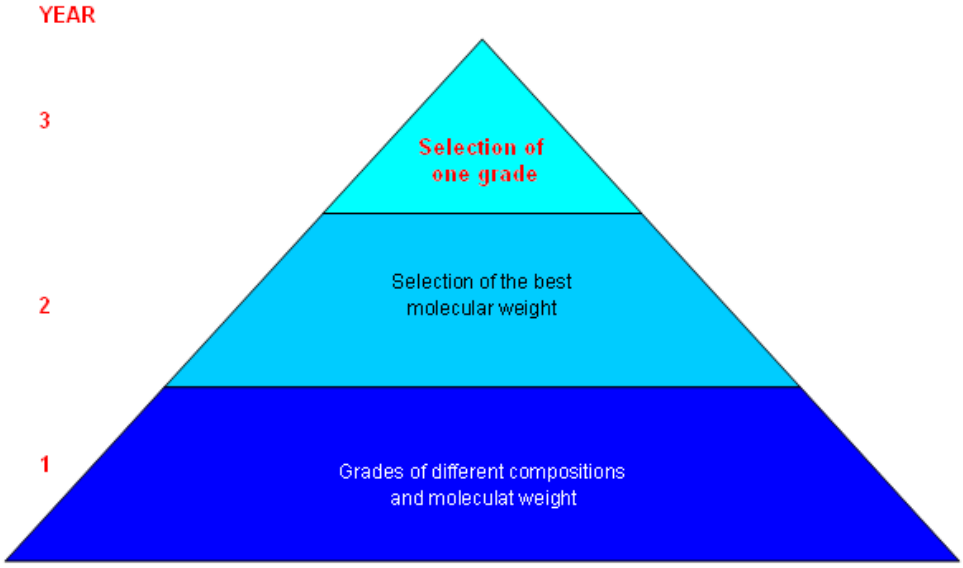


Figure 2: *conceptual graph showing the mode of operation to select final grades of ferroelectric polymers per deposition technique and/or type of ferroelectric memory device.*

During the first year, P(VDF-TrFE) grades of different VDF:TrFE composition and molecular weight were evaluated in terms of performance in ferroelectric transistors and diodes. In the second year, molecular weights and Curie points/melting points were optimized resulting in fine tuning of the formulations for different deposition and/or patterning processes.

P(VDF-TrFE) grade	Deposition/ patterning technique	Memory type	VDF:TrFE composition (% w/w)	Molecular weight (kD)	Curie point (ºC)	Melting point (ºC)
A	Spincoating		77:23	220	128	143
A	Photo patterning		77:23	220	128	143
B	Inkjet printing		77:23	130	128	142
C	Nano imprinting		65:35	290	95	148
A2	Wirebar coating		77:23 65:35	220 380	128 110	143 151
A		FeFETs	77:23	220	128	143
A2		Fe diodes	77:23 65:35	220 380	128 110	143 151

Table 2: *selected grades of P(VDF-TrFE) optimized for use in different deposition/patterning techniques and/or memory type.*

In the final year Solvay did an upscaling of selected grades presented in Table 2. Batches of ~500 g were synthesized to be used in the final MOMA demonstrators.

3.2 Patterning of P(VDF-TrFE) by photo cross linking

A 'negative' photolithography process for patterning P(VDF-TrFE) and its application in ferroelectric capacitors and transistors was evaluated. The lithography is based on photo-crosslinking. A commercial bisazide photoinitiator, 2,6-bis (4-azidebenzylidene)-4-methylcyclohexanone, is used as crosslinking agent. Its chemical structure is shown in Figure 3. The photoinitiator is sensitive to UV light, more specifically to 365 nm (I-line) radiation. Photochemical decomposition of azides leads to formation of singlet nitrenes and, by intersystem crossing, also to triplet nitrenes. Both can react with C–H and C-F bonds, yielding the desired cross-linked network.

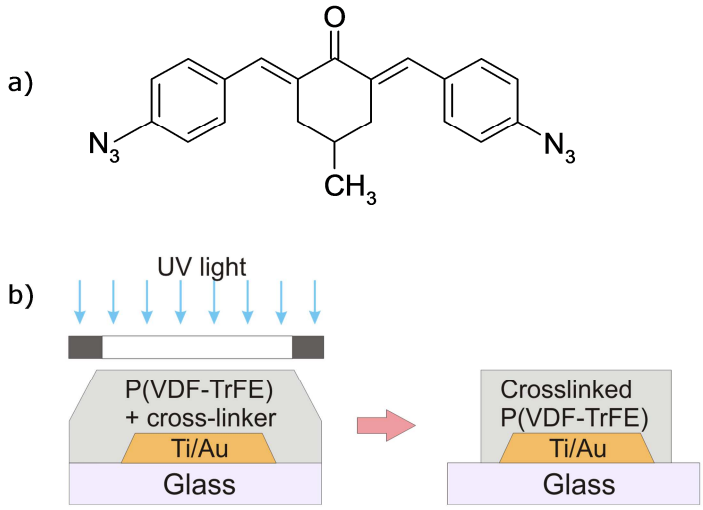


Figure 3: *(a) Chemical structure of the bisazide photocrosslinker (2,6-bis (4-azidebenzylidene)-4-methylcyclohexanone) (b) Schematical representation of the photo-crosslinking process.*

By careful optimization of the photoinitiator concentration, the exposure dose, and the development conditions features down to 1-2 µm lines and spacings could be realized. Figure 4 shows a SEM picture of patterned P(VDF-TrFE) using a P(VDF-TrFE): photoinitiator ratio of 40:1, an exposure dose of 950 mJ/cm^2 and methyl isobutyl ketone as developer.

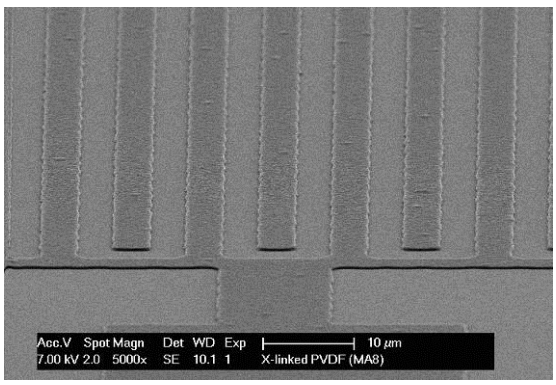


Figure 4: SEM image of patterned P(VDF-TrFE) using the optimized crosslink procedure. Features down to 1-2 µm lines and spacings could be realized.

To investigate the influence of P(VDF-TrFE) patterning on the FeFET performance, the transfer characteristics of a FeFET with crosslinked but non-patterned dielectric layer were compared to

the transfer characteristics of a FeFET with patterned P(VDF-TrFE). For both samples, pentacene and Au top-contact deposition were done in the same run to eliminate run to run variation. The results are summarized in Figure 5. No clear difference could be observed between both devices.

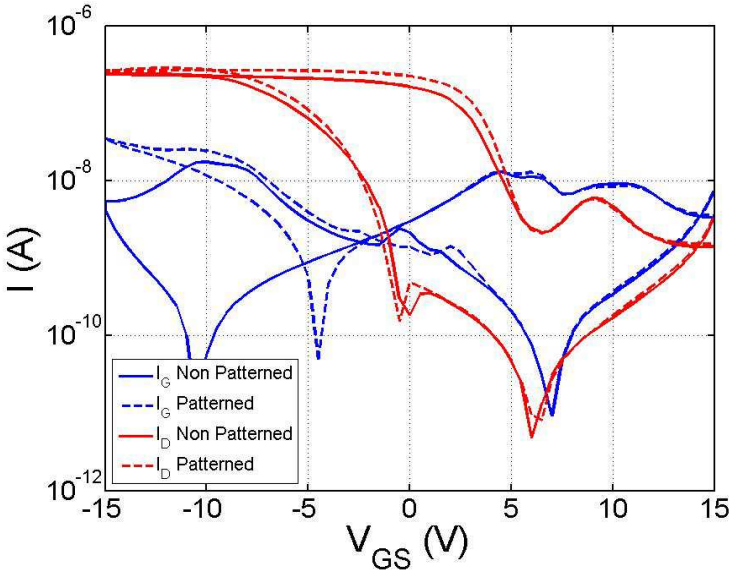


Figure 5: *Transfer characteristics of bottom-gate top-contact pentacene FeFETs. The full lines represent the characteristics of a FeFET with crosslinked but non-patterned P(VDF-TrFE), while the dotted lines correspond to the characteristics of a FeFET with patterned P(VDF-TrFE).*

3.3 Nano imprinting of P(VDF-TrFE)

Nano imprinting was used to control the morphology of P(VDF-TrFE) with the aim to lower the programming voltage in ferroelectric transistors and diodes. A special grade of P(VDF-TrFE) containing carboxylic acid moieties along the polymer backbone was developed to improve the adhesion on (oxidized) metals. The geometry of the imprinting mold and imprinting cases of complete confinement, limiting state, and partial confinement are shown in Figure 6.

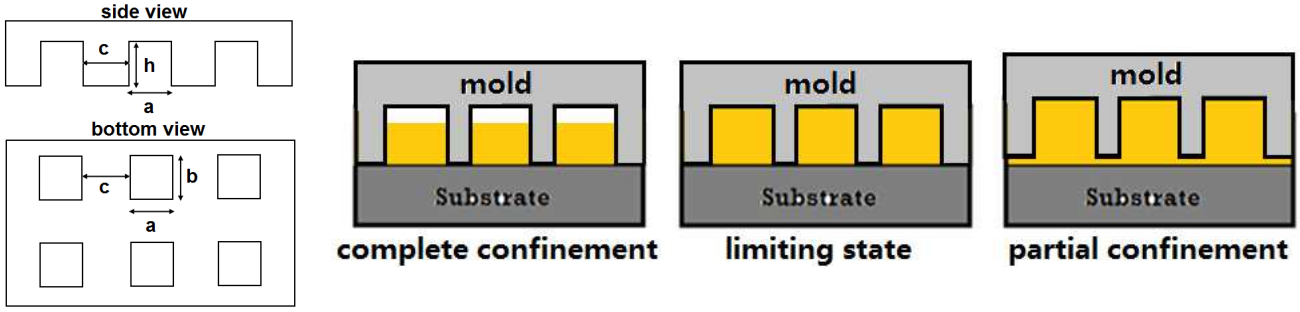


Figure 6: *Left: geometry of the imprinting mold (a=b=h=200 nm, c=80 nm); right:. Sketch of different imprinting cases.*

In theory, given the depth of the cavities of the mold and the areal fraction of cavities, we need to imprint on P(VDF-TrFE) film of 102 nm to reach the limiting state.
To get good imprinting patterns, we have to make sure that the adhesion between P(VDF-TrFE) and the metal (gold or silver) is larger than that between P(VDF-TrFE) and the mold. Clearly, complete confinement or the limiting state of Figure 6 are more demanding with respect to the adhesion of PVDF-TrFE onto the substrate than the case of partial confinement, due to the

differences of surface of contact between polymer and substrate. The adhesion was tested both for complete confinement and partial confinement. The morphology of all the imprinting samples is checked by AFM in tapping mode (Figure 7).
Because the surface of silver is oxidized, a stronger adhesion with the modified PVDF-TrFE grade is to be expected. The imprinting result of P(VDF-TrFE) on silver is shown in Figure 5. There is only 1 defect out of 225 nano dots (0.4% defects) in the case of partial confinement, and 11 defects (5% defects) in the case of complete confinement (Table 3). Although the number of defects of complete confinement is still larger than that of partial confinement, the overall adhesion of P(VDF-TrFE) on silver is clearly much better than that on bare gold, or gold modified with 11-mercaptoundecanoic acid. Moreover, the chemically-modified P(VDF-TrFE) has clearly a better adhesion on silver (5% defects) than the standard grade of P(VDF-TrFE) (18% defects) in case of complete confinement. confirming the interest of the chemical modification. This shows that the modified P(VDF-TrFE) imprint grade is excellent for improving adhesion on metals that bear a native layer of oxide.

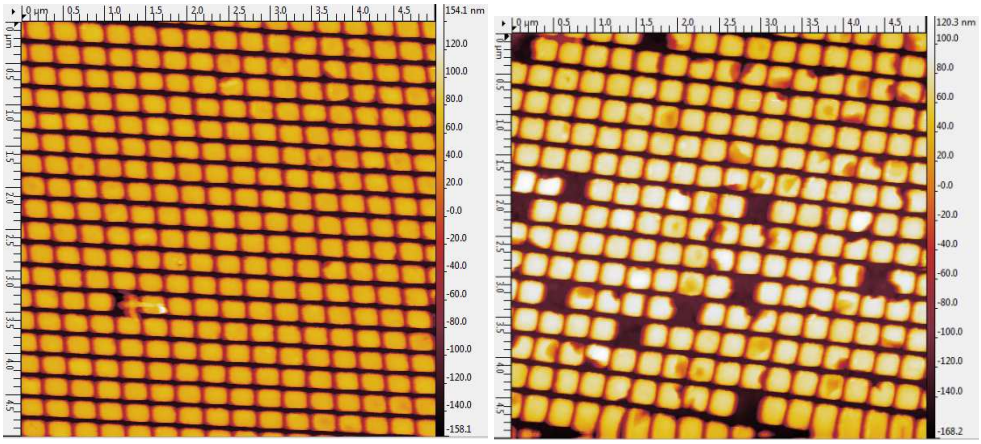


Figure 7: *AFM topographic images (tapping mode) of, Left: a sample imprinted in partial confinement on Silver (layer thickness: 120 nm before imprinting); Right: a sample imprinted in complete confinement on Silver (layer thickness: 100 nm before imprinting).*

substrate	**% defects partial confinement (imprint grade, standard grade)**	**% defects complete confinement (imprint grade, standard grade)**
Au	16 %, 15 %	45 %, 47 %
Au + 11-mercapto undecanoic acid	32 %	35 %
Silver	0.4 %, 0.4 %	5 %, 18 %

Table 3: *overview of defect densities for imprinting with partial and complete confinement. Different substrates and P(VDF-TrFE) grades were evaluated.*

3.4 High yield processes to make re-programmable, non-volatile elements

Processing of ferroelectric transistors

The electrical schematic of the arrays is shown in Figure 8a, and a picture of a finished flexible array is shown in Figure 8b. The cross-sectional view of the top-gate ferroelectric transistor is shown in Figure 8c.

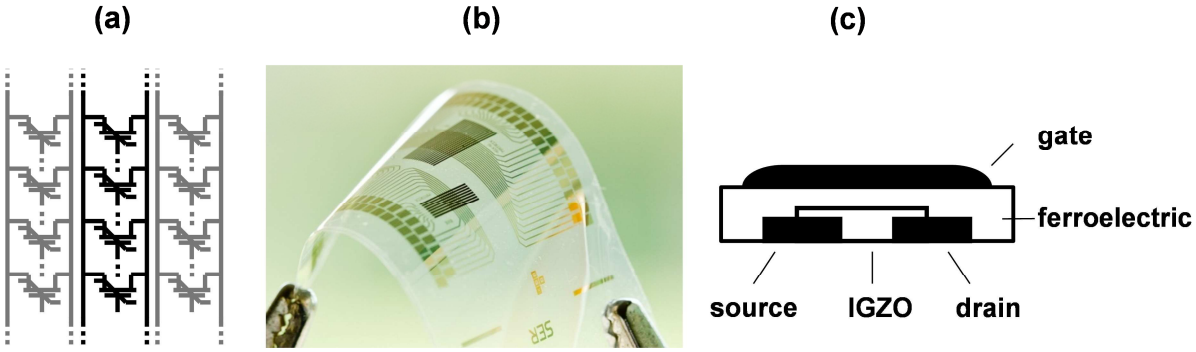


Figure 8: *(a) Schematic of the memory array. (b) Micrograph of a flexible array. (c) Cross section of the ferroelectric transistor, and the materials used in its implementation.*

Arrays of different sizes are processed on 6 inch, 25 µm thin plastic substrates. A top-gate geometry is used for the FeFETs. Processing starts with the source-drain electrodes and column lines that are obtained by deposition of a gold layer (30 nm) followed by structuring. Next, a 20 nm thick amorphous oxide semiconductor, indium-gallium-zinc oxide, IGZO, is deposited using rf sputtering at room temperature and subsequently annealed at 150ºC. IGZO as well as related n-type metal oxide semiconductors have also been used successfully in combination with P(VDF-TrFE) by several groups to make top gate FeFETs. The IGZO layer is patterned using conventional photolithography and wet etching techniques. Then, a 190 nm thick film of poly(vinylidene fluoride-trifluoroethylene), P(VDF-TrFE), grade 209-16, with 77 mol% VDF was spincoated from a 5 wt.% cyclopentanone solution.

In Figure 9a drain current, I_D, is plotted as a function of the gate voltage, V_G. Channel length and width were 5 µm and 80 µm respectively. The anti-clockwise hysteresis in the drain current is the result of ferroelectric polarization switching of the gate dielectric and its influence on the channel conductance. This hysteresis defines the two states of the bistable memory. The maximum ON/OFF ratio, I_{ON}/I_{OFF} is $>10^5$ at $V_G = \sim -2V$, among the highest reported for P(VDF-TrFE) memory transistors. The arrays can be bent to a radius below 2 cm repeatedly without apparent degradation.
A high I_{ON}/I_{OFF} is desired for unambiguous read-out of the memory states. The ON/OFF current ratio remains higher than 1000 after 10^6 seconds (*i.e.*, 12 days), (Figure 9b). This represents a major improvement compared to previously reported values of minutes to hours for P(VDF-TrFE)/oxide semiconductor FeFETs. In Figure 2c the low conductance OFF state and high conductance ON state are continuously monitored by measuring I_D at a fixed V_{SD} and V_G, while the FeFET is switched between ON and OFF states by a V_G pulse of +/-20 V. The FeFETs show reversible switching over many cycles between the ON and OFF states, with the I_{ON}/I_{OFF} ratio of nearly 10^5 (*i.e.*, from 1 µA to 10 pA) being maintained for at least 1,000 cycles. At the highest applied bias, V_G = |22.5| V, the ferroelectric switching occurs faster than 1 µs (Figure 9d). At lower V_G values, the switching speed decreases strongly. Although these switching times are substantially shorter than the previously reported values for oxide-semiconductor P(VDF-TrFE)-based FeFETs of about 1s, they are still considerably longer than those obtained for P(VDF-TrFE) capacitors.
During programming of the cells in the array, we apply half the programming voltage (+10V) on the gate (row) electrode and another half with opposite polarity (-10V) on the source and drain (column) electrodes whilst keeping all other electrodes grounded. The selected cell is programmed to the desired state with this procedure because it experiences an effective programming voltage of |20|V. Meanwhile, the unselected memory cells are subjected to only one-half of the programming voltage. Under such conditions, the ferroelectric may exhibit a finite probability of switching their polarization state. This may lead to data corruption, in particular for larger size arrays.

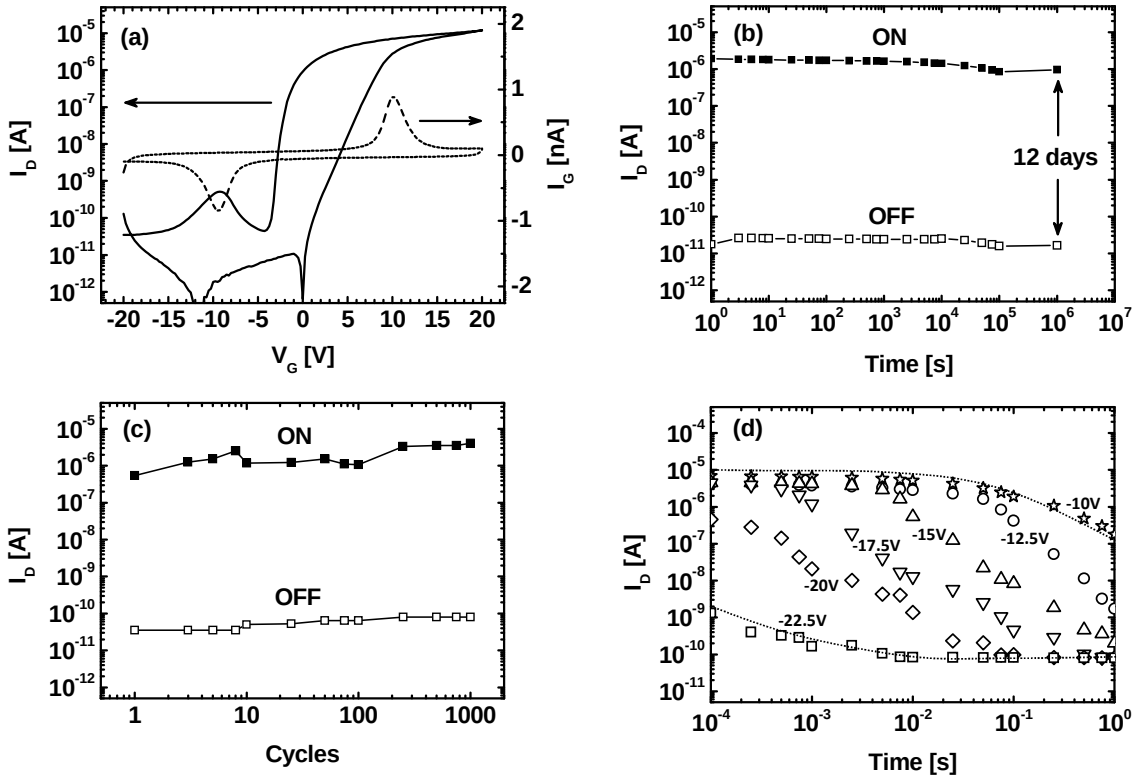


Figure 9: *Electrical characteristics. (a) J-V characteristics. Solid line: drain current. Dotted line: gate current (b) Data retention as a function of time after programming at a gate bias of -3V. (c) Endurance data for 1000 consecutive program-erase cycles, readout at 0.1V. (d) The ON to OFF transition is measured for different negative gate pulses after the FeFET was first set to the on-state by a set pulse of 25 V for 100 ms. The voltage of the program pulse is indicated, and ranged from -22.5V to -10V. Channel length and width were 5 µm and 80 µm respectively.*

Similarly, during "read" operation when the memory is read to determine the state (logic 0 or 1), memory cell disturb can also occur and is called read disturb. It is therefore important to know how stable the transistors are towards repetitive disturb pulses. Figure 10 shows the evolution of the on- and off-state of a discrete FeFET after repetitive application of ±10V pulses of 100 ms.

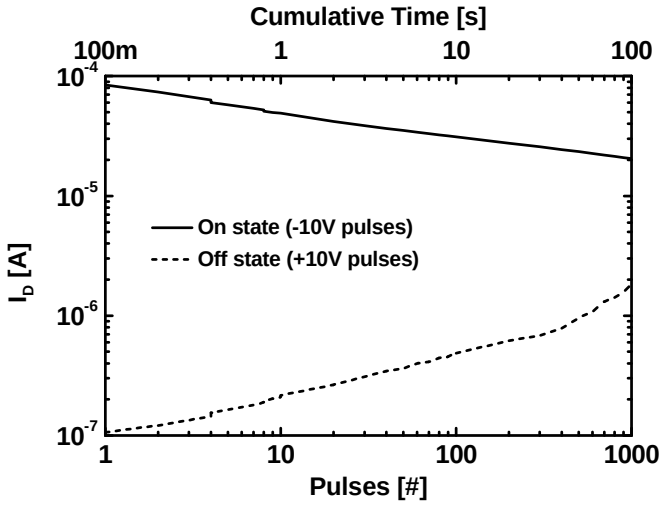


Figure 10: *Disturb measurements - Drain current (I_D) after application of gate pulses of 100 ms at +/-10V. Channel length and width were 5 µm and 80 µm respectively and the drain bias was held at 0.1V for readout operations only.*

There is a small and steady decrease of the channel current with increasing number of -10V disturb pulses. After 100 disturb pulses, corresponding to an accumulated stress time of 10 s the

current has dropped a factor of 2.6. After 1,000 disturb pulses (accumulated stress time of 100 s) the current drop by a factor of 4.2. For positive disturb pulses we see a similar trend in channel current in the opposite direction. These results can be used to optimize the array addressing scheme further.

These individual FeFET devices were integrated into arrays of different sizes. We first set out to program a 3x3 array using the half-voltage addressing scheme. To program each individual cell, a programming voltage pulse sufficient to fully switch the FeFET is applied, i.e., +/−20 V for 100ms. In order to reduce any effect of the programming pulse on the logic state of the neighboring cells, we applied half the programming voltage (+/−10 V) on the column lines and half of the voltage (−/+10 V) on the row lines. All other lines were grounded. In order to determine whether a transistor is in the ON or OFF state the difference of the current in both states has to be large enough with respect to noise and leakage contributions from unaddressed transistors.

In our addressing scheme the neighboring cells experience a voltage pulse insufficient to change their state, as shown in the aforementioned disturb and speed measurements. During programming all lines are sequentially addressed. After programming, the logic state of each individual cell was read out nondestructively using a similar reading scheme. A small source-drain voltage difference of 0.5V is applied, and all gate lines except one are set to -10V. The selected cell has its gate line held at 0V. As the measurement time elapsed, different columns and gate lines were selected to probe the resistance of all 9 cells.

The 3x3 memory cells are programmed in a checker board pattern (Figure 11a). The measured currents are presented in Figure 11b. The '1' and '0' currents exhibit good uniformity and the low to high conductivity state differ by at least three orders of magnitude across the array. These results demonstrate that the selected transistor can be switched repeatedly (programmed) without affecting (disturbing) the other memories in the column. Because the semiconductor is patterned there is no significant leakage current from one column to another during read-out. The large on-off ratio allows facile and fast read operation using relative simple (external) readout electronics.

Using the same read and program voltages of the 3x3 array, larger arrays of 8x8 and 16x16 cells were tested. The programming and erasing were carried out based only on the input pattern and ignored the existing state of the memory cells. In all cases a single programming/erase pulse was sufficient for each cell. Figure 11c plots the histogram of the currents obtained from the 64 cells in the 8 x 8 array when programmed first to the '0' and then to the '1' state, with intermittent readout. A tight distribution with an average current of $5.9 \cdot 10^{-7}$A and $7.2 \cdot 10^{-9}$A, and a standard deviation of $1.2 \cdot 10^{-6}$A and $2.3 \cdot 10^{-9}$A for the '1' and '0' state, respectively, is measured. When we take a current level of 10^{-7} A as threshold, then each memory element can be programmed and read out without error. The average ON/OFF ratio is smaller than the values obtained for the discrete transistors and 3x3 array. This can have several causes: hard faults ('electrical shorts'), transistor parameter variation and/or array scaling effects. The latter effect is not dominant as we find no significant drift in the measured characteristics during readout, in agreement with our disturb measurements. Instead, we found that the decrease in ON/OFF ratio from ~1000 to ~100 is related to 3 FeFETs with abnormally high OFF current due to parasitic gate leakage. This illustrates that in addition to improving the performance of individual FeFETs and limiting the effect of disturb voltages, achieving consistent characteristics across an array is also important for memory integration. In the 16x16 array seven FeFETs were shorted. This corresponds to a device yield of 97%. This value is to be compared to the 4% yield reported previously. Because these defected devices lead to complete lines and columns malfunctioning, only 170 FeFETs could be controlled individually by applying row and column voltages. The histograms of these FeFETs are shown in Figure 11d. In this case, the array was programmed in a checkerboard pattern. Both I_{OFF} and I_{ON} values were distributed in a range of approximately one order of magnitude. As for the 8x8 arrays, the I_{OFF} values are higher than in the discrete FeFETs and small 3x3 array, most likely for the same reason. However, the ON and OFF currents were distinctly separated by more than one order of magnitude.

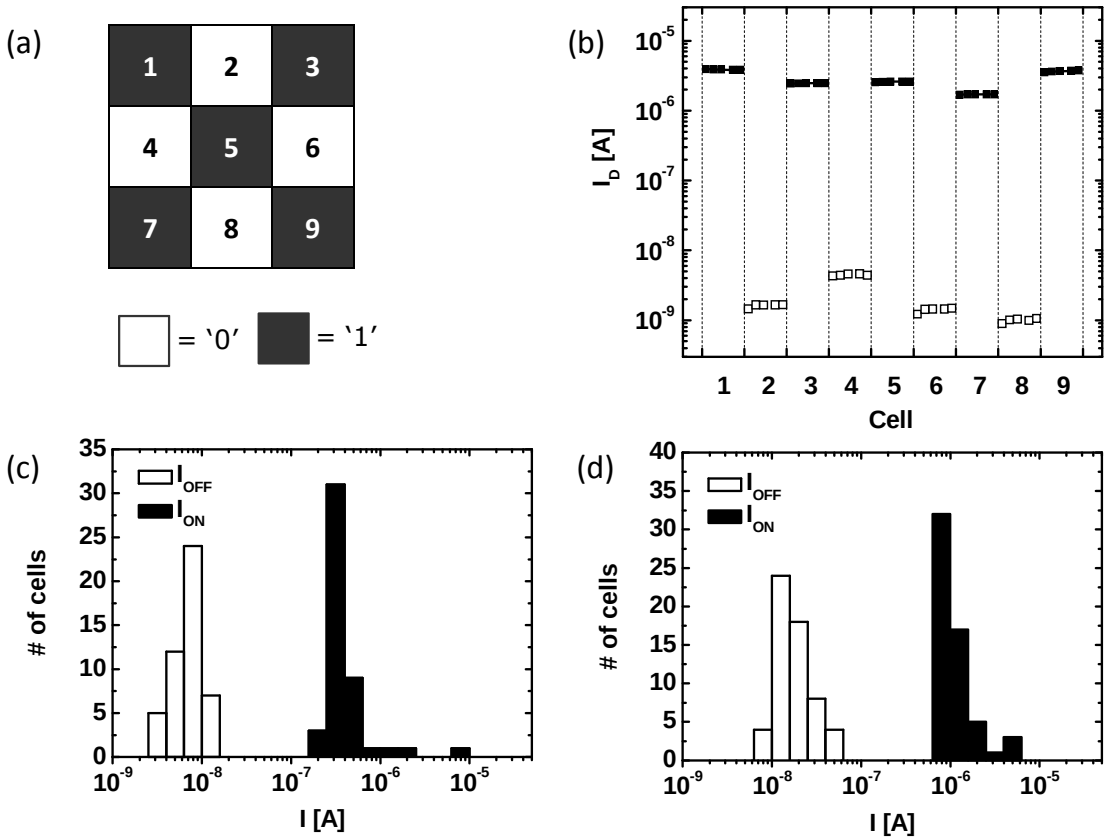


Figure 11: *(a) Numbering of cells and programmed cell pattern of the 3x3 FeFET array. (b) Read-out of programmed cells of the 3x3 FeFET array. (c) Distributions of log (I_{OFF}), log (I_{ON}) in the 8x8 array with all cells programmed first to the '0' state, and subsequently to the '1' state, (b) Distributions of log (I_{OFF}), log (I_{ON}) in the 16x16 array that was programmed in a checkerboard pattern. Channel length and width were 5 µm and 80 µm respectively.*

Fully organic passive NAND ferroelectric transistor arrays

imec has developed the technology for fabricating lithographically patterned bottom-gate FeFET (ferro-electric field-effect transistors) which was needed to realize embeddable memory arrays as laid out in the final objective of this project. Discrete memory devices using pentacene as the organic semiconductor were fabricated on glass substrates and the memory functionality was demonstrated.

This technology was further optimized and transferred to flexible (foil-on-Si carrier) substrates (see Figure 12(a) for cross-section). Passive NAND memory arrays on flexible substrates have been fabricated and successfully characterized as shown below. Passive FeFET arrays have the potential for the highest memory density and yield as they have a smaller area footprint compared to active arrays. So far only active arrays have been shown in literature, passive arrays have not been shown in literature yet. As a proof-of-concept, only the 1x4 passive NAND array is shown: larger arrays can be constructed with multiple rows of these 1x4 arrays. Read/Write cycles up to 2500 times is demonstrated.

The schematic and optical microscope image of a 1x4 passive NAND array is shown in Figure 12: it consists of 4 FeFETs connected in series. Each of the FeFETs can be individually accessed and measured as shown by the transfer characteristics measurement in Figure 13. The four curves lie on top of each other which indicates a good local uniformity of the device characteristics.

The fabricated 1x4 memory array can be programmed up to 2500 times while maintaining a clear distinction between the binary "0" and "1", as shown in Figure 14. Technically, the memory array can be programmed up to 10000 times without failure if a variable reference level is used.

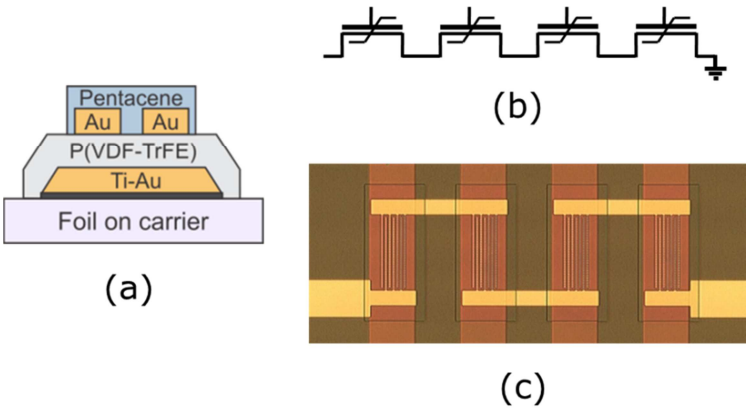


Figure 12: *(a) Cross-section schematic of the bottom-gate bottom-contact pentacene FeFET technology which was developed at imec. (b) Schematic of a 1x4 NAND array: the FeFET devices are connected in series. (c) Optical microscope image of a fabricated 1x4 NAND array.*

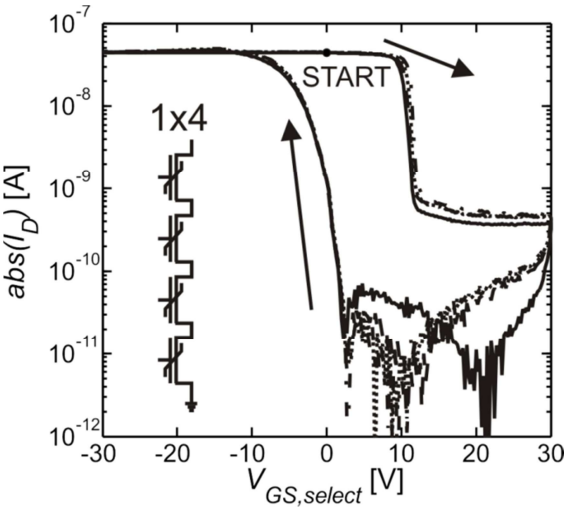


Figure 13*: Transfer characteristics of each FeFET in the 1x4 NAND array. The gate voltage is swept from zero volts and in the direction as indicated by the arrows.*

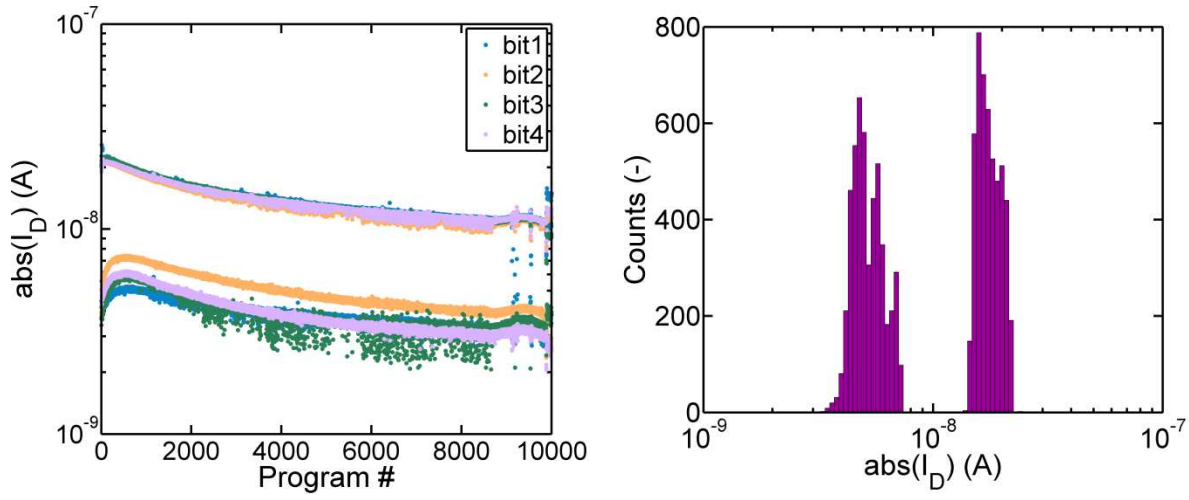


Figure 14: *(Left) Drain current as a function of #ON/OFF programming cycles. (Right) Histogram of the drain current up to 2500 ON/OFF programming cycles. Two distributions representing a binary "0" and "1" are clearly distinguishable.*

Processing of ferroelectric memory diodes

Within the MOMA project we focused on processing blends of the ferroelectric polymer P(VDF-TrFE) with the semiconductors F8BT and PFO. Figure 15a displays a detail of a single Fe diode showing the phase separated blend of the ferroelectric polymer P(VDF-TrFE) and the semiconductor. We have investigated the processing of solution-based binary blends of the ferroelectric random copolymer poly(vinylidene fluoride-trifluoroethylene) P(VDF-TrFE) and the semiconducting polymer poly(9,9-dioctylfluorenyl-2,7-diyl) (PFO), applied by spin-coating and wire-bar coating. By systematic variation of blend composition, solvent, and deposition temperature we show that much smoother blend films can be obtained than reported thus far. At a low PFO:P(VDF-TrFE) ratio the blend film consists of disk-shaped PFO domains embedded in a P(VDF-TrFE) matrix, while an inverted structure is obtained in case the P(VDF-TrFE) is the minority component. The microstructure of the phase separated blend films is self-affine. From this observation and from the domain size distribution we conclude that the phase separation occurs via spinodal decomposition, irrespectively of blend ratio. We explain this by the strong incompatibility of the two polymers expressed by the binary phase diagram, as constructed from thermal analysis data. In order to control the deposition temperature accurately, we selected to produce the P(VDF-TrFE):PFO films by wire-bar coating, rather than by spin-coating. To this end, films were cast at 50 °C. Reassuringly, the roughness decreased drastically upon increasing the deposition temperature (i.e. substrate temperature); in fact improved large area solution processing of ferroelectric diodes on flexible substrates, guided by modeling of polymer-polymer demixing, led to a reduced surface roughness of less than 10 nm (Figure 15d), which relates to device yields close to unity over large area.

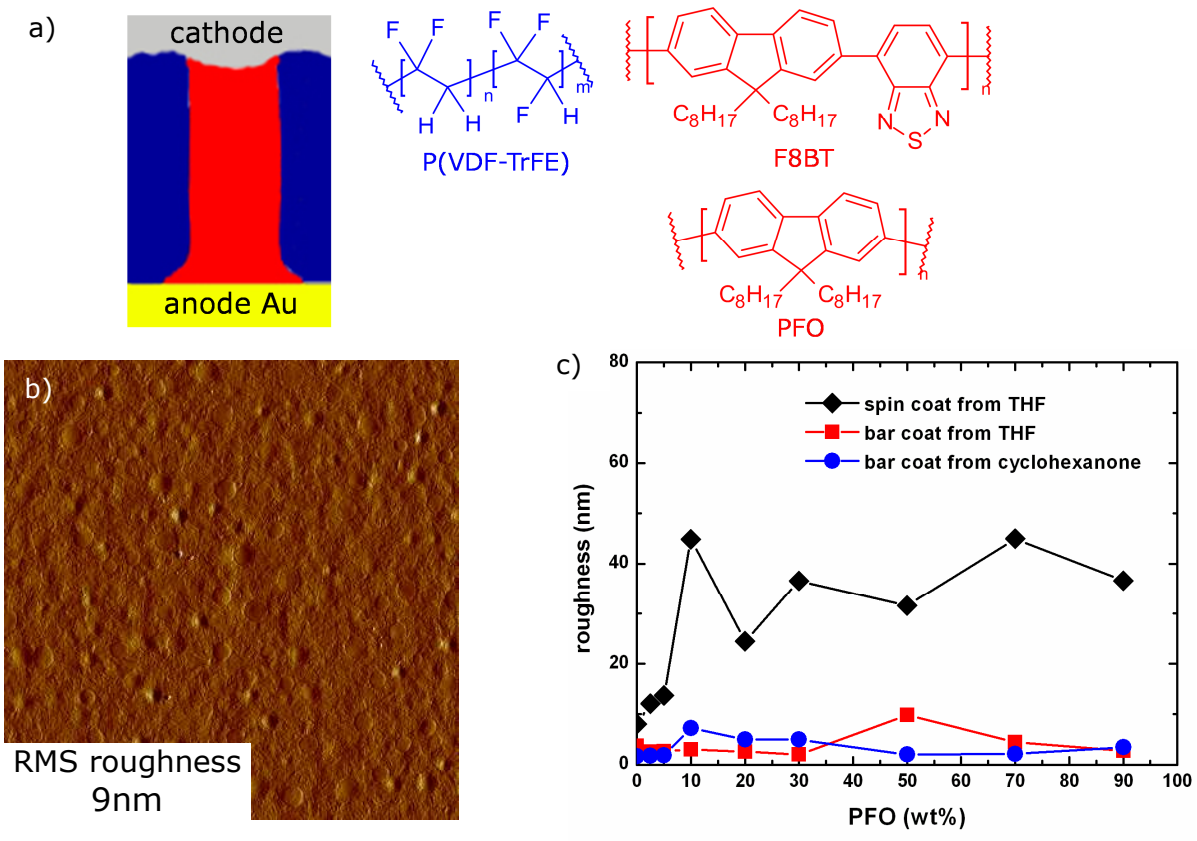


Figure 15: *(a) Detail of a single Fe diode in the memory array showing the phase separated blend of the ferroelectric polymer P(VDF-TrFE) and the semiconductor, (b) AFM image of a wirebar coated phase separated film of P(VDF-TrFE):PFO. Circular featureless PFO domains that are randomly embedded in the P(VDF-TrFE) matrix can be seen, (c) The rms roughness of P(VDF-TrFE):PFO blend films as a function of PFO content.*

In addition to the compatibilization of the two components, the use of higher deposition temperatures, of course, also lead to an enhanced solvent evaporation rate. The system will vitrify at an earlier stage during deposition, which leaves, among other things, less time for solidification. We therefore attempted to disentangle these two effects and tried to elucidate if compatibilization of the two polymers at elevated temperatures or a reduced solidification rate results in smoother film morphologies. For this purpose, we selected cyclohexanone as a solvent, which has a higher boiling temperature (and thus a lower evaporation rate) than THF.
The roughness of the resulting films, produced at 50 °C from cyclohexanone was again smaller than the one observed for films spin-coated from THF. From plotting the roughness of blend films as a function of composition (Figure 15d) the significant improvement in film quality is evident. Blend film roughness's of less than 10 nm are consistently obtained at all compositions, also when this solvent is utilized for film fabrication. Comparable results are obtained using both solvents (cyclohexanone and THF) as long as the blends are cast at elevated temperatures. This indicates that the smoothness of the resulting blend structures originates not from a vitrifying effect due to rapid solvent removal, but because the two polymers are more miscible at these temperatures.

Numerical morphology simulations

Close inspection of the AFM images reveals why selection of deposition temperature and solvent can have such a beneficial effect on the blend microstructure. The overall roughness of the blend films has two contributions: (*i*) internal roughness of the predominantly crystalline P(VDF-TrFE) matrix and, more importantly, (*ii*) the roughness originating from the difference in domain height between P(VDF-TrFE) and PFO. Our coating experiments show that it is this latter contribution which shows the strong dependence on deposition temperature. This is supported by the fact that the film roughness of P(VDF-TrFE):PFO blends was not found to change upon annealing (which leads to the crystallization of the ferroelectric).
To understand how the roughness depends on domain height differences time-resolved level-set numerical simulations of cross-sections of phase separating blend layers according to the protocol recently published by Michels *et al.* were performed. Time snapshots of the simulations are presented by Figure 16(a): low temperature (b): high temperature.

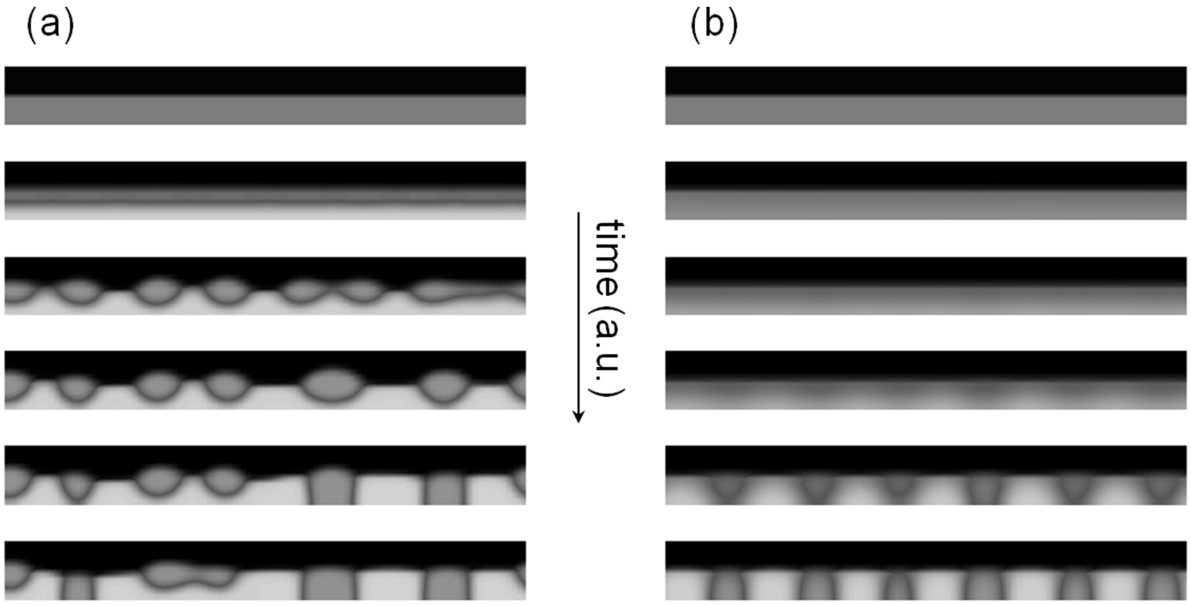


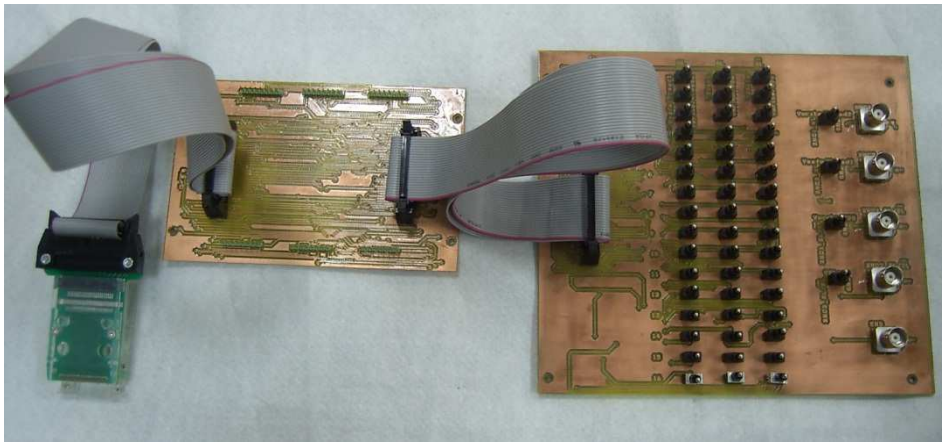
Figure 16: *Evolution of blend topography with time. Simulated cross sections of blend films are presented as a function of time (the time increases from top to bottom): (a) simulation at low temperature and (b) simulation at high temperature.*

The simulation clearly shows two important aspects: (*i*) the weak repulsion between the polymers at high temperature slows down phase separation (assuming the diffusivity of the components not to depend significantly on temperature), and (*ii*) the stratification effect is less pronounced at elevated temperature, leading to a reduction in roughness at any time during de-mixing. The simulations, although representing a simplified version of the physical reality, qualitatively explain the smoothening effect of an increased deposition temperature by a reduction of the polymer-polymer repulsion.

3.5 Infrastructure characterization memory arrays

A ready to use testing system or module to evaluate and characterise ferroelectric memory arrays is not commercially available. Therefore, two measurement set-ups were developed by ST and TNO/imec to measure stand alone memory arrays. The measurement set-up developed by TNO/imec has the advantage of full programmability through the use of the Lab View platform that helps a lot on fast parameters settings via software. The ST set-up (Figure 17a) is oriented to exploit all the advantages offered by the programmability and power of the Keithley SCS4200 and to provide full flexibility on probe signal connections. The two available measearument set-ups furthermore allow a comparison of results in different labs.
The automatic measurement setup, consists of hardware ("FerrOrgan") and Labview based software. This setup is able to control all contact pads of a memory array, which is (for larger) arrays not possible with probes. It allows measurement of FeFET arrays of different sizes (1x4, 4x4, 1x8, 8x8, 8x12 and up to 16x16 bits) as well as Fe diode arrays of different sizes (4x4, 16x16 up to 32x32 bits). A picture of the "FerrOrgan", and a screenshot of (part) of the Labview software is shown in Figure 17b and c respectively.

(a)



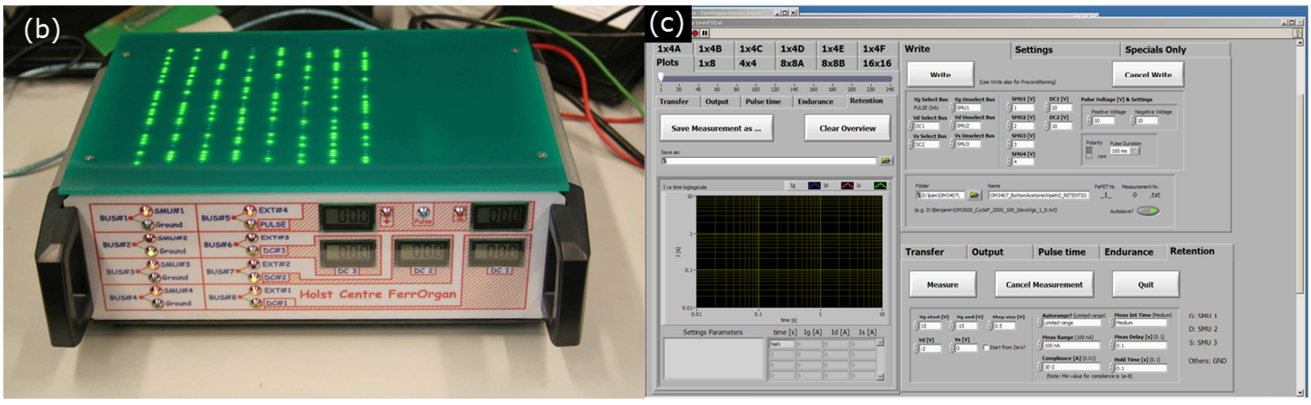


Figure 17: *(a) Bench set-up for memory matrix array testing and characterization, (b) picture of "FerrOrgan" and (c) screenshot of (part of) the Labview software.*

A custom test bench was created to test the embedded memories. It is built around a development board and a microprocessor. Custom PCB boards were designed and fabricated. The first took a single voltage supply input, and output a series of DC voltages to apply to the foil circuitry. Due to the research nature of this project, a design was made in the design phase to allow these voltages to be generated by an external source, rather than fixed with voltage dividers on the foil itself.

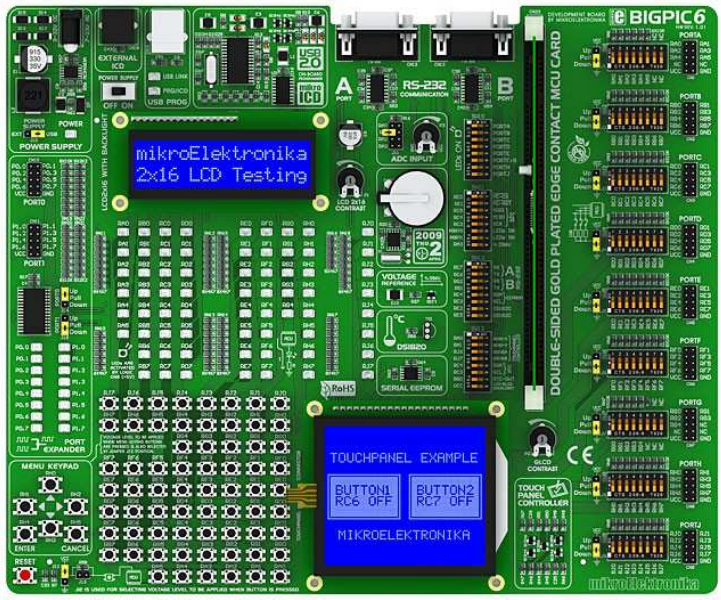


***Figure 18**: BigPic 6 development board used in combination with a PIC18F microprocessor.*

3.6 Operation mechanism and rational design rules for ferroelectric diodes

Figure 18 elucidates the operation mechanism, *i.e.* the lowering of the injection barrier by the ferroelectric polarization and the resulting current injection in the on-state. The top contact is the injecting contact, characterized by a certain hole injection barrier. The current collecting bottom contact is grounded. The electrical transport is calculated by numerically solving the coupled drift-diffusion, Poisson, and current continuity equations on a rectangular grid. The 3D phase separated morphology is therefore mapped onto a simplified 2D structure of alternating ferroelectric and semiconducting slabs, implemented by periodic boundary conditions. The electric current runs only through the semiconducting phase since the ferroelectric P(VDF-TrFE) is an insulator. The schematic in Figure 18a shows the polarization charges in the ferroelectric phase. The electric field lines (blue arrows) run from positive to negative polarization charges. Importantly, near the top contact field lines also run from the positive image charges in the electrode to the negative polarization charges in the ferroelectric. Similar field lines run at the bottom contact. At the injecting top contact, it is this stray field of the positive image charges and the negative polarization charges, shown by the curved arrows, that causes a strong lowering of the hole injection barrier by the image force effect. As a result the contact becomes Ohmic and charges can be injected into the semiconductor phase. Since the lateral x-component of the stray field is directed towards the ferroelectric phase, the injected holes (Figure 18c) are accumulated at the phase boundary and consequently the current, shown by the white arrows, will be confined into a narrow region at the phase boundary (Figure 18b). This spatial confinement causes space charge effects to limit the diode current in the on-state. In the lower half of the semiconductor phase the lateral x-component of the stray field becomes smaller and the current spreads over the whole semiconductor phase before it reaches the collecting contact at $y = 0$.
The result is that at the injecting contact of the diode the injection can be switched between an on-state and an off-state, depending on the direction of the ferroelectric polarization. The current

in the on-state is space-charge limited (SCLC), which is the maximum electrostatically current that the semiconductor can supply. In the off-state of the diode the current is injection limited (ILC).

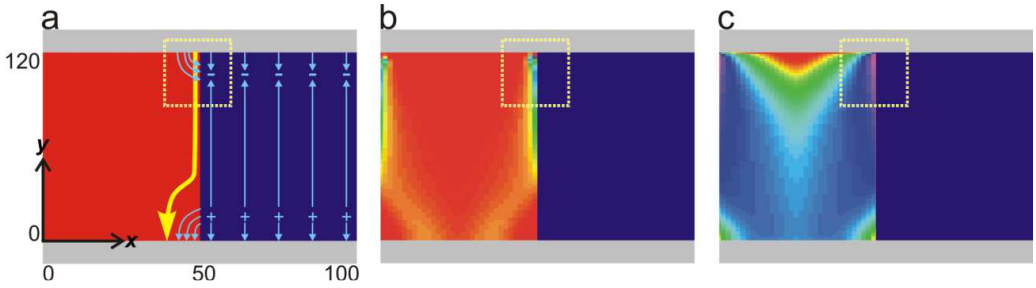


Figure 18: *Operation principle of a bistable ferroelectric diode. a) Schematic mechanism of injection barrier lowering and current injection. The ferroelectric, semiconductor and electrodes are indicated by blue, red and gray planes, respectively. The top electrode at y = 120 nm is the injecting contact characterized by an injection barrier of 0.7 eV. The collecting bottom electrode at y= 0 nm is grounded. Blue and yellow arrows indicate electric fields and current flow, respectively. + and – indicate polarization charges. b) Current density, and c) Hole density (10log-scale) of a ferroelectric diode in the on-state.*

In the ultimate memory the discrete elements are integrated in a cross-bar array, *i.e.* an un-patterned storage medium that is sandwiched between rows and columns of metal electrode lines where each intersection makes up one memory bit. The rows and columns then form the word and bit lines. Using an un-patterned storage medium a cross-bar array is simple to make because it does not require strict alignment. However, for electrically symmetric switching elements application of cross-bar arrays is hampered by cross talk. To eliminate this cross-talk the memory element can be a bistable rectifying diode or a symmetric diode depending on the addressing mode. This automatically leads to the following design rules:

1- To prevent electron trapping, the semiconductor preferably should be *p*-type.
2- One contact should be blocking for holes and certainly not inject electrons.
3- The on-off current ratio in the forward direction should be optimised by choosing the injection barrier. Here again the number of pixels that can be addressed is about the on-off current ratio but now in the forward direction divided by 10. Hence taken the array size the injection barrier is fixed which in turn sets the anode workfunction as the current modulation scales about 1 decade per 0.25 eV barrier.
4- The maximum on current is the space charge limited current. The lay-out of the array sets the optimised on-current. This current is the space charge limited current, and can be tuned to the design by adjusting the mobility.
5- Although not discussed at length, preliminary calculations showed that the minimum diameter of a semiconductor domain is 50 nm. When smaller the current cannot be modulated.
6- For phase separated blends that demix by binodal phase separation, the current modulation is a strong function of domain area and hence of the semiconductor content. For an optimum domain diameter of about 100-300 nm, this yields a semiconductor content of about 10 w%.

3.7 Technical prototypes of 1 kbit ferroelectric memory arrays.

One of the final MOMA demonstrators is a 1 kBit memory diode array. These arrays are based on solution processed phase separated blends of a selected grade of the ferroelectric polymer P(VDF-TrFE) and a semiconductor as described in section 3.2. As semiconductor, both F8BT and PFO were used. Processing was upscaled to 6 inch flexible foils. The lay-out of the Fe diode array chiplet with the 32x32, 1 kBit array and a picture of a finished flexible 32x32, 1 kBit Fe diode array is shown in Figure 19a and b respectively.
Both arrays consisting of rectifying and symmetric diodes were evaluated. A comprehensive characterization including optimized addressing mode, operating voltages, switching speed, retention time and scaling, etc. is presented.

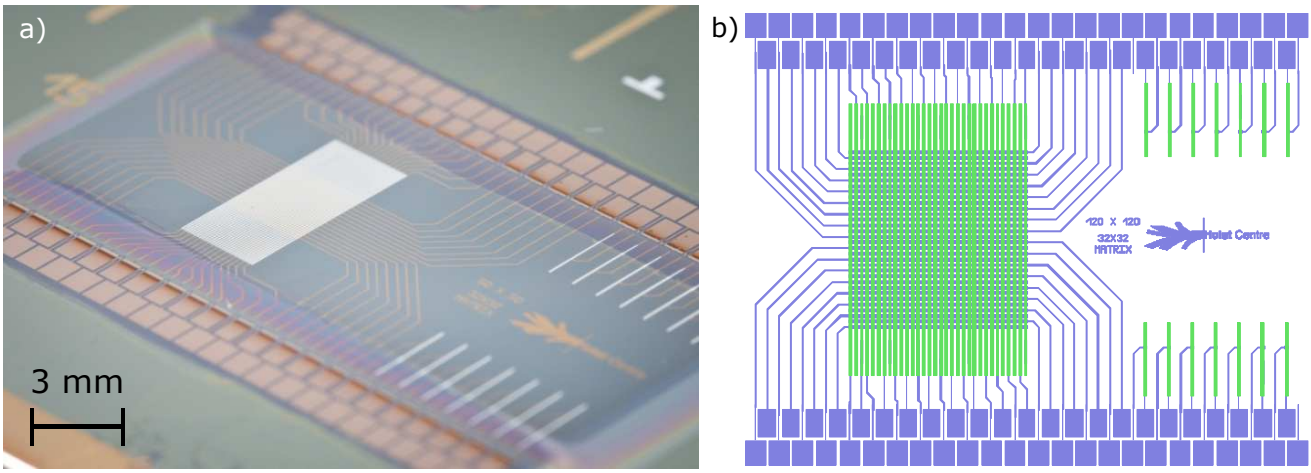
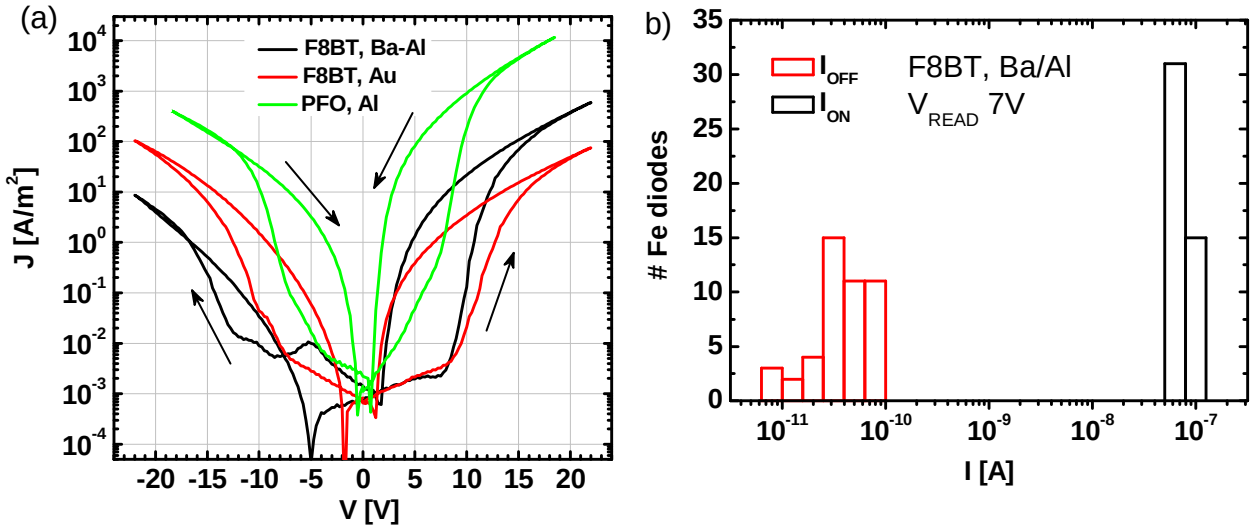


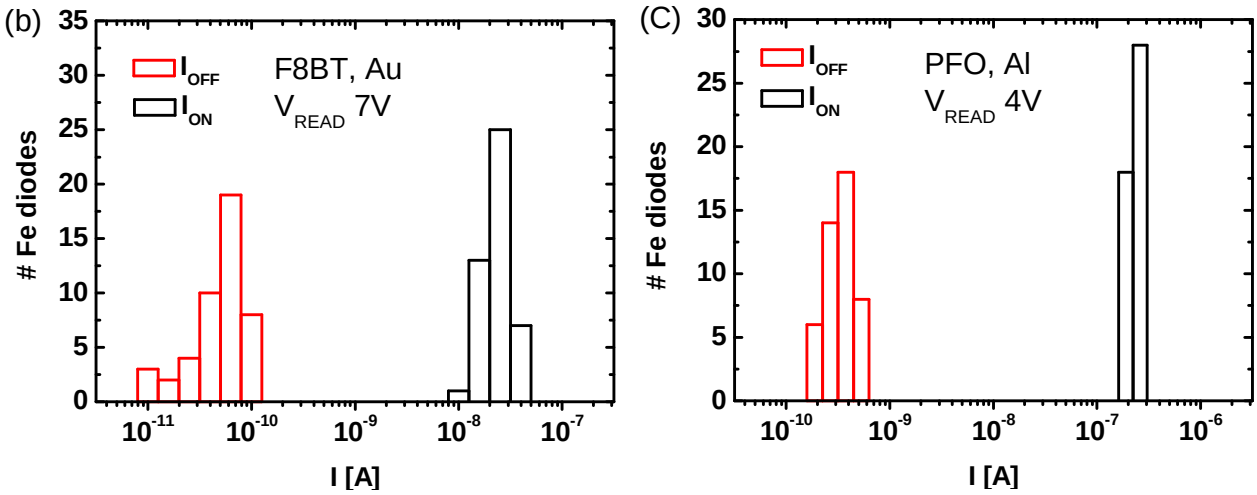
Figure 19: *(a) picture of a finished flexible 32x32, 1 kBit Fe diode array, (b) lay-out Fe diode array chiplet with the 32x32, 1 kBit array.*

Discrete P(VDF-TrFE):F8BT and P(VDF-TrFE):PFO memory diodes.

Current density vs voltage hysteretic sweep of memory switches are shown in Figure 20. Au was used as bottom contact metal. Top electrode was either Au or BaAl for the F8BT blend and Al for the PFO blend. Arrows indicate the voltage-scanning direction. F8BT on gold forms a (hole) injection barrier of ~0.8 eV. BaAl forms an ohmic contact for electron injection and a (hole) injection barrier of ~3.3 eV. When the electric field exceeds the coercive field of P(VDF-TrFE), the injection barrier of Au is modulated and leads to on/off ratio of more than 3 orders of magnitude measured at fields lower than the coercive field. The large hole injection barrier of F8BT/BaAl cannot be overcome and effectively results in a low current at negative voltages compared to Au.

As can be seen in Figure 20d , the yield of the memory diodes is close to unity. Histograms of the ON state resistance and the OFF state resistance distribution from over 40 F8BT based devices for the two top contact metals are displayed in Figure 20b. Current response is read at +7V, after the memories were programmed at +/- 20V. Similarly, results for PFO based diodes are shown where the current response is read at +4V after the memories were programmed at +/- 18.5V





(d)

Fe diode	Yield (%)	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}
F8BT, BaAl	100	7.4E-8 (± 8.8E-9)	4.2E-11 (± 2.1E-11)	1800
F8BT, Au V_{READ} +7V F8BT, Au V_{READ} -7V	95	2.4E-8 (± 6.7E-9) 3.9E-9 (± 8.5E-10)	5.5E-11 (± 2.4E-11) 5.1E-11 (± 2.0E-11)	450 80
PFO, Al	95	5.5E-7 (± 5.7E-8)	3.5E-10 (± 1.1E-10)	1600

Figure 20: *(a) JV curves of memory switches, (b) Histograms of the I_{ON}/I_{OFF} distribution from over 40 F8BT based devices for the two top contact metals. Current response is read at +7V, after the memories were programmed at +/- 20V, (c) Histograms of the I_{ON}/I_{OFF} distribution from over 40 PFO based devices. Current response is read at +4V after the memories were programmed at +/- 18.5V, (d) Yield and current values for different Fe diodes.*

Characterisation of FE diode arrays

Optimization of read/write protocol.
During programming of the cells in the array, we apply half the programming voltage (+/-10V) on the anode (word line) and another half with opposite polarity (+/-10V) on the cathode (bit line) whilst keeping all other electrodes grounded. The selected cell is programmed to the desired state with this procedure because it experiences an effective programming voltage of |20|V. Meanwhile, the unselected memory cells are subjected to only one-half of the programming voltage. After programming, the logic state of each individual bit was read out nondestructively using a different reading scheme. Typically, half the read voltage is applied on the word line and half the voltage applied on the bit line (half-voltage addressing scheme). However, when the read voltage is fully applied over de anode as depicted in Figure 21, we get a higher I_{ON}/I_{OFF} ratio.

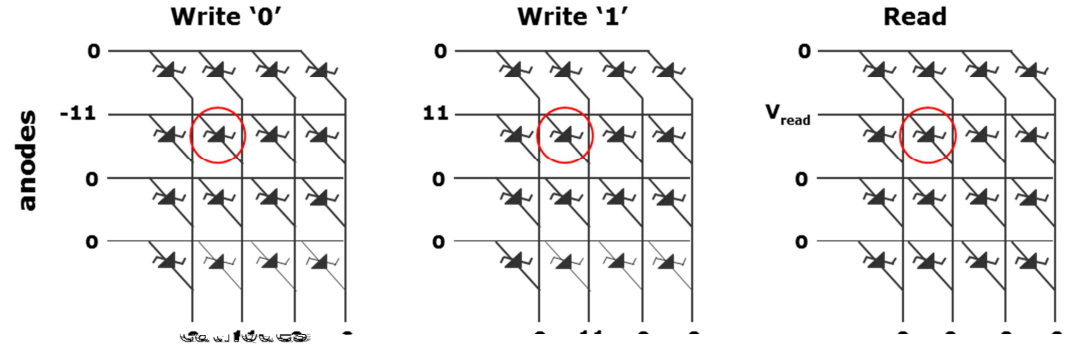


Figure 21: *Addressing scheme used for FE diode arrays.*

In order to further improve the read/write protocol, the influence of the programming pulse width and the read out voltage were investigated. A 4x4 F8BT based Fe diode array with BaAl cathodes was sequentially programmed in the OFF and ON state. Although the I_{ON}/I_{OFF} ratio increases slightly for longer programming pulse widths, a value of 5 ms was used for all subsequent array measurements. Both the OFF and ON currents increase upon increasing read out voltage. An optimum I_{ON}/I_{OFF} of ~500 was found for a V_{READ} of 7V.
Similarly, a checkerboard pattern was programmed into a 4x4 PFO based Fe diode array. In this case the memory diode blend was deposited using the large area compatible wire bar coating resulting in a yield of 100%. The measured currents are presented in Figure 22.

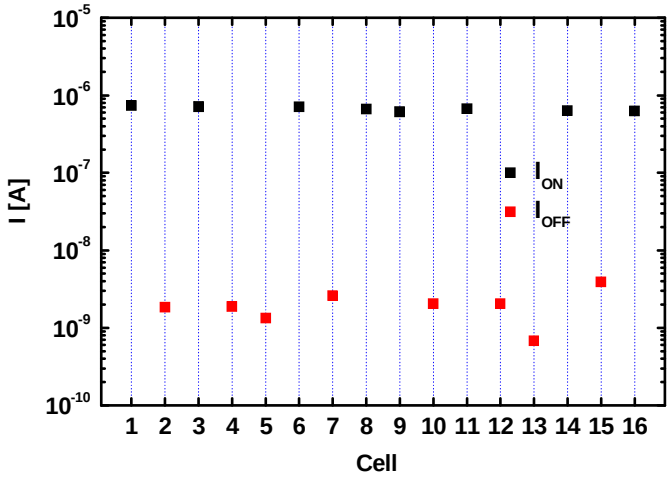


Figure 22: *ON and OFF currents for a wirebar coated 4x4 PFO based Fe diode array with Au anodes and Al cathodes.*
Table 4 shows an overview of the average and standard deviation of ON and OFF currents and I_{ON}/I_{OFF} ratio for different 4x4 Fe diode arrays.

4x4 Fe diode array	**I_{ON} (A)**	**I_{OFF} (A)**	**I_{ON}/I_{OFF}**
F8BT, BaAl	$1 \pm 0.6 \times 10^{-8}$	$3 \pm 0.9 \times 10^{-11}$	500 ± 200
F8BT, Au (V_{READ} 7V)	$6 \pm 1 \times 10^{-9}$	$2 \pm 0.5 \times 10^{-11}$	425 ± 200
F8BT, Au (V_{READ} -7V)	$2 \pm 0.3 \times 10^{-9}$	$9 \pm 5 \times 10^{-12}$	200 ± 75
PFO, Al	$7 \pm 0.4 \times 10^{-7}$	$2 \pm 0.9 \times 10^{-9}$	400 ± 200

Table 4: *overview of extracted parameters for different 4x4 Fe diode arrays.*

Scaling of array size toward 1 kBit for different device areas.
Using the same read and program voltages of the 4x4 array, larger arrays of 16x16 and 32x32 (1 kBit) size were tested. Only the results of the F8BT based 1 kBit arrays are shown here. The arrays were programmed in a checkerboard pattern. Histograms of log (I_{OFF}) and log (I_{ON}) of the 1 kBit arrays (BaAl cathode) with 120x120 µm and 50x50 µm device areas are shown in Figure 23a and b respectively. The ON and OFF currents were distinctly separated by more than two orders of magnitude. Figure 23c shows the read-out of programmed cells of row 16 of the 32x32 crossbar array right after programming (closed squares) and after 6 days (open squares). In both cases the programmed checkerboard pattern can easily be recognized. Both the ON and OFF currents decrease by a factor of 10 over this period.

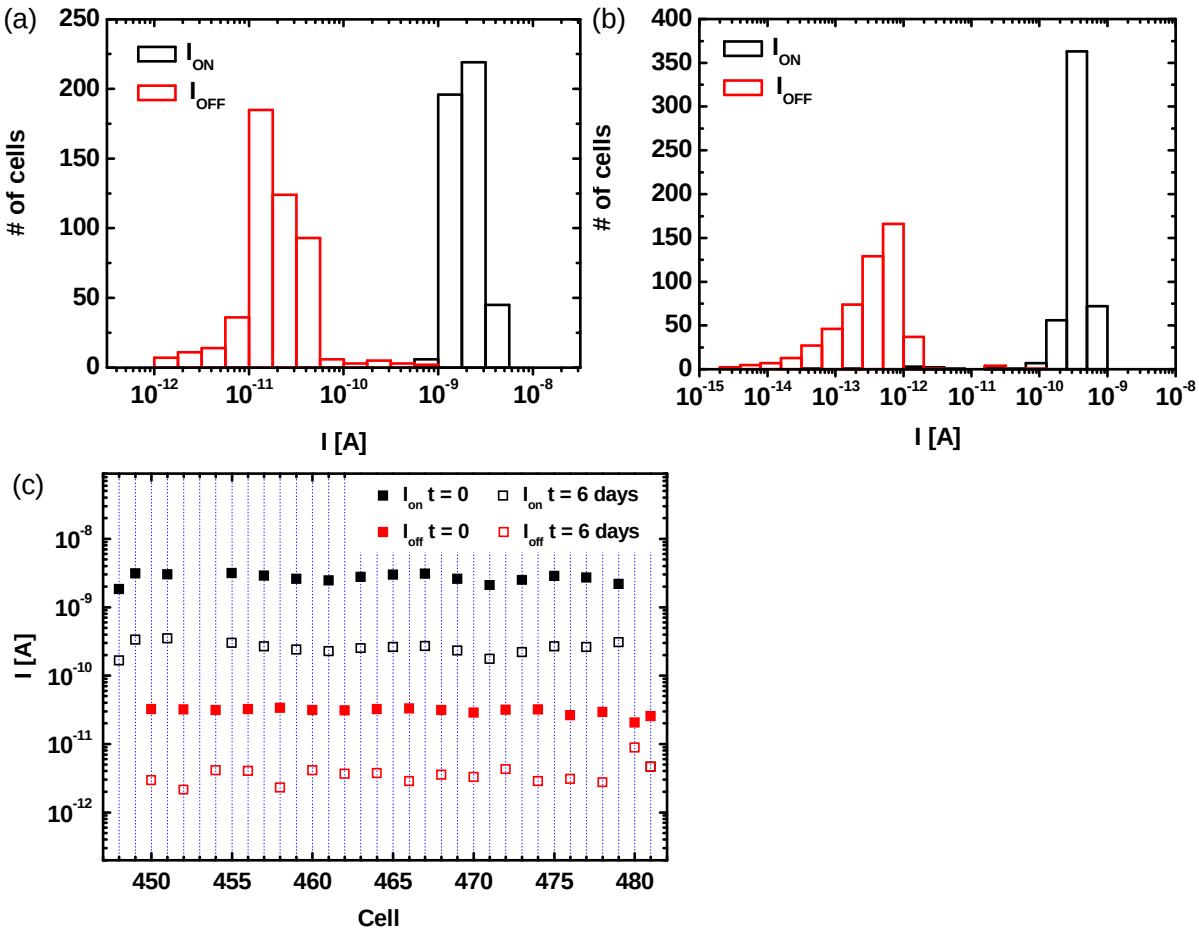


Figure 23: *(a) Distributions of log (I_{OFF}), log (I_{ON}) of the 120x120 µm cells in the 32x32 array with BaAl cathode. (b) Distributions of log (I_{OFF}), log (I_{ON}) of the 50x50 µm cells in the 32x32 array with BaAl cathode. Neighbouring cells were programmed alternatingly to the '0' and the '1' state, the so-called checkerboard pattern, (c) Read-out of programmed cells of row 16 of the 32x32 array (detail of a) right after programming (t = 0, closed squares) and after t = 6 days (open squares).*

The read protocol used above allows the use of symmetric Fe diode arrays, i.e arrays where both electrodes can be switched. Similar results were obtained for a symmetric 1 kBit array with both Au anodes and cathodes. The arrays was again programmed in a checkerboard pattern. Histograms of log (I_{OFF}) and log (I_{ON}) of the 1 kBit array with 50x50 µm device area is shown in Figure 24a. The ON and OFF currents were distinctly separated by two orders of magnitude. Figure 24b shows the correct read-out of programmed cells of row 16 of the 32x32 crossbar array right after programming.

Extracted parameters (I_{ON} and I_{ON}/I_{OFF}) of all tested 1 kBit arrays are summarized in Table 5. Scaling down of device area by a factor ~6 (from 120x120 µm to 50x50 µm) results in a decrease of the average ON current of the same magnitude. Hence array scaling effects are limited for a bit density up to ~100 bits/mm^2 for these 1 kBit memory arrays.

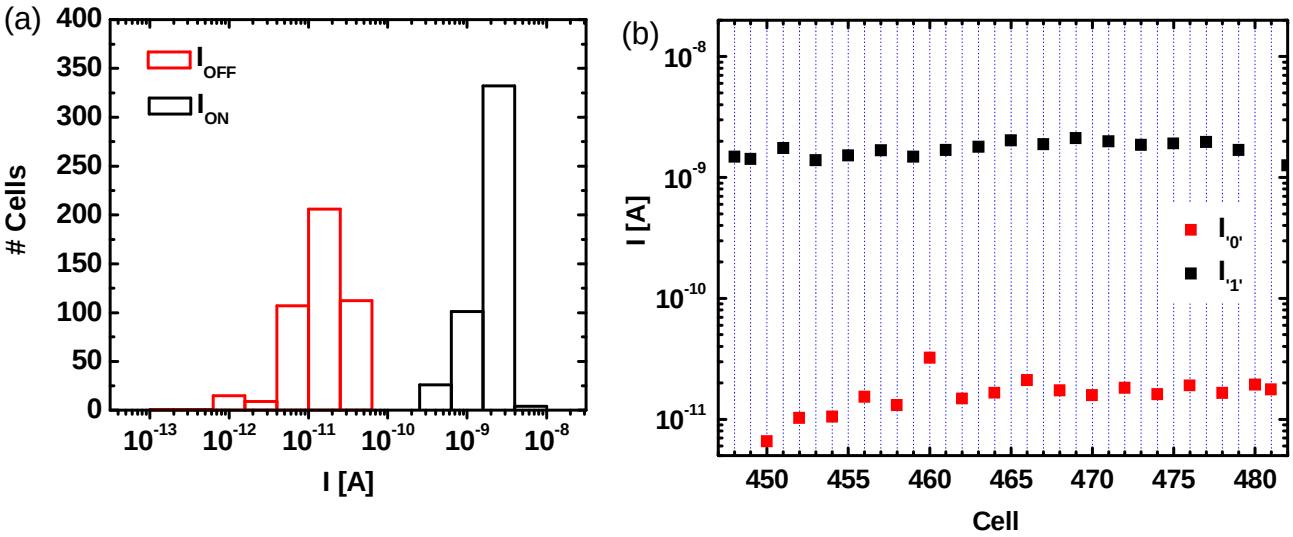


Figure 24: *(a) Distributions of log (I_{OFF}), log (I_{ON}) of the 50x50 µm cells in the 32x32 array with Au cathode. Neighbouring cells were programmed alternatingly to the '0' state and the '1' state, the so-called checkerboard pattern, (c) Read-out of programmed cells of row 16 of the 32x32 crossbar array (detail of a) right after programming.*

1 kBit Fe diode array	Device area	I_{ON} (A)	I_{ON}/I_{OFF}
F8BT, BaAl	120x120 µm (14.4x10^{-9} m^2)	2 ± 0.5 x10^{-9}	575 ± 200
	50x50 µm (2.5x10^{-9} m^2)	4 ± 1 x10^{-10}	625 ± 200
F8BT, Au	50x50 µm (2.5x10^{-9} m^2)	2 ± 0.8 x10^{-10}	100 ± 75

Table 5: *overview of extracted parameters for the 1 kBit Fe diode arrays under investigation.*

3.8 Design and fabrication of low-temperature, high-quality TFT driving circuitry

In order to fabricate the circuits, a combination of materials was chosen in order to be fully compatible with the structure of the memory arrays. This entails the use of a Indium Gallium Zinc Oxide (IGZO) as the semiconductor, in combination with Au contacts and an Al_2O_3 bottom gate dielectric. Discrete devices have mobility of 20 cm^2/Vs. much larger than that of organic semiconductors. As seen in Figure 25, because of this overlap, only two additional process steps are necessary for the realization of a combination of the memories and circuits.

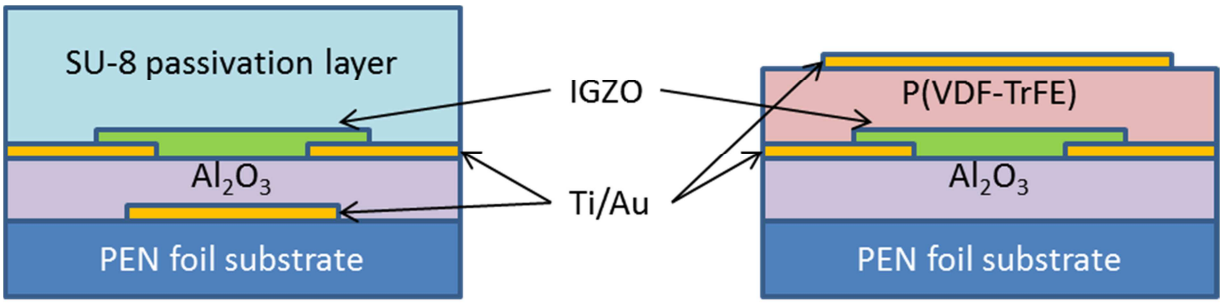


Figure 25*: Device structure of TFTs for circuit operation compared to memory TFTs, showing deliberate similarities.*

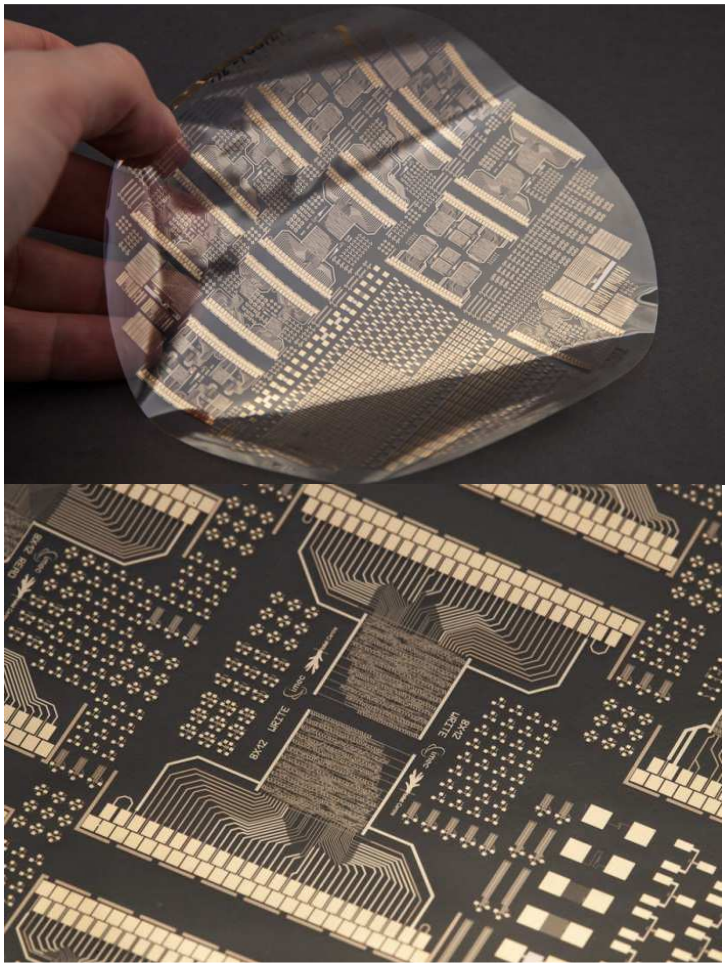


Figure 26*: Top: Flexible circuitry fabricated on a 25um PEN foil. Bottom: Fabricated circuits for read and write operation of 8x12 arrays.*

The choice of a zero-Vgs logic family in which to design the digital circuitry necessitates that these transistors switch 'on' at a voltage below 0V, with circuit operation voltage and performance being affected by this onset voltage. We were able to 'tune' this value through the use of a high temperature anneal step after fabrication. This affects the noise margin of inverters as well as speed of operation. Figure 11 plots read and write signals from a 4x4 circuit array. The proper patterns are displayed, along with the correct timings between column and row applied signals.

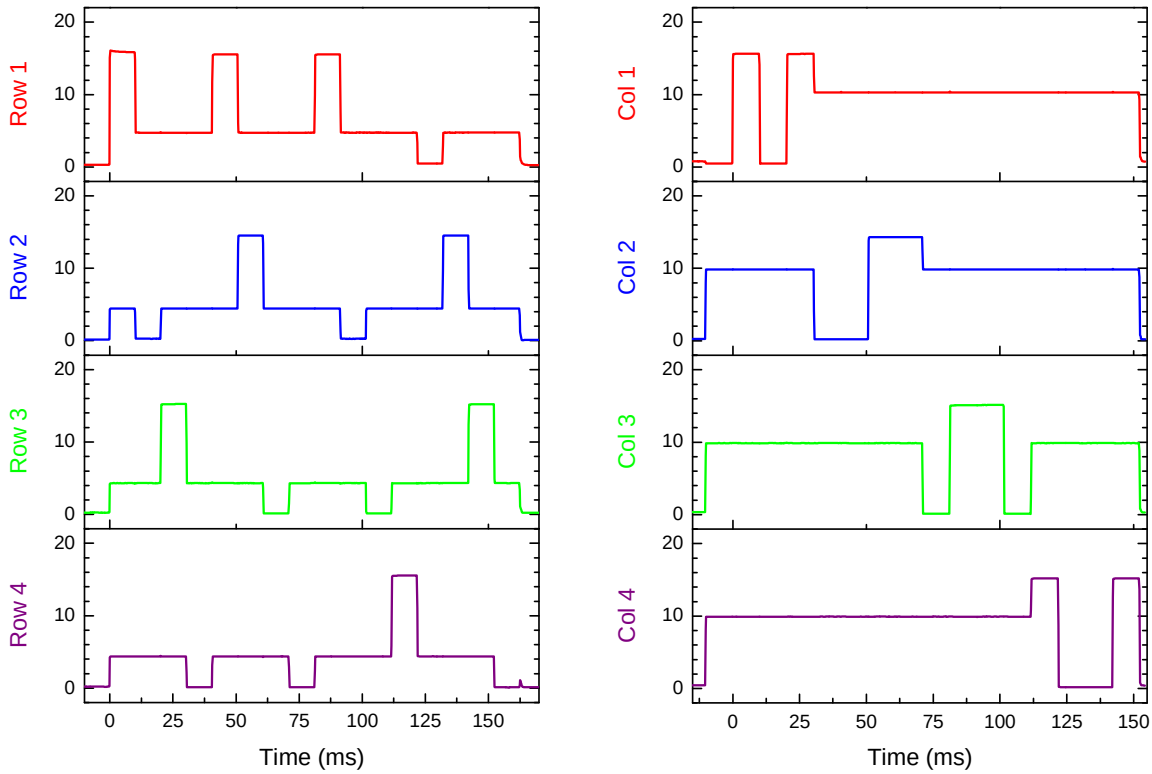


***Figure 27**: Row and column output for two different write patterns.*

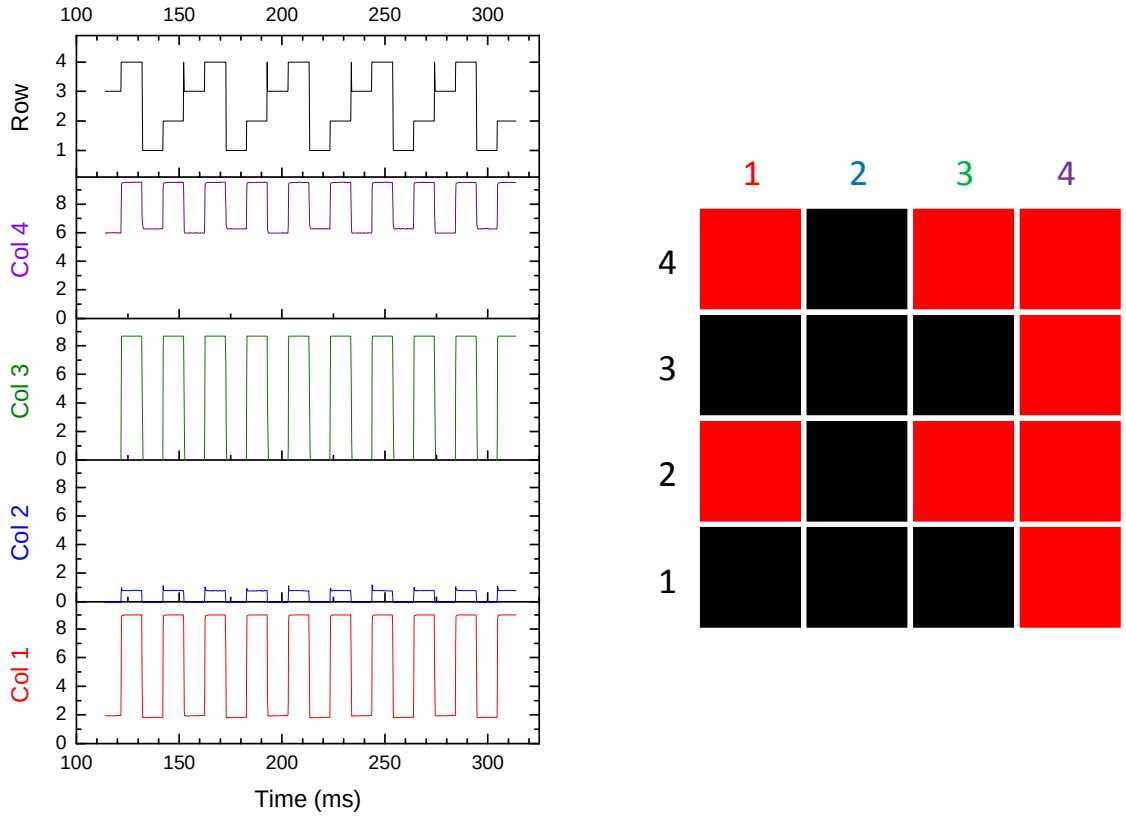


***Figure 28**: Output from a read block connected to a 4x4 memory array with the shown programmed pattern. The top graph demonstrates which row is being measured at a given time.*

4. Potential impact

4.1 Introduction

The developed non-volatile re-programmable memories, within the MOMA project, offer a huge opportunity for ST in providing an integrated memory suitable for mass production that has all the features to perform new products in the field of printed and flexible electronics. In fact, such new frontier of electronics is continuously enjoying growth, as new applications and technologies emerge. Since many years, ST as a global leader in developing and delivering semiconductor is able to manage the whole supply chain referred to flexible and printed electronics, starting from latest research and developments activities through the market analysis for applications, systems and devices to be addressed, as well as manufacturing, fabrication processes, equipment and materials choices. Of course, one of the major challenges for the Integrated Smart Systems using this technology is that components have to be integrated into established or new products and systems. ST has all the capabilities to succeed in this mission that is in line with its strategic plan to maintain and to enforce its market leadership in specific market segment that can take advantage of the undisputed features offered from this technology.

4.2 Market assessment on identified applications

At the start of 2010 IDTechEx ("RFID Forecasts, Players, Opportunities 2011-2021) reported the value of the entire RFID market was $5.63 billion, up from the consolidated $5.03 billion in 2009. The cumulative number of RFID tags sold in 2009 accounted nearly 2 billion for a worth of $2.23 billion. The following table shows the number of tags sold by application in 2009 ranked by average standard price (ASP).

Table 6: *number of tags sold by application in 2009 ranked by average standard price (ASP).*

(source: IDTechEx) **Tag Location**	**Number of tags supplied in 2009 (millions)**	**Value of spend on tags (USD $ millions)**	**ASP ($)**
Pharma/Healthcare	**0.4**	**16**	40.00
Shelf Edge Labels	**0.2**	**5.2**	26.00
Cold retail supply chain	**0.01**	**0.08**	8.00
People (excluding other sectors)	1.3	9.3	7.15
Vehicles	7	29.8	4.26
Passport page/secure documents	65	247	3.80
Postal	2.3	6.3	2.74
Smart cards/payment key fobs	559	1313	2.35
Military	54.5	86.5	1.59
Conveyances/Rollcages/ULD/Totes	28.3	30.3	1.07
Animals	90	90	1.00
Car clickers	48	48	1.00
Other tag applications	200	170	0.85
Other Healthcare	15	11	0.73

Manufacturing parts, tools	70	30	0.43
Archiving (documents/samples)	9	3.1	0.34
Books	85	25.5	0.30
Drugs	10	2.1	0.21
Air baggage	60	12	0.20
Consumer goods	8	1.28	0.16
Smart tickets	325	52	0.16
Retail apparel	130	18	0.14
Retail CPG Pallet/case	200	22	0.11
Total	1,968	2,230	1.13

Not all of the products belonging to the list have "smartness" but it is evident that the two categories, the one related to *Pharma/Healthcare* and the other referred to *Cold retail supply chain,* are on the top of the rank in term of ASP because of the high value offered as system solution. These products have in common as key blocks one or more sensors, a memory and a communication unit. Other product categories show higher volumes but in front of modest standard prices. ST believes there is not much room to compete in these applications. Differently, it is clear how much it could be profitable to take advantage from flexible electronics with a system approach targeting products having higher market value. In this case, benefits offered from flexible electronics together with cost effective process manufacturing and implementation one time they reach similar performances as those offered by conventional electronics will carry to significant volumes even at higher margins. The advantage is not only on behalf of industry but it is dual because, from the user side, many products, being more attractive due to the attainable market price, will pervade the everyday life bringing undisputed benefits in terms of goods quality feedback, effective diagnostic and more in general augmented quality of life.

Just as example we report that data from ABI Research suggest there will be 400 million medical devices in use worldwide with wireless sensors by 2014; by early 2012, Americans will use about 15 million wireless health-monitoring devices (Figure 2). For clinical and remote continuous monitoring, where the most rising opportunities are seen, it is expected a market volume of 48 million units in 2016, showing a 60% CAGR (2011-2016).

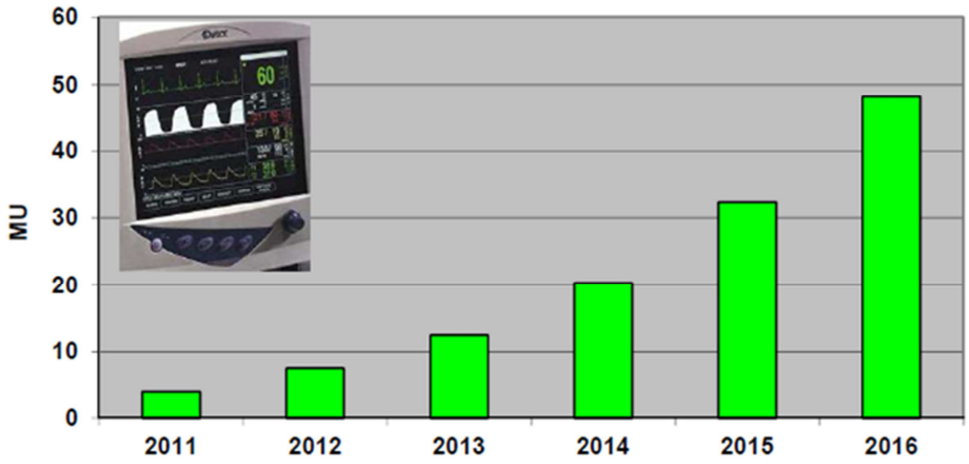


Figure 29: *Wireless clinical and remote continuous monitoring (source: Abi Research 2012).*

According to the same source, potentially disruptive technologies as flexible electronics will play a predominant role in this growth bursting the consumer medical arena in the coming three to five years. Systems in bundle made with flexible electronics will create the ability to shrink devices, create them in a wider range of form factors, and use them for longer-term application such as monitoring patients over months or years.

IMARC Group, one of the world's leading research and advisory firms in its Global Healthcare Cold Chain Logistics Market Report & Forecast (2011-2016) asserts that driven by a strong growth in the sales of temperature sensitive healthcare products, the demand for cold chain logistic services is currently experiencing explosive growth. Just to mention an example, the total size of the healthcare cold chain logistic services market is expected to expand from its current figures of US$ 6.1 billion to nearly US$ 9.5 billion by 2016.

Concerning the third strategic area, Ambient/Building Intelligence, IDC Energy Insights in its Smart Building Maturity Model reports (April 2011) predicts that the global market for smart building systems will grow at a rate of 26.6% a year to reach $10.2 billion in 2015. Interestingly, it predicts the market will grow slightly faster in Western Europe (28.8% per year) than in the US (28.4%).

IDC defines the Smart Buildings' market in six technology verticals:

- Heating, ventilation, and air conditioning (HVAC)
- Lighting
- Plug loads
- Fire & security
- Distributed energy resources
- Analytics & data management

ST application roadmap is tailored on systems that initially present low grades of complexity and at the same time have small dimensions so that it will be possible to implement a preproduction phase using current production assets. Prime target applications are ***Smart Sensor Systems***. These represent high value products. Moreover, ST can take advantage of its expertise on sensors and front-end electronics, made in different technologies including flexible substrates, to combine with organic NVM memories. Later, once the basic products meets the market recognition, manufacturing process reaches its maturity on small area (wafer carrier), system complexity, size and functionality will increase demanding higher production volumes. At a certain point in time a transition from wafer based to larger area (display-like) manufacturing is foreseen. This transition requires significant investment in process development and perhaps investment in large area equipment. Obviously, these industry investments will have to be balanced by a return from initial market results.

4.3 Dissemination

Scientific papers
In total, 11 peer-reviewed scientific papers were published in high ranked journals. An overview is given in Table 7.

NO	Title	Main author	Title of the periodical or the series	Number, date or frequency	Year of publication	Relevant pages	Permanent identifiers (if available)
1	*Crossbar memory array of organic bistable rectifying diodes for nonvolatile data storage.*	*Kamal Asadi*	*APPLIED PHYSICS LETTERS*	*97*	*2010*	*pp. 193308-193308-3*	*http://apl.aip.org/resource/1/applab/v97/i19/p193308_s1*

2	*Polymer and Organic Nonvolatile Memory Devices*	*G. Gelinck*	*Chemistry of Materials*	*23*	*2011*	*pp. 341-358*	*http://pubs.acs.org/doi/pdf/10.1021/cm102006v*
3	*Photocrosslinking of ferroelectric polymers and its application in three-dimensional memory arrays.*	*A.J.J.M. van Breemen*	*APPLIED PHYSICS LETTERS*	*98*	*2011*	*pp. 183302-183302-3*	*http://apl.aip.org/resource/1/applab/v98/i18/p183302_s1*
4	*Multilevel Information Storage in Ferroelectric Polymer Memories.*	*Ashutosh K. Tripathi*	*Advanced Materials*	*23*	*2011*	*pp. 4146-4151*	*http://onlinelibrary.wiley.com/doi/10.1002/adma.201101511/abstract*
5	*Liquid phase demixing in ferroelectric/semiconducting polymer blends: An experimental and theoretical study.*	*Jasper J. Michels*	*Journal of Polymer Science Part B: Polymer Physics*	*49*	*2011*	*pp. 1255-1262*	*http://onlinelibrary.wiley.com/doi/10.1002/polb.22289/abstract*
6	*Organic ferroelectric opto-electronic memories.*	*Kamal Asadi*	*Materials Today*	*14*	*2011*	*pp. 592-599*	*http://www.materialstoday.com/view/22959/organic-ferroelectric-opto-electronic-memories-review-article/*
7	*Processing and low voltage switching of organic ferroelectric phase separated bistable diodes.*	*Mengyuan Li*	*Advanced Functional Materials*	*22*	*2012*	*pp. 2750-2757*	*http://onlinelibrary.wiley.com/doi/10.1002/adfm.201102898/abstract?deniedAccessCustomisedMessage=&userIsAuthenticated=false*
8	*Origin of multiple memory states in organic ferroelectric field-effect transistors*	*B. Kam*	*APPLIED PHYSICS LETTERS*	*101*	*2012*	*033304-033304-5*	*http://apl-oep.aip.org/resource/1/aploep/v5/i7/p153_s1*
9	*Ferroelectric phase diagram of PVDF:PMMA*	*M. Li*	*Macromolecules*	*45*	*2012*	*pp. 7477-7485*	*http://pubs.acs.org/doi/abs/10.1021/ma301460h*
10	*Solution-processed ferroelectric thin films: the forgotten δ-phase of poly(vinylidene-fluoride).*	*Mengyuan Li*	*Nature Materials*	*Accepted for publication*	*2013*		
11	*Ferroelectric transistor memory arrays on flexible foils*	*A.J.J.M. van Breemen*	*Organic Electronics*	*Accepted for publication*	*2013*		

Table 7: *Peer-reviewed scientific publications resulting from the MOMA-project.*

Presentations

In total, 25 presentations were given at prestigious conferences. An overview is given in Table 8.

NO.	Type of activities	Main leader	Title	Date/Period	Place	Type of audience
1	Presentation, workshop		OLAE concertation meeting	June 14/15 2010	Brussels	Scientific Community, Industry, Policy makers
2	Presentation		ISFOE	July 7 2010	Halkidiki	Scientific Community, Industry
3	Presentation		SID Plastic Electronic UK Chapter	Sept 22 2010	London	Scientific Community, Industry
4	Presentation		Plastic Electronic Conference	Oct 21 2010	Dresden	Scientific Community, Industry
5	Presentation		Plastic Electronic Conference	Oct 19 2010	Dresden	Scientific Community, Industry
6	Presentation		Functional Polymer Systems FPS mini-symposium	Oct. 13-14 2010	Noordwijkerhout	Scientific Community, Industry
7	Presentation		MRS Spring 2011	25-29 April 2011	San Francisco	Scientific Community, Industry
8	Presentation		SPIE Photonics West 2011 (invited talk)	Jan 2011	San Fransisco	Scientific Community, Industry
9	Presentation		Flextech Conference (invited talk)	Feb 2011	Phoenix	Scientific Community, Industry
10	Presentation		LOPE-C 2011,	June 2011	Frankfurt	Scientific Community, Industry

11	Presentation		F-n-10	2011	Beijing	Scientific Community, Industry
12	Presentation		ISFOE 11	2011	Thessaloniki	Scientific Community, Industry
13	Presentation		Semicon Europe 2011 (invited talk),	Oct 2011	Dresden	Scientific Community, Industry
14	Presentation		X Brazilian Materials Research Society	September, 2011	Brazil	Scientific Community, Industry
15	Presentation		2011 MRS Spring Meeting & Exhibit	April 24-28, 2011	San Francisco	Scientific Community, Industry
16	Presentation		MRS Fall 2011 (invited talk)	Dec. 2011	Boston	Scientific Community, Industry
17	Presentation		5th Solvay-COPE symposium	2011	Atlanta	
18	Presentation		TCM Crete	22-25 Oct 2012	Crete	Scientific Community, Industry
19	Presentation		IC FPE	05 Sept 2012	Tokyo	Scientific Community, Industry
20	Presentation		MRS spring 2012	9-13 april 2012	San Francisco	Scientific Community, Industry
21	Presentation		MRS spring 2012	9-13 april 2012	San Francisco	Scientific Community, Industry
22	Presentation		MRS spring 2012	9-13 april 2012	San Francisco	Scientific Community, Industry
23	Presentation		4th International Conference on Smart Materials, Structures and Systems	June 10-14, 2012	Montecatini Terme	Scientific Community, Industry
24	Presentation		4th International Conference on Smart Materials, Structures and Systems	June 10-14, 2012	Montecatini Terme	Scientific Community, Industry
25	Presentation		Ph.D student's day, Université catholique de Louvain,	June 1, 2012	Louvain la Neuve, Belgium,	Scientific Community

Table 8: *Conference presentations resulting from the MOMA-project.*

Press release

A press release was launched on December 18, 2012 on behalf of the MOMA project. The complete text is depicted below:

European consortium creates largest flexible memory arrays to date

EINDHOVEN – 18 December 2012 - The EU-funded eMbedded Organic Memory Arrays (MOMA) project has announced the largest re-programmable non-volatile memory arrays yet produced on flexible substrates. Its 256-bit transistor-based and 1-kbit diode-based arrays exhibit state-of-the-art performance in numerous key memory parameters, plus excellent production yields. With the project drawing to a successful close, these latest results provide a starting point for the commercialization of flexible electronics applications with embedded memory.

In recent years, flexible electronics technology has developed rapidly and is now on the verge of commercialization, promising new applications from smart food packaging to wearable health monitors. All these applications require programmable non-volatile memory (similar to the well-known Flash memory), and the more complex the application, the more memory it needs. However, flexible memory development hadn't kept pace with other areas of flexible electronics, limiting market opportunities. So the European Union launched the MOMA project in 2010 to develop low-cost, reprogrammable polymer memories and integrate them with thin-film transistors on flexible plastic substrates.

The MOMA consortium brings together commercial and research partners from across the memory value chain. These partners are chip maker STMicroelectronics, materials supplier Solvay Specialty Polymers, innovation centers imec and Holst Centre plus Catholic University of Louvain and University of Groningen.

The project focuses on ferroelectric memories based on soluble ferroelectric polymers and organic and oxide semiconductors. It has successfully developed new grades of memory materials that can be tailored to specific applications and deposition techniques (including spin-coating, inkjet printing and imprinting). The project partners used these materials to develop memory arrays based on both transistors and diodes, optimizing production processes to deliver high yields and excellent memory performance.

"We're looking to minimize the total cost of the application. The reprogrammable polymer memories currently available require expensive silicon MOSFET technology. It makes no sense reducing cost-per-bit if you then need expensive external silicon components to get it working. Hence we concentrated on ferroelectric memories that are based on resistance rather than charge as these allow for simpler read-out electronics, reducing overall costs" said Albert van Breemen, Senior Researcher at Holst Centre and member of the MOMA project team.

With its 1-kbit (32x32) array, MOMA has delivered the largest flexible memory arrays to date and achieved production yields close to 100%. Furthermore, it has created the thin-film read-out electronics necessary for use in real applications. In the remaining months of the project, the partners will combine all these building blocks into a 96-bit array with the related read/write circuitry, creating a complete embedded flexible memory suitable for applications such as Electronic Product Code (EPC) tags. The project partners are now looking for interested parties to cooperate on further development and commercialization of the technology.

The MOMA project is funded under the European Union's Seventh Framework Programme (FP7). For more details, please visit http://www.moma-project.eu/

--- *end* –

4.4 Exploitation plans per partner

MOMA fits in a larger series of projects that develop technologies which can be considered in a broader horizon, apart from the direct exploitation of the MOMA results. In this respect, MOMA both contributes to, and stimulate, innovation in the field of flexible and printed memory technology.

ST

ST Microelectronics is contributing to lead the Flexible and/or printed electronics to reach a proper grade of maturity to be ready to meet the challenges and requirements of electronics market. This disruptive technology is becoming always more attractive because of its potential in providing operative solutions both to products that can be processed on large area manufacturing processes and products that can be cost effective in order to enable a wide application line-up of disposable electronics. In addition to this features the flexible electronics implies undisputed advantages that make it the perfect candidate for next-generation of electronic products which need being lightweight, bendable, portable, and low-power. These products require all manner of electronic components being assembled, including logics, energy harvesters, photovoltaics, interconnects, antennas and last but not the least memories. The MOMA project has perfectly fulfilled the need to provide embedded re-programmable non-volatile memory arrays that represent a real opportunity for the commercialization of stand-alone products based on flexible electronics.
After years of research, development and market surveys ST has started to catch the first market opportunities for flexible electronics. Initially, these will pass through the design and implementation of sensing platform circuits able to feature products that are serviceable for the medical, healthcare and fitness market segments. In these fields a typical application comes from the possibility to embed thin and flexible smart sensors into diagnostic tools to make them less cumbersome and invasive for the final users.
Afterward, once that this technology will be consolidated across all the value chain it is possible to further lower the production cost. This point remains the market driver in order to make of flexible electronics a vehicle for the pervasive diffusion of electronics and 'intelligence' in everyday

objects. This happening will pave the way to create the forthcoming world of the Internet Of Things. ST goal is to become a protagonist in the described scenario as a leader supplier of devices and solutions taking advantage of this technological revolution. During the past years, the established European partnerships thanks to the participations to MOMA and other funded projects have contributed to strengthen the ST position at worldwide level in the challenging field of flexible electronics and in the meantime it has permitted to build a wide network of relationships on which rely for future developments and achievements of the whole European industry.

SOLVAY SPECIALTY POLYMERS

The Solvay group sees a high potential in the field of printed electronics. Solvay Research and Innovation, at corporate level, has created a Printed Electronics platform in Brussels, focused on new materials for OLEDS and OTFTS. Different building blocks are needed to bring printed electronics to life, memory being one of them. Other building blocks are logic, sensors, displays, battery to name a few. In addition to developing the ferroelectric materials for the memory, SSP collaborates to this platform by developing new materials.

Solvay Specialty Polymers (SSP) is a leading company in high performance polymers, with a portfolio of more than 35 product lines. Amongst its most innovative products are piezo, pyro and ferro electric polymers. SSP has developed a proprietary technology allowing a polymerization process fully scalable at industrial level. With this safe process, Solvay Specialty Polymers is in the right position to supply piezo, pyro and ferro electric polymers to the growing Printed Electronic industry.

A key advantage of SSP polymers for printed electronics is their solubility and printability. In the frame of the MOMA project, SSP has deepen its know-how in developing specific grades tailored for different large area printing techniques that will be used to produce final devices industrially. Ferroelectric polymer formulations have been comprehensively studied in the frame of the MOMA, from preparation and filtration to rheology and viscosity properties, in order to gain a deeper understanding of these complex systems. This know-how in formulation will be usefully leveraged in developing different new applications.

SSP will continue to work with technology developers and integrators to develop new smart devices and to establish the value chain that is needed to deliver printed electronics products to end-users. SSP will also continue to market directly towards potential end-users its piezo, pyro and ferroelectric polymers in various printed electronics applications. Beyond printed memories, opportunities for SSP piezo electric polymers are seen in printed pressure sensor and actuators.

TNO

Being a leading research organization of Europe, TNO aims to further strengthen the research and development activities in Europe by implementing the expertise gained in MOMA in other European projects as well as research and development activities within TNO.

MOMA has delivered the largest flexible memory arrays to date and achieved production yields close to 100%. In addition, these re-programmable non-volatile memory arrays exhibit state-of-the-art performance in numerous key memory parameters. These successful developments puts TNO in a strong position in the area of non-volatile memories, that will be exploited in contacts after the project with existing and new partners.

TNO has already started to extend the low-temperature, high volume compatible processing of ferroelectric polymers to similar fluorinated polymers from Solvay in next generation thin film transistors and circuits. The fundamental building blocks developed during the MOMA project (ferroelectric transistors and diodes) and device knowledge thereof, are currently investigated in other integrated micro-electronics applications like pressure sensors and MEM-OLED displays. A MEM-OLED is an organic light-emitting diode with a built-in ferroelectric switch that can be used as a pixel in a simple passive matrix electronic display. MEM-OLED displays using such a cost-effective driving scheme have great potential for large area applications like signage. The knowledge generated within MOMA gives TNO a head start in these fields and will be further explored with partners within the current consortium, whenever applicable, but also extended to new partners.

IMEC

Within the MOMA project, imec has developed matrixes of organic memory transistors and circuitry on foil to read and write the data of this organic memory foil. This developed knowledge (both in the field of the memory matrixes as in the field of read-out circuitry on foil for memory) enables imec to develop future products and technologies, such as:

- Advanced demonstrators of organic and hybrid RFID tags for product labelling. Current RFID tags on foil (that imec and TNO have reported earlier) comprise hardwired memory. The functionality and the applicability RFID tags on foil will increase substantially when rewritable memory can be included on the TAG. Examples of increased functionality are tags where the unique code can be altered depending on the application, tags where some bits of the generated code can be changed by input from an embedded sensor, tags where some bits of the generated code can be changed to indicate expiration date on the moment the tag is attached to the product or tags where some bits of the generated code can be changed to indicate that a product has been paid for.
- Reprogrammable source code memory for processors on foil. The field of applications for organic microprocessors or other processors that threat sensor signals on foil is currently restricted because the program code for these processors is hardwired. Also here, there are many opportunities for future demonstrators and applications when a dedicated software program can be uploaded on a processor on foil from a future generation of MOMA memory.
- Logging of sensor data from distributed sensor on foil systems. As ambient intelligence is getting increasingly more attention in our modern society, more logging of distributed sensor data will be required. IMEC wants to analyse how the MOMA memories can be used in future applications of sensor logging.

As a consequence, we can conclude that the MOMA results paved the way to include organic memories on foil in various applications in the frame of continue ongoing state-of-the-art research. Each of the new applications will be subsequently proposed to partners and elaborated together with partners towards new valorisation in future products.

RUG

The University of Groningen (22,500 students, 6,000 employees) provides high quality research and education, is internationally oriented, respects differences in ambition and talent, works actively with business, the government and the public, and ranks among the best universities in Europe. The Zernike Institute for Advanced Materials, located at the University of Groningen, focuses on the design and scientific study of materials for functionality. It is one of the six recognized top research schools in The Netherlands The group physics of organic semiconductors at the University of Groningen is one of the leading groups in transport physics of organic devices, e.g. polymer light-emitting diodes, solar cells, and large area molecular junctions. The group is widely recognised for their ground breaking work on organic ferroelectric transistors and organic ferroelectric diodes.

The knowledge gained in MOMA will be used to enhance the profile of the University. The results of MOMA have been and will be disseminated externally via publications in peer-reviewed high-quality journals, and will be presented at international conferences. Due to the access to state-of-art materials, the performance of the devices has been improved. The results obtained will be used to apply for new research projects, both nationally and via the European Union.

The group did hold the basic patents on tunable injection barriers. The patents are now at TNO. The knowledge that we build up in MOMA, improved processing and understanding of the device physics, will be used by the improve the performance of discrete ferroelectric memory elements, and, in this way, can be used to enhance the value.

UCL

As a higher education institution, UCL aims at disseminating knowledge to students and the general public, and at developing research at the forefront of science and technology. The study of some published results from MOMA are currently integrated in the project-based master course 'Macromolecular Nanotechnology' delivered to Engineering students of the materials Science

engineering and of the physical engineering specialties of UCL, thereby promoting the interest of ferroelectric polymers for electronics applications.
In addition, the knowledge gained within MOMA is now being used to study by PFM the imprinting of P(VDF-TrFE) using the samples provided by Solvay Specialty Polymers (PhD of Hailu Kassa), to develop alternative memory transistors (PhD of Ronggang Cai) and to investigate hybrid multiferroic layers (PhD of Yang Li, paid by the China Scholarship Council; new project submitted in coll. with Luc Piraux, a specialist of ferromagnetism). Applications in the field of organic solar cells are also being developed using nanoimprinted P(VDF-TrFE) layers in collaboration with the group of R. Lazzaroni of the University of Mons, within the frame of an interuniversity attraction pole (IAP "Functional Supramolecular Systems"). Interactions with the Holst center and Solvay Specialty Polymers will be continued for some of these projects.
Finally, UCL is finalizing the writing of articles related to the MOMA project. One paper is currently submitted, with another one being currently written.

5. Public website and contact details

A project website (http://www.moma-project.eu) has been set up during the first month of the MOMA project to

- exchange information between partners
- provide information on the progress of the project to the reviewers and the European commission
- provide information on the project to the general public.

The MOMA project is coordinated by Holst Centre/TNO. For more information please contact:

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