

Publishable summary

This project is bound to demonstrate working GaN power transistors with normally-off switching characteristics in a real industrial system environment and to show that these devices can be fabricated on a 6" GaN-on-Si industrial process line. This target requires considerable developments along the whole value added chain from epitaxy to device processing, packaging, device modelling and full in system modelling up to the design of a demonstrator system (3 KW power converters). In this connection the partners are working in close interaction to achieve this goal. The mainstream activities are supported by characterization and lifetime testing activities in order to give a feedback on typical device behaviour and potential stability and/or reliability problems in an early phase of the project. Furthermore, new technological approaches to improve normally-off, breakdown and device leakage behaviour are analysed with the goal to decide on further exploitation of these results in the course of the project.

In order to describe the benefit of GaN transistors embodied in the final demonstrator, a full modelling of both, normally-off and normally-on GaN transistors has been provided. The models are based on extensive characterizations of prototype GaN transistors fabricated and delivered within the project. They are incorporated in a SPICE design environment. By simulating static and switching behaviour, topologies of the power factor correction circuits ideally matched to the properties of GaN transistors could be selected. In fact, it is now possible to predict circuit performance in dependence on specific technological parameters of the GaN transistors (virtual prototyping).

The GaN devices to be delivered for the demonstrator will be mounted in a specific power package characterized by extremely low inductances and parasitic capacitances. Furthermore it will provide a heat sink adopted for the high power density of the devices. The packages are currently developed, characterized and simulated. In order to get chip and packaging technology adjusted to each other, tests have been performed which are taking care of a suitable chip backside and front side metallization to enable die attach and wire bonding.

Improvements of GaN chip technology have been focussed on three main topics, the transfer of p-GaN normally-off transistor technology to epitaxial GaN structures grown on Si wafers, the optimization of epitaxy and processing technology towards normally-off transistors with improved switching capabilities (reduction of dynamic on-state resistance increase) and the development of quasi vertical device architectures. While power transistors delivered for characterization and modelling purposes (100mΩ on-state resistance) have been realized on SiC substrates, the first normally-off devices fabricated on Si substrates have been demonstrated recently. The devices are based on a 2-stage epitaxial approach, forming the intrinsic device epitaxial layers in the first stage followed by a p-GaN overgrowth in the second stage. For improving dynamic switching properties at high bias voltage levels (600V) suitable technological solutions are matter of on-going experimental and theoretical investigations. The vertical device approach considered in this project relies on metallic interconnects between the source or the drain regions of power transistors and the conductive Si substrate.

In terms of epitaxial growth of GaN device layers on Si <111> substrates considerable improvements have been made. On 4" substrates epi structures demonstrated breakdown voltage levels of up to 1200 V. Furthermore, homogeneous GaN device layers on 150 mm Si substrates have been shown. These very promising results are due to an intensive cooperation between epi growers and the manufacturers of the growth machines. In

particular, the homogeneity of the wafers is the result of careful susceptor engineering ensuring a homogeneous temperature distribution across the wafer during epitaxial growth.

GaN power devices require very specific characterization methods in order to understand switching and drift properties and, last but not least, degradation mechanisms. Therefore characterization techniques need to be applied that suitable for a full device understanding such as static and dynamic characterization up to more than 1000V, parasitic capacitance evaluation, pulsed measurement techniques for high voltages and high currents, breakdown characterization, drain current trapping technique, deep level transient spectroscopy and dynamic thermal and e-field mapping. All these techniques are now made available for the consortium. Goal is to identify the physical root cause of drift, lagging and degradation effects and to feed back this knowledge in technological improvements.

Regarding the project's explorative branch, a strong emphasis has been put to the development of MOS type of GaN devices in order to cope with the demands of having extremely low gate leakage current levels. Furthermore, novel normally-off transistors using polarization engineered heterostructures which are creating localized negative charges underneath the gate have been designed and realized practically. These devices demonstrated good normally-off behaviour with threshold voltage levels around 0.3 V.

In conclusion, the project started successfully, all milestones have been met so far, and similarly all deliverables have been handed in in time.