PUBLISHABLE SUMMARY

Grant Agreement number: 287602

Project acronym: HIPOSWITCH

Project title: GaN-based normally-off high power switching transistors for efficient power converters

Funding Scheme: STREP (ICT-2011-7)

Date of latest version of Annex I against which the assessment will be made:

19.08.2011

Periodic report: 1st ☐ 2nd ■ 3rd ☐ 4th ☐

Period covered: from 01.09.2012 to 31.08.2013

Name, title and organisation of the scientific representative of the project's coordinator:

Dr.-Ing. Joachim Würfl
Ferdinand-Braun-Institut
Leibniz-Institut für Höchstfrequenztechnik
Gustav-Kirchhoff-Straße 4
12489 Berlin - Germany

Tel: +49 30 6392 2690

Fax: +49 30 6392 2685

E-mail: joachim.wuerfl@fbh-berlin.de

Project website address: www.hiposwitch.eu

Publishable summary

This project is bound to demonstrate GaN power transistors with normally-off switching characteristics in a real industrial system environment and to show that these devices can be fabricated on a 6" GaN-on-Si industrial process line with the possibility of an extension to 200 mm wafers. This target requires considerable developments along the whole value added chain form epitaxy to device processing, packaging, device modelling and full in system modelling up to the design of a demonstrator system (3 KW power converters). In this connection the partners are working in close interaction to achieve this goal. The mainstream activities are supported by characterization and lifetime testing activities in order to give a feedback on typical device behaviour and potential stability and/or reliability problems in an early phase of the project. Furthermore, new technological approaches to improve normally-off, breakdown and device leakage behaviour are analysed with the goal to decide on further exploitation of these results in the course of the project.

In order to describe the benefit of GaN transistors embodied in the final demonstrator, a full modelling of both, normally-off and normally-on GaN transistors has been provided. The models are based on extensive characterizations of prototype GaN transistors fabricated and delivered within the project. They are incorporated in a SPICE design environment. For the selection of optimum performing circuit topologies different circuit concepts have been simulated in terms of the energy consumption of different circuit building blocks. Outcome of this work is an optimum circuit topology being perfectly matched to the requirements and the properties of the GaN power switching devices developed in HiPoSwitch. In fact, due to the combination of device models obtained from physical device simulation and the simulation tools for circuit design, it is now possible to predict circuit performance in dependence on specific technological parameters of the GaN transistors (virtual prototyping).

GaN devices considered for demonstrator implementation are mounted in a specific power package characterized by extremely low parasitic inductances and capacitances along with the possibility of suitable heat sinking. Optimum packages have been identified, characterized and simulated. In parallel to the package implementation and characterization both, the topology of the GaN chips and the interfacing metallic layers on the chip front side and on the backside and last but not least the thickness of the chips had to be adjusted properly.

Improvements of GaN chip technology have been focussed on the transfer of p-GaN normally-off transistor technology to epitaxial GaN structures grown on Si wafers, the optimization of epitaxy and processing technology towards transistors with improved switching capabilities (reduction of dynamic on-state resistance increase) and the development of quasi vertical device architectures. While power transistors delivered for characterization and modelling purposes (100mΩ on-state resistance) have been realized on SiC substrates, normally-off devices fabricated on Si substrates had been in the focus of the developments. The devices are based on a 2-stage epitaxial approach, forming the intrinsic device epitaxial layers in the first stage followed by a p-GaN overgrowth in the second stage. For improving dynamic switching properties at high bias voltage levels (600V) suitable technological solutions are matter of on-going experimental and theoretical investigations. It has been demonstrated that the design and the epitaxial quality of the buffer structures is extremely decisive. Carbon doped buffer structures in combination with AlGaN barrier layers demonstrate best performing devices. Furthermore, in order to further improve switching performance and device reliability, dedicated field plate structures have been simulated and realized experimentally.

The quasi vertical device approach considered in this project relies on metallic interconnects between source or drain regions of power transistors, respectively, and the conductive Si substrate. In this connection a newly developed trench technology allows for interconnecting either drain or source contact stripes to a conductive Si substrate. Ohmic contacts perfectly working on both, GaN and Si surfaces provide the electrical interface from top to bottom. Quasi vertical device designs facilitate a simple grouping individual source or drain cells, respectively, to a larger metallic plate on the chip surface. Therefore, the chip top metallization

may consist of an extended metallic area also covering active device regions, of course separated by a suitable insulating layer. In order to facilitate bonding over active device areas passivation and metallization of the top metallic layer has been successfully optimized for Au wire bonding. Now all process modules towards quasi vertical GaN devices have been developed, process integration is on the way current.

In terms of epitaxial growth of GaN device layers on Si <111> substrates considerable improvements have been made. Epi structures demonstrated breakdown voltage levels of up to 1200 V for floating substrate biasing conditions and more than 500 V for vertical breakdown to a fixed substrate potential. Epitaxial growth on 150 mm wafers has significantly improved in thickness homogeneity (less than 3.5 %) and wafer bow (less than 15 µm for 150 mm wafers) after epitaxy. Due to new insitu characterization methods fast development cycles are possible leading to an ever improved device quality in terms of breakdown voltage and leakage currents. Very homogeneous GaN device layers have even been shown on 200 mm Si substrates. These very promising results are due to an intensive cooperation between epi growers and the manufacturers of the growth machines. In particular, the homogeneity of the wafers is the result of careful susceptor engineering ensuring a homogeneous temperature distribution across the wafer during epitaxial growth.

GaN power devices require very specific characterization methods in order to understand switching and drift properties and, last but not least, degradation mechanisms. Therefore characterization techniques adjusted to the specific device properties need to be applied in order to gain a full device understanding on burning GaN issues. Techniques for static and dynamic characterization up to more than 1000V, parasitic capacitance evaluation, high voltage and high current pulse characterizations, breakdown characterizations, drain current trapping techniques, deep level transient spectroscopic measurements and dynamic thermal and e-field mapping techniques are now made available for systematically gaining improved device understanding. Goal is to identify the physical root cause of drift, lagging and degradation effects and to feed back this knowledge in technological improvements. In the actual reporting period, mainly normally off devices, processed in the frame of HiPoSwitch have been characterized; DC, pulsed, breakdown and dynamic thermal and E-field mapping have been carried out. Traps in device active area have been identified thanks to a detailed drain current transient characterization carried out at different temperatures. Reliability testing and failure modes and mechanisms identification activity has been started and preliminary results are very promising for the reaching of the project target. Reliability testing and failure modes and mechanisms identification activity has been started and preliminary results are very promising for the reaching of the project target.

Regarding the project´s explorative branch, a strong emphasis has been put to the development of MOS type of GaN devices in order to cope with the demands of having extremely low gate leakage current levels. Different types of gate oxides, oxide growth conditions and pre-treatment technologies have been investigated. Furthermore, novel normally-off transistors using polarization engineered heterostructures which are creating localized negative charges underneath the gate have been designed and realized practically. These devices demonstrated good normally-off behaviour with threshold voltage levels above 1 V.

In conclusion, the project is running quite successfully, however chip delivery for demonstrator fabrication is slightly delayed now because of additional work related to device processing. However means on mitigating the effect of this delay on final project achievements have been taken. All deliverables have been handed in in time.