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Summary

TDK4PE relies in the successful fabrication of organic based circuits using inkjet printed materials. These circuits use thin film transistors (TFTs), diodes and resistors as basic build blocks. The performance of these devices is essential controlled by intrinsic material parameters (such as carrier mobility, free carrier concentration), and by extrinsic parameters, among these the most important one is the density of electrical active impurities present at interfaces. For TFTs the most relevant interface is the dielectric/semiconductor interface, while for diodes and resistors the metal/semiconductor interface is critical. This report provides an account of the parameters (and appropriate techniques) to be measured/extracted according to the electrical device models. The measurements proposed should provide feedback information for adjustment of the fabrication process and in this case the speed of the measurement is crucial. This task will be undertaken on a phenomenological basis, relying on experience and statistical correlations, this is justified because the understanding of fundamental relationships between cause and effect is still lacking.

Understanding than variability and yield are key issues for building circuits out of a large number of devices lets us to consider the variability issues at circuit simulation level that have to agree with the results of model parameters extraction.

Finally it is presented a technology to design experiments called InputSampler.

As a summary this report:

a) Specifies the models to be used and the parameters to be extracted.

b) Defines techniques and measurement protocols suitable for all inkjet organic based electronics (low mobility, poor environmental stability, drifts). The objective is to minimize data dispersion caused by inadequate measurement procedures.

c) Specifies the devices modelling and validation procedure.

d) Proposes a two phase strategy to cope with circuit simulation according to the selection and usage of limited number of transistors sizes.

Applicable Documents

List of previous project reports needed or useful to understand this one, in chronological order:

1. Deliverable D2.3: TDK Development Guide: Cell Library Development and Characterization.
2. Deliverable D6.1: TDK Multi-Printing Process organization and schedule.

1 MODELING

This section describes the modeling techniques going from physical to behavioral modeling.

The goal of is to clarify the concepts and procedures concerning Modeling, Validation and Variability Management for the devices built inside the TDK4PE project, especially for Organic Thin Film Transistors.

This clarification is needed due to the different understanding that we noticed among the different communities involved in the project, basically the organic and the silicon ones.

Once these main goals are clarified, a proposal will be made for managing in the project, the whole process from device fabrication to circuit simulation using those devices.

1.1 Physical modeling

Physical modeling consists in elaborating physical model based on physics knowledge and adjusting them if necessary from experiment measures. Figure 1 describes this framework.

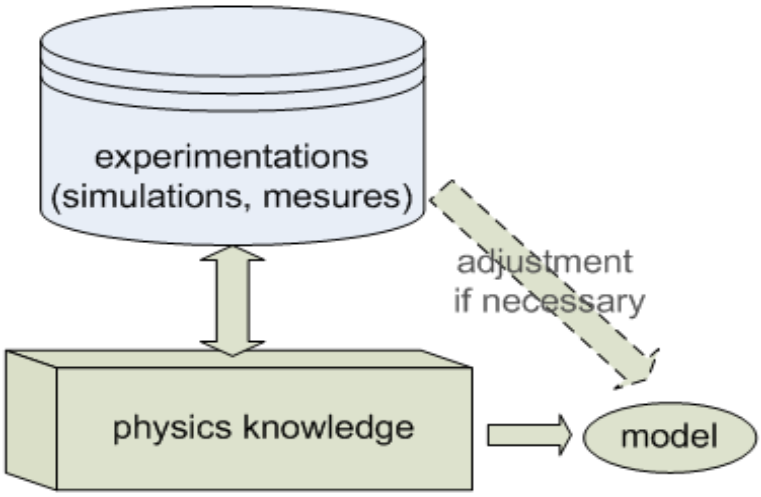


Figure 1: Physical modeling.

One main advantage of this approach is to have a physically certified model. Nevertheless the cost of this advantage is a coarse-grain simplification of the model that could become far away from real complex phenomena.

1.2 Behavioral modeling

Face to time and cost consuming experimentations, behavioral modeling proposes to model the physical phenomena from a mathematical point of view. These models are often called black-box models because their comportment is complex and also often directly intractable from a human analysis.

Their own benefit is to tackle whole phenomena[5] by replacing time consuming and costly experimentation with fast evaluation of models[6]. Figure 2 shows this kind of modeling. These models are grounded on mathematical formulation. Nevertheless they can help to analyze whole physical phenomena and to build simplified (but physically inspired) models. For example these simplified models could handle phenomena only in specific zone of data, or only some aspect of phenomena.

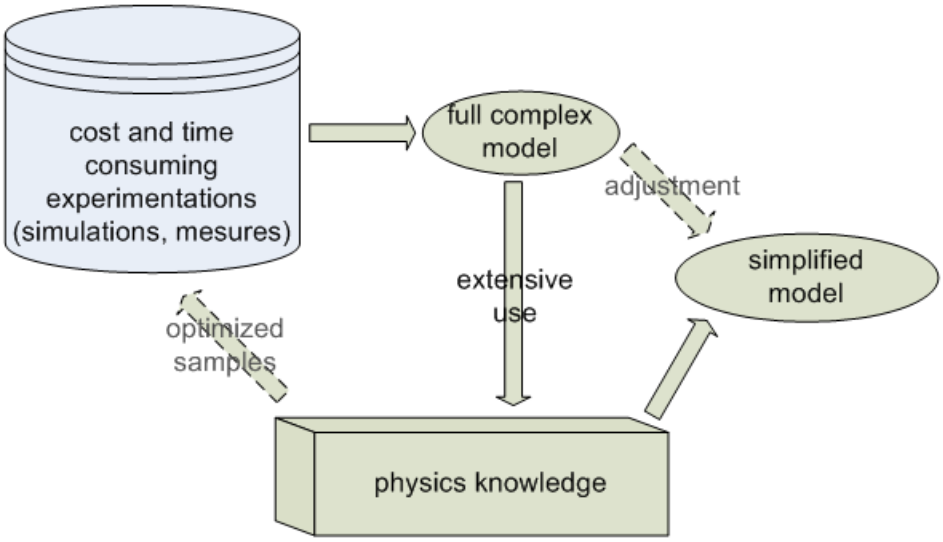


Figure 2: Behavioral modeling.

1.3 Semi-physical modeling

To combine the advantages of physical modeling and behavioral modeling, semi-physical modeling propose to design a physical model prototype from physics knowledge. This prototype is grounded on physical certified formula and has some indeterminate part such as undefined constant (as generally in physical modeling) but also undetermined function of some variable[7]. Then some behavioral modeling technique could be adapted to handle the physical model prototype instead of a mathematical model that could be incompatible with physics knowledge. The model is often compared as a gray-box: some physical aspects of the model are visible and tractable, other are handled by mathematics formula that could be physically erroneous. Very soon, the modeler will be able to treat semi-physical modeling.

[5] to be more exact the model is defined with a confidence interval and is only an approximation of phenomena
[6] this suppose that the model has lower cost than experimentation which it's generally the case.
[7] In a way semi-physical modeling can be viewed as a generalization of physical modeling

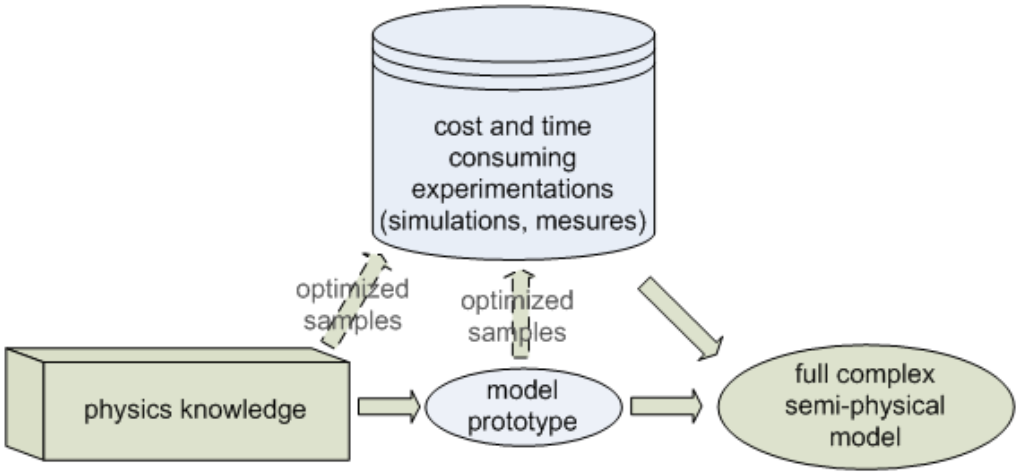


Figure 3: Semi-physical modeling.

1.4 Complete story

Needed data for sampling can be optimized. An advanced technology called "Optimal experiment design" has been developed to generate samples in multi-dimension space. Samples are chosen in a way to cover the input space of parameters while removing redundancy, i.e. avoiding samples that do not bring more information, for example those that are too close from initial samples. The flow can be detailed as in Figure 4.

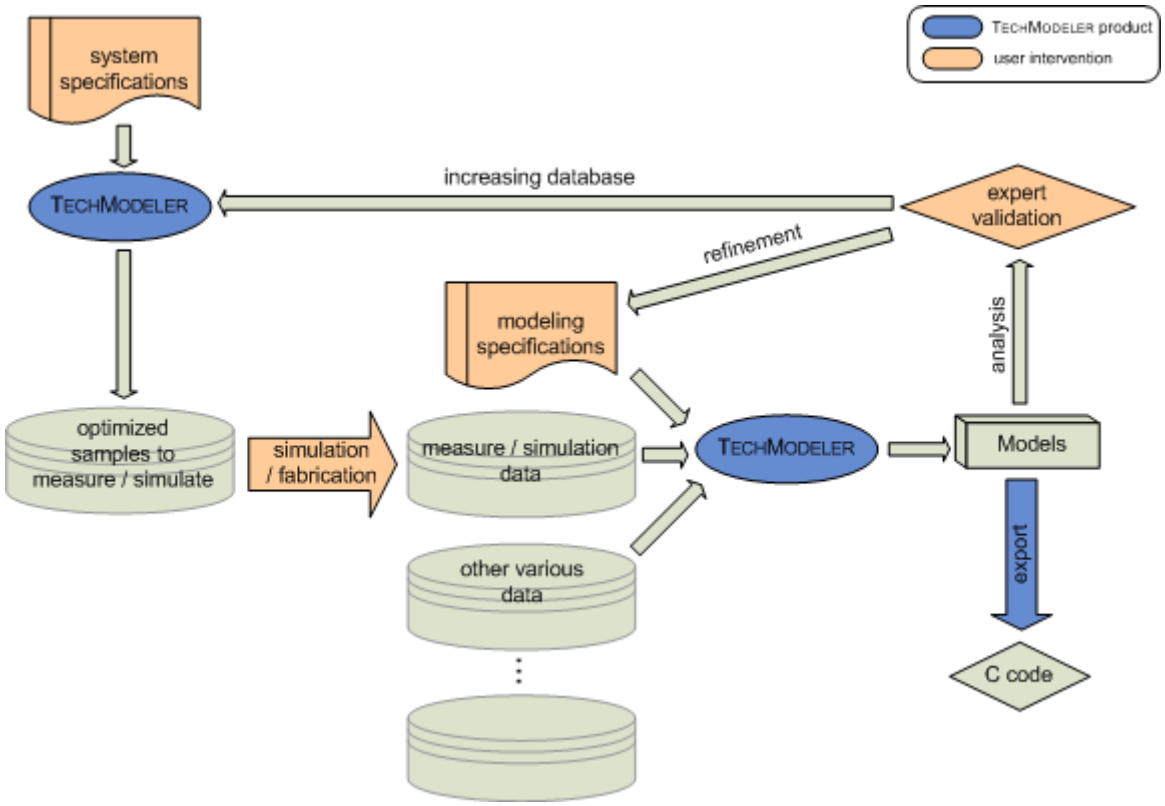


Figure 4: Modeling complete flow.

First the user describes the physical system and then creates an optimized database. After simulation or fabrication and measures of the samples, the user defines modeling specifications to create models. The models can be refine by changing modeling specifications

2 Parameter extraction for electrical characterization

In this section, we will discuss the need off electrical parameters for the device models a complete technology characterization.

2.1 Test vehicles for parameter extraction

Electrical characterization can be carried out in three different samples such as (i) witness samples, (ii) test vehicles and (iii) non specialized final circuits.

Witness samples are samples without active function. These samples are used to obtain information of a particular manufacturing step. Examples include the morphology or the roughness of a particular layer. However, the interaction of layers varies from batch to batch. In the case of the non-specialized circuits, the sample contains all the processing steps, but the characterization may not be as straightforward as in witness samples. Because of these constraints, test vehicles were specially designed to allow effortlessly the extraction of the device parameters using electrical techniques. Simulation programs such as SPICE, employ devices models (BSIM3, BSIM4 –more information in D2.3-) for circuit simulation, which uses electrical (and physical) parameters.

In this section we will focus on the test vehicles designed to be probed using electrical measurements. The electrical characterization includes both DC or quasi-static techniques such as current-voltage measurements (*I*-*V*) and small signal (AC) impedance based techniques such as capacitance-voltage (*C*-*V*) profiling. A detailed description of test equipment used for this characterization in each TDK4PE node is listed in D6.1.

Regarding the physical-based models for circuit simulation, two main classes of parameters are taken into account, electrical and geometrical parameters. For instance, concerning the drain current in linear regime equation of an OTFT, as shown equation 1, the electrical parameters are the mobility (μ), capacitor per unit area (C_i) and the threshold voltage (V_T); the geometrical parameters are the length (L) and width (W) and the insulator thickness (d_i). V_{GS} and V_{DS} are the electrical test parameters. The electrical characterization of the test vehicle allows the electrical parameters extraction and to obtain the values of the device model.

$$I_{DS} = \frac{W}{L}\mu C_i (V_{GS} - V_T)V_{DS} \qquad (1)$$

The basic role of electrical characterization in the technology is shown in Figure 5. In order to find the parameters value for a device, according to a specific device model, different characterization procedures are required. A good fitting between the model and the parameters occurs when the simulation and the real measurements matches.

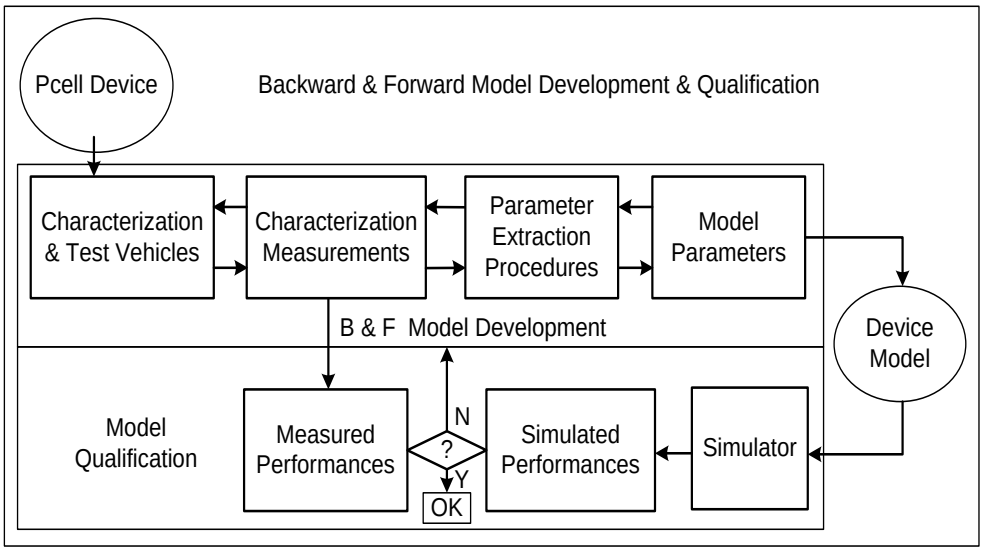


Figure 5. Schematic diagram of the characterization vehicles and parameter extraction in the development and qualification of the technology.

3 Device models and parameters

In this section we will focus on the models and parameters to be extracted for linear and snake resistors, capacitors, inductors, diodes and OTFTs.

The devices are function of the material stack arrangement because of the interaction among them is important. Regarding TDK4PE technology, which is based on PMOS technology, the material stack is shown in Figure 6. The schematic represents a metal-insulator semiconductor (MIS) structure. It is worth to note that this order of the materials leads to the bottom gate contact OTFT structure.

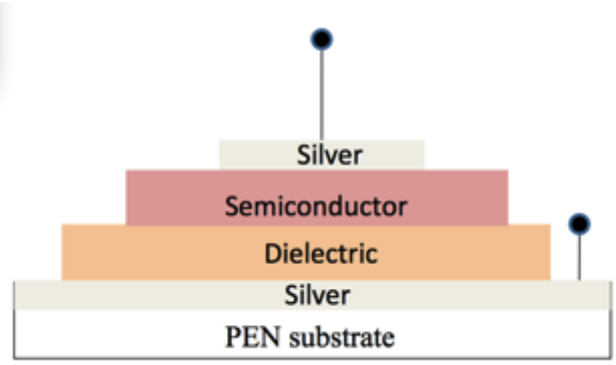


Figure 6. Schematic structure of the different layers used to make MIS capacitors or TFT devices.

3.1 Resistor model

The most elementary of all devices is the resistor. It consists of a bar of homogeneous materials with two contacts at the extremes. Injection of carriers is assumed to be unhindered and the current only limited by the resistivity of the material. The electrical parameter of a resistor is its resistance *R* of the material, which is defined by Ohm's Law (equation 2):

$$R = \frac{V}{I} \qquad (2)$$

The reciprocal of this resistance is called conductance *G* and is a more adequate entity in electrical characterization. Both device parameters resistance (equation 3) and conductance (equation 4) can be expressed in their material parameters, resistivity ρ and conductivity σ, according to

$$R = \rho \frac{d}{A} \qquad (3)$$

$$G = \sigma \frac{A}{d} \qquad (4)$$

where *A* is the cross-section area and d the length of the device (Figure 7).

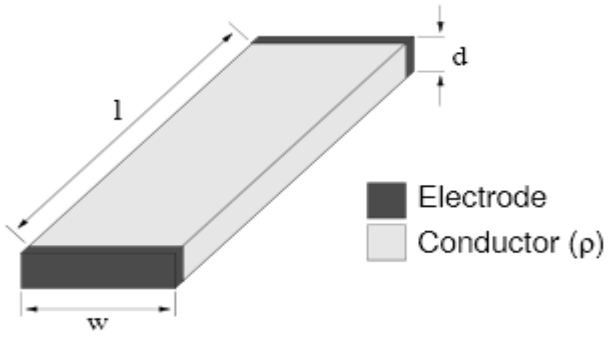


Figure 7. Physical parameters used to estimate the resistance of a material.

However the Ohm's Law and if we consider the whole resistor device, a parasitic series resistance is created at the junction of the resistive material and the pads due to the difference in their work functions. This parasitic resistance is called contact resistance, $R_{contact}$. Then, the resistance of the resistor device is composited by the material and the contacts (equation 5). The following expression is used to model the device, having two areas of interfacial contact as shown in Figure 8. For simplicity, it is assume that both contact resistances are equal which may not be true.

$$R = R_{material} + 2R_{contact} \quad (5)$$

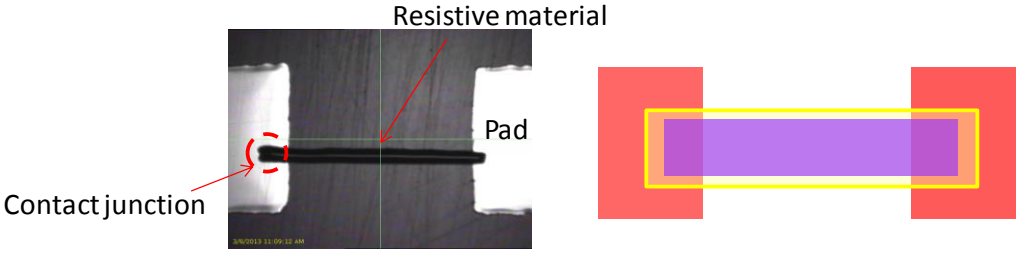


Figure 8. (a) Photograph of a linear resistor, (b) schematic arrangement of the layer layout.

3.1.1 General parameter extraction procedure

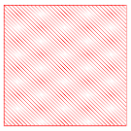
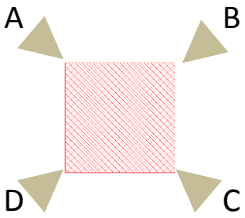
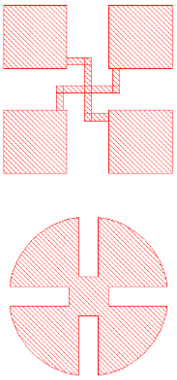
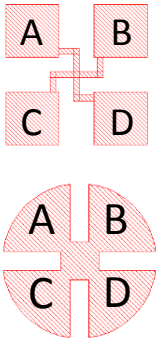
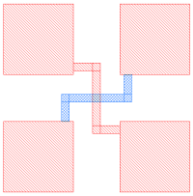
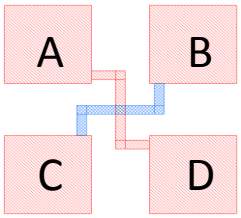
Parameters extracted	Test vehicle	Test vehicle layout	Characterization measurements	Characterization procedure
Rsheet Resistivity	**Van Der Pauw**		 Contacts in the extremes	Four- probe measurement. Apply a curve from 0V to 1-2V between A & B contacts, and measure current (I) between C & D contacts.
Rsheet Resisitivity Linewidth	**Greek cross**		 Contacts on the pads	Four- probe measurement. Apply a curve from 0 V to 1-2V between A & B contacts, and measure current (I) between C & D contacts.
Rcontact	**Greek cross for $R_{contact}$**	Material 1 (Blue pattern) and Material 2 (Red pattern) 	 Contacts on the pads	Four- probe measurement. Apply a curve from 0 V to 1-2 V between A & B contacts, and measure current (I) between C & D contacts.

Table 1. General parameter extraction procedure.

3.2 Capacitors model

Printed capacitors are Metal-Insulator-Metal (MIM) sandwich structure as shown in Figure 9.

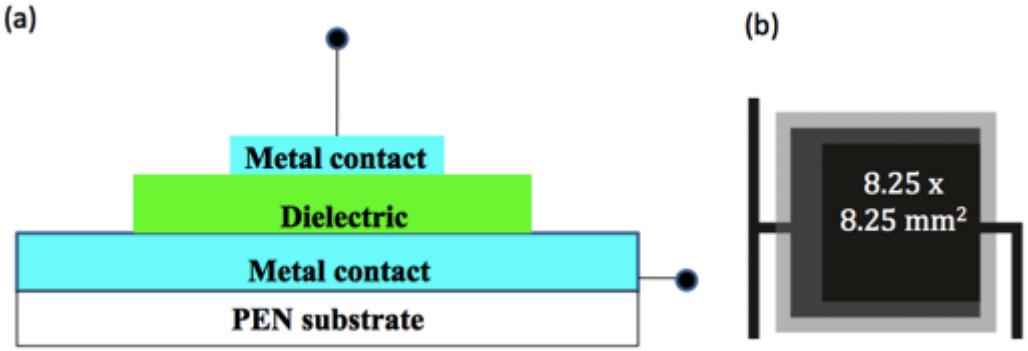


Figure 9. (a) Schematic cross section view of a printed capacitor, (b) Schematics of a top view showing the active area and printed tracks.

Capacitor structures were used to extract the insulator parameters such as dielectric constant, leakage currents, and parasitic effects due to inkjet printing. The two major sources of parasitic effects are: (i) fringing effects, (iii) lateral conduction and (ii) series resistance caused by the metal tracks. In addition capacitors may also be used to inspect for layer thickness variations with the area.

As shown in Figure 9b the physical area of the bottom electrode coated with the dielectric is larger than the top metal layer. In a MIM structure the number of free carriers in the polymer is low and fringing effects are not really expected. Fringing may be significant in metal-insulator-semiconductor (MIS) structures. However, the presence of atmospheric moisture may contribute to fringing by making the dielectric surface conductive. When measurements are done under vacuum conditions, the additional parasitic capacitance observed in MIM structures may be due to a lateral conduction along the polymer near the bottom contact surface. This is schematically represented in Figure 10 and can enhance the effective area of the capacitor.

Other sources parasitic capacitance may appear due to the alignment of top and bottom electrode tracks.

Series resistance due to the printed silver tracks may limit the frequency response of the capacitors. Series resistance effects must be minimized by printing wide and short silver tracks.

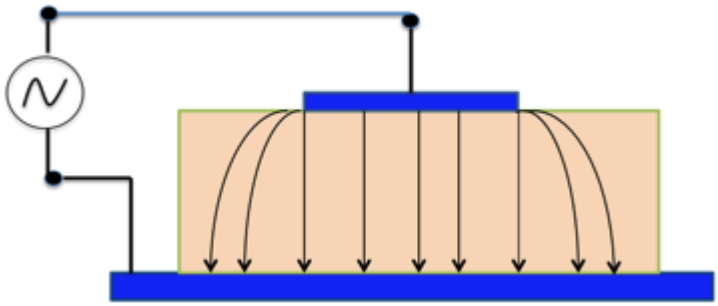


Figure 10. Schematic representation of an increase in the effective area of the top electrode caused by lateral conduction. This effect can enhance the measured capacitance.

3.2.1 Parameter extraction procedure

Figure 11 shows the equivalent circuit for a printed capacitance. C_P and R_P can be evaluated by measuring the impedance at low frequencies (f<1 kHz) using an impedance analyzer. To estimate R_S one must measure the impedance as function of frequency. The presence of a small series resistance (R< 10 Ω) due to the silver electrodes can a cause a relaxation frequency above or within the MHz range.

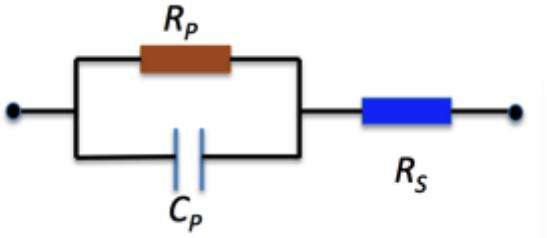


Figure 11. Equivalent circuit for a printed MIM structure including the series resistance caused by metal tracks.

Figure 12 show the capacitance and loss (G/ω), where $\omega = 2.\pi.f$, as a function of the frequency for a printed capacitor. As commonly observed in organic based electronic devices the capacitance decreases slightly in a linear fashion with frequency. This is a well-know process that is modeled by a constant phase element. The admittance (Y) of the capacitor can be expressed by the empirical relation $Y=A_0(i\omega)^n$ where $1 \geq n \geq 0$ and Ao a constant. The physical origin of the process is unclear. In semiconductor materials it is reasonable to assume that is caused by to dipolar relaxation with a wide distribution of relaxation times. However, this frequency dependence is relatively small and it can be neglected.

The model of a printed capacitor will only take into account the parameters described in Figure 11. Table 2 summarizes the electrical measurements used to extract capacitor parameters.

Model parameter	Parameter extraction procedures	Characterization equipment	Test vehicle
R_p and C_p	Test frequency of 1 kHz, AC signal 100 mV	LCR meter, Impedance Analyzer	MIM
R_S	Rs causes major disperison in the impedance as function of frequency. The frequency of this dispersion allows the estimation of *Rs*.	LCR meter, Impedance Analyzer	MIM

Table 2. Parameter extraction for capacitors.

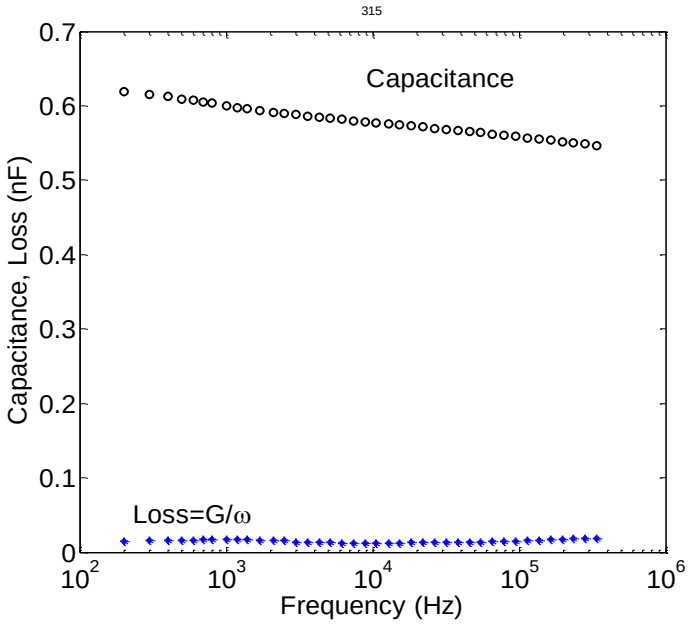


Figure 12. Capacitance and loss (G/ω) as function of the frequency for a printed capacitor based on a Altana Bectron dielectric. Apart from a small decrease in capacitance with frequency, the behaviour is typical of a pure capacitor. The flat behavior upon with frequency shows that the resistance of the metal track is small.

Figure 13 show the capacitance as function of the frequency recorded in several MIM structures fabricated using two different dielectrics. The cross linked PVP and the Altana Bectron. For each dielectric the printed area as well as the bottom electrode area were kept constant. However the area of top electrode is varied. This allows us to inspect for

fringing effects. From the data in Figure 13 we can see that when the area of top electrode is significant smaller (70%) than the bottom dielectric, there is an excess capacitance. This is possible caused by lateral conduction as discussed above.

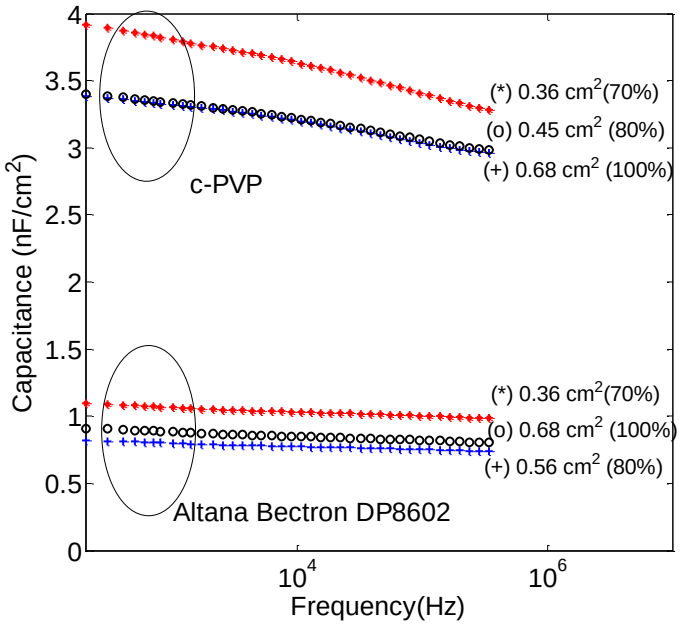


Figure 13. The frequency dependence of the capacitance of several printed MIM structures. The area of the top electrode was varied in respect to the total dielectric area.

3.3 Inductor models

An inductor is a passive component that stores energy in form of magnetic field. It consists on a wire or other conductor wounded into a coil (this coil can be air). The inductance is a property by which a variation of the current produces a varying magnetic field that induces voltage in the conductor (inductor) itself and/or other conductors nearby. For RF applications a typical implementation is a printed spiral on the substrate. Several topologies can be used, as is shown in Figure 14.

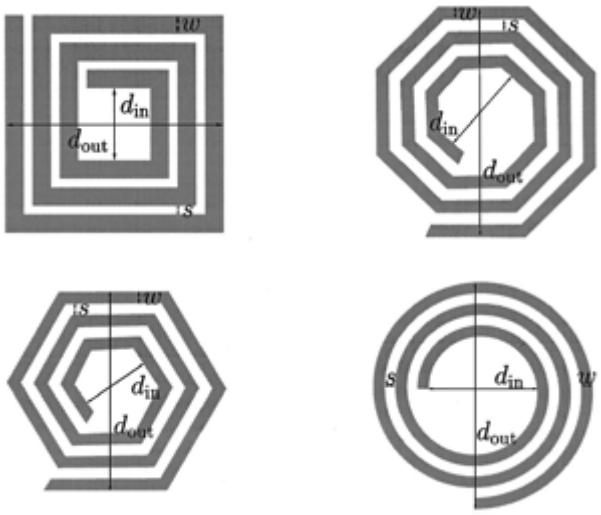


Figure 14.Typical spiral inductor topologies (square, hexagonal, octagonal and circular). Extracted from [5]

Inductance must be calculated in function of the used implementation. For planar spiral inductances, expressions introduced in [5] are typically used:

$$Lmw = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \rho} \quad (13)$$

$$L_{gmd} = \frac{\mu n^2 d_{avg} c_1}{2} (ln(c_2/\rho) + c_3 \rho + c_4 \rho^2) \quad (14)$$

The first approximation (L_{mw}) is based on a modification of an expression developed by Wheeler; the second (L_{gmd}) is derived from electromagnetic principles by approximating the sides of the spirals as current-sheets. In these expressions, μ_0 is the vacuum permeability, d_{avg} is the average diameter of the spiral $(davg = 0.5(dout + din))$ and ρ is the fill ratio$(\rho = (dout - din)/(dout + din))$. K_i and c_i are topology depending coefficients. Tables are given in [5].

3.3.1 Parameter extraction procedure

A printed spiral inductor can be modeled as shown in Figure 15.

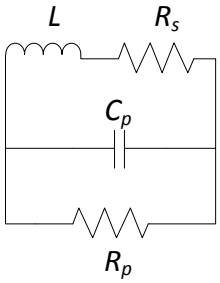


Figure 15. Electrical model of an inductor.

R_s represents the metal loss (resistance of the conductor), R_p is the coil loss and C_p is the distributed capacitance between the turns of the conductor. In the considered structures, R_p can be neglected because L is small and the capacitance between the turns dominates over these losses.

Using a LCR meter is possible to extract the inductor parameters. Measuring in L_s-R_s mode, L_s value can be expressed as:

$$L_s = \frac{X}{\omega} = \frac{L\left(1 - \omega^2 LCp - \frac{CpRs^2}{L}\right)}{(1 - \omega^2 LCp)^2 + \omega^2 Cp^2 Rs^2} \quad (15)$$

If $\omega^2 Cp^2 Rs^2$ <<1 and $\frac{CpRs2}{L}$ <<1, is possible to simplify L_s:

$$L_s \cong \frac{L}{1 - \omega^2 LC_p} \quad (16)$$

The stray capacitance C_p determines the self-resonant frequency (SRF) of the inductor. At SRF, the inductor presents maximum impedance. At frequencies above SRF, C_p is dominant and inductor exhibits a capacitive behavior.

Quality factor can be obtained from L_s-R_s characterization since:

$$Q = \frac{2\pi f L_s}{R_s} \quad (17)$$

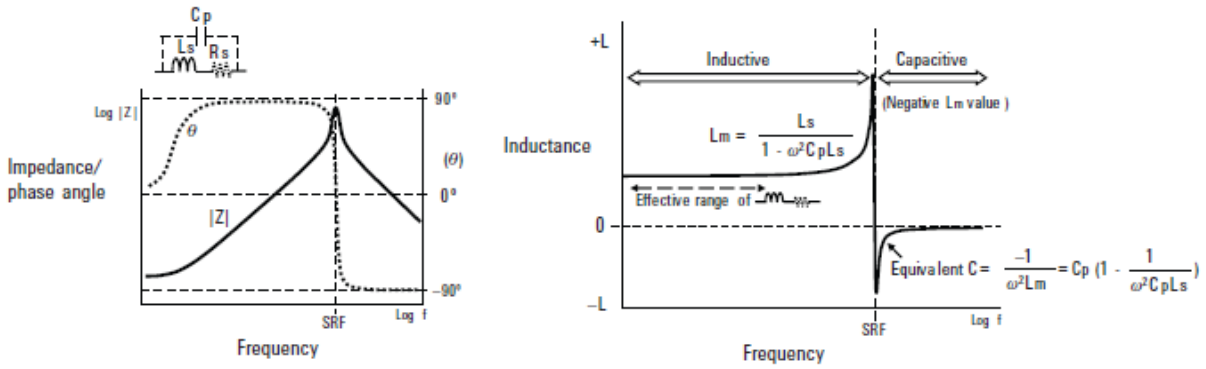


Figure 16. Typical inductor frequency response: Impedance absolute value and phase (a) and inductance frequency response (b). Extracted from [6]

As can be seen in Figure 16(b), the measured inductance (L_m) takes its maximum value at SRF.

Using LCR meter is possible the characterization of inductors up to 2 MHz. A vector network analyzer can be used for measurements at higher frequencies. In this case we can obtain S-parameters of the inductor under test and inductor parameters can be extracted from measured impedances using commercial circuit simulation tools, such as *Agilent Advanced Design System*. Real part of input impedance gives us the series resistance value (R_s), and from imaginary part we obtain the reactance. Taking these values at low frequencies, stray capacitance (C_p) is negligible and inductance (L) can be obtained from reactance.

Measuring at higher frequencies allows also obtaining SRF, typically higher than 2 MHz for the characterized inductors, and, from this frequency, C_p can be obtained:

$$\omega_{SRF} = \frac{1}{\sqrt{LC_p}} \qquad (18)$$

Table 3 shows a summary of the electrical test vehicles and its parameter extraction.

Model parameter	Parameter extraction procedures	Characterization measurements	Characterization equipment	Test vehicle
L_s- R_s; $Q=\omega L_s/R_s$	Use a sweep test frequency from 20Hz up to 2 MHz, AC signal 1V	2 points-measurement Measure L_s- R_s	LCR meter, Impedance Analyzer	Spiral Inductors
L_s-R_s-C_p; $Q=\omega L_s/R_s$ **SRF**	Use a sweep test frequency from 10 MHz up to GHz. Extract inductor parameters from S-parameters using software	1 RF port measurement Measure S-parameters	Network Analyzer	Spiral Inductors

Table 3. Summary the electrical test vehicle and parameter extraction for inductors.

3.4 RF devices and transmission line models

Radiofrequency components, such as filters, couplers, mixers, etc. are an important part in the design of electronic systems. At certain frequencies (from UHF bands) guided wavelengths become shorter and RF devices can be often implemented using planar technology, by means of transmission lines, transmission line sections (stubs) and/or semi-lumped elements. This kind of circuits, usually implemented using conventional PCB techniques, can be also fabricated by means of Printed Electronics.

3.4.1 Parameter extraction procedure

For the electrical characterization of the structures, a vector network analyser is typically used for the measure of scattering (S-) parameters. These parameters give information about the electrical properties, such as transmission and reflection characteristics, of the device under test. However, before designing and characterizing RF devices in a given substrate is necessary to know its electrical properties.

Substrate electrical characterization

For the design of RF devices using printing electronics techniques, it is necessary the electrical characterization of the substrates. Relative dielectric permittivity (ε_r) (dielectric constant) and loss tangent ($tan\ \delta$) (dissipation factor) of the substrate can be extracted using several techniques. A simple method is measuring the resonances of a microstrip ring resonator as show in Figure 17.

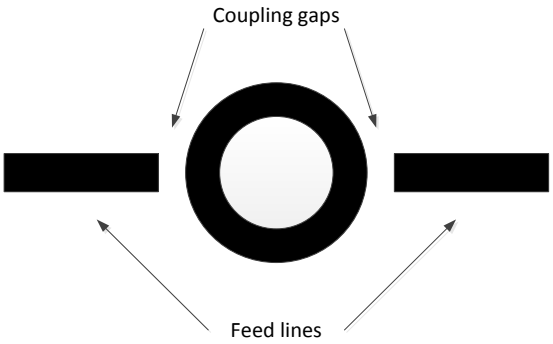


Figure 17. Microstrip ring resonator. Bottom ground plane not represented.

The distance between feed lines and ring resonator (coupling gaps) must be large in order to avoid variation of the intrinsic resonant frequency of the ring and minimize coupling effects (Figure 17). When the mean circumference of the ring (*L*), is equal to an integral multiple of the guided wavelength, resonance appears:

$$L = 2\pi r = n\lambda_g \qquad \text{for } n = 1,2,3\ldots \tag{19}$$

Where *r* is the mean radius of the ring (difference between inner and outer radius) and λ_g is the guided wavelength, which can be expressed as:

$$\lambda_g = \frac{\lambda_0}{\sqrt{\varepsilon_{eff}}} = \frac{c/f_n}{\sqrt{\varepsilon_{eff}}} \tag{20}$$

being f_n the ring resonant frequencies and *c* the speed of light in free space.

From equation (19) and (20):

$$\lambda_g = \frac{L}{n} = \frac{2\pi r}{n} \tag{21}$$

From these expressions, it is possible to obtain the effective permittivity, parameter that takes into account that, in a microstrip line, a fraction of electric fields are not constrained within the substrate:

$$\varepsilon_{eff} = \left(\frac{nc}{2\pi r f_n}\right)^2 \tag{22}$$

And, finally, from the following empirical expression, the relative permittivity (ε_r) can be obtained [7]:

$$\varepsilon_{eff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left(1 + 12\frac{h}{W}\right)^{-1/2} \tag{23}$$

Where *h* is the height of the substrate and *W* is the width of the microstrip transmission line. This expression is valid when *W*/*h* > 1, condition satisfied in most cases.

Summarizing, for obtaining the dielectric constant of the substrate at several frequencies we can measure S-parameters of a microstrip ring resonator using a network analyser and obtain the resonant frequencies, where peaks of transmitted power appear, and apply the expressions presented.

In order to obtain the dissipation factor is necessary to calculate the attenuation constant using the following expression:

$$\alpha = \frac{8.686\pi}{Q\lambda_g} \quad \text{(dB/m)} \qquad (24)$$

Where Q is the unloaded quality factor of the ring resonator:

$$Q = \frac{f_n}{f_2 - f_1} \qquad (25)$$

Being f_2 and f_1 the limits of the band (-3dB insertion loss frequencies). The loss tangent (tan δ) can be obtained from the expression [8]:

$$\alpha = 8.686\pi \frac{\varepsilon_{eff}-1}{\varepsilon_r - 1} \frac{\varepsilon_r}{\varepsilon_{eff}} \frac{tan\delta}{\lambda_g} \quad \text{(dB/m)} \qquad (26)$$

Devices electrical characterization

For the electrical characterization of the structures, S-parameters will be measured using a network analyser, in combination with a probe station or using 2.4 mm end launch connectors.

As mentioned before, measuring these parameters we are able to obtain transmission and reflection characteristics of the devices. A typical band pass filter response represented by means of S-parameters is shown in Figure 18.

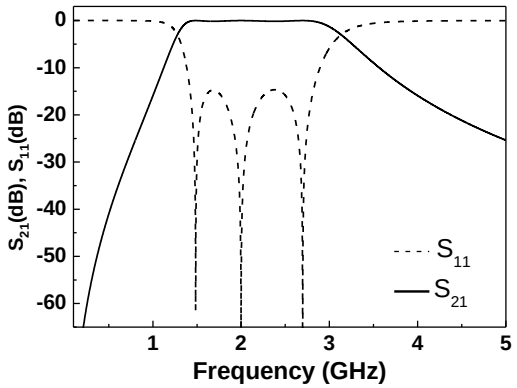


Figure 18. Typical S-parameters response of a band-pass filter. S_{21} represents transmission or gain and S_{11} is the reflection loss (in dB).

In order to obtain correct measures, a calibration process must be performed before measuring, with the goal of correcting systematic errors in the instrument, characteristics of the cables and adapters. The most typical calibrations are SOLT and TRL. SOLT (Short-Open-Load-Thru) is the simplest one and only requires connecting these standards. In some devices is necessary to remove the contribution of connectors and/or transmission lines included in the device under test. Using the same access lines in all the devices is possible to obtain accurate measurements of the designed components by means of de-embedding techniques. De-embedding is a mathematical process that removes the effects of unwanted portions of the structure that are embedded in the measured data by subtracting their contribution. To this end, is necessary to perform TRL (Thru, Reflect, Line) calibration by means of a specifically-designed TRL calibration kit. Figure 19 is an example of a differential TRL kit and devices under test using the same access lines implemented in conventional PCB.

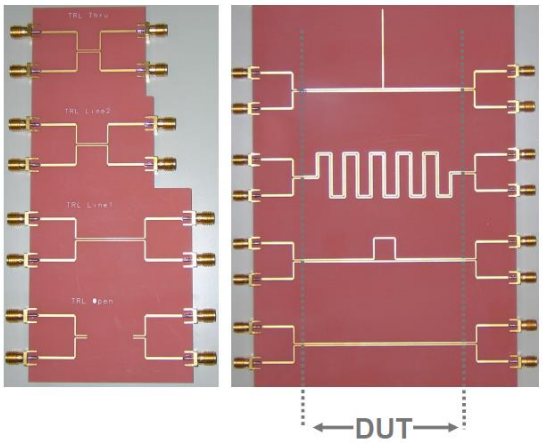


Figure 19. TRL differential calibration kit (left) and devices under test PCB (right). Extracted from [9].

Table 4 shows a summary of the electrical test vehicles and its parameter extraction.

Test vehicle	Test vehicle layout	Characterization measurements	Characterization procedure	Parameters extracted
Printed Microstrip Ring Resonator (substrate characterization)		2 RF ports measurement Network Analyzer	Frequency from 10 MHz up to GHz Measure S-parameters → Extract ring resonant frequencies and bandwidths → Process data using equations	ε_r – tan δ at several frequencies
TRL calibration kit for de-embedding (device characterization)		TRL calibration Network Analyzer	TRL calibration in combination with de-embedding techniques	Corrected S-parameters

Table 4. Summary the electrical test vehicle and parameter extraction for inductors

3.5 Rectifying diodes

There are several strategies to implement a rectifying element. Therefore, before device parameters and models are presented, it is important to analyze the different approachs and select the most suitable rectifying element.
In this section rectifying diodes fabricated by ink-jet printing were evaluated. We compare the direct current (dc) and high-frequency performance of three different rectifying diode structures, (i) a Schottky diode a (ii) diode connect TFT and (iii) a MIS diode.
Since the most challenging applications are radio-frequency-identification (RFID) tags, the emphasis was put on the ability of the rectifying elements to follow the base-carrier frequency of 13.56 MHz. A suitable diode configuration was identified and an appropriate model proposed.

3.5.1 Review

In 2006 Poly IC presented the world first "roll-to-roll" organic RFID tag (a 64-bit tag working at a bit rate higher than 100 b/s, readout by inductive coupling at a base carrier frequency of 13.56 MHz [10,11]. More recently, full organic RFID tags for barcode replacement, generating code sequences up to 128 bits, have been demonstrated operating at the carrier frequency of 13.56 MHz [12,13].

Although impressive high frequency rectifying circuits have been reported [13-18]. All these devices use expensive fabrication technologies (vacuum sublimation and photolithography) as well as high mobility materials mostly relying on small molecules. To the best of our knowledge until now a RFID tag fabricated using all-inkjet printed devices has not been reported.

The most critical component in a RFID tag is the rectifying diode. There are basically two strategies to fabricated rectifying components, Schottky barrier diodes and diode connected TFTs. The diode connected TFT approach has the advantage of easy integration. However, TFTs have relatively long channels. By using photolithography the channel can be reduced but channel lengths below 10 μm are not easy to produce by ink-jet printing. Cantatore et al. [17] have shown that it is possible to rectify a sinusoidal signal of 13.56 MHz using a diode connected TFT. However, an ac signal with 80 V peak amplitude was required to be obtained a dc level of 10 V. Schottky based diodes perform much better. A pentacene based diode can rectify an incoming ac signal of 18 V amplitude to a dc signal of 11 V at 13.56 MHz [18].

Depending on the channel length used, the diode connected transistor requires a several hundred times lager area as compared to the Schottky diode, which translates in a larger capacitance. The capacitance may not directly limit the frequency response, but the channel length due to slow carrier transport.

Table 5 provides a summary of the main characteristics and limitations of both type of devices.

Rectifying diode	Comments	Refs.
Schottky diode	The cut-off frequency is limited by the carrier time-of-flight and not by the diode capacitance. The low carrier mobility must be compensated by a thinner active layer. For high frequency response high mobility and thin organic layers must be used.	[19]
Diode connected TFT	Have a low current density. Requires the fabrication of large area TFTs which increases the occurrence of defects The channel length must be kept small.	[17]

Table 5. Basic characteristics of the two approaches to fabricate rectifying diodes.

3.5.2 Electrical characterization of rectifying elements

Schottky diodes

A Schottky diode structure is shown in Figure 20. This diode has a barrier at the interface between cooper and the PTAA semiconductor. This diode was fabricated outside of the TDK4PE consortium and the cooper electrode was evaporated. Although, there is a debate if these diodes can be named Schottky type diodes, for the sake of simplicity we used the conventional terminology. Current-voltage characteristics and the frequency dependence capacitance and loss are show in Figure 21. The analysis of the forward *I-V* characteristics in a log-log plot (see Figure 22) shows that the charge carrier transport is space charged limited (SCL) and follows approximately Child's law (slope 2). As it will be discussed later, this imposes an intrinsic limitation of the diode ability to rectify high frequency signals.

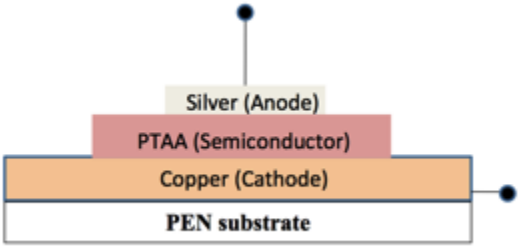


Figure 20. Schottky diode structure.

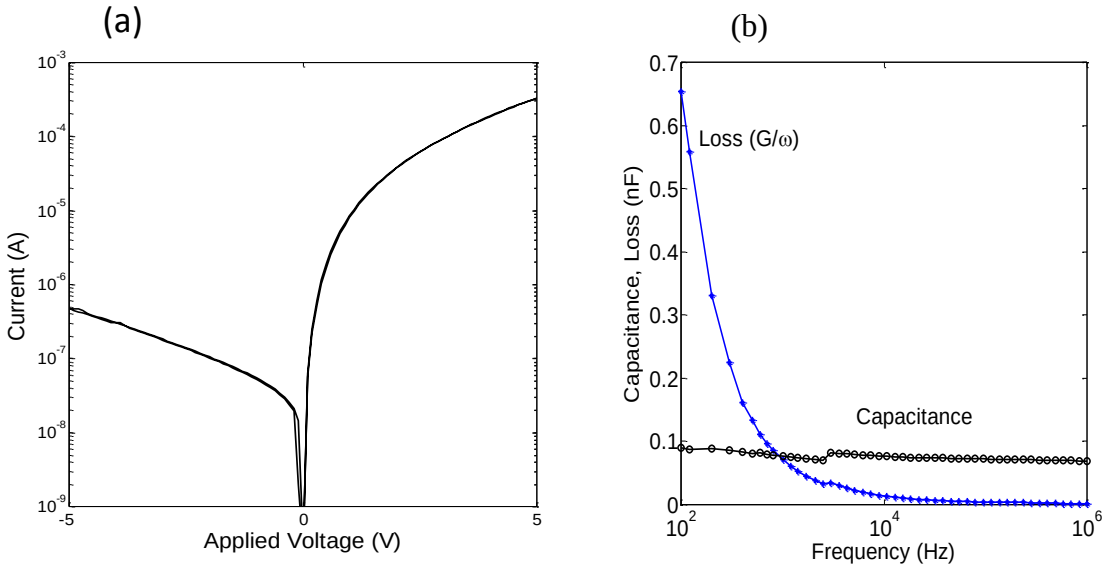


Figure 21. (a) I-V characteristic and (b) capacitance and loss (G/ω) as function of frequency for a Schottky diode.

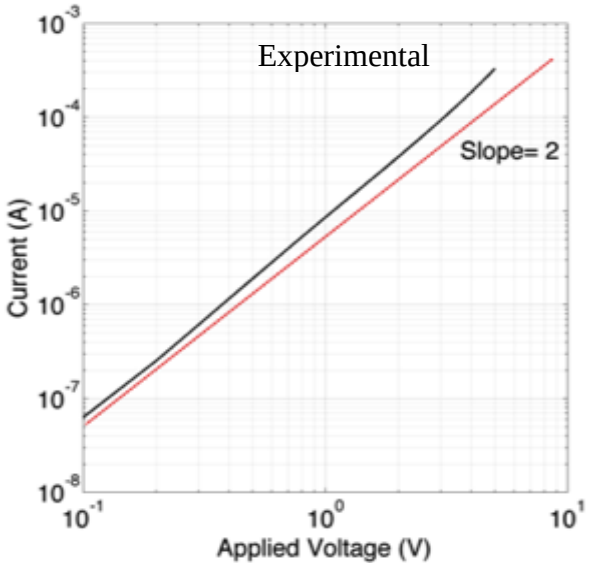
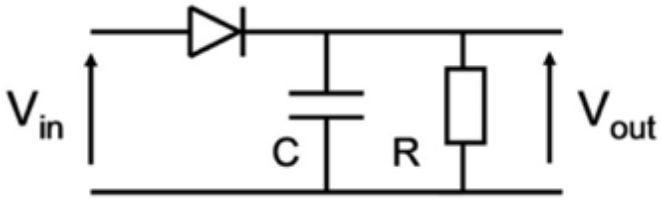


Figure 22. Log-log plot of the forward bias current-voltage characteristic showing that the slope is slightly higher than 2.

(a)



(b)

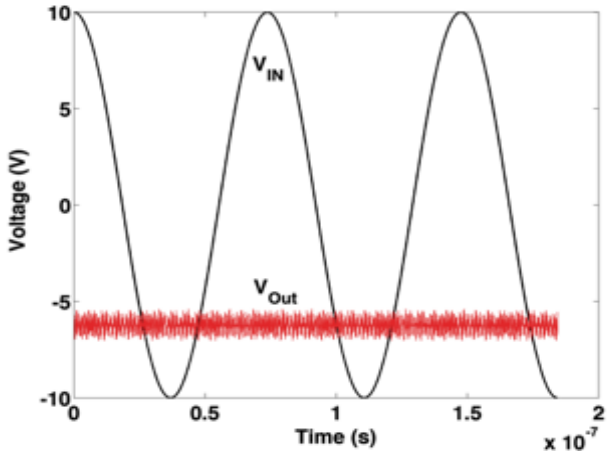


Figure 23. (a) Rectifying circuit. (b) Comparison between the input signal and the output DC signal. The load circuit uses a capacitor of 100 nF and a resistance of 1 MΩ. f=13.56 MHz.

MIS diodes

The electrical properties of rectifying diodes based on metal-insulator-semiconductor (MIS) diodes are described. The diode structure and a typical I-V curve is shown in Figure 24. Based on the device structure the MIS diode should behave as capacitor because the insulator is 1 μm thick. The fact that there is a substantial leakage current particularly when the semiconductor/insulator interface is driven into accumulation, suggest that the insulator is in reality thin enough to allow current passing trough. We propose that the dielectric has pinholes, which are filled by the top semiconductor layer. The system is in reality nanostructured dielectric/semiconducting matrix as show in Figure 25. When negative bias is applied in the dielectric a high free carrier density is induced in the semiconductor. At local thinner regions as show in Figure 25 these carriers can tunnel across the dielectric. When a negative bias is applied to the dielectric no free carriers are induced in the semiconductor and the leakage is substantially smaller. This view explains the asymmetric I-V characteristics.

These diodes have a rectification ratio of 120 at |10V|. They behave as non-linear resistors. The forward *I-V* curve follows space charge limited behavior in all the voltage range (see Figure 26). Capacitance-voltage characteristics confirm the absence of depletion layers associated with interfacial barriers (see Figure 27b). The decrease in the

capacitance with increasing bias is due to a high leakage current that bypass the diode capacitance.

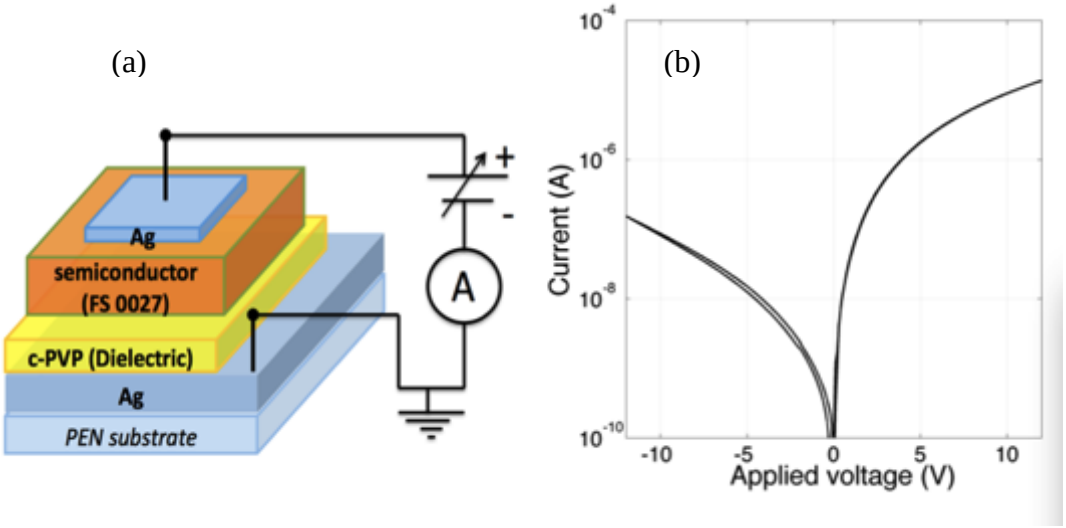


Figure 24. (a) Schematic representation of a MIS-Diode, (b) typical current voltage characteristic showing an asymmetric behaviour.

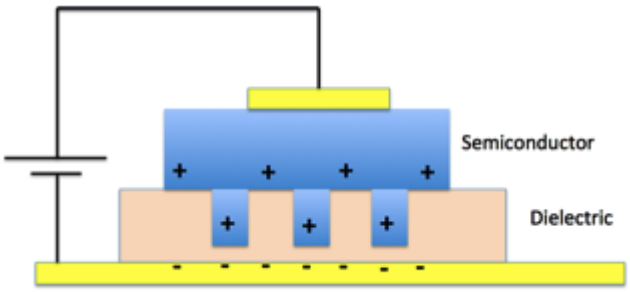


Figure 25. Schematic diagram showing the proposed mechanism to explain non-symmetric *I-V* curves in MIS structures.

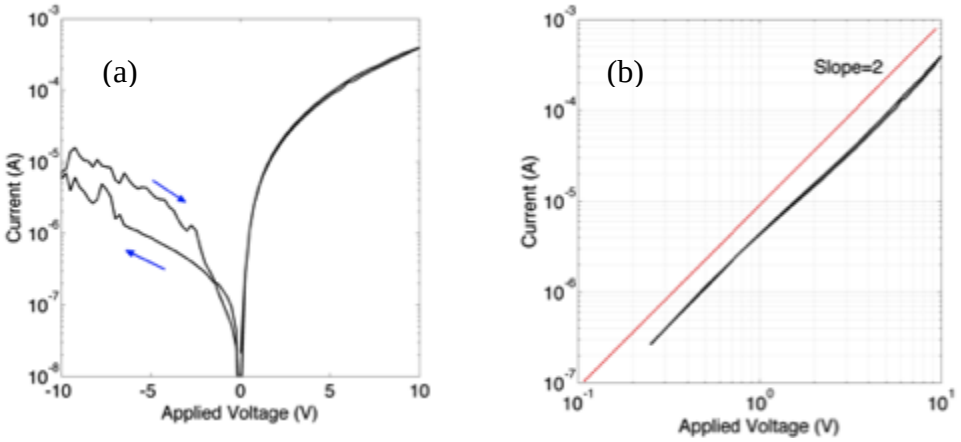


Figure 26. Electrical characteristics of MIS diode. (a) Semilog plot showing the existence of hysteresis in reverse bias. (b) Log-log plot of the forward bias current.

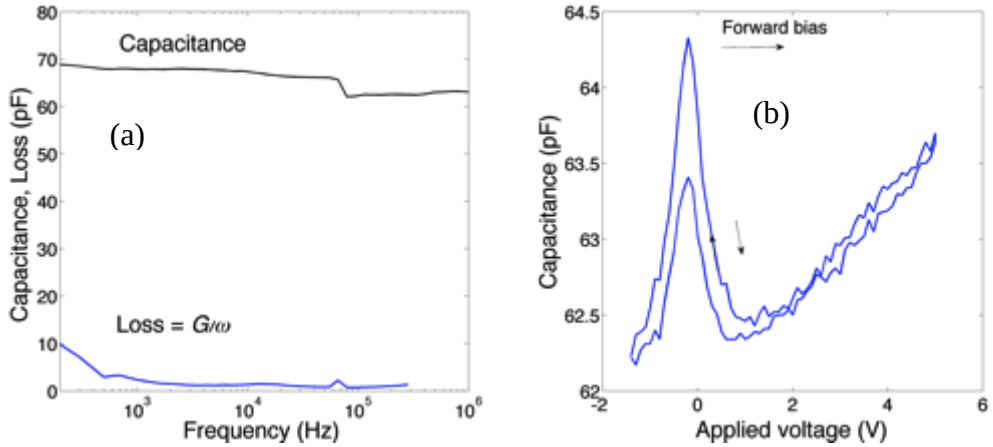


Figure 27. (a) Capacitance and loss as function of the frequency (b) Capacitance voltage plot recorded at a test frequency of 1 kHz. The diode area is 1 mm^2.

When the MIS diode is mounted in a rectifying circuit with C=470 nF and R=1 MΩ the signal is strongly attenuated for frequencies above 1 MHz. At the operating frequency of 2 MHz the DC rectified output reaches only 0.5 V for an input amplitude of |10V| as shown in Figure 28. These diodes do not fulfill the requirements for a 13.56 MHz rectifier circuit. Accordingly to Altazin et al. [19] the reason is because the charge carrier mobility is too low. Although, the oxide is thin at local regions, it must have traps, which limit the carrier flow.

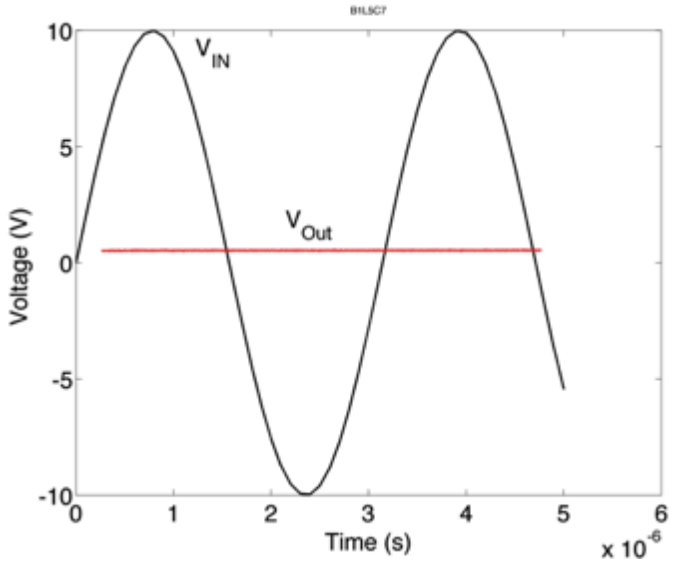


Figure 28. Rectified signal at 2 MHz the load capacitor is 470 nF and the load resistance of 1 MΩ.

Figure 29 shows the frequency dependence of V_{out}/V_{in} .

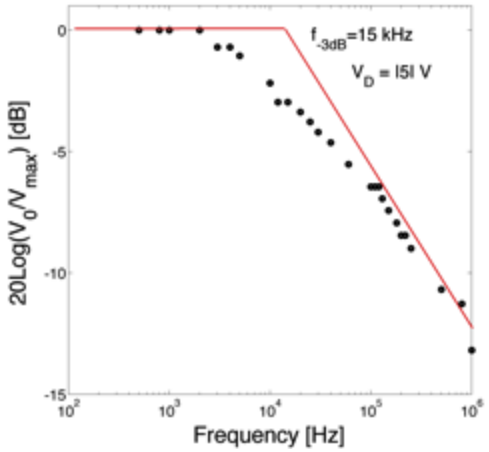


Figure 29. Frequency dependence of V_{out} /V_{in} for a MIS diode is connected in a rectifying circuit. The load is a RC parallel circuit (R=1 MΩ, 100 nF).

Diode connected TFT.

Figure 30 shows the current voltage characteristic of a diode connected TFT. Under a forward bias of -20 V, it can supply 250 nA. Rectifying circuits were tested but the signal is strongly attenuated in the kHz range. This limitation is caused by a long channel length (L=40 μm) and low charge carrier mobility (10^{-3} cm^2/V.s). This diode was not considered an option for high frequency rectifying circuits because it requires and optimization not compatible with ink-jet printing (very small channel lengths and high mobility materials).

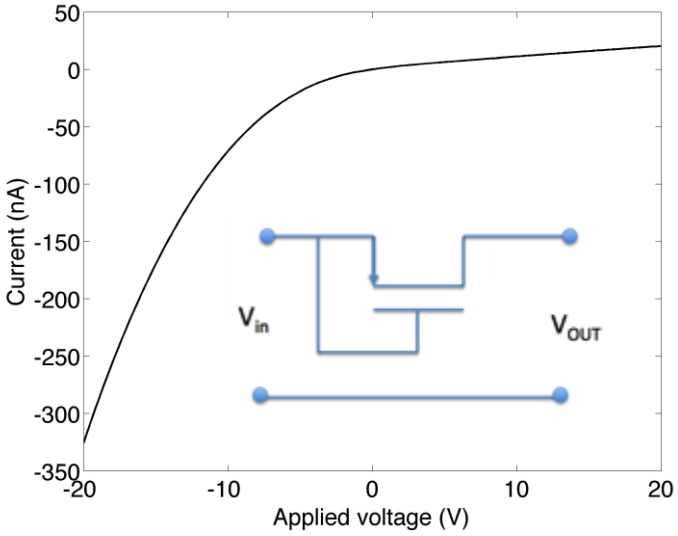


Figure 30. *I-V* characteristic of a diode connected TFT. The Inset shows the circuit configuration. The area of the TFT is 2.5x1.8 mm^2.

Summary

All the diode structures were characterized in rectifying circuits. The conclusions are summarized in Table 6. Only the Schottky diode perform reasonable well at frequencies used in RF tags (13.56 MHz). Both diode connected TFTs and MIS diodes cannot produce rectified DC signals for frequencies above 1 MHz.

Rectifying diode	Characteritics
Schottky diode	Rectification ratio: 200 @|5V| Forward current: 0.3 mA @5 V Reverse leakage current: 0.5 μA SCL conduction: $I \propto V^{\alpha}$ with $\alpha=2$ (Child's law) Area: $1mm^2$
MIS diode	Rectification ratio: 120 @ |10V| Forward current: 0.3 mA @ 10 V Reverse leakage current: 10 μA SCL conduction: $I \propto V^{\alpha}$, $\alpha=[2 - 4]$ Frequency response limited by: the high thickness of the semiconductor layer (carrier transport in the semiconductor) Area: $1mm^2$
Diode connected TFT	Rectification ratio: 25 @ |20V| Forward current: 250 nA @ 20V (Area: 2.5x1.8 mm^2) Reverse leakage current: 10 nA Carrier transport: TFT model $I \propto V^2$ Frequency response limited by the TFT channel length

Table 6. Rectifying diodes characteristics.

3.5.3 Diode model in a rectifying circuit

The non-linear nature of the rectifying process prevents to apply any standard small signal approach. The diode cannot be simulated alone, but together with the load resistance and capacitance in a time dependent approach. The time dependent drift and diffusion equations have to be numerically solved to model the carrier transport within the diode, coupled with time dependent circuit equations. This approach has been developed by Altazin et al. [19] and it is adopted here.

The time dependent operation of the diode is modeled by solving the continuity equation coupled with the Poisson equation.

Considering that applied voltage V_a is related to the input voltage V_{in}. V_0 and the output voltage V_{out} by the following set of equations:

$$V_a(t) = V_{out}(t) - V_{in}(t) \quad (27)$$

$$C\frac{dV_{out}}{dt} + \frac{V_{out}}{R} = i_d(V_{out}(t) - V_{in}(t), t) \quad (28)$$

Where *C* and *R* are the external capacitance and resistance of the rectifying circuit, and i_d the current flowing through the diode.
In the high frequency regime, simulations are time-consuming and a simplified model has been proposed by Altazin et al. [19]. In their approximation the conductance is modeled by a time dependent function G_d (*V*,*t*), responding to the applied signal with a characteristic delay time τ. The dynamic of this response is empirically modeled by the following first order differential equation

$$\frac{dG_d}{dt} = \frac{G_d(V) - G_{do}(V)}{\tau} \quad (29)$$

A good approximation of the characteristic time constant, τ in a unipolar device is proportional to the carrier time-of-flight, given by:

$$\tau = \frac{L^2}{\mu_p(V_a - V_T)} \quad (30)$$

Here V_a represents the applied bias on the diode and V_T, an empirical threshold voltage. *L* is the polymer thickness and μ_p the charge carrier mobility. In absence of traps this threshold voltage simply given by the built in potential. In all case, it can be extracted using the semilogarithmic plot of the static *I*-*V* curve, and its value is equal to the voltage at which the *I*-*V* curve, in the forward regime, is not an exponential anymore.
The basic diode model is basically illustrated in Figure 31 as discussed above the G_d (*V*,*t*), is considered to responding to the applied signal with a characteristic delay time τ as described by equation 30.

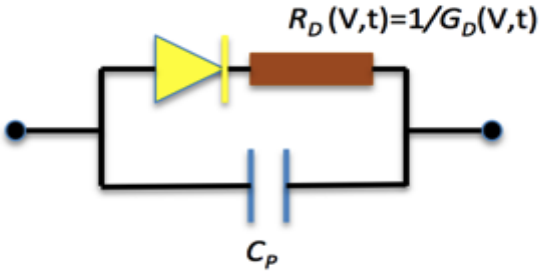


Figure 31. Basic model for a Schottky barrier diode. The resistance is frequency dependent and related with the charge carrier transport limitations at high frequencies.

3.5.4 Parameter extraction procedure

Model parameter	Parameter extraction procedures	Equipment Test vehicle
Parameters required to simulate the diode high frequency response		
Geometric capacitance C_p (F/cm^2)	Measure the capacitance at a resonable high frequency (f >100 kHz) to elminate possible relaxation caused by interfacial effects such as electrode polarization or depletion layer effects.	Impedance Analyzer (Schottky diode)
Threshold volatge V_T (v)	Extracted from the semilogarithmic plot of the static I-V curve, and its value is equal to the voltage at which the I-V curve, in forward bias, is not an exponential anymore.	I-V meter (Schottky diode)
Trap concentration N_t (cm^{-3}) Doping concentration N_a (cm^{-3}) Hole concentration at injecting contact N_h(cm^{-3}) Mobility μ (cm^2/(Vs)) Work function difference between the two contacts Φ (eV)	By fitting the static I-V characteristic of diodes of several thicknesses, fabricated using the same process.	I-V curves of diodes of several thicknesses (Schottky diode)
Cut-off frequency f_c (Hz)	Estimated from the measured V_T and the active diode layer thickness (L). V_A is the applied voltage.	$f_c = \mu \frac{V_A - V_T}{L^2}$
Parameters required to specify the operation point in a rectifier circuit		
Maximum forward current I_{Dfmax} (A/cm^2) Reverse leakage current $I_{leakage}$ (A/cm^2)	Measure the I-V curve in the highest voltage range tolerable by the diode.	I-V meter (Schottky diode)
Reverse breakdown voltage V_{Rmax} (V)	Apply a reverse voltage to cause breakdown or a very high reverse leakage current.	I-V meter (Schottky diode)

Table 7. Summary of the electrical test vehicle and parameter extraction for Schottky diodes.

3.6 Organic Thin Film Transistors (OTFTs) models (new – August Report)

The physical model than conveniently describes the OTFT behavior is the Unified Compact Model and parameter Extraction Method (UMEM) developed by A. Cerdeira and M. Estrada [20-26].

3.6.1 Parameter extraction procedure

The model is a physical based model and allows the extraction of DOS parameters of the organic semiconductor material used in the device. The mobility in OTFTs is based on analytical expressions obtained under the assumption that in all operating range of OTFTs, the concentration of localized charge predominates over free charge. The mobility expression can be written in the form of a power dependence of the gate voltage, allowing the use of the procedure UMEM (Unified model and extraction methodology) to determine all parameters to model the mobility, as well as the electrical characteristics of these transistors. With this method, DOS parameters, considering the typical exponential distribution assumed for OTFTs, can be easily extracted from the transfer characteristic of the device.

In the UMEM model the drain current in the linear region and for $V_{GS} > V_T$ can be written as

$$I_{DS(lin)} = \frac{K}{V_{AA}^{\gamma}}\left(V_{GS} - V_T\right)^{1+\gamma} V_{DS} \qquad (31)$$

Or alternatively in the saturation region

$$I_{DS(sat)} = \frac{1}{2}\frac{K}{V_{AA}^{g}}\left(V_{GS} - V_T\right)^{2+g} \qquad (32)$$

The field effect mobility μ_{FET} is assumed to be given by

$$\mu_{FET} = \mu_0 . \frac{(V_{GS} - V_T)^{\gamma}}{V_{AA}^{\gamma}}$$

Where V_{AA}, K and γ are parameters to be extracted.

$$g = 2\frac{T}{T_0} - 2 \qquad (33)$$

T is the absolute temperature and T_0 the characteristic temperature of the DOS

The energy distribution of the DOS $g_d(E)$, is expressed as

$$g_d(E) = g_{do} \exp\left(\frac{E}{K_b T_0}\right) \qquad (34)$$

where K_b is the Boltzmann constant.

γ can be extracted from the transfer curves (in the linear region) when plotted as: $I_{DS}^{1/(1+\gamma))}$ versus V_{GS}. This can be done by trial and error or by an integration procedure [20,23].

$$H(V_{GS}) = \frac{\int_0^{V_{GS}\max} I_{DSlin}(V_{GS})\,dV_{GS}}{I_{DS}lin(V_{GS})} \qquad (35)$$

Using the measured linear transfer characteristics I_{DSlin} in the integral function, the slope P and intercept of $H(V_{GS})$ are calculated

$$V_T = \frac{Intercept}{P} \qquad (36)$$

and

$$\gamma = \frac{1}{P} - 2 \qquad (37)$$

since

$$\gamma = 2\frac{To}{T} - 2 \qquad (38)$$

T_o is calculated after extracting γ

Using an exponential DOS and considering that $Q_{free} << Q_{loc}$ the following expression for mobility is derived [20-23]:

$$\mu_{FET}(T) = \mu_0.q.k_b.N_V.\varepsilon_s.T\left[\frac{sin(\pi T/T_0)}{2.\pi.q.\varepsilon_s.k_b^2.T.T_0.g_{do}(T)}\right]^{\frac{T_0}{T}}[C_i]^{\left(\frac{2T_0}{T}-2\right)}(V_{GS}-V_T)^{\left(\frac{2T_o}{T}-2\right)} \qquad (39)$$

Which allows modeling mobility as function of temperature and other device parameters.

For parameter extraction, output characteristics at different values of V_{GS} as well as transfer characteristics in linear and saturation regimes are need; nevertheless it is suggested to generate the transfer characteristics from the output ones, so data can effectively match.

Table 8 summarizes all the parameters to be extracted together with recommend procedures.

Extracting and modeling procedures using the Unified Compact Model					
Fixed parameters					
Q	***ε_0***	***k_b***	***$V_{th}= k_bT$***		
$1.6x10^{-19}$	$8.86x10^{-14}$	$8.62x10^{-5}$			
Input data					
Temperature and dimensions	***T*** (K) 300 K	***W*** (cm) $4000x10^{-4}$	***L*** (cm) $40x10^{-4}$	***d_i*** (cm) $1000x10^{-7}$	
Relative dielectric constant of the semiconductor layer in F/cm.					ε_{ir}=2.1
Relative dielectric constant of the semiconductor layer in F/cm.					ε_{sr}=6.5
Density of states at HOMO and LUMO in cm^{-3}.					$N_c=2\ 10^{21}$ $N_v=210^{21}$
Drain voltage at which linear transfer characteristic was measured in volts.					V_{d1}=0.5
Maximum gate voltage, (V_{gsmax}), up to which linear transfer curve was measured.					V_{gsmax}=20
Maximum gate voltage, (V_{gsmaxS}), up to which transfer curve in saturation was measured. It is recommended to use the same value as for the linear transfer curve.					V_{gsmaxS}=25
Drain voltage at which transfer characteristic in saturation was measured.					V_{d2} = 40
Maximum drain voltage, (V_{dmax}), up to which output characteristics were measured.					V_{dmax}=40
Gate voltage for output characteristics.					V_{gs1} =0 V_{gs2} =10 V_{gs3} =20 V_{gs4} =30 V_{gs5} =40
Minimum value of gate voltage to calculate model parameters in linear transfer curve is given by V_{gsmax}-ΔV_{gslin}. Default is ΔV_{gslin}=10					ΔV_{gslin}=10
Minimum value of gate voltage to calculate α is given by V_{gsmaxS}-ΔV_{gsS}. Default for ΔV_{gsS}=10.					ΔV_{gsS}=10
Maximum value of gate voltage to calculate model parameters in linear transfer curve is given by V_{gsmax}-Δ2. Default is Δ2□0.					Δ2□0
Maximum value of gate voltage to calculate model parameters in transfer curve in saturation is given by V_{gsmax}-Δ3. Default is Δ3=0.					Δ3□0
Sequential calculations					
1-	Interpolation of measured linear transfer curves for $V_{DS}=V_{d1}$				
2-	Interpolation of measured transfer curve in saturation, $V_{DS}=V_{d2}$				
3-	Interpolation of measured output curves				
4-	Calculating slope of I_{DS} vs V_{DS} at $V_{GS}<V_T$ between				

	V_{Dmax} and V_{Dmax-2} to correct channel conductivity due to involuntary doping
5-	Interpolation of corrected linear transfer curves
6-	Corrected transfer curves in saturation
7-	Corrected output curves for 4 (or more) V_{GS} values
8-	Calculation of the Modeled Characteristics
9-	Interval V_{GS} (between V_{gs2} and V_{gs1}) where function *H* will be calculated. It is recommended to use values near the maximum measured V_{GS} voltage and select the region where function *H i*s linear.
10-	Input modification to calculate interval. Default value is V_{gsmax}-V_{gsmin}
11-	Estimation of series resistance (*R*) $R1 := \frac{Vd1}{idl1kcor(Vgsmax)} - \frac{1}{\left[K \cdot \mu fet0\,(Vgsmax - Vt)^{\gamma+1}\right]}$ The extraction of *R* in this way is quite approximate. If the resistance is not sufficiently high, it has practically no effect on the characteristics and the extraction method can produce negative values. In those cases the resistance is taken to be zero. However, sometimes devices have very high *R* and it must be taken into account for precise modeling.
12-	Calculation of parameter α_s. $Ps := slope(ks1, ips1)$ $\alpha s := \frac{Vaa^{\gamma}}{K} \cdot Ps^{2+\gamma} \cdot \sqrt{2}$
13-	Calculation of parameter *m*. $m := \frac{\log(2)}{\log\left[K \cdot \mu fet0 \cdot \frac{\left[\left(\frac{VDsat}{\alpha s}\right)^{1+\gamma} \cdot \frac{VDsat}{iDsat}\right]}{\left[1 + \left[R \cdot (K \cdot \mu fet0) \cdot \left(\frac{VDsat}{\alpha s}\right)^{(1+\gamma)}\right]\right]}\right]}$
14-	Calculation of parameter λ.

	$$\lambda := \frac{\frac{i2}{V2^2}}{K\cdot\mu fet0\cdot\left(\frac{VDsat}{\alpha s}\right)^{1+\gamma}} - \frac{}{\left[1+\left[R\cdot(K\cdot\mu fet0)\cdot\left(\frac{VDsat}{\alpha s}\right)^{(1+\gamma)}\right]\right]\cdot\left[\left[1+\left(\frac{V2}{VDsat}\right)^{m}\right]\right]^{\frac{1}{m}}}$$
15-	Calculation of the corrected currents. $$idc(Vgs,Vds) := \frac{K\cdot\mu fet0}{\left[1+\left[R\cdot(K\cdot\mu fet0)\cdot(Vgs-Vt)^{(1+\gamma)}\right]\right]}\cdot\frac{(Vgs-Vt)^{1+\gamma}\cdot Vds\cdot(1+\lambda\cdot Vds)}{\left[1+\left[\frac{Vds}{\alpha s\cdot(Vgs-Vt)}\right]^{m}\right]^{\frac{1}{m}}}$$
16-	Comparison of modeled and corrected measured characteristics.
17-	Comparing modeled with experimental curves.
18-	Calculation of the characteristic temperature. $$T2 := \frac{1}{P}\cdot\frac{T}{2}$$ $$T2 = 348.75$$ $$ffc := \left(\frac{1}{Vaa}\right)^{\left(\frac{2T2}{T}\right)-2}$$
20-	Calculation of the density of states g_{do}. $$FF1 := \left[\frac{Ci^{\left[\left(2\cdot\frac{T2}{T}\right)-2\right]}}{es^{\left[\left(\frac{T2}{T}\right)-1\right]}\cdot(2\cdot kb\cdot T2)^{\frac{T2}{T}}}\right]$$ $$FF2 := q\cdot Nv\cdot(kb\cdot T)\cdot\left[\frac{\left(\sin\left(\pi\cdot\frac{T}{T2}\right)\right)}{\pi\cdot((kb\cdot T)\cdot q}\right]^{\frac{T2}{T}}$$ $$gdo := \left(\frac{FF1\cdot FF2}{ffc}\right)^{\frac{T}{T2}}$$

EXTRACTED PARAMETERS							
V_T	γ	V_{aa}	T_o	R_c	α_s	λ	μ

Table 8. Parameter extraction using the Unified Compact Model and parameter Extraction Method (UMEM).

The so call contact resistance (R_C) deserves some attention. Due to the presence of contacts, the self organization process of molecules is disrupted and hence, very small grains and even voids are formed at the contact edges, resulting in a large number of traps which capture the passing carriers and significantly reduce the carrier mobility in the contact region, manifesting as higher contact resistance. Contact resistance can also be modeled by using a non-linear voltage dependent resistance.

3.6.2 Parasitic effects

There are number of parasitic effects which can lead to errors in the estimation of intrinsic TFT parameters. The most common one is fringing currents flowing on the surface of the organic semiconductor and near the interdigitate silver electrode array. Fringing currents may become important for small transistors operating under high bias. This effect is reflected in the saturation region of the output characteristics, which will display a finite and decreasing output resistance (increasing slope) as *W* and *L* decrease to lower values [27].

Contact pads and silver tracks that connect the interdigitate source and drain electrodes may cause also additional parasitic currents. When the dielectric is not patterned these metal lines can create an additional very large TFT in parallel with the one being measured.

Printed electrodes are not perfect straight lines. The small fluctuations in the channel length may cause variations of the electric field between drain and source electrodes.

These and other parasitic effects will be inspected and quantified by measuring TFTs with different sizes and different layout designs. Once quantified the parasitic effects will be added to the TFT model.

Parameter	Measurement procedure	Comments
γ (gamma)	Find γ required to linearize the transfer curve. Plot $I_{DS}^{\frac{1}{1+\gamma}}$ versus V_{GS} If the *I-V* curves do not show a distortion near the origin caused by contact effects the linear region is recommended.	The γ parameter is related with the number of immobile charge density. Therefore, is most determined by the fabrication procedures. Does not depend on gate bias-stress. Contamination from environment may change it with time.
Threshold Voltage (V_T)	V_T is defined as the intercept of the linear $I_{DS}^{\frac{1}{1+\gamma}}$ versus V_{GS} curve if linear region is region is used. For saturation region use $I_{DS}^{\frac{1}{2+\gamma}}$ versus V_{GS}.	The measurements must be carried out in unstressed OTFTs and in dark conditions.
Field effect mobility (μ_{FET})	Once γ is extracted then mobility is estimated from the equation: $m_{FET} = m_{FET0}(V_{GS} - V_T)^g$	
Parasitic contact resistance (R_C)	It is a voltage dependent resistance required to fit the *I-V* curves on the low bias V_{DS} region. It can be obtained by fitting the *I-V* curves, or as described in Table 7	It depends essentially on the trap concentration. Therefore, is most determined by the fabrication procedures.
Off-current (I_{OFF})	Measure I_{DS} in saturation for V_{GS}= 0 V	The initial value is mostly determined by the organic semiconductor layer thickness and doping. It may evolve with ageing, gate-bias-stress and atmospheric contamination.
Leakage current across the gate dielectric (I_G)	Measure the gate current at a particular gate voltage (V_{GS}= -20 V)	

Table 9. Experimental OFET parameters and measurement procedures.

In addition to these physical parameters listed in Table 9, there is also variability on the geometrical parameters namely on the channel width (*W*), channel length (*L*), and insulator thickness (d_I). Variability on the internal geometric capacitances is also important for OTFT dynamic behavior.

4 Designing experiments by Input Sampler

4.1 Introduction

INFINISCALE holds a technology to design experiments. This technology aims to explore as optimized as possible the multi-dimensional space of input parameters with a sphere filling-like algorithm.

4.2 Optimal experiment design

All the modeling approach needs experimentation that could have high cost and users want to efficiently choose which experimentations those have to be done. Some optimal experiment design (OED) can be combined with modeling approach to design efficiently the experimentation database. The term efficient could have different meaning depending on which OED we focus on. In general for a given confidence level on the model, the designer wants to minimize the number of experimentation.

The optimized samples in the experimentation database could be just elaborated from physical knowledge[8] and in some techniques more optimized when model prototype is given. In some modeling technique (such as design of experiment) the whole given database is necessary to elaborate model and depend of model prototype and in other more flexible approaches the database is just suggested and not necessarily optimized for one model prototype.

4.3 Generating new experiments

User only needs to specify their input parameters and ranges of variation. InputSampler will manage samples generation by guaranteeing a best distribution of your samples in N-dimension. Figure shows how input sampler generates new samples (red points) based on precedent ones (blue points) by regularly distributing them in multi-dimensions space.

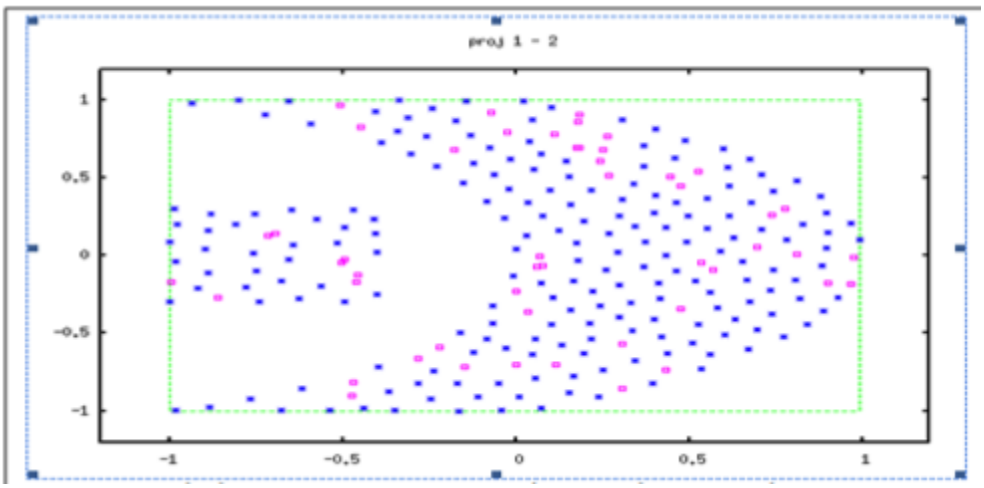


Figure 32. Incremental input sampler.

[8] in most of the cases the role of physics knowledge consist of defining and/or limiting the parameter space domain of interest and specifying experimentation protocols

Please note that input sampler can be very efficient for validation. As it guarantees a good distribution of the new generated samples depending on the existing ones, these new samples can be used to validate the models in an external validation.

Based on data provided by ENEA on the fabricated OTFTs, the results of modeling are shown in Figure .

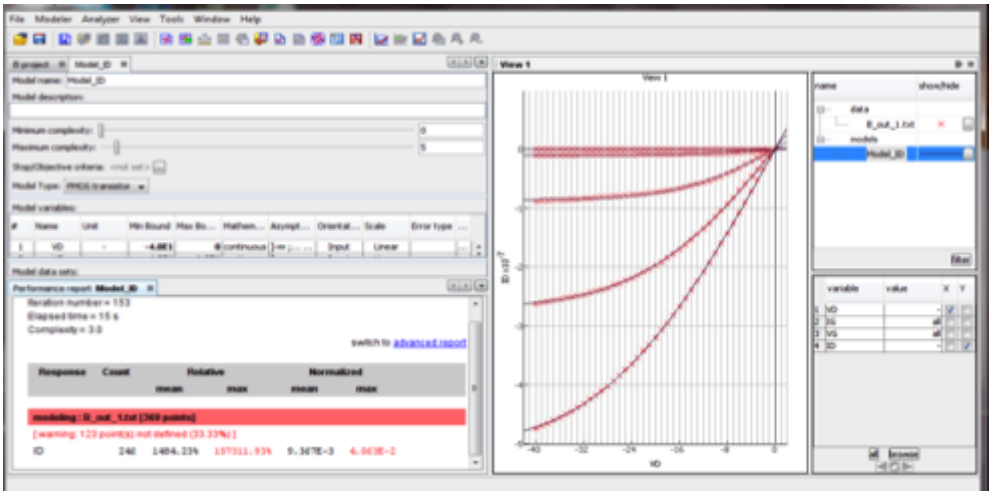


Figure 33. Modeling ENEA OTFT

The same data have been used for the semi-physical modeling method (Figure). Fitting seems to be very good between measurements and the resulting analytical model. This model has been exported into Verilog-A format in order to use into spice simulators.

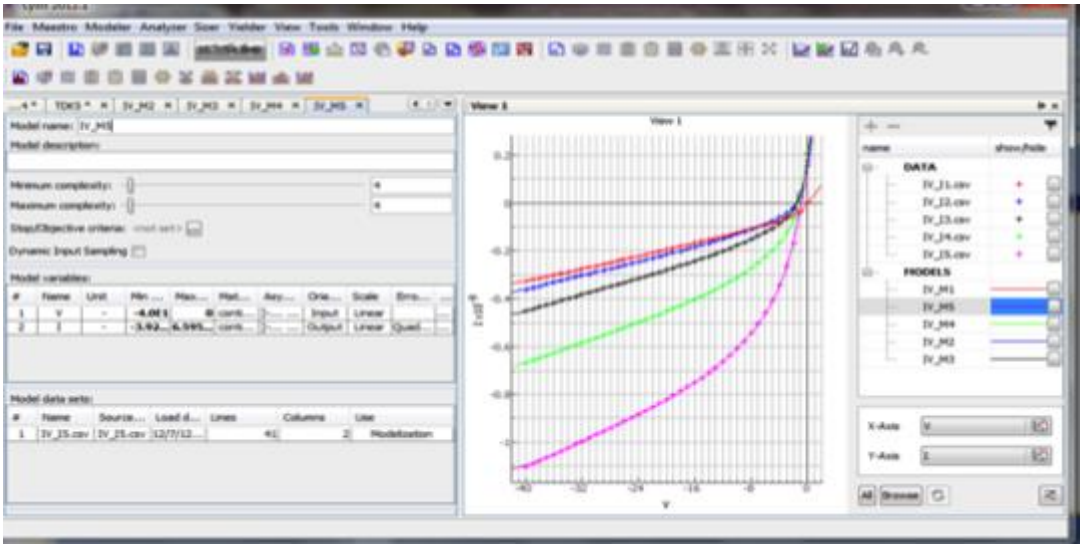


Figure 34. Semi-Physical modeling of OTFTs data.

4.4 Modeling trial of the horizontal linear resistor LR01

Modeling shows R as function of L and W (curves in blue) where red points are the measurements. However, printing variations make that even if we intend to print the same dimensions, variability impacts the printed resistors.

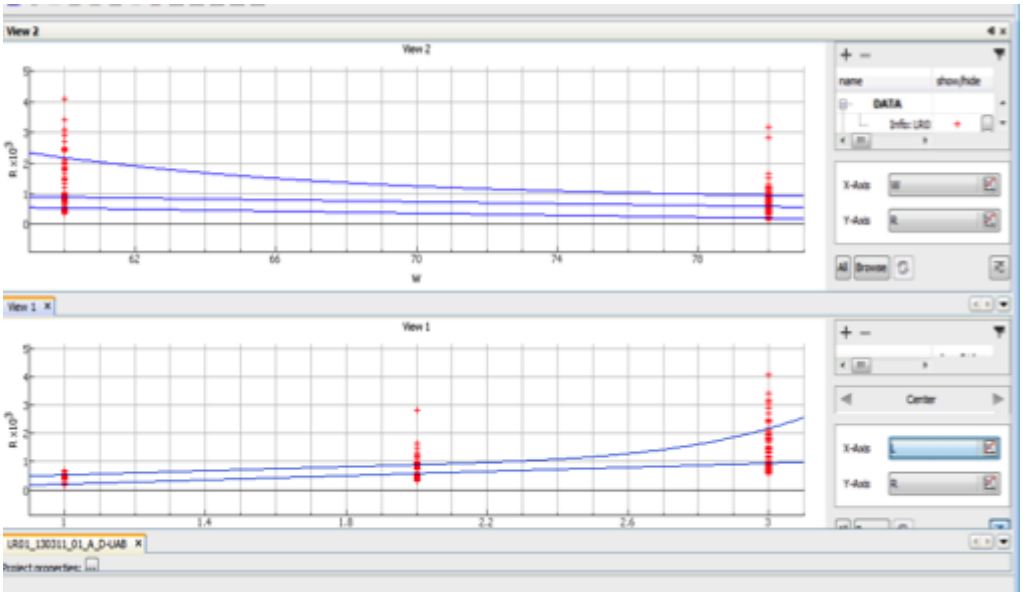


Figure 35. Variability curves for LR01_A_130405_01_D-UAB_130423

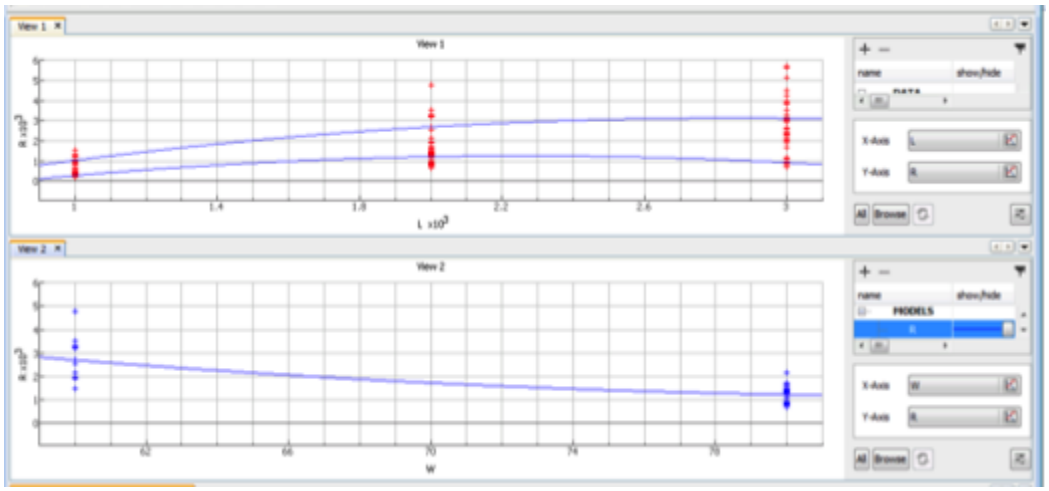


Figure 36. Variability curves for LR02_130321_01_A_D-UAB

5 Validation

5.1 Blind validation

Data set (measurements) are divided into two subsets: one for modeling and the other for validation. The first subset, the modeling data, is used to fit the phenomena. The modeling process does not see the validation data. The second subset is then used only for validation. Generally, validation data subset size should be 10 to 20% of the whole data set.

Through modeling operation, an error report is displayed showing errors on the 2 subsets. This report includes global mean and maximum error (for different kind of errors) and more detailed error statistics for each loaded datasets and each output variable of the model.

After modeling a model performance report of computed model can be obtained.

This report describes modeling error for different kind of error (quadratic, relative and normalized error) and for the different data sets and areas of data. This report contains a summary of mean and maximum error for each data set, areas and each output variables.

The following figure (Figure) shows that the modeling data in green and the validation one in red. Red curve is not seen by the modeling process.

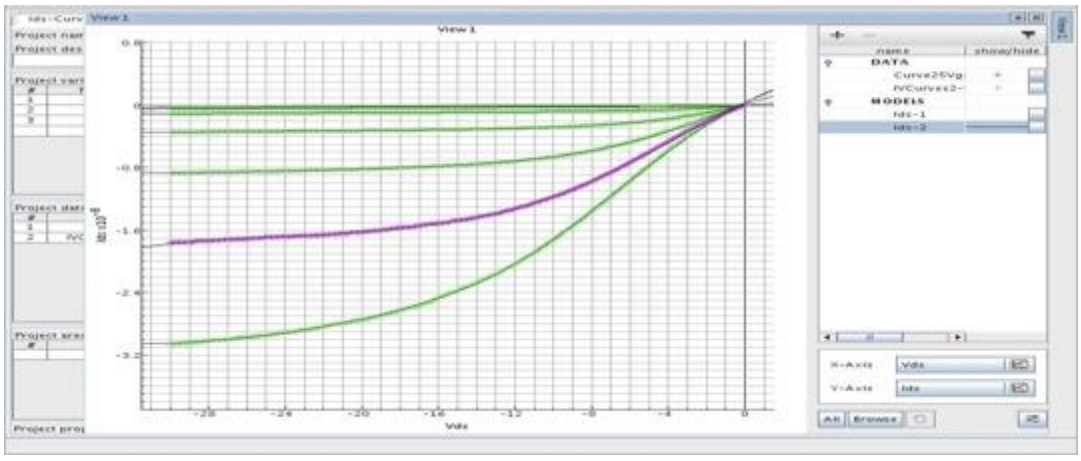


Figure 37. Semi-Physical modeling of OTFTs data.

The following snapshot (Figure) shows in red the error report on modeling data and in blue the errors on validation data. One can see the relative and the normalized errors on the modeling (green curves) and validation (red curve).

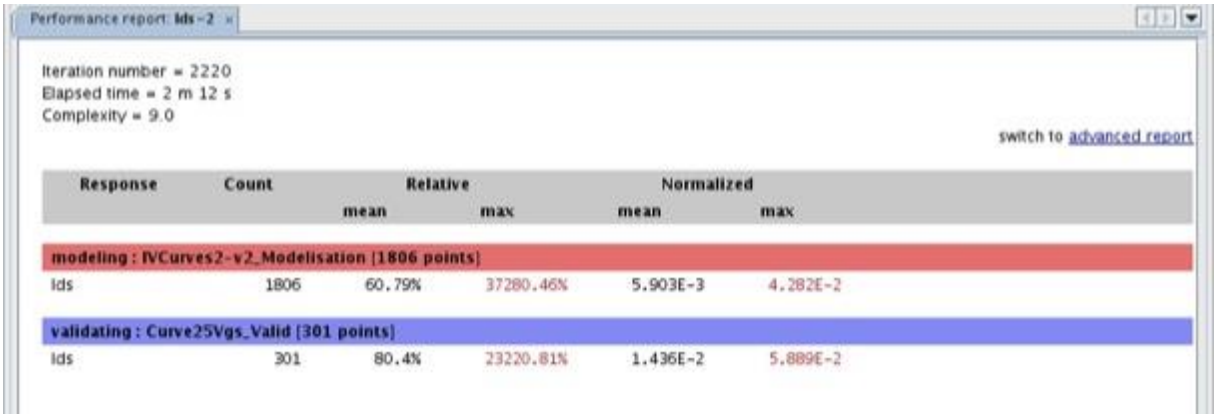


Figure 38. Error report on modeling and validation data.

5.2 Viewing models behavior

At first validation level the physician can view the new created models. He will be able to see if curves represent what he was expecting from his knowledge of the physical phenomena.

5.3 Validation based on new printed samples

Once models are generated, they can be used for extrapolation. New samples can be generated (thanks to the input sampler) and the models are called to provide their performances.

These samples can be printed and then comparison can be done between model-based performances and lab measurements.

5.4 Models Validity & export

The model is valid in the range extracted from the given data. The model is guaranteed within this range. However, the Input Sampler can be used to generate samples within given ranges for all parameters. Input Sampler generates optimized data base and enable the modeler to create validated models on these ranges. The input sampler has many advantages as optimizing the needed samples, better coverage and better validation.

Models are exported in various formats such as c-coded program or Verilog-A.

6 Dynamic modeling

INFINISCALE will develop templates for each device in order to integrate dynamic behavior to generated models. The model that has been already delivered in Verilog-A format was integrating the dynamic. So when exporting the models, the dynamic is automatically added.

The strategy is to have a template for each device.

Here after is a sample of an already delivered Verilog-A model.

```
`include "disciplines.h"
module tm_trans_pmos_id(D,G,S);

 `include "tm_ids_curve2_ids_function.v"

 inout D, G, S;
 electrical D, G, S;
 real id;
 real vd, vg;

 analog begin

  vd = V(D,S);
  if (vd > 0) begin
   vg = V(G,D);
   vd = V(S,D);
   id = -tm_vlg_ids_curve2_ids(vd, vg);
  end
  else begin
   vg = V(G,S);
   vd = V(D,S);
   id = tm_vlg_ids_curve2_ids(vd, vg);
  end

  I(D,S) <+ id;
 end
endmodule
```

```
[VERILOG-AMS Module]
 NAME = tm_trans_pmos_id
 SOURCE = tm_trans_pmos_id.va

[Ports]
(PORT TERMINAL  D  INOUT
electrical )
(PORT TERMINAL  G  INOUT
electrical )
(PORT TERMINAL  S  INOUT
electrical )
[Declarations]
(BRANCH  D,S )
(BRANCH  G,D )
(BRANCH  G,S )
```

```
analog function real
tm_vlg_ids_curve2_ids;
input Vds;
real Vds;
input Vgs;
real Vgs;

[...]
begin
[...]
x17 = (-2.4929409568106327E-9) +
(x16) * (3.0588790784003937E-9);

tm_vlg_ids_curve2_ids = x17;

end

endfunction
```

7 Variability

Having defined the parameters and their extraction procedure, large number of measurements will be carried out to quantify variability. The statistical distribution of each parameter is then provided to the simulation models described above.

Variability in OTFTs is more acute than in silicon-based technologies by an inherently much higher parameter spread. Reasons for that, include, irregular morphology of the semiconductor, difficulty in controlling the precise dimensions of OTFTs, immobile trapped charges in the dielectric, uneven material deposition, roughness of the semiconductor-gate dielectric interface which leads to mobility variations between the different transistors.

Furthermore, it is important to have in mind that *I-V* characteristics of OTFTs are known to change with the application of prolonged voltages, i.e. bias-stress effect, which leads to operational instability. This means that measurements procedures can introduce extrinsic variability on the OTFT parameter. (V_T may depend on the history, of the device, ambient light and setting parameters to record the OTFT electrical characteristics)

Accurate and efficient characterization of the different types of variation requires a large number of measurements on a variety of devices, layout styles, and environments. Most important it also requires:

1. A physical model that can unambiguously define the parameters to be extracted.
2. A fixed and harmonized procedure for parameter extraction that minimizes extrinsic causes for variability.

7.1 Variability Management

7.1.1 Variability management on mathematical models

INFINISCALE modeling is able to take into account the measurement variability. To consider variability in this case, this could be done in different ways:

1. Modelize a kind of envelope that delimits the variability range of each model (Figure)

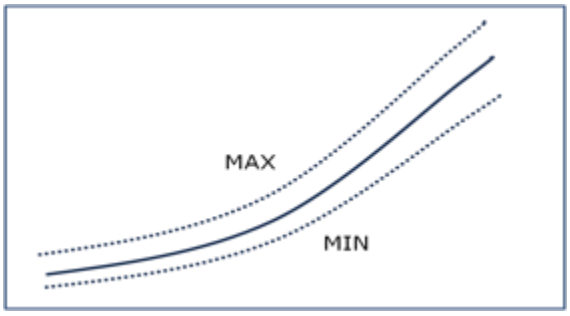


Figure 39. Managing Variability by MIN/MAX modeling.

2. Or to add statistical distributions of technological parameters. In this case, many measurements should be repeated on the same device to capture variations.

7.1.2 Variability management on physical models

Physical models should represent variability. Here after some examples, extracted from a free 45n DK, showing how variability is expressed:

```
** FREE PTM 45nm MOS Library
** GLOBAL Variability

.LIB PTM45_STAT
.PARAM NTOXP_CMOS045 = AGAUSS(0.0, 1.0)
.PARAM NTOXM_CMOS045 = AGAUSS(0.0, 1.0)
...
// NTOXP_CMOS045 is define as a Gaussian distribution with 0 as mean and sigma =1
// NTOXM_CMOS045 is define as a Gaussian distribution with 0 as mean and sigma =1
.LIB "ptm45.lib" PTM45_EQ
.LIB "ptm45.lib" PTM45_MODEL
.ENDL

.LIB PTM45_EQ
.PARAM NMOS_TOXP = '1.10e-09 + 5.0e-11 * NTOXP_CMOS045'
.PARAM NMOS_TOXM = '1.75e-09 + 5.0e-11 * NTOXM_CMOS045'
...
.ENDL

** LOCAL Variability
.LIB PTM45_MODEL
.SUBCKT NPTM45 D G S B
+       W=50 L=50 MULT=1
.PARAM TOXE_CMOS0451 = AGAUSS(0.0, 1.0)
// TOXE-CMOS0451 is define as a Gaussian distribution with 0 as mean and sigma =1

.PARAM NMOS_TOXE = '1.75e-09 + 5.0e-11 * TOXE_CMOS0451'

.PARAM TOMETER = 1.0e-9

.PARAM XL = 'L * TOMETER'
.PARAM XW = 'W * TOMETER'

M1 D G S B NMOS W='XW'L='XL' M='MULT'

.model  NMOS  nmos  level = 54
……..

* parameters customized by the user
+toxe = 'NMOS_TOXE'    toxp = NMOS_TOXP     toxm = NMOS_TOXM     toxref = 1.75e-09
+dtox = 6.5e-10    lint = 3.75e-09
…

.ENDS
```

Statistical distributions are used by the spice simulator Monte Carlo (MC) analysis to achieve different simulations by picking up for each parameter (defined with statistical distribution) a new value following its PDF (Probability Density function).

The Monte Carlo procedure is the following:

1. Define inputs as probability distributions
2. Generate inputs values as randomly from a probability distribution.

3. For each inputs vector (which is deterministic) perform the computation
4. The operation is repeated depending the number of required MC runs

Statistically talking, the number of MC runs should be big enough in order to guarantee acceptable accuracy.

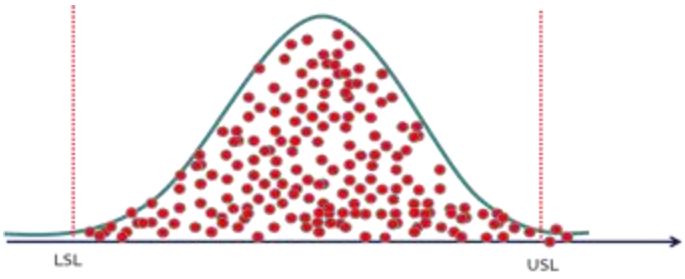


Figure 40. Monte Carlo sampling.

7.2 Strategy to cope with variability and yield

The basic idea to cope variability is to introduce additional parameters to model what could explain the diverse variability effects. These additional parameters will be of two forms:

(a) Physical parameters. The values of these parameters will be extracted from the measurement curves. Their probability density functions (pdf) will be estimated from these data. The pdf estimation parameter will be simple Gaussian/uniform distribution or based on a weighted sum of Gaussian/uniform distributions.

(b) Mathematical parameters. These parameters will be pure mathematical variables that help to reduce residual error between model (without variability) and measurement data. The pdf will also be estimated from this residual error.

7.2.1 One model per transistor dimension

The current inkjet process developed in our project, has still a limited yield. This forced us to take a strategy oriented to optimize the yield by restricting the size of the transistors to those that show better yield often related to better morphological results (according to coffee ring effects, etc.).

This lets to the use of a limited number of transistors dimensions. This strategy is even best suited for the inherent regularity of the Inkjet Gate Array architecture, and let us to look for models in which W and L are fixed parameters.

In this case, statistical analysis will manage inherent variability to provide the physical and/or mathematical parameters.

For Infiniscale semi-physical model (see section 9.1.1), additional parameters are already supported by the tool, and the tool will provide VerilogA models for the transistor current

in the form I(VT, VG, X1, X2, ...) where X1, X2, ... are additional physical or mathematical parameters.

For UCM physical model, the additional physical parameters are already incorporated, and the mathematical parameters will be added in the equation when there is a lack of accuracy of the model. Then, this new equation will be edited and optimized in the modeller tool presented previously.

7.2.2 General model for OTFTs

For a general model integrating the dependency on transistor dimensions, the process parameter of form (b) must be carefully defined to be pertinent for all the various dimension of the transistors.

Then, for Infiniscale semi-physical model, the length/width will be considered as parameter in the tool (as in section 8.2.1) and the behavioral modeling tool will automatically link these new variables with output data.

For UCM physical model, we need to consider the interaction (if any) of transistor dimension and parameter of form (b) in the equation. And thus the impact of dimension on residual error between model (without variability) and measurement data must be carefully studied.

7.2.3 Preliminary example of the application of the UMEM model to simulates I-V characteristics of OTFTs produced within the TDK4PE consortium

Figure shows a transfer curve of typical OFET fabricated and characterized by the TDK4PE consortium. The OFET uses a solgel dielectric layer provided by Sun Chemical and as active semiconducting layer a blend of a soluble small molecule organic semiconductor and a polymeric additive designed to control the crystallization of the semiconductor upon film formation. This blend is named FS 0013 and is provided by Flexink. The transfer curve was measured in the linear region. In contrast to a trap-free OTFT the curve is not linear as expected. Therefore, neither the mobility (μ) neither the threshold voltage (V_{th}) can be unambiguously determined.

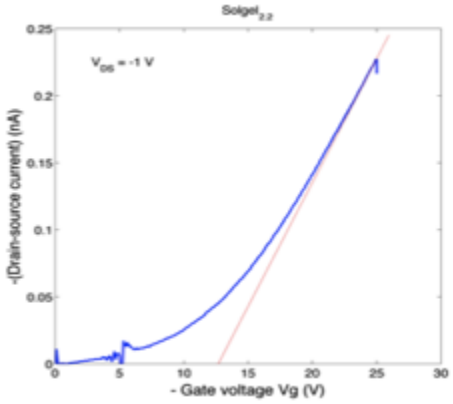


Figure 41. Transfer curve measured in the liner region (V_{DS}= -1V)

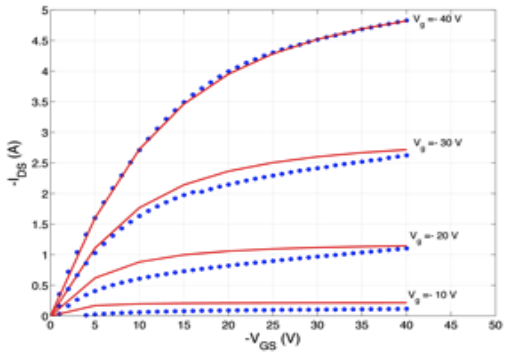


Figure 42. Comparison between experimental (dotted line) and simulated (full line) *I-V* characteristics using the UMEM model

The fact that transfer curve is not linear is taken into account by the UMEM model trough a parameter γ. Gamma (γ) is a parameter that takes into account how far the OFET deviates from a trap-free OFET. The non-linear behavior is due to the presence of traps.

The output characteristics also suffer from "contact effects" as explained previously these effect can be take into account by adding a voltage dependent contact resistance. These effects have not being considered in this particular fit, for this reason the fitting is not perfect for all the curves. TFT parameters extracted from the simulation of the output I-V curves are shown in Table 10.

TFT parameters						
μ	γ	(V_T)	Sharpness of Knee region parameter (m)	Saturation parameter (α) $V_{SAT}=\alpha\ (V_{GS}-V_T)$	Channel length modulation parameter (λ)	Contact resistance (R_C)
$1x10^{-4}$ ($cm^2/(Vs)$)	0.9	-2.55 (V)	1.27	0.39	$-3.5e^{-3}$ (1/V)	0

Table 10. TFT parameters extracted from the simulation of the output *I-V* curves

Physical parameters used are *W/L*=1000/30, dielectric thickness (d_i) = 1 μm, C_{ox} = 2.3 nF/cm^2. The OFET was fabricated using printed layer of a solgel dielectric and FS 0013 as a semiconductor.

8 Methodology proposed inside TDK4PE

Variability and design verification could be done by Pre-defined Corners (PDC). However, PDC proved to be no more sufficient for new nanometer nodes for silicon electronics where number of impacting parameters became huge and physical impact became highly non linear. This is exactly why Monte Carlo analysis has emerged as a suitable technique for variability treatment. But, MC analysis is time consuming especially for long-simulated designs, which pushed for the need to new MC analysis as Fast Monte Carlo recently introduced.

Anyway, both techniques could be studied within TDK4PE and the most suitable will be selected.

The next schema (Figure 43) shows the involved groups and their responsibilities for variability management taking into account all the steps of the chain and the different WP activities.

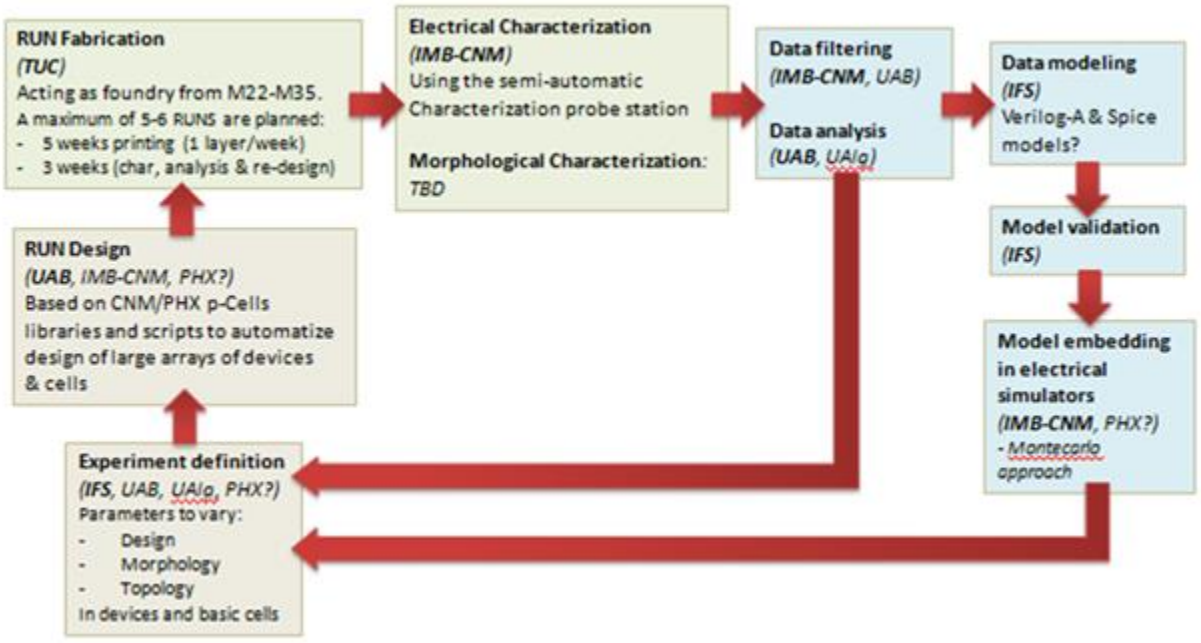


Figure 43. Managing variability within the consortium

8.1 Integrated models

8.1.1 Infiniscale Semi-physical model

What is called Infiniscale semi-physical modeling is based on mathematical function plus information that physician can provide to guarantee that the generated model respect physical aspects.

To be noted that this model doesn't provide mobility or threshold voltage information, only the drain current as a function of drain and gate voltages (and potentially other parameters, if provided, as for example length, width of transistors, ...).

The "physical" information/constraints integrated in these models concern (mainly) the monotony, asymptotic behavior, cross of zero of the curves but not physical parameter (that are used in common physical model). Note that this drain current function (compiled in verilog-A) is sufficient to simulate the circuit [17].

8.1.2 UCM Semi-physical model

Infiniscale's extractor GUI has been developed (Figure). Infiniscale team is also working on the integration of UCM models.

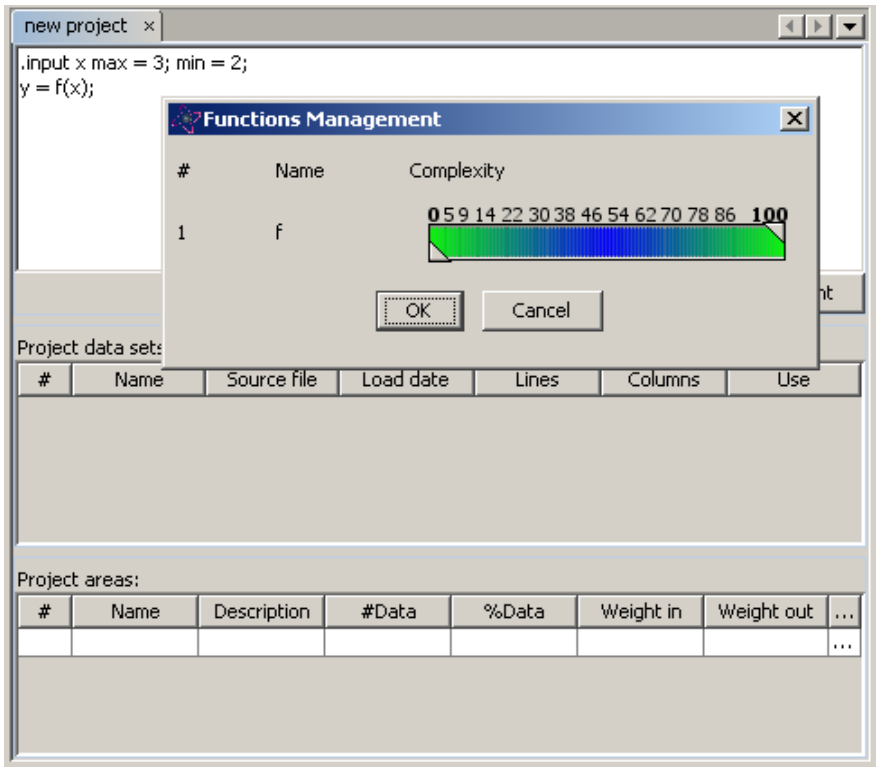


Figure 44. Semi-physical GUI

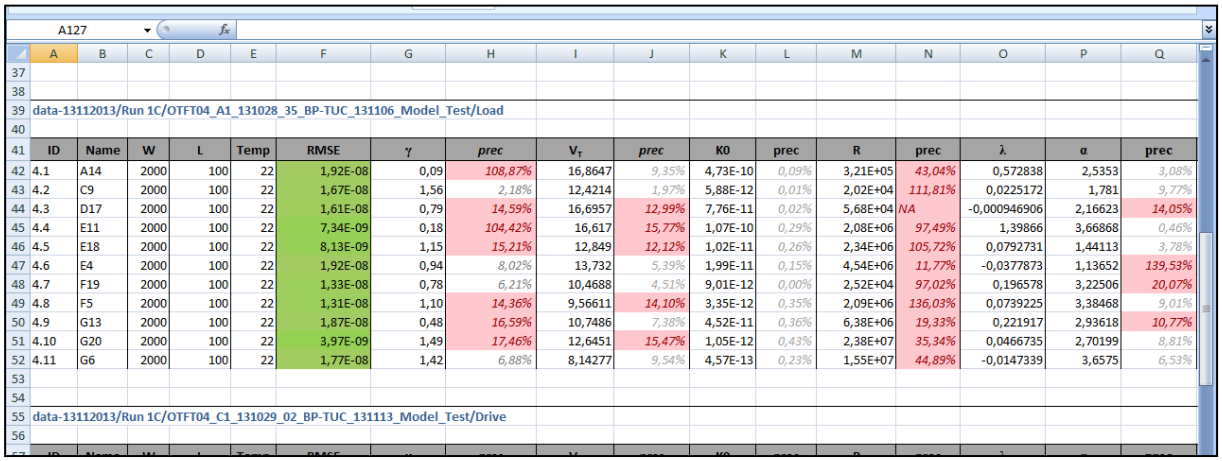
8.1.3 UCM parameter extractor

The tool for UMEM model parameter extraction has been developed according to extraction procedure described in 3.6.1. This tool can be run in batch mode on all available the measurements and provides as result a table with the following information:

- Extracted parameter value for each transistor: parameter such as voltage threshold, mobility, ... (see 3.6.1) are reported
- Uncertainty of the parameter regarding the extraction process: for each extracted parameter the precision about the extracted parameter is given as a percentage.

- Goodness of fit indicator of UCM model versus measurement: the Root Mean Squared Error (RSME) indicator is listed in the results and measure the discrepancy between the model and the measure.

The snapshot below shows some of the extractor results imported in an excel spreadsheet.



	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q
37																	
38																	
39	data-13112013/Run 1C/OTFT04_A1_131028_35_BP-TUC_131106_Model_Test/Load																
40																	
41	ID	Name	W	L	Temp	RMSE	γ	*prec*	V_T	*prec*	K0	prec	R	prec	λ	α	prec
42	4.1	A14	2000	100	22	1,92E-08	0,09	*108,87%*	16,8647	*9,35%*	4,73E-10	*0,09%*	3,21E+05	*43,04%*	0,572838	2,5353	*3,08%*
43	4.2	C9	2000	100	22	1,67E-08	1,56	*2,18%*	12,4214	*1,97%*	5,88E-12	*0,01%*	2,02E+04	*111,81%*	0,0225172	1,781	*9,77%*
44	4.3	D17	2000	100	22	1,61E-08	0,79	*14,59%*	16,6957	*12,99%*	7,76E-11	*0,02%*	5,68E+04	*NA*	-0,000946906	2,16623	*14,05%*
45	4.4	E11	2000	100	22	7,34E-09	0,18	*104,42%*	16,617	*15,77%*	1,07E-10	*0,29%*	2,08E+06	*97,49%*	1,39866	3,66868	*0,46%*
46	4.5	E18	2000	100	22	8,13E-09	1,15	*15,21%*	12,849	*12,12%*	1,02E-11	*0,26%*	2,34E+06	*105,72%*	0,0792731	1,44113	*3,78%*
47	4.6	E4	2000	100	22	1,92E-08	0,94	*8,02%*	13,732	*5,39%*	1,99E-11	*0,15%*	4,54E+06	*11,77%*	-0,0377873	1,13652	*139,53%*
48	4.7	F19	2000	100	22	1,33E-08	0,78	*6,21%*	10,4688	*4,51%*	9,01E-12	*0,00%*	2,52E+04	*97,02%*	0,196578	3,22506	*20,07%*
49	4.8	F5	2000	100	22	1,31E-08	1,10	*14,36%*	9,56611	*14,10%*	3,35E-12	*0,35%*	2,09E+06	*136,03%*	0,0739225	3,38468	*9,01%*
50	4.9	G13	2000	100	22	1,87E-08	0,48	*16,59%*	10,7486	*7,38%*	4,52E-11	*0,36%*	6,38E+06	*19,33%*	0,221917	2,93618	*10,77%*
51	4.10	G20	2000	100	22	3,97E-09	1,49	*17,46%*	12,6451	*15,47%*	1,05E-12	*0,43%*	2,38E+07	*35,34%*	0,0466735	2,70199	*8,81%*
52	4.11	G6	2000	100	22	1,77E-08	1,42	*6,88%*	8,14277	*9,54%*	4,57E-13	*0,23%*	1,55E+07	*44,89%*	-0,0147339	3,6575	*6,53%*
53																	
54																	
55	data-13112013/Run 1C/OTFT04_C1_131029_02_BP-TUC_131113_Model_Test/Drive																
56																	

These extracted parameters can then be exported as a spice library file. The following sections are defined in this library file:

- Library section for each individual transistor: these sections for each transistor report the extracted parameters of one transistor (e.g. A14 in the previous table). One specific transistor can thus be simulated
- Library section for lot of transistor: these section report "average" model parameter for a given lot of transistors.

  These sections also incorporate deviation on the mobility and threshold voltage parameter of the transistor inside this lot. These deviations are then combined with random variable in spice library to make possible monte carlo simulation.

The following snapshot gives a partial view of the spice library for ELDO simulator.

```
* otft_ucm-eldo.lib file
[…]
*********************************
* Section to include UCM verilogA model
.lib otft_ucm_va_model
  .hdl model_otft_ucm_pmos.va
  .model model_otft_ucm_pmos macro lang=veriloga
.endl
[…]

*********************************
*   Section of extracted parameter and model for
*     lot 1:  data-05112013/Drive OTFT04_C2_130916_141-TUC_131029_different Vd
.lib otft_ucm_lot1

  * device model
  .subckt otft_ucm_pmos_lot1 D G S W=14000 L=100

    * nominal parameters
    .param e_W=14000
    .param e_L=100
    .param e_Vt=13.892
    .param e_gamma=0.47036
   […]
    * monte carlo parameters
    .param e_gamma_dev=0.39572
    .param e_gamma_mc0=agauss(0,1,1)
    .param e_gamma_mc=e_gamma+e_gamma_dev*e_gamma_mc0
   […]
    X1 D G S model_otft_ucm_pmos W=W L=L
+       Vt=e_Vt_mc gamma=e_gamma_mc K0p=e_K0p R=e_R
+       alpha=e_alpha m=e_m lambda=e_lambda
  .ends
.endl

[…]
```

8.2 Devices Examples

8.2.1 Load and Drive OTFTs

Two models for load (Figure) and drive (Figure) OTFTs have been generated. Load and drive names correspond to current pseudo-PMOS cell design style naming. Models are ID(VD, VG) were range of VD and VG are between [-30V, 0V]. Models were exported to verilogA for spice simulation purposes.

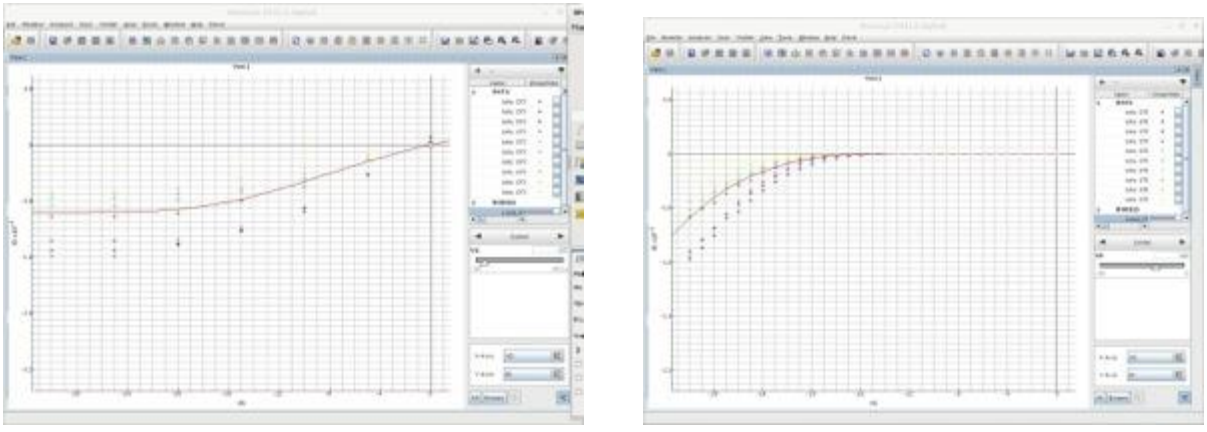


Figure 45. Load OTFT: ID-vs-VD and Load OTFT ID vs VG

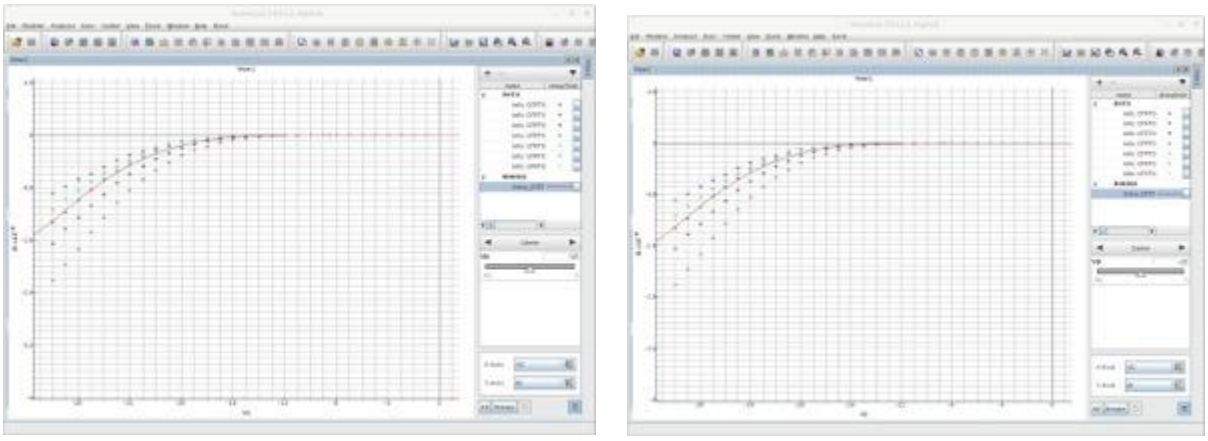


Figure 46. Drive OTFT modeling: ID vs VD and ID vs VG

8.2.2 Integration in the TDK4PE framework

Verilog-A models have been integrated in the TDK4PE framework by inserting them in the NGspice simulator. In order to verigy the validity of the simulation models together with the simulation tool we alse performed the simulation using CADENCE.

Figure 47 shows the plots of those simulations for a couple of transistors (g2 and a21 from different rectangles). We have compared these two samples with the extraction data and they fit.

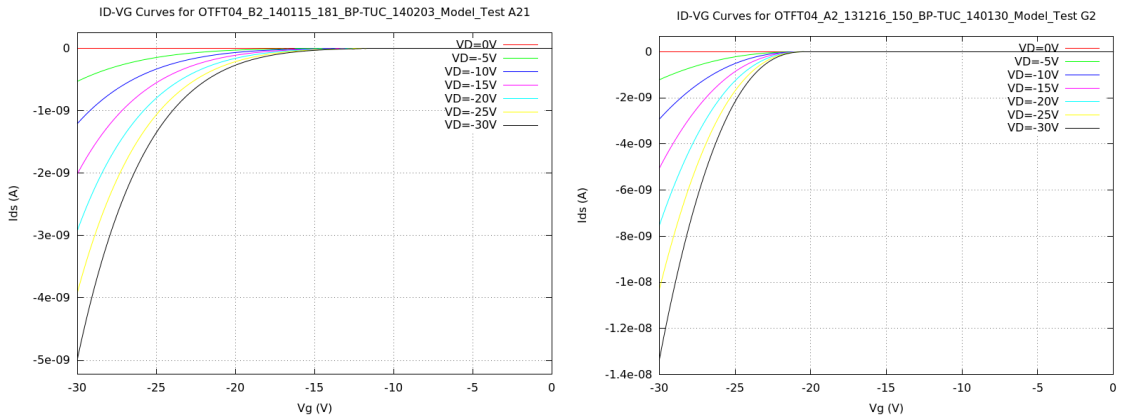


Figure 47. Plots of OTFT curves simulated in NGspice using the Verilog-A models.

8.3 Circuits Example

8.3.1 Inverters and Ring Oscillator

A three-step ring oscillator using the latest models provided by Infiniscale has been simulated. However, good results could not be obtained.

Inspecting the inverters made using the 'drive' and 'load' transistor models, a quite poor performance for the transfer curve has been observed due to the low transistor transconductance.

Attached you can find two graph (figure 48) showing the inverter transfer curve (look a the poor '0'), and its derivative (i.e. the gain). Since the gain is not reaching -1, no ring oscillator can be made, and it will be difficult to construct logical gates using this structures.

However, we could close the loop for the first time.

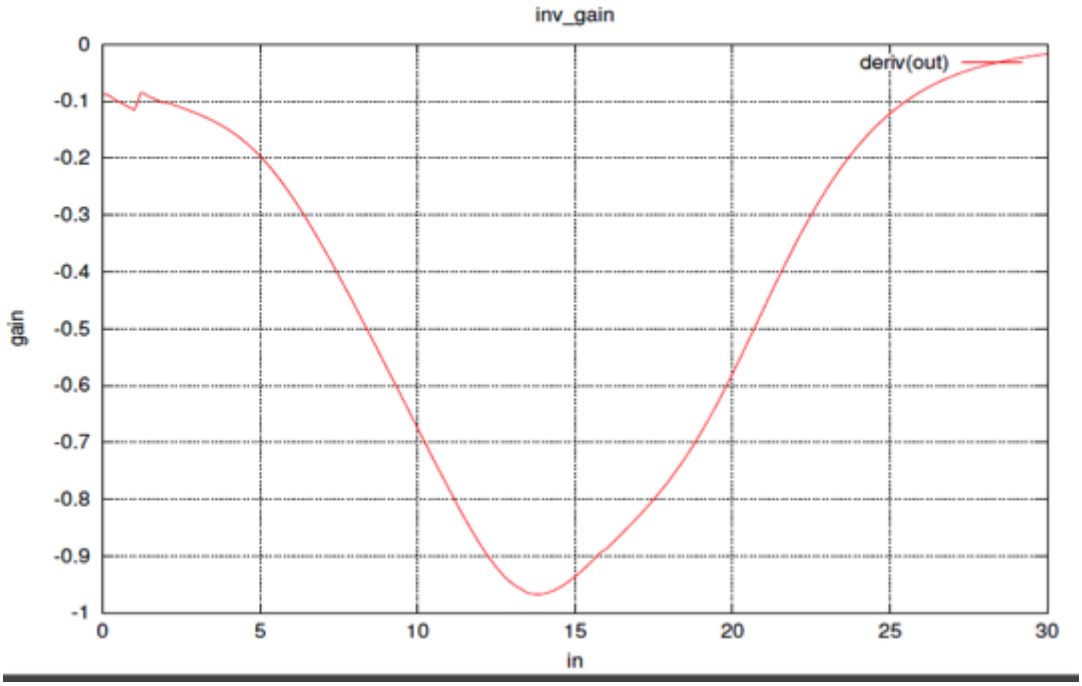


Figure 47. Simulated inverter transfer curve based on semi-physical models

9 Conclusions

This document clarifies the concepts and procedures concerning Modeling, Validation and Variability Management for the devices built inside the TDK4PE project, especially for Organic Thin Film Transistors.

Critical issues that clarify our approach are:

1. Separate: (i) the concept of statistical variability on the parameters measured for a given set of devices, from (ii) the concept of variation on the model parameters considering the results from the extraction-modeling tool.
2. Propose a model in which the corner or the Monte Carlo analysis can be implemented considering different variations for every single transistor. That is to say, since every transistor is different from each other, each transistor instance should pass to the OTFT transistor model a different parameter to reflect that different behavior. Then, INFINISCALE (IFS) will provide a solution to be compatible with the existing model cells and simulation engines.
3. Consider that we have a reduced set of OTFTs sizes in our circuits (those that can be produced with highest yield), so that there will be a reduced set of models (i.e. OTFT1cm or OTFT4cm) that will be used/called from the circuit structures. This means that, at this first stage, we are not going to have one model for all OTFTs considering channel width (W) and channel length (L) variations but a model for a reduced set of fixed W and L values that take into account their statistical fabrication variation. Variability should then refer to the working conditions (i.e. power supply, V_{DD}, G_{ND}, $-V_{SS}$) and physical parameters (gamma, mobility, threshold voltage, etc.). A global general model can also be used if a wide range of working OTFTs is available with sufficient performance.

10 References

10.1 Documents

[1] S.Smith, "Sheet Resistance and Electrical Linewidth test structure for semiconductor process characterization", M.S. thesis. Univ. of Edinburgh, 2003.

[2] A.L.Walton "Microelectronic Test Structures", abstract presented to Semicon97, Geneva.

[3] N.Stavitski, J.H.Klootwijk, H.W. van Zeijl, B.K. Boksteen, A.Y. Kovalgin, R.A.M. Wolters, "Cross-Bridge Kelvin Resistor (CBKR) Structures for Measurement of Low Contact Resistances", IEEE Transactions on Semiconductor Manufacturing, Vol. 22, n. 1, February 2009.

[4] N.Stavitski, J.H.Klootwijk, H.W. van Zeijl, A.Y. Kovalgin, R.A.M. Wolters, "A study of Cross-Bridge Kelvin Resistor Structures for Reliable Measurement of Low Contact Resistances", 2008 IEEE Conference on Microelectronics Test Structures, March 24-27, Edinburgh, UK.

[5] Mohan, S.S.; del Mar Hershenson, M.; Boyd, S.P.; Lee, T.H., "Simple accurate expressions for planar spiral inductances," Solid-State Circuits, IEEE Journal of, vol.34, no.10, pp.1419-1424, Oct 1999 doi: 10.1109/4.792620

[6] "Agilent Impedance Measurement Handbook", Application Note 5950-3000, 4th Edition, Agilent Technologies, Inc., 2009

[7] Hammerstad, E.O., "Equations for Microstrip Circuit Design," Microwave Conference, 1975. 5th European, vol., no., pp.268,272, 1-4 Sept. 1975, doi: 10.1109/EUMA.1975.332206

[8] Pucel, Robert A.; Masse, D.J.; Hartwig, C.P., "Losses in Microstrip," Microwave Theory and Techniques, IEEE Transactions on, vol.16, no.6, pp.342,350, Jun 1968 doi: 10.1109/TMTT.1968.1126691

[9] "De-embedding Techniques in Advanced Design System", Agilent Technologies S.L.

[10] M. Bohm, A. Ullmann, D. Zipperer, A. Knobloch, W. H. Glauert, and W.Fix, in IEEE International Solid-State Circuits Conference Digest Technical Papers, pp. 270 – 271 (2006).

[11] A. Ullmann, M. Bohm, J. Krumm, and W. Fix, in Proceeding of the International Conference on Organic Electronics, p. 53, The Netherlands, Eindhoven, 2007.

[12] K. Myny, S. Steudel, P. Vicca, M. J. Beenhakkers, N. A. J. M. Van Aerle, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, Solid-State Electron. 53, 1220 (2009).

[13] K. Myny, S. Steudel, S. Smout, P. Vicca, F. Furthner, B. van der Putten, A. K. Tripathi, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, Org. Electron. 11, 1176 (2010).

[14] R. Blache, J. Krumm, and W. Fix, in IEEE International Solid-StateCircuits Conference Digest Technical Papers, pp. 208–209 (2009).

[15] S. Steudel, K. Myny, V. Arkhipov, C. Deibel, S. D. Vusser, J. Genoe, and P. Heremans, Nature Mater. 4, 597 (2005).

[16] K. Myny, S. Steudel, P. Vicca, J. Genoe, and P. Heremans, Appl. Phys. Lett. 93, 093305 (2008).

[17] E. Cantatore, T. Geuns, A. Gruijthuijsen, G. Gelinck, S. Drews, and D. de Leeuw, ISSCC 2006, Digest of Technical Papers, 2006, San Francisco, Feb. 5–9, 2006, pp. 272–273.

[18] Soeren Steudel, Stijn De Vusser, Kris Myny, Martijn Lenes, Jan Genoe, and Paul Heremans, J. Apply. Phys. 99, 114519 (2006).

[19] Stéphane Altazin, Raphael Clerc, Romain Gwoziecki, Jean-Marie Verilhac, Damien Boudinet, Georges Pananakakis, Gerard Ghibaudo, Isabelle Chartier, and Romain Coppard, J. Appl. Phys. 11, 064509 (2014).

[20] A. Cerdeira, M. Estrada, R. García, A. Ortiz-Conde, F.J. García Sanchez, "New Procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions", Solid State Electronics 45 (2001) 1077.

[21] M. Estrada, A. Cerdeira, I. Mejia, M. Avila, R. Picos, L.F. Marsal, J. Pallares and B. Iñiguez, "Modeling the behavior of charge carrier mobility with temperature in thin-film polymeric transistors", Microelectronic Engineering 87 (2010) 2565-2570.

[22] M. Estrada, I. Mejía, A. Cerdeira, J. Pallares, L.F. Marsab, B. Iñiguez, "Stability of PMMA on P3HT PTFTs under stress",SSE 53 (2009) p 1063-1066.

[23] M. Estrada, I. Mejıa, A. Cerdeira, J. Pallares, L.F. Marsal, B. Iniguez, "Mobility model for compact device modeling of OTFTs made with different materials", Solid-State Electronics 52 (2008) 787.

[24] I. Mejia, M. Estrada, M. Avila, "Improved upper contacts PMMA on P3HT PTFTS using photolithographic processes", Microelectronics Reliability, 48, 11-12, 2008, 1795-1799.

[25] M. Estrada, I. Mejia, A. Cerdeira, J. Pallares, L.F. Marsal, B. Iniguez, Solid-State Electronics, 52, (2008), 787-794.

[26] S. Jacob et al. "Compact modeling for Flexible Organic and Large Area Electronics: a new fast and reliable method", LOPE-C, 31 May 2010 - 2 June 2010, Frankfurt.

[27] E.R. Patchett, A. Williams, Z. Ding, G.A.W. Abbas, H.E. Assender, J.J. Morrison, S. G. Yeates and D.M.Taylor, "A high-yield vacuum-evaporation-based R2R-compatible fabrication route for organic electronic circuits" Org. Electron. Vol. 15,7 (2014) 1493-1502.