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Partner:	**PHX (6)**	PhoeniX Software Solutions for Micro and Nano Technologies
Partner:	**STX (7)**	Sensing·Tex
Partner:	**TUC (8)**	baumann printing research
Partner:	**UALG (9)**	CEDT
Partner:	**3DMM (10)**	3DMICROMAC First Choice in microMachining

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List of Acronyms

TDK4PE	Technology Design Kit for Printed Electronics
CO	Dissemination level Confidential, only for members of the consortium (including the Commission Services)
R	Nature of the deliverable Report
CAD	Computer Aided Design (EDA tools)
CPI	Centre for Process Innovation
CSEM	Centre Suiss d'Electronique et Microtechnique.
DRC	Design Rules Checker
ERC	Electrical Rules Checker
EDA	Electronic Design Automation (CAD tools)
FPGA	Field Programmable Gate Arrays
IC	Integrated Circuit
pCell	Parametric Cell (cell generated automatically considering design parameters)
PDK	Process Design Kit (Physical Design Kit)
PE	Printed Electronics
R2R	Roll-to-Roll
R2S	Roll-to-Sheet
S2S	Sheet-to-Sheet
TDK	Technology & Design Kit
TDK4PE	Technology & Design Kit for Printed-Electronics
XML	Extensible Markup Language
XSL	Extensible Stylesheet Language
XSD	Extensible Specifications Definition
XTR	Electrical eXTraction Rules (from geometric circuit layout)

1. Public Project Summary

1.1. Executive Summary

Organic electronics technologies seems to be in continuous evolution even the number of success cases is still quite limited to restricted niches and applications domains (displays, sensors,…). Increasing the number of users (industry, research, academia) accessing that technology will give more chances to develop solutions for real market applications and therefore for the success of the technology.

The goal of TDK4PE has been the proposal of design and technology methodological flows for building Technologies and related Design Kits (TDK). Within the project itself we have applied such methodologies to address both, a full-inkjet PE development technology and its corresponding Process Design Kits (PDK) and design flows. Those PDKs for organic electronics are the first step for opening access to experienced circuit designers to technological processes, in a similar way done by the microelectronic industry. TDKs allow a clear separation between technology and design such that designers can develop their circuits using electronic design automation (EDA) tools to produce "files" that are converted into "foils" through the technological processes. This means that technological processes are "frozen", repetitive and offer sufficient quality from a design and fabrication perspective: with higher reliability and high yield. Reliability, variability and yield are the key issues for the efficient implementation of applications and the widespread of the technology.

Selected EDA tools have been MaskEngineer/Clewin from Phoenix Software™ and the open/free tools suite built around Glade. Technology independence has been achieved through the TDK4PE information structure (managed using XML descriptors) following the OpenAccess standard from the silicon industry and PDAFlow promoted by Phoenix Software™. NGspice electrical simulator has been primarily used (other spice versions have been validated). Verilog-A was selected as description language for device models.

TDK4PE approach has been validated with 3 different organic electronics technologies capable of building OTFTs: full-inkjet, gravure and evaporation. Full-inkjet technology has been developed and optimized in the project. Around 50.000 transistors and 17.000 DRC structures have been fabricated in a process that converged towards a balanced performance-yield goal provided by real applications (flexible textile systems for user interfaces). Semi-automatic characterization and analysis procedures and have been set-up to analyse huge amounts of data used for process optimization and model generation. The full-custom design kit for full-inkjet technology has been developed and validated whereas cell-based design kit could not be validated during the duration of the project.

TDK4PE approach has also been validated using third party technologies showing the powerfulness of the approach towards a virtual foundry model. A full-custom design TDK has been generated for gravure printing (provided by CSEM) and validated by them. A full-based design kit has been produced and validated for an evaporation process (provided by CPI) and used for the characterization and modelling process developed in the project on 12700 transistors, 620 logic gates and 15000 DRC structures designed in the project and fabricated by CPI. The cell-based design kit for CPI could not be validated during the duration of the project.

1.2. PROJECT CONTEXT AND OBJECTIVES

At the beginning of the project, there was not any printed electronic process being offered publically, as it is common in silicon inorganic technologies, to widespread the advantages of the technology and open opportunity for applications. This was due to several reasons. As an immature industry, almost all business models were vertical, providing in-house the complete solution from application to fabrication. Public funded institutions like technology centres, research institutions or universities have also technological processes oriented to research and prototyping (not to high productions) that could be ideal for feasibility studies. In these cases, the main reason for not opening them is their continuous evolution that avoids a stable public offer for a significant period of time. Furthermore, both scenarios suffer from the fact that there was not a standardisation initiative to promote a common format to exchange technology information, that in silicon technologies in provided by technology (or process) design kits (TDK or PDK), attached to electronic design automation tools (EDA). That would promote a clear interface between application design and fabrication technologies towards a more horizontal business model, allowing open foundries offer to the industries and research to exploit new opportunities.

TDK4PE was built to offer to the PE community a higher degree of design automation by building the set of tools and methodology to develop complex circuits and systems, which is a real requirement for a sustainable growth of the technology. Therefore, TDK4PE addressed the idea of how to abstract the Printed Electronics (PE) technology process details and identify the knowledge, methods and tools needed to design circuits for organic electronics emerging technologies without having to bear the entire burden of technology details regarding equipment, inks and substrates. This idea was already developed in the 80's for the silicon industry by developing their related Process Design Kits (PDK) containing all technology related information for low end full-custom design, and Design Kits (DK) including libraries for cell-based semi-custom design.

By providing the required information and facilities ("technology and design kit plus EDA tools") to circuit designers, we allow designing without being experts on process details and enabling the concept of design reuse based on cell libraries, both design productivity and circuit reliability will be improved.

In order to reach such targets, TDK4PE defined a methodology for technology specification and characterization, TDK formalization and cell library development.

PE technology processes evolution, due to its flexibility needs, is often tuned by changing printing system parameters, functional inks and substrates. This somehow restricts the widespread of PE technology. This also leads to the point that our strategy of building a TDK has not been previously published from a generic point of view. For its development, we fixed an application domain, textile flexible electronics for building user interfaces, and identified a suitable technological process: the full inkjet process that is able to cover that domain.

From this point, we started developing all the above mentioned points using a meet-in-the-middle methodology that includes: (1) A top-down approach from the selected application to identify and specify the main functional blocks in advance and the basic

devices to then build such blocks using synthesis tools when possible; and (2) a bottom-up approach to fix and characterize the baseline technology and to develop the basic building blocks that at the end will compose the functional blocks needed for the application.

Based on this strategy, we proposed a S/T methodology which provides measurements and guidance for the TDK generation that contribute to establishing the complete TDK4PE methodology. Once this strategy is materialized on a TDK customized over a concrete EDA environment, we have a complete design flow useful for full-custom based design using basic information technology or semi-custom design based on cell libraries and functional blocks. This result shows the power of the methodology and contributes to its spread among the industrial community.

Objective 1: Create TDKs for Printed Electronics EDA environments

The projects goal was to integrate TDKs for printed electronics processes with new features concerning layer descriptions, device models, simulation toolboxes, p-cell topologies or even more complex processing.

The project has proposed a TDK Development Methodology that collects the different abstraction levels of TDK development addressed within this project: physical level, full-custom and cell-based design strategies.

Technology documentation has been produced as the basic complementary information to physical design oriented to interactive design (layout editor, on-line DRC and netlist extractor) and backend processing levels oriented to automated processes (verification, compensations and format conversion). This work generated the TDK Database Information and related reports on physical verification strategies and backend post-processing. Its usefulness has been shown for de development of devices and cells from different partners in the project. The potential of that approach has also been demonstrated through the technology data exchange in the development of 2 additional design kits for 3rd party organic electronics processes (CSEM and CPI) generated in a short period of time (~3 months). Validation of CSEM design kits has partly been done by CSEM using their own process and design resources while validation of CPI design kits has been done by UAB, PHX and CSIC up to the simple digital gate levels.

Base-line technology files have been proposed and created to address TDK backend processing: layers definition, geometrical design rules, basic electrical parameters (Rsq, Cs), compensation rules and inkjet printing patterns. Inkjet drop spacing and compensation management have been implemented in a layout to bitmap tool (l2b) that was integrated in the EDA tools and made publically available.

Basic active & passive patameterisable cells (pCells) devices library information (device representations and spice models) has been formalized to work on full-custom design. We implemented device representations and Verilog-A and Spice models. Those models have been used for the fully inkjet technology developed in the project, and also for CPI by using the Infiniscale extraction tools that generated model parameter from device characterization results.

Cell & Block library documentation and related software tools, including data-sheets for cell-based design, allowed the partners to formalize and implement cells, pCells (parameterized cells) and structures (such as the Inkjet Gate Array or IGA).

The project also reached to integrate design kits in two different electronic design automation (EDA) tools: PhoeniX Software and open-source. Its implementation of circuit designs has been completed and demonstrated in: (1) the CleWin-PEDK tool with design kits for the full-inkjet process developed in the project and for one 3rd party foundry (CPI) and (2) on the Glade/NGspice tools also for our own process and for 3rd parties CSEM and CPI. Both have been customized with layout-to bitmap backend tool for the full inkjet process. The tools include installation procedures and scripts. In both cases there exist clear methods to update parameters related with technology refinement when required.

As a conclusion, Objective 1 was reached and TDKs are being made available via both open access and commercial environments.

Objective 2. Develop, establish and characterize the inkjet fabrication process

The main goal was to develop and establish an inkjet based technology able to address the application domain. The project started from the experience of TU Chemnitz, ENEA and UAB in building organic transistors in a moment in which any external process was neither available nor interested for this approach. Hopefully, nowadays, this has changed and several organic electronics processes are announced to become publically available.

In order to build a technology consistent with the methodology and required documentation, we started with a base-line technology process definition and characterization, as a result of the development and description of processes and recipes combining materials (inks and substrates) and printing engines (S2S implementation and R2R estimation). Different test vehicles were developed to characterize material performance and device stacks in order to select a suitable recipe for fabrication..

Additionally, by using the fabricated DRC structures, the device geometries were defined taking into account the printing tolerances related to the employed printing systems.

Once materials were selected, we started the fabrication and characterization of passive and active electronic devices, such as resistors, capacitors, inductors, diodes and thin film transistors (TFTs) in sheet-fed configuration (S2S). These devices were investigated singularly, as basic components of complex electronic circuits. Several tens of thousands of devices were fabricated and characterized. We conducted several activities to improve the material formulation, device geometries and process design to reduce failures and improve yield.

The amount of samples manufactured by the fully inkjet printing approach can be considered an outstanding achievement and contributes to a better knowledge of the behaviour and failure origins of organic and printed devices.

Yield is a key issue for the scaling up to both public offer and industrialisation, therefore the project proceeded with the quantification of the device operational yield (in sheet-to-

sheet -S2S- processes) through the characterization of devices and cells over different runs to get significant statistical data about technological stability.

At the end, we obtained, technology files (layers and patterns definitions, electrical parameters and models) and rules for design and verification (layout, electrical simulation, DRC/ERC, LVS, 3D-Viewer) that are key elements for its design kit.

The second key element obtained for the design kit is the models of devices (R, C, D and OTFTs) for its electrical simulation, using Spice-like simulators. Verilog-A was selected for modelling. Statistical information has been collected to account for model variability. Simulation models use both UCM and semi-physical modelling (from Infiniscale) in order to cope with transistors scalability on width and length and also to ensure convergence for static and dynamic analysis.

Unfortunately, to the end of the project, the convergent process developed did not reach a sufficient maturity level to be able to implement the minimum set of gates and circuits with a reasonable trade-off between performance, yield and variability to achieve a stable general-purpose process. Different balances were achieved reaching corner situations (good yield-high variability, lower variability-lower yield, high-yield-low performance) measured on thousands of transistors, hundreds of inverters, and very few logic gates. As a consequence we have been unable to implement any functional circuit using a cell-library approach. We have been able to obtain OTFT models for individual transistors, but not at all a unique parameterisable model (depending on W and L) matching inside some common technology corners.

As a conclusion, Objective 2 was not reached but progress was made in mass inkjet printing of transistors with 90% yield achieved on occasions.

Objective 3: Cells, circuits and design methodology

In order to make circuit design easier, according to the current technology-independent design methodologies, the project proposed to build a basic device and cell library using design styles based on p-transistors that allows a better sign-off procedure between designer and foundry. Several steps have been accomplished to reach that goal.

Physical design and backend processing level kit was initially developed to allow layout design, verification, compensation and conversion into printable files for specific processes (our full-inkjet process and also CPI and CSEM processes). This work was completed as specification of the API for PE design flow implementation and reporting on physical verification strategies and backend post-processing (i.e. layout-to-bitmap for inkjet or gravure file conversions).

The project produce also a full-custom design demonstration kit (including device libraries) with the TDK customised on the selected EDA tools including backend processes and test-vehicles. This work was completed by collecting technology files we have been able to build 2 design kits for Phoenix tools (full-inkjet from TUC/ENEA/UAB, evaporation from CPI) and 3 design kits for open/free EDA tools (full-inkjet from TUC/ENEA/UAB, gravure from CSEM, evaporation from CPI). Finally, the project generated a cell-based design kit (with cell libraries) for PhoeniX Software and open/free tools including design examples on modules designed and produced using TDK4PE cell-based design. This work has been extensively done for TDK4PE (device and cell level) and specially CPI (standard

cells and IGA). We have developed and promoted use of parameterisable cells (pCells) in order to automate the generation of sets of structures that allow the automatic capture of design rules and device and cell models by electrical and optical characterization and the generation of complex structures such as arrays or complete circuits. The project design methodology, tool and training material (class & labs) has been demonstrated at the OTFT Design Course celebrated together with the COLAE project.

Finally, incremental application-driven demonstrators composed of heterogeneous printed elements such as textile pressure sensors, RF elementary circuits, digital cells and compiled regular structures have been fabricated and are ready for application customizations. Hybridization techniques have been developed to connect those arrays to foils composed of organic devices through connectors. Unfortunately, these arrays have not been used in fully organic demonstrators due to above mentioned (lack of sufficient yield-performance). A complete circuit (147 OTFTs and 30 I/O pads) has been prototyped using textile sensors and LEDs and standard silicon microelectronic devices. Out of its results, a fully functional combinational circuit has been designed using our own standard cell library and has been fabricated at CPI. Any of the fabricated circuits were working properly.

As a consequence, Objective 3 was not reached but progress was made in transporting the TDK to a gravure process (CSEM) and an evaporation process (CPI) although at the level of inverters only.

TDK4PE project structure

The TDK4PE way of working has been organised according of WP1: Management, dissemination and standardization, WP2: TDK development methodology, WP3: Baseline technology development and characterization, WP4: Device and cell libraries, WP5: EDA flow and TDK integration, WP6: Circuit Integration using Technology and Design Kit. The industry input, mainly through WP2 and WP6 actions, is applied as requirements and commercial products to the project and the project provided feedback to them. WP2 has been the methodological core that expands to the new generation of businesses.

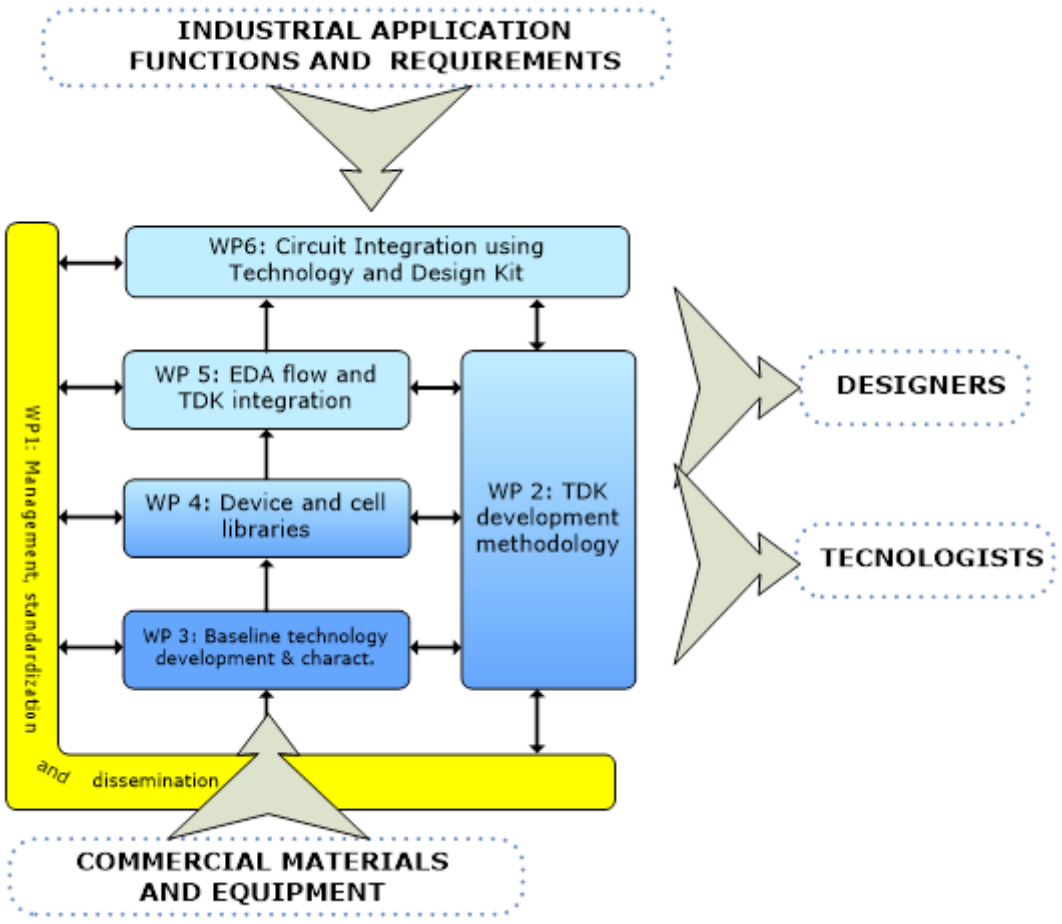


Figure 1. Interaction of the project structure with the external industry.

1.3. MAIN S&T RESULTS/FOREGROUNDS

The TDK4PE project has been strategically oriented to build the design and technology methodology that will boost the distributed printed electronics business in Europe (getting closer to end-users) in the sense that there has to be a tool chain support for the complete design and fabrication from professional users to final products. Final products can come from diversity of application domains (packaging, RFID, sensors, photovoltaic, lighting, biomedical, food, eHealth, etc.) that can share technology, materials but far more important, a similar design methodology.

Printed electronics, as in many other well established technological domains, has to move from a vertical business model to a horizontally segmented one. To achieve that, the project helped to demonstrate by a methodological approach that:

- Materials manufacturers are developing and supplying complete sets of necessary compatible materials (semiconductor, conductive and insulating inks and flexible substrates) for any given FOLAE fabrication process.
- Machinery manufacturers and technology developers are optimizing production parameters and tools for those inks and substrates that allow building devices and circuits and, from them, provide technology files with basic information concerning electrical parameters and geometrical-mechanical accuracies and rules.
- EDA manufacturers are providing better design tools in the sense that they provide a path to fabrication of highly reliable and productive FOLAE products. This refers mainly to the back-end tools and simulation model integration (including variability).
- Instrumentation is integrating characterization methods and set-ups oriented to FOLAE devices.
- Service providers can set up business models and can easily reuse their classical microelectronic knowledge into this new technological and applications domain.
- End-users are able to develop domain-related application specifications in order to cope with the technological limitations.

In this way, Europe will profit from reusing the existing deep knowledge and well established industry, and reuse the experience in microelectronics, printing, machinery and materials industry towards this new "non-planar" (nor that clean) processes inherent to FOLAE production.

1.3.1. Project Findings

I. TDKs for Printed Electronics EDA environments

Key topics in TDK4PE methodologies and tools

In this section the key topics to understand goals and advances in methods and tools along this project are highlighted.

Partition/parameterization of technology and development processes

A wide "divide & conquer" partition strategy strongly based on parameterization applied to different abstraction levels related to both technology and design processes has been successfully applied along this project.

Building a seamless technology-design interface

One of the key topics in such kind of projects where implementation technology shall be developed in order to allow later on open the design activities against such technology is to have an early and clear definition of "technology-design interface"; thus, to answer two key questions:

- What is the basic technology information needed to address the design processes?
- How the results (layout) from a design process shall be translated into printing processes to get the expected physical samples?

To this concern we have addressed at the very beginning the following topics: (1) Differentiating printing layers versus design layers, that means to identify which are the printing layers and their properties (geometrical and electrical), what are the minimum set of design layers with the inherited properties from its printing layer counterparts and how to transform the design layers into printing ones to allow design fabrication and (2) generic electrical parameters and geometrical design rules for design layers and their mapping into printing layers.

Once those points have been defined we could address concurrently the technology development to reach good results from printable files, and the development of design kits, methods and tools development. Such strategy has been complemented by a wider technology-design co-development approach based on a definition of methods, equipment's and tools to address the cycle "design-prototyping-characterization-modelling" in a systematic way to keep updated the above defined generic parameters (geometric and electric) that feeds the design processes and drives the technology development ones.

The characterization loop

Another key point, which was distributed over different partners on the initial proposal, was the characterization at different abstraction levels (structures, devices and cells). Finally we kept the initial distributed activities for the so specific characterizations but we added a centralized task to perform automatic characterizations on large amounts of devices duly arranged on a previously formalized test foils to allow such systematic measurements to extract geometric and electrical parameters with enough accuracy and statistical meanings.

A characterization environment has been setup at CSIC facilities around a probe station adapted for plastic foils and including all the measurement equipment's previously virtualized to get a flexible setup.

XML structured information collection and exploitation

Another key topic of this project strongly related to above parameterization activities but intended to collect most of the fundamental information related to technology and physical design is the usage of XML databases which allows both:

- A structured and pseudo-formalized recollection of such fundamental information
- A potential automated exploitation of this information to perform either a direct link to EDA tools, i.e. Phoenix API, or an automatic generation of technology files or physical design kits (PDKs), as the case for Glade based environment.

This strategy, not only become very effective for mapping TDK4PE methods into third party technologies, but recently it has been verified that a very similar strategy was adopted as an standard by SI consortia to address similar topics for advanced nanometric silicon technologies. So, our proposal is almost compliant with such recent new standard.

Development processes strongly based on PCells

Next natural step after parameterization on technology-design interface issues is to use parameterized cells to develop devices and circuits. Nevertheless in our case we have gone further to support almost all the development processes by means of PCells in combination with scripts done with Python language to address: (1) test & characterization vehicles correct by construction and ready to drive the already mentioned automatic characterization environment; (2) technology and DRC/Compensation qualification structures; (3) basic devices and Cell libraries and (4) hierarchical and parameterized Inkjet Gate-Array (IGA) structure.

Based on this strategy it is quite easy and fast by now to do complete loops of "design - prototyping – measurement" cycle.

Project EDA tools: Phoenix & Glade+

As already planned in the project proposal we have been working with two EDA environments:

- The Phoenix MaskEngineer-CleWin based industrial framework
- The open/free Glade based environment where we have integrated different complementary tools to get a complete design flow.

Both environments are fed from TDK4PE XML information system and both of them have been customized for third party technologies (CPI and CSEM) in addition to our own TDK4PE technology.

TDK methodology and related environments and tools

The fundamental elements

As already mentioned, identifying the technology-design interface in terms of generic parameters for fundamental drawing rules and electrical parameters is a key point to allow concurrent technology process and design methodologies development. Based on this initial effort we have defined:

- Design layers versus printing layers or patterns and the basic rules to move from geometrical layout into printable bitmap files.
- The fundamental design rules and related structures and strategies for its definition from technology side.
- The elemental electrical parameters for basic structures (connections) and devices (passive and active) to be fixed by technology.
- A generic strategy to represent design rules and electrical characteristics to allow its usage as parameters into the design flows.

Once defined the above topics ("agree-in-the-middle") we were able to start working simultaneously in both sides, technology to reach stable processes and feed the above rules and parameters with right values to produce design kits and tool flows to allow circuits development to meet-in-the-middle of technology-design interface and close the way from electronics design down to its fabrication by means of PE technologies.

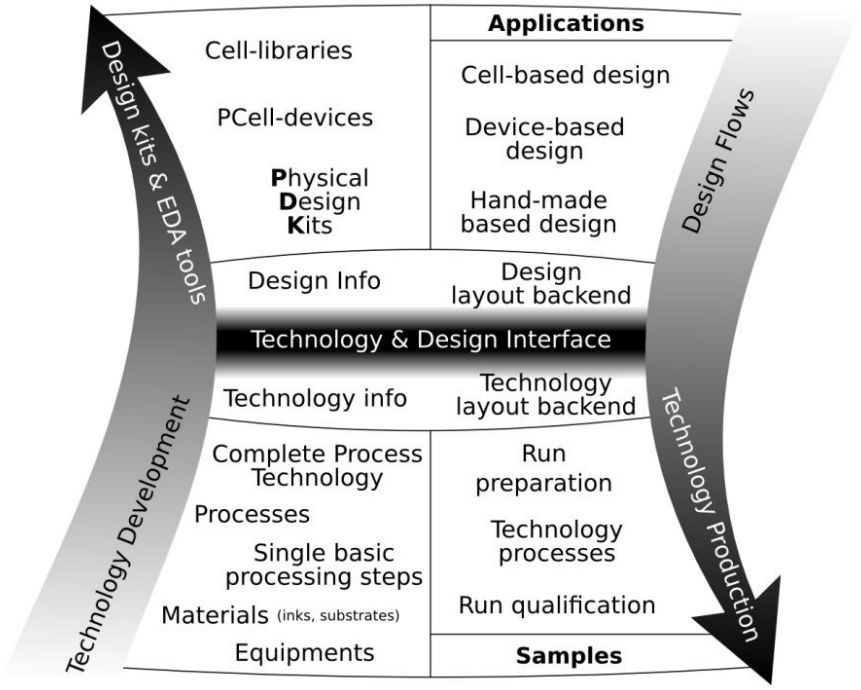


Figure 2. Agree-in-the-middle to Meet-in-the-middle concept. From Technology development to design kits, from design flows to final products.

Global TDK development strategies

In order to address the development from technology to design we needed to follow the cycle "design-prototyping-characterization-modelling" at so different abstraction levels:

- Single/multiple layer structures to characterize the printing processes and related results (physical morphology and electrical parameters).
- Simple passive and active devices to characterise their specific performances.
- Basic cell libraries to characterise its behaviour and performances.

Figure 3 shows this cycle in a bottom-up loop from technology to feed design kits and customize design flows.

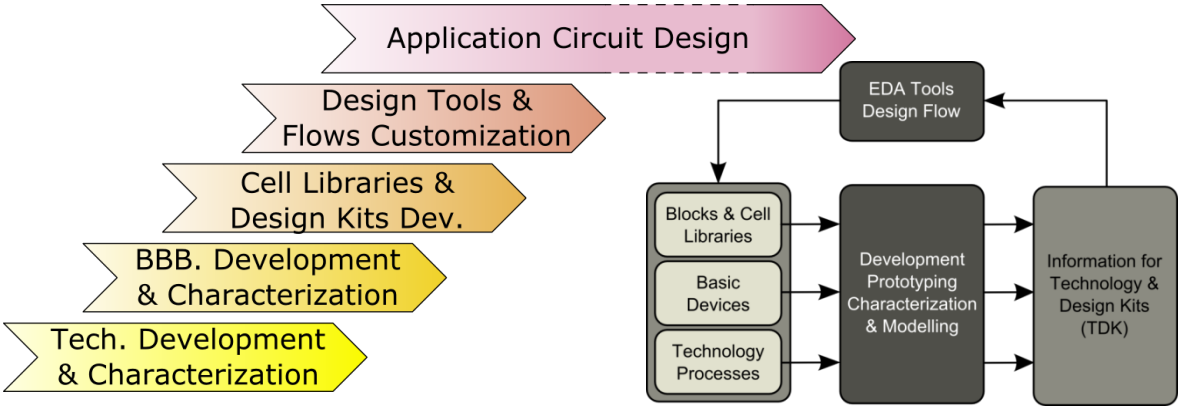


Figure 3. TDK development cycle from basic technology to circuit design

Combining this idea with the previous parameterized meet-in-the-middle figure allows an important speedup in the complete TDK development cycle and its customization on top of selected tools, as we can develop most of the task concurrently.

The measurement and characterization environment

As seen in the previous figure one of the central processes of the defined development loop is the "characterization" iterations. The measurements and characterizations for specific and detailed purposes have been done by different partners with a close relationship with technology, as scheduled; but once we started to produce lots of structures and devices we realized that an automatic approach was needed to address a more systematic and robust way to process and make an initial analysis such large samples production.

A **characterization environment** has been setup at CSIC facilities around a semiautomatic probe station adapted for plastic foils and including all the measurement equipment's previously virtualized and the related software application developed to control all the involved equipment including the probe-station. In this way we got a very flexible setup.

In order to have an efficient, systematic, robust and safe usage of this environment we defined a set of rules for the related test-vehicles on a foil: alignment marks, samples distribution and coordinates, probes relative position, etc. Each test-vehicle shall have all its characteristic data contained in a description file (.TVD) to drive the complete measurement procedure from the computer acting as a host running the application to control the complete environment (configure, do actions, know the status, collect and exchange data from different instruments). Later on the collected data is used for specific analysis processes which are dependent of each specific structure or device in the related test-vehicle.

The probe station has a microscope with a video acquisition device that has been connected to the PC through a standard digitalizer. This allows the Labview application to capture still images of the devices under test when needed (i.e. for devices detected as

'fail'). A variety of communication standards allows the use of a large variety of instruments, with different communication protocols, to cover most of characterization needs.

A **parameterised strategy** has also been applied to improve the exploitation of this environment and is based on:

- PCells to design the structure or device under characterization.
- Parameterized scripts using the above PCells and providing a complete test-vehicle layout including all the requested variations of related PCells and the needed additional alignment and identification information plus the related TVD file.

This **environment** under the parameterised approach has been **used with different strategies and goals**:

- Electrical characterization procedures for devices in order to address the parameter extraction for its further modelling.
- Electrical characterization strategies to obtain some basic geometrical design rules like width-spacing.
- Image driven characterization to address either geometrical design rules or compensation rules and patterns based on image processing and scoring using original layout plus compensation pattern versus final image from related samples.

Finally some early data post-processing and analysis is also performed on the results collected from this characterization environment. The resulting processed and filtered data is then going into modelling stage, which is explained in next section.

As an example of the benefits of this measurement and characterization environment, we have recently designed and printed one run of ten foils, with about 30.000 compensation test vehicles per foil. Comparison of the captured images versus the designed ones has been done and relevant data has been obtained not only for compensation and design patterns and rules, but also concerning the printing processes and quality variations depending on the sequence and direction of printing steps. The high degree of automation of the whole procedure has reduced drastically the measurements, image captions and analysis times.

Modelling strategies, processes and tools

Partners have achieved a complete work on modelling techniques and could implemented different ones starting from physical to behavioural modelling through an innovative approach called semi-physical modelling developed by Infiniscale.

The ultimate goal was to clarify the concepts and procedures concerning Modelling, Validation and Variability Management for the devices built inside the TDK4PE project, especially for Organic Thin Film Transistors.

Device models and parameters

A complete work has covered models and parameters to be extracted for linear and snake resistors, capacitors, inductors, diodes and OTFTs. A General parameter extraction methodology has been developed.

Concerning OTFTs, a Unified Compact Model and parameter extraction method has been developed as physical-based model. Infiniscale team has developed an UCM (developed by A. Cerdeira and M. Estrada.) model based extractor, which has been successfully used for last models generation.

Variability

Having defined the parameters and their extraction procedure, large number of measurements has been carried out to quantify variability, which is largely more acute in OTFTs than in silicon-based technologies. INFINISCALE modelling is able to take into account the measurement variability, which could be done by Modelling a kind of envelope that delimits the variability range of each model or by adding statistical distributions of technological parameters. However, a complete strategy has been defined to cope with variability and yield.

Devices Examples

Two models for load and drive OTFTs have been generated. Load and drive names correspond to current pseudo-PMOS cell design style naming. Models are ID(VD, VG) were range of VD and VG are between [-30V, 0V]. Models were exported to Werilog-A for spice simulation purposes.

And finally, a three-step ring oscillator using the latest models provided by Infiniscale has been simulated. We could close the loop for the first time.

TDK-XML information system for PDK generation

In order to build Physical Design Kits (PDK) that are as independent as possible to the final set of tools and the technology, we need an abstract information representation, and the eXtensible Markup Language (XML) format has been the chosen option to describe and store all the technology information.

Trough XML Schema Definition files (XSD) we have defined the style and format of the XML technological files that each technology database will contain. In addition, we have created a web-based application divided into two main modules:

- Front-End: Allows the user to create, modify, delete and export technological information in XML format using a custom form. This form is automatically created from thew XSD file specification.
- Back-End: Allows an administrator user to define a new structure for the information related to the TDK.

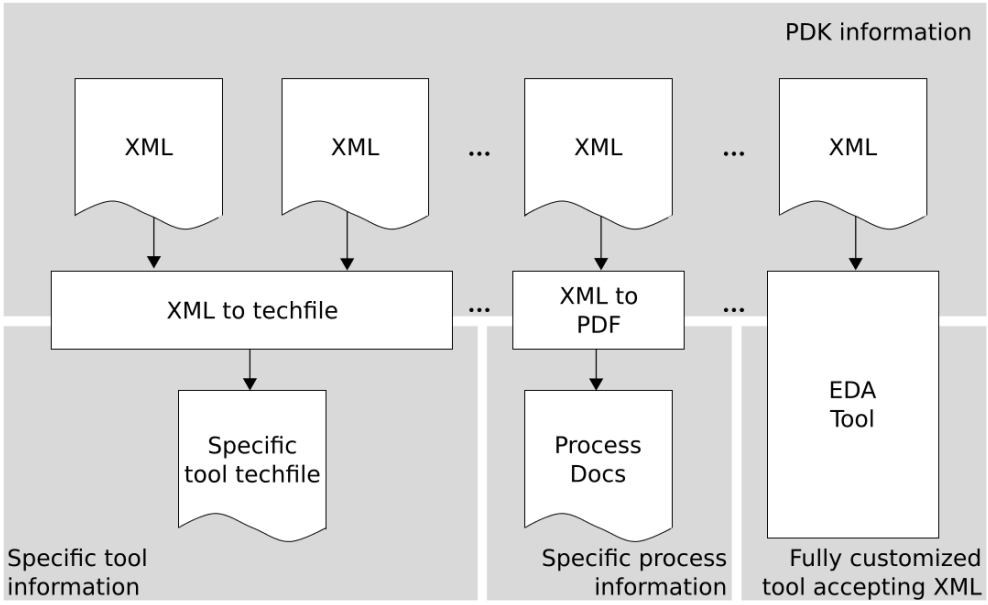


Figure 4. From XML database to EDA tools strategies

As Figure 4 shows, we have defined and successfully used two different strategies for EDA tools connection to the XML database:

- Using eXtensible Stylesheet Language (XSL) files, we can extract specific information from the XML files and store it in a PDK techfile with an specific format, ready to be used by its associated EDA tools. This is the case for the open/free EDA tools suite. This strategy is also used also for generating documentation.
- For the MAskEngineer environment, the tools are capable of reading the XML format directly. The C++ photonics standard Application Programming Interface (API, called PDAFlow) is extended with the XML format, via a set of XML parsers which are generated automatically from the XSD files.

It is worthy to note that the Silicon Integration Initiative (Si2) released on November 5 2013 their Open Process Specification v1.1., containing all of the data elements that are necessary to automatically create a Process Design Kit (PDK) in any EDA vendor's or company proprietary design flow. The OPS standard is a formal grammar based on the standard XML Schema Definition XSD, and therefore, it follows the same strategy started two years before by our consortium.

PE design flows

The open/free tools suite has been compiled to be used in personal computers having Windows® and Linux-based operating systems, and it's composed by:

- Schematics editor: device based schematics using **gschem** (open tool)
- Netlister: **gnetlist** (open tool)
- Electrical simulation spice-like: **ngspice** (open tool)
- Layout editor, DRC, XTR : **Glade** (free tool)
- Layout versus schematic (LVS): **Gemini** (free tool)

- Back-end compensation for inkjet: **Layout2Bitmap** (open tool from CSIC)

Based on this set of tools we have defined the following physical design flow for full-custom circuits

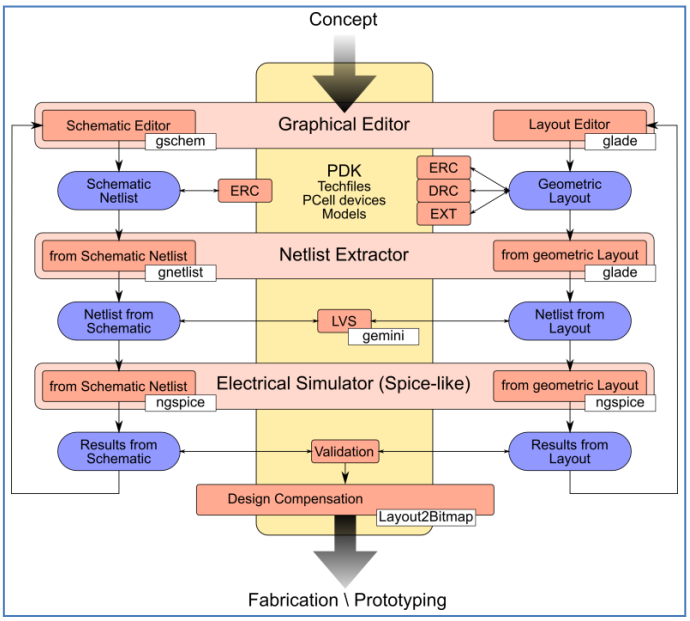


Figure 5. Glade based physical design flow

The whole Phoenix tools design suite is composed by:

- Schematics editor: **CleWin Schematic**
- Electrical simulation spice-like: **ngspice** (integrated open tool in MaskEngineer)
- Layout editor, DRC, XTR & netlister: **MaskEngineer**
- Back-end compensation for inkjet: **Layout2Bitmap** (open tool from CSIC integrated in MaskEngineer)

Specific tools development for PE

One of the first developments of the project was a tool for vector-to-discrete layout data conversion. This tool, called layout2bitmap (L2B), converts a layout design in GDS format into a set of bitmap files (one for each layer) ready to be printed. This conversion is enriched with some features as:

- Estimated drop diameter size compensation, obtaining more accurate sizes by shrinking shapes by the drop radius.
- Different drop spacing selection for each layer.
- Performing basic Boolean operations, allowing the differentiation of layer zones, which can be filled or have different estimated drop diameters.
- Area filling with certain patterns more suitable for each ink stack combination.

An auto router for IGA channel routing inside the MaskEngineer environment has been implemented, ensuring a rapid functionalization of the IGA combined with the fast

characterization of Known Good OTFT's (KGO) from the fully-automated characterization system.

Another important activity on the Phoenix tools has been the creation of the CleWin Schematic, where schemes can be created and edited, complementary to CleWin which acts as a the layout editor. This allows Schematic Driven Layout (SDL) within a single user interface.

TDK methodology, design kits & EDA tools applied to third party technologies

One of the main results of the developments in the methodologies and tools has been the creation of design kits for third party technologies.

The main motivations to address the development of those design kits have been:

- Prove the TDK4PE development methodology on external technologies other than our own inkjet technology.
- Get access to third party technologies, different than inkjet, but having better performance than our technology.

We have contacted with partners of the EU FP7 COLAE project and finally some of them agreed to do this trial with two different processes: CSEM (gravure printing) and CPI (evaporation technology).

The expected EDA tool suite for those technologies match very well with our two environments:

- Glade base environment for CSEM as their technology and feature shapes are similar to classical Manhattan silicon geometries. . Also a Manhattan version of CPI PDK has been implemented into Glade environment.
- Phoenix environment for CPI as their technology uses geometrical primitives (round and any angle shapes) which are better managed from MaskEngineer layout strategies.

The creation of these two third-party design kits included the porting and integrating their corresponding design rule sets, what let to variations in the way layers are handled and design verification is implemented. In addition, a set of basic PCells has been added to each design kit, and some of the EDA tools have been customized to achieve the functionalities required for each technology. The foreseen advantage of using the XML-based strategy has been successfully proved by the easiness in the CSEM and CPI design kits development process.

II. Full-inkjet fabrication process

State of the art

For the last decades, electronics has been dominated by silicon technology. [i] The reasons for this are quite a lot and very easy to understand. As example, has been the capability of having up to several of millions of transistors in silicon integrated circuits the responsible of the informatics revolution we are still immerse in. The development of

informatics and microelectronics has been adapted to the diverse computing and information needs of society, from supercomputers to portable media devices, complex systems containing intelligent sensors with low-power processor platform. Other devices, such as MEMS (silicon micro systems) or image sensors (for CMOS cameras), could be considered as side products of silicon electronics' development.

This technological evolution has drawn a highly complex panorama that still works efficiently. However, at this point, the manufacture of integrated circuits requires really high investments, often needs to be performed in expensive laboratories that maintain strictly controlled environmental parameters, known as "clean rooms".

The main disadvantages of silicon technology can be outlined in: building a new foundry is very expensive, and require very large scale productions,[ii] it can be environmentally aggressive, [iii] -as an example, obtaining pure silicon leaves a heavy ecological footprint-,[iv] and it is centralized into big companies.

In this context, printed electronics appears to be a necessary renewal of the rigid precepts of conventional electronics, opening new market niches –associated with the flexibility of the materials and systems–.[v,vi,vii] Also printed electronics allows better adaptation to the environmental requirements demanded by current circumstances,[vii] as well to new models of electronic systems' usability claimed by society.

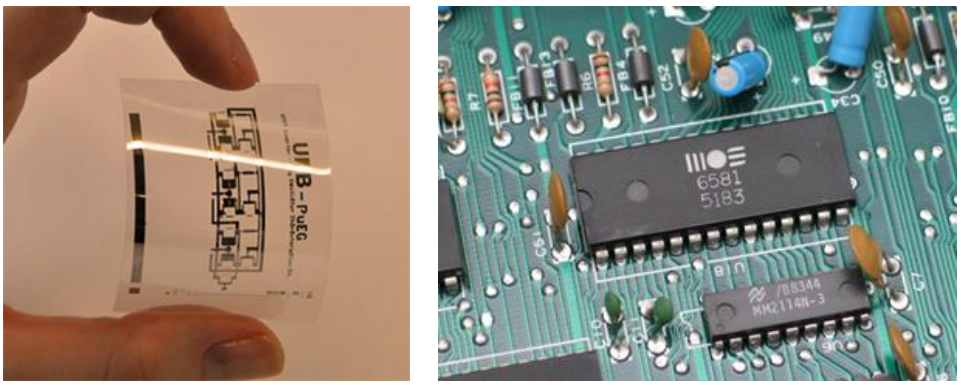


Figure 6. Inkjet printed inverter, manufactured on flexible substrate (left) and conventional printed circuit board (PCB) (right).

Printed devices are made from processable solutions of functional materials which can be inorganic nanoparticles or salts either organic molecules or polymers. But all tend to have in common that they need much lower temperatures to be processed than is required for polycrystalline silicon or for wiring a conventional printed circuit board (PCB). This feature extends the range of materials that can be used as substrate, including a wide variety of low-cost and flexible polymers. They can be developed many low-cost applications, as RFIDs tags, or higher value applications where are required light weight and flexibility, such as flat panel displays.[viii]

Printed electronics can be manufactured using different material deposition techniques. These printing techniques can be mainly divided into those that use discontinuous sheets, known as *sheet-to-sheet* techniques, and the ones that the substrate is a continuous foil printed using rotary printing techniques, which is known as *roll-to-roll*.

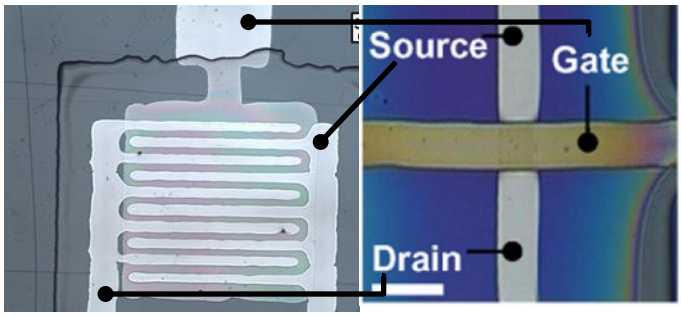
Techniques based on discrete quantities of substrate, sheet-to-sheet, offers versatility and effectiveness with no comparison to conventional electronics, really suitable for small volumes of work, prototypes or extremely specific applications. In this category can be included inkjet printers, a barely modified version of desktop printers found in every home today, or screen printing technique, which is also used in conventional processes of silicon electronics. On the roll-to-roll side, more complex techniques such as prints by offset or gravure techniques, without forgetting ink jet printing, are more common for massive and industrial production. For example, solar cells, a growing market that has shown a great interest in these techniques. It has been already achieved a production of 10,000 square meters per hour (m^2/h).[ix]

Among all the printing deposition techniques, manufacturing electronic devices by ink jet printing deposition seems to be the most suitable for both small and massive production: it is digital (which means that from one image/design it is economically viable manufacture just a single copy),[x] only small volumes of ink are involved,[x] it is easily scalable,[x] is an additive technology (in principle, they can be deposited as many layers of materials as it is desired, one above the others),[x] and implies low demand on materials involved in manufacturing.[x] Also it is easy to achieve an accurate positioning of the material to be deposited and it is a non-contact technique.[x]

Another of the main advantages of these printing technologies is that they can be easily adapted to massive production.[vi] For example, ink-jet printing technique associated to roll-to-roll substrate feeding concept is a well-established technology for obtaining large quantities of printed stuff at really low cost. Lots of printed electronics' research efforts have been focused in transfer these attributes to the field of electronics.[vi,xi] Obtain electronic devices with the same costs, in resources and time, as newspapers, opens new market opportunities and big industries are really interested in them.

Currently this technology has some restrictions in functionality and complexity of manufactured systems achieved. This is mainly due to two factors: limitations in commercially available substrates and functionalized inks, and because the development of techniques is still in progress. That's the major reason why resolution and performance of generated circuits by printed electronics are still far from the ones achieved when using traditional processes. But also opens the door to research and improvement.

For example, if the attention is focused in obtaining fully inkjet-printed thin-film transistors (TFTs). Transistors are key components for building computer processing units. In literature can be found some examples of fully inkjet-printed TFTs,[xii] all manufactured using discrete amounts of substrate and similar desktop printers: or Dimatix DMP 2830, a desktop printer specifically conceived by Fujifilm for depositing functional materials, with one printhead equipped with 16 nozzles, or a single nozzle inkjet dispenser device. Of course, with these laboratory scale printers it is possible to achieve really accurate deposition of materials, and some of the best examples of TFTs in literature have been manufactured like this, but it is unlikely this can be up-scaled to industrial manufacturing, and also does not take advantage of some of the most important skills of printed techniques: depositions may take long time to finish, they use small areas of substrate and the number of printed devices is limited.



Interdigitated electrodes (source and drain)

1-channel geometry device Not interdigitated electrodes (source and drain) [xii(c)]

Figure 7. Fully inkjet - printed TFTs. On left it is shown our TFTs, with interdigitated electrodes architecture. On right, Tseng et al TFT, with non interdigitated electrodes.

But the most important thing to remark from literature is that in all cases there is an obvious lack of information about the real scope of the TFT they are reporting. There is no data concerning yields, or the process stability, failure origins etc. There is no statistical data about the reliability of fully inkjet-printed OTFT. And all of these points are key factors towards industrialization and commercialization.

Objectives

The development of a manufacturing process based on inkjet printing technology was proposed to address the application domain. The main idea was to design a strategy to up-scaling manufacturing process, starting from usual laboratory equipment to semi industrial equipment (using industrial printheads).

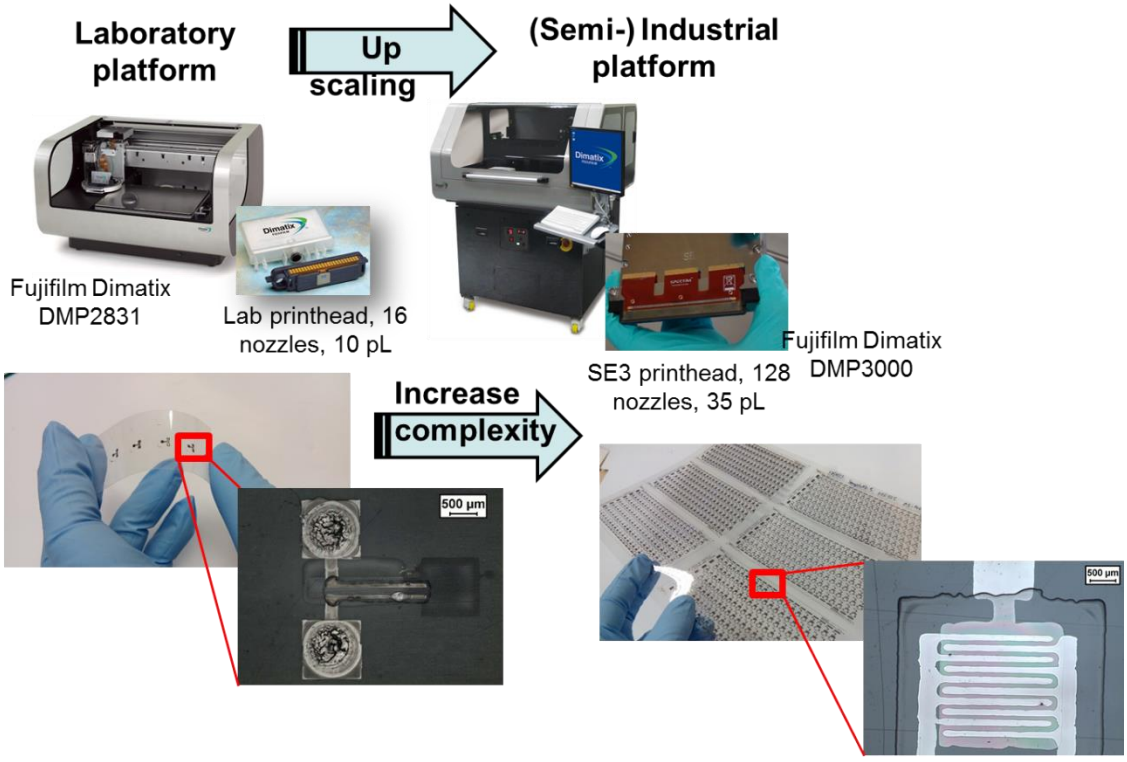


Figure 8. Scaling-up strategy towards high productivity.

The focus was set on a sheet-to-sheet (S2S) processing which enables high positioning accuracy and also high productivity as we could demonstrate during the project.

A manufacturing concept for thin film transistors (TFTs) was developed based on a combination of an industrial printing platform (DMP3000) and laboratory printing platforms (DMP2831). This allowed us to exploit efficiently the advantages of both systems and to share the manufacturing and optimization tasks among the printing partners ENEA, UAB and TUC.

Dimatix DMP2831 printer is laboratory-scale equipment. It works with little number of nozzles and small pieces of substrate in small areas to obtain few samples. We started working with them, testing our materials in test samples and structures. Then, we started manufacturing some TFTs. These TFTs also gained in complexity.

When all procedures and materials, designs and tests were proved and optimized, was time to move to semi-industrial equipment, which means using DMP-3000 printer. The printhead of this printer can afford a large number of nozzles and can be fed with bigger foils to cover large areas in order to obtain high number of samples.

Development and Achieves

The proposed inkjet technology and its processes and materials were defined during the first period of the project by a screening of available print heads within the consortium and materials. It resulted in a definition of print technologies and process parameters for both – S2S and R2R - e.g. registration limits, print resolution, substrate handling etc. This can be considered as basis for the developed manufacturing route for the printed devices.

Different functional ink materials were investigated concerning their jettability, layer formation and functional performance. Whereas the substrate and the ink formulation for the metal electrodes were found quite fast due to the experience of the printing consortium, the dielectric material can be considered a main challenge within the project. As a result, more than 50 dielectric formulations were considered and more than 30 dielectrics formulations were investigated by printing tests. All these preliminary tests were performed using the DMP 2831, at lab scale. Also were tested several TFTs architectures, sizes and models, in order to optimize our devices before starting with the semi-industrial proceedings, were other parameters would be taken into account.

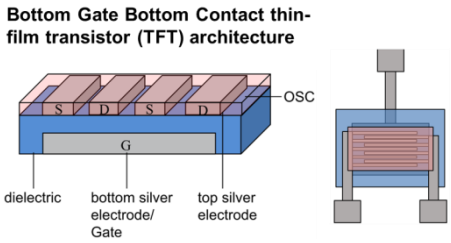
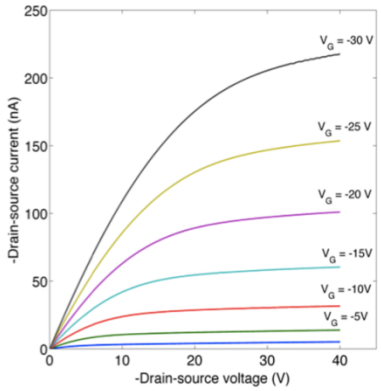


Figure 9. Selected architecture for our OTFTs.

Updates of the fabrication parameters were provided until end of the project due to incremental performance improvements by application of new materials or optimized

processing parameters. In all cases, unification documents were provided and shared among the printing partners to obtain a manufacturing standard and the final printing recipe. Final recipe shows the selected materials, deposition processes, pre- and post-treatment methods to obtain printed transistors with the best compromise between yield and performance. Typical curve and performance parameters obtained for transistors are shown in Figure 10.



- Threshold voltage of -12 V
- On/Off ratio of 10^3-10^4
- Mobility around 1.5 10^{-2}
- Drain currents up to 1.5 µA

Figure 10. Example of measured transfer curve (left) and performance parameters (right) obtained for full-inkjet OTFTs

Comparing these values to the state of the art of fully inkjet-printed transistors indicates that we obtained good results. Of course, there are several publications available showing inkjet-printed transistors with much lower threshold voltage, much higher mobility as well as on/off ratio and drain currents. However, one has to mention that in most cases some of the layers are not deposited by inkjet printing or even not solution-processed and that they do not report about a high number of transistors. There is no indication of yield in these publications.

It also has to be said that did also improvements of the performance during the last period for the project, when we have been able to manufacture devices with µ = 0.1 cm^2/Vs, better that global characteristics shown in Figure 10. Improvements are mainly due to the use of improved dielectric layer and the use of passivation layers.

Our strategy has been to develop a stable and reliable printed electronics process with a reasonable balance of yield and performance instead of manufacturing few high performance transistors (out of hundreds or thousands). For that we performed the analysis

With the printing recipe clear and the architecture optimized, the up-scaling process started. New parameters need to be optimized when using the DMP3000. It has lots of nozzles and much more velocity in ink deposition, but, for example, it has less accuracy and precision in printing for larger areas. For small devices, precision and accuracy are key issues in TFT manufacturing. In scheme from Figure 11 are represented the most common causes of failure (low yield) in devices. Those directly depend on layer thickness and printing precision and accuracy.

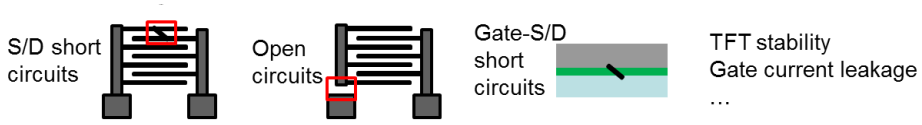


Figure 11. OTFT failures related to device yield

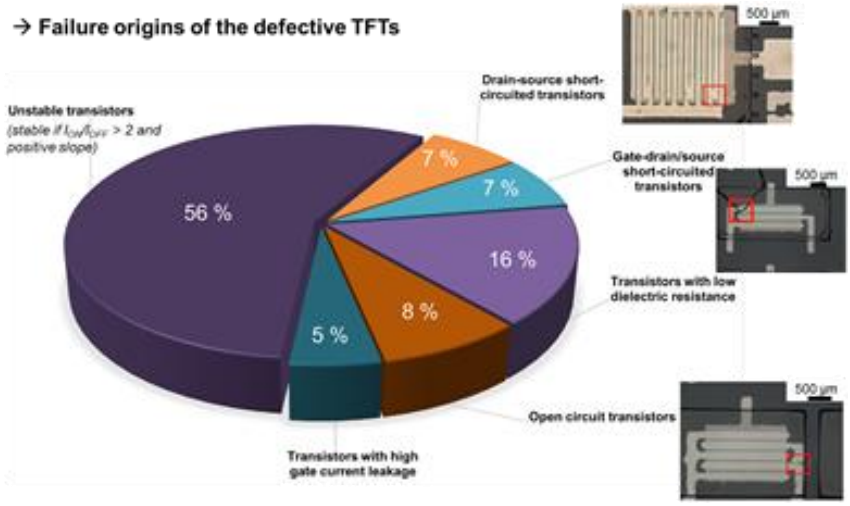


Figure 12. Failure statistics for full inkjet OTFTs according to the common faults detected presented as schematic drawing (top) and actual printing (bottom right)

A set of experiments were designed in order to fix these crucial parameters and its influence in quality of our samples.

For example, an experiment was performed to optimize drop spacing to be used in Dimatix DMP3000. Drop spacing (DS) is the space between drops and can be controlled by the operator. Higher drop spacing allows having less amount of ink for area, which uses to results in thinner layers and better accuracy. But, it is achieved less resolution. In the other hand, low drop spacing allows higher print resolutions and thicker layers, but accuracy decreases (Figure 13).

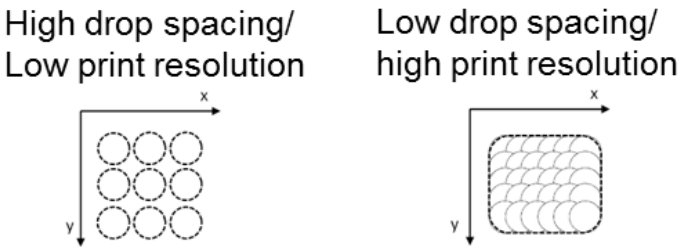


Figure 13. Differences between different drop spacings

In a first stage they were planned several drop spacing variations for the S-D layer as well as for the dielectric layer, depending on the print resolution we expect following results: the higher the resolution, the shorter the distance between the electrodes (the channel length), but also the lower the yield.

Graph inside Figure 14 shows in Y axis the % of short-circuited S-D electrodes as a function of print resolution (DS) related to the channel length (right Y axis). So, it could be easily concluded the higher the DS, the larger the channel length (therefore the lower the speed performance) and the higher the yield.

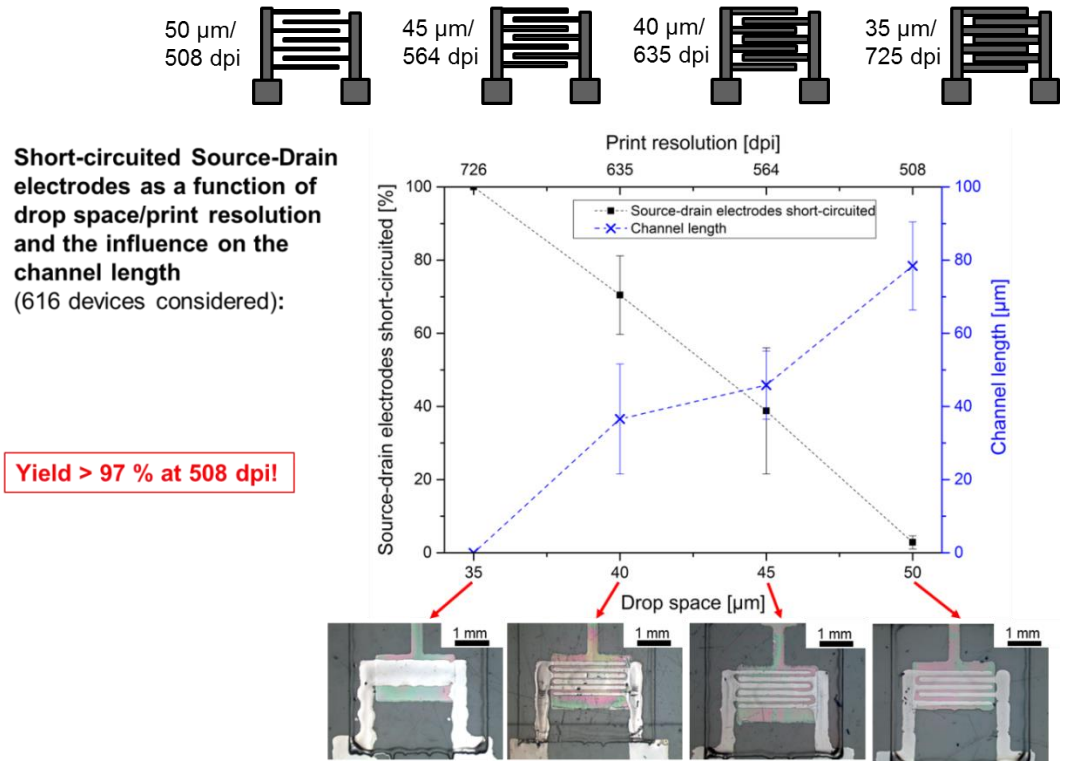


Figure 14. Effect of the variation of print resolution (DS) of source-drain electrodes as a schematic drawing (top) and actual printing (bottom)

In a second stage it was investigated the influence of dielectric layer thickness: we expect higher yields and lower leakage currents for higher print resolutions

2) Variation of print resolution/drop space of the dielectric cPVP layer

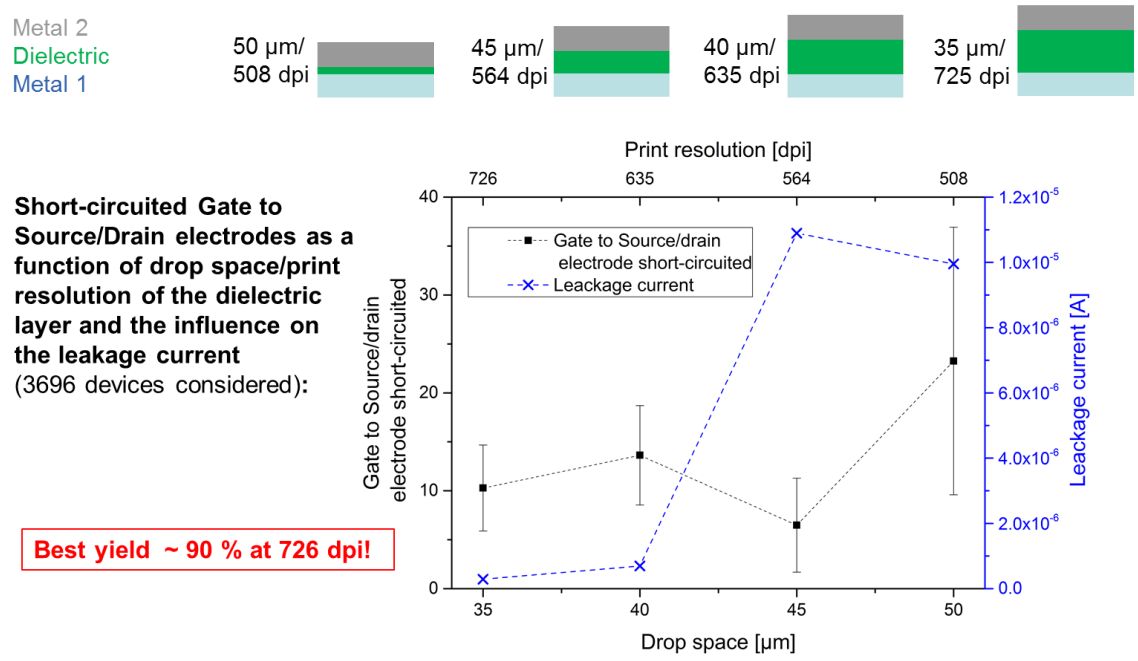


Figure 15. Effect of the variation of print resolution (DS) of dielectric cPVP layer as a schematic drawing (top) and actual printing (bottom)

Once all parameters have been optimized, we increased the manufacturing yield up to 90 % for transistors. This high yield is based on processes in ambient conditions (no vacuum processing has been used) and with several manual process steps since it is a batch approach (no inline-processing). The average device yield for transistors is about 70 %. The less numbers of layers we use, the higher is the yield. In consequence, the yield increases incrementally when manufacturing diodes, capacitors, antennas and resistors.

In this respect, we consider following points as main achievements:

(i) Successful development of manufacturing approach for electronic devices solely based on inkjet printing

(ii) Successful transfer of the manufacturing approach from laboratory scale to semi-industrial scale

(iii) Successful development of a semi-automatic characterization tool for the manufactured device

Concerning (i), we could successfully develop a manufacturing process for functional resistors, antennas, capacitors, diodes, transistors and inverters using solely S2S inkjet printing technology. Therefore, materials were selected, tested and adapted to the inkjet process. For each device, different variations were done concerning the material used and printing as well as post-printing parameters to obtain the best set of parameters for the manufacturing. As already mentioned our approach is based in a batch process.

Layer by layer was deposited (Figure 16) and different physical and chemical treatments were applied between the depositions, e.g. to dry and sinter layers, to change the surface energy of layers, to crosslink layers or to perform a surface passivation. Each layer was optimized concerning its functionality and its compatibility towards the layer underneath or on top. All these adjustments resulted in the successful development of manufacturing approach – mainly using laboratory inkjet printing.

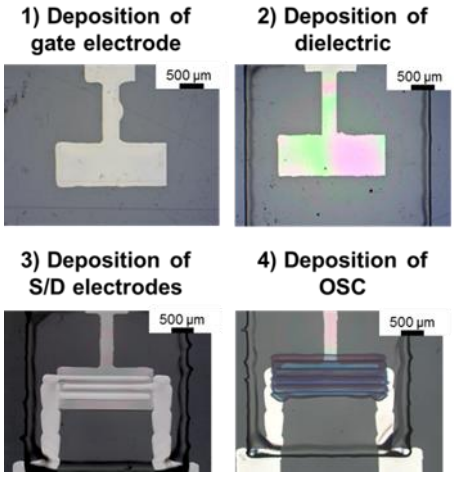


Figure 16. Results of the each processing step after inkjet printing of functional layers

However, many efforts were also dedicated to the development of a roll-to-roll (R2R) inkjet printing process during the first period of the project. Finally, only a test setup has been realized successfully at TUC consisting of two industrial printheads with a camera system for drop visualization integrated in a R2R system with accessories such as pre-

and post-treatment tools. A IR sintering tool for inorganic inks was developed in close cooperation with the company Heraeus and installed in the R2R system.

With respect to (ii), we could successfully transfer the manufacturing from laboratory printheads to industrial printheads. Up-scaling processes are challenging, since materials, inks and inkjet process parameters needs to be optimized and thus differ from these used in laboratory printing. With the up-scaling, we are able to go towards industrial printing and could increase the productivity remarkably. This was required, e.g. to obtain statistically relevant data for transistors about manufacturing yield, device performance variability and device performance scalability. Within the three years of TDK4PE, the printing consortium manufactured about 50,000 transistors, about 2,000 capacitors, about 3,500 resistors and several 100 diodes. The yield for the transistors was finally about 70 %, for optimized transistor design even up to 90 %. The capacitor yield was up to 80 %. Yields for the resistors vary depending on printing direction and geometry the resistor (line resistor vs snake resistor). The yield for short-length line resistors are close to 100 % demonstrating the high potential of inkjet printing as manufacturing process. Next to the afore mentioned devices, also several spiral inductors, circular- and square-shaped, as well as antennas were manufactured.

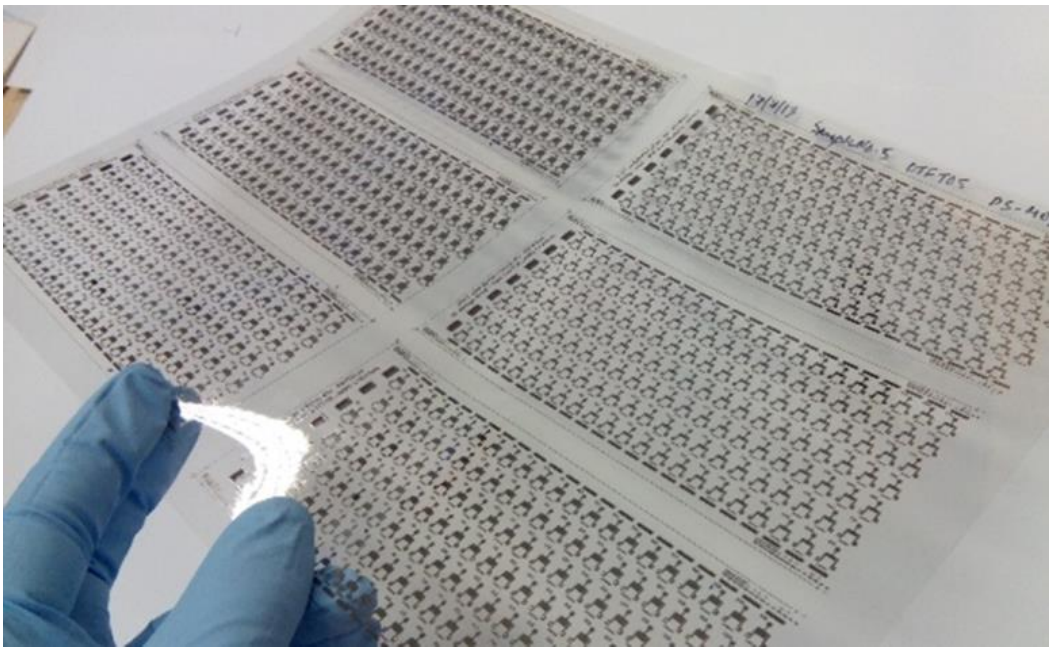


Figure 17. Example of A4 sheet composed of 6 different rectangles ready for semi-automatic characterisation

About (iii), a semi-automatic characterization tool was developed by CSIC. It was required to enable the extraction of all the data for all the printed devices. Measurement procedures dedicated to the printed devices were generated allowing a reliable and fast characterization and analysis. Each printed device was designed to meet the requirements of characterization tool. The semi-automatic characterization system turned out as important tool allowing not only the device characterization but also the characterization of the manufacturing process, mainly inkjet printing.

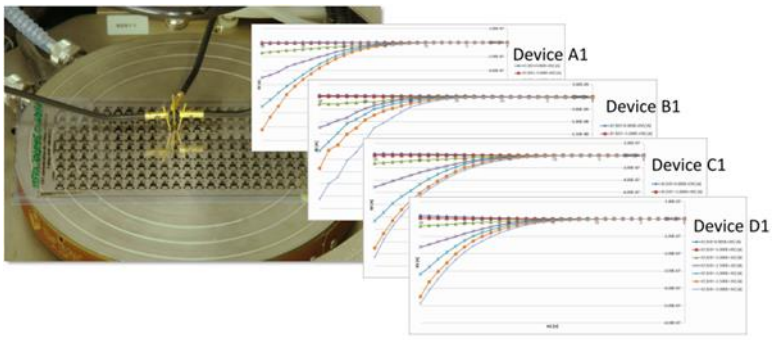


Figure 18. Semi-automated probe station use for device characterization

As already mentioned, during the duration of the project, our process development did not reach a sufficient maturity level to be able to implement the minimum set of devices and circuits with a reasonable trade-off between performance, yield and variability to achieve a stable process for fabrication large quantities of OTFTs. Different balances were achieved reaching corner situations (good yield-high variability, lower variability-lower yield, high-yield-low performance). We have been able to obtain OTFT models for individual transistors, but not at all a reliable and unique parameterisable model (depending on W and L) matching inside technology corners.

III. Cells, circuits and design methodology

State of the art

In the late 1970`s, the Mead-Conway[xiii] design rules concept revolutionized silicon integrate circuit (IC) design. Their idea was to abstract physics to a point where electronic design engineers could address physical design with sufficient certainty. An evolution of that idea led to the modern relationship between silicon foundries and design teams (and fabless semiconductor companies) and also the process design kit concept, and finally to the complex multi-processor systems-on-a-chip making intensive use of virtual components (managed through Intellectual Property rules).

Later, in the 1980's, many circuit design techniques were developed and later collected in Weste and Eshragian[xiv]. Those design techniques are still valid to build FOLAE cell libraries according to the availability of devices (and related performance). For instance, for only p-type based circuits we can use rationed logic techniques to build gates and libraries.

According to semiconductors industry we can divide ASIC circuit design flow into two parts: technology independent (or front-end) and technology dependent (or back-end). For inkjet based FOLAE systems, these two parts suggest two different approaches for system design and implementation. With regard to the front-end, at the current level of technology, a top-down design approach would be valid, and it will result in library cell requirements for cell-based design. We can consider this front-end quite well covered by current silicon microelectronics EDA tools and methodologies and therefore it can be almost directly reused. Main advantage of technology independent approach is based on the sign-off capabilities concerning speed at cell level, since cells from a library are already pre-fabricated and pre-characterized, and therefore can be guaranteed by the foundry (according to its process tolerances).

In contrast, for the back-end, technology dependence for library cells and design kits construction requires a bottom-up approach according to the new fabrication processes involved resulting in a design kit for full-custom design. Overall, this leads to a classic meet-in-the-middle approach as is common in platform-based designs. The meet-in-the-middle approach is a proper design flow for the next generation of inkjet FOLAE technology facing circuits with thousands of OTFTs.

The TDK as it has commonly agreed did not exist for printed electronics at the beginning of the project. In some parallel R&D projects, something close to this concept has been planned for in-house usage, parallel to de development of the technology. POLARIC[xv] and COSMIC[xvi] are two FP7 projects (running parallel to TDK4PE) addressing similar activities pursuing key advances on printed/organic technologies. POLARIC focused in gravure printing at device level focusing on low resolution and high performance while COSMIC uses clean-room evaporation techniques to build high performance complementary circuits and end up recently producing design kits for every technology. Furthermore COLAE[xvii] FP7 project has been focusing on commercialization, addressing the virtual foundry concept, much closer to the design hits proposed here.

TDK4PE is also addressing application driven technology developments, but specially focused on how to define the contents of a TDK with the related libraries and to fix the methodology to its whole development and deployment to customize design tools and flows which will allow any further application development.

Methodologies for circuit design and optimization are crucial for closing the gap between devices and real practical applications of OTFT flexible electronics. Efforts in building digital integrated circuits using OTFT have been carried out, but in a very limited number and small and medium scale[xviii]. Reported designs used the same circuit design approaches as in Si-MOSFET circuits.

At the beginning of the project, no public dedicated design kit exists for printed electronics. State of the art was to design a layout with existing tools like L-Edit (generic VLSI layout editor), CleWin (mask layout editor) or general purpose drawing tools (i.e. CorelDRAW or AutoCAD) and also using expensive CADENCE EDA tools, available in universities, research centers and large industries. A conversion from the layout to the actual printer files is performed either manually, by simple home-made software tools or provided by machine manufacturers. These files were not at all capable of incorporating technology parameters from the actual manufacturing process into the design cycle. Furthermore Design Rule Checking (DRC), Layout versus Schematic (LVS) checking, Mechanical Rule Checking (MRC) and other processes were all non-existent.

Objectives

The goal of the project concerning cells was to build a basic device and cell library using design styles based on p-transistors using the automation tools at its maximum extend in order to quickly develop a cell-based design kit for as much technology independent design as possible. This approach also covers the frequent update of technologies in the sense that minimizes the number of redesigns at physical layout and tool customization levels. These cells have to be fully characterized at physical level, specified as data-

sheets and different representations shall be available to cover the different steps in design flow processes from design capture down to printable circuits.

The goal was to make available cell libraries inside a TDK from which anybody can build more complex circuits. Cell libraries are considered collections of: (1) basic passive & active devices (and its corresponding p-cells): resistors, capacitors, diodes, thin film transistors (p-type) and antennas for RF; (2) digital cells; (3) Elemental I/O blocks for external connections (power supply, input and output pads).

Development and Achieves

Parameterisable Cells (pCells)

PCell stands for "Parameterized Cell" and usually it means a piece of code (Master PCell) which instance or execution allows the customization of certain parameters (basically related to technology and design) to address the generation of all specific cell related views as a function of such parameters values. Instead of having just fixed cells, such approach will provide more flexibility and productivity to circuit designers (PCell users) to customize each PCell to its specific design environment conditions (size, shape, signal drive strength, fan-in/fan-out…).

A parameterized cell, or PCell, is a software procedure or routine that generates specific cell-views for each coherent set of values assigned to customize its parameters. Once the PCells library has been developed shall be integrated into EDA frameworks to allow its application under a specific usage strategy. Every time a PCell is executed-interpreted with a customized set of parameters, a set of available views for such customization are generated (Figure 19).

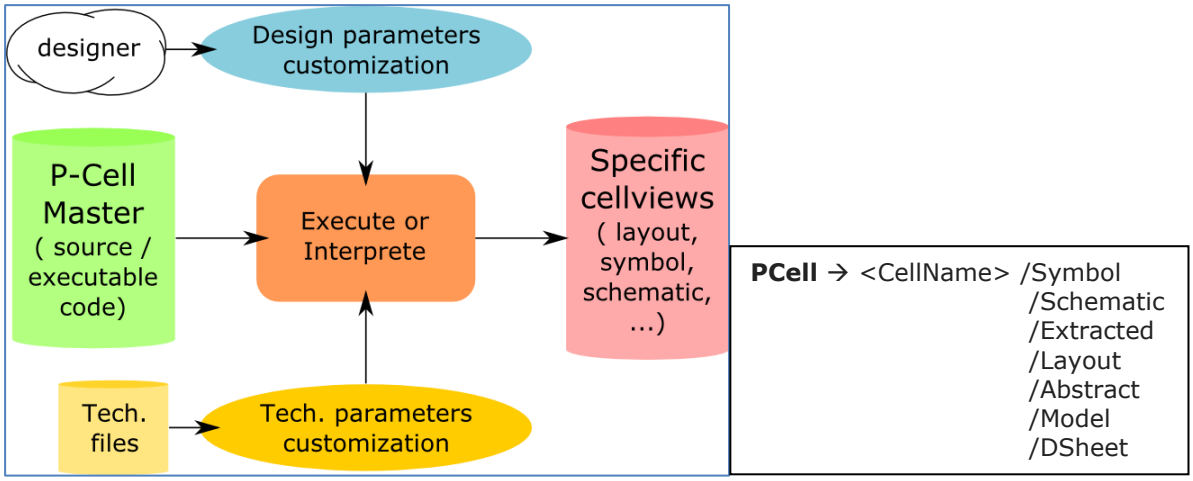


Figure 19. Simplified PCells concept and potential cell-views

Above concepts around PCells are addressing just its standard usage from designers point of view, but along TDK4PE project this concept has also been used from technology point of view to get the geometrical design and compensation rules.

The usual PCell approach in microelectronics is just applied to basic devices (contacts, transistors, polarizations, etc.) to simplify the generation of such devices layouts for full-

custom designers. Such a basic devices PCell libraries are provided by either the foundries or the library developers, or just developed by the design team. Whatever such a library comes, the designers will instantiate the PCell inside their layout design and customize its design-parameters accordingly to the specific usage requirements and performances of each PCell instance.

Another usage of PCell strategy is being addressed by standard-cell library developers in order to have the complete set of library cells fully parameterized from technology point of view (basically the geometrical design rules and the global library properties) and being able to customize a few basic design parameters to obtain a few different versions (i.e. multiple fan-outs) of each cell.

There is another development strategy for structured blocks (memories, PLAs, pixel arrays, etc.) within silicon microelectronics based on "structure compiler" tools. In those cases the designer prepares the elemental layout puzzle pieces and then customizes its composition into the final structured block by means of structure compiler including some sizing parameters (i.e. number of bits and words for a memory). Each time such a block is executed by the structure compiler those parameters are customized and the resulting layout is done accordingly.

In TDK4PE we have applied the PCells approach for the following goals:

- Standard PCell usage for basic devices. Each device is a PCell which design parameters could be customized by designers for each PCell instantiation, while the customization of technology parameters is done from "Technology-files".
- Standard-cell library development based on PCells. This approach is more devoted to its usage by library developers to provide the standard cell library and then designers will work with such library. Nevertheless this approach could also allow designers to use the PCells to generate new versions for any specific standard cell to get some new cell performances to allow a more accurate cell accommodation to its context.
- PCells/Scripts for test & characterization vehicles development. We have combined the PCells with Scripts to automatically generate test & characterization vehicles which contains a large matrix for each device or cell with different customized values for design parameters. Also the additional information to drive the automated measurement environment at IMB-CNM (CSIC) is generated from those scripts.
- IGA structure compiler + Gate level cells library development based on PCells strategy. The IGA bulk has been developed using a specific hierarchical PCells structure for any different IGA architecture where the design parameters are devoted to customize the specific architecture and the technology parameters allows the generation of bulks compliant with selected technology. Also the gate level cells to customize specific circuits on top of the gate-array are being generated from its related PCells.
- PCells/Scripts for technology characterization purposes (DRC + Compensation rules): basic structures + characterization vehicles. Finally we have also been used the PCell strategy to develop a lot of basic physical structures devoted to characterize and extract both design and compensation rules for a given technology. Again such PCells for basic structures have been combined into Scripts that generates the final test &

characterization vehicles layouts and the related information files to drive the automated measurement environment.

Not all the structures, devices, cells and blocks in the framework of TDK4PE project for the different technologies we have addressed (TDK4PE, CSEM and CPI) have been developed using the proposed PCell strategy, but most of them.

Cells Libraries

Two pCells libraries for design rules characterization (electrical and optical), for full inkjet and CPI technologies, have been created in order to extract the basic technology design rules. Since large amount of data is needed to extract the DRC values with enough statistical significance, these cells contain geometrical structures that can be checked using automated procedures of electrical or optical inspection. The libraries contain PCells that are intended to be instantiated in a large test matrix using scripts also parameterized.

One pCells library has been created for compensation patterns characterization obtained by extracting the rules that compensate for inkjet fluidic effects in an automated way using scripts for large matrix generation combined with automatic image capture and graphics comparison algorithms.

Three pCell libraries basic devices have been implemented for full-custom (pcell-driven) layout design. Passive (resistors –shown inFigure 20- , capacitors, inductors) and active (OTFT and diode) devices cells have been designed for the full inkjet process developed in the project. While for CPI (example in Figure 21) and CSEM technologies, device libraries only contain the OTFT cells.

Technology: TDK4PE			*Library:* PASSIVE_TDK4PE			
Cells type: Basic device			*Dev. Strategy:* PCell			
Cell name: rlin_lw						
Cell Function: linear strip resistor						
Available views:	*Pcell* ☑	*Symbol* ☑	*Model* ☑ lr			
	Available layouts:	*CleWin / Mask Engineer* ☐	*Glade* ☑			
Pcell Parameters:	**w:** strip width **wcon:** contact pad width **l:** strip length **lcon:** contact pad length (all units in um)					
Dev. Process	Design ☑	Prototypes Measurement ☑	Param. extraction & model dev. ☑	DK integration ☑	Sim. vs Measur. results validation ☐	OK & ready ☐
Examples (layouts)						
Parameters: w=400, l=1000 wcon=2000, lcon=750			*Parameters:* w=200, l=1000 wcon=1000, lcon=750			

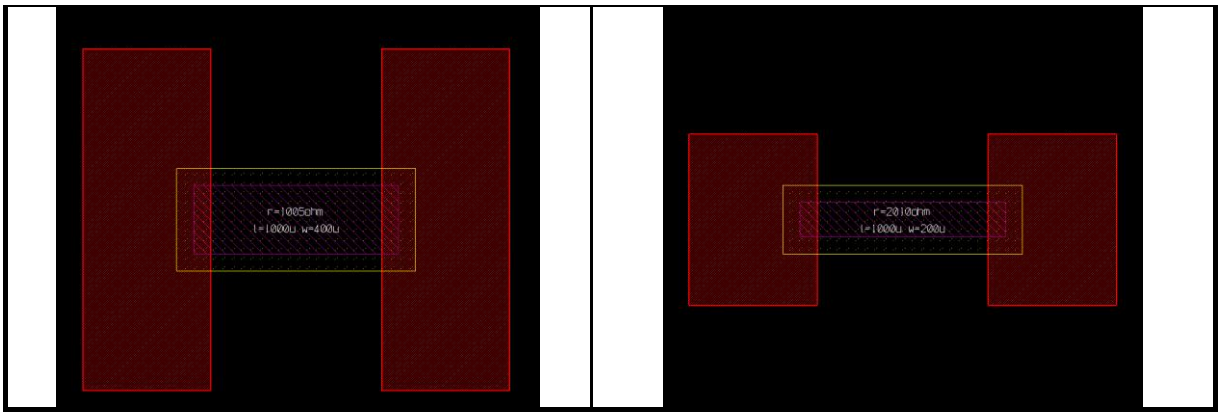


Figure 20. Example of data sheet for the resistor pCell will all parameters considered in its description

Technology: CPI			*Library:* ACTIVE_CPI (interdigitated)		
Cells type: Basic device			*Dev. Strategy:* PCell		
ell name: inter_otft					
Cell Function: multi-fingered OTFT					
Available views:	*Pcell* ☑	*Symbol* ☑	*Model* ☑ model_GreenLys_lot31-ngspice		
	Available layouts:	*CleWin / Mask Engineer* ☐	*Glade* ☑		
Pcell Parameters:	**l:** channel length **w:** channel width **nf:** number of fingers				
Dev. Process	Design ☑	Prototypes Measurement ☑	Param. extraction & model dev. ☑	DK integration ☑	Sim. vs Measur. results validation ☑	OK & ready ☐
Examples (layouts)					
Parameters: **w:** 80 **l:** 6 **nf:** 8			*Parameters:* **w:** 50 **l:** 6 **nf:** 1		

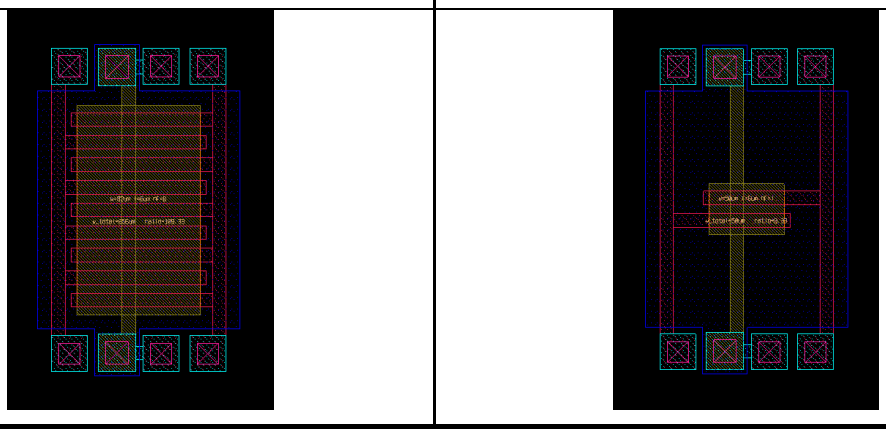


Figure 21. Example of data sheet for the resistor pCell will all parameters considered in its description

One logic cell library has been created in order to be able to cope with the full inkjet process while providing a flexible structure to evaluate the feasibility of the standard cell approach for foils with reduced yield. This library has been implemented allow testing transistors before its final wiring.

Two logic cell libraries have been created addressing CPI technology (one for Corbino and another one for interdigitated transistors). The library was used successfully for designing a small ASPEC circuit and therefore demonstrating the validity of the Standard Cell approach.

One pClell library containing basic cells for transistors (parameterisable combination of load and drive PMOS OTFTs), wiring and I/O Pads has been built and used to implement the Inkjet Gate Array (IGA) bulk structure.

Inkjet Gate Arrays (IGA)

The Inkjet Gate Array strategy has been proposed in order to cope with the reduced yield in terms of working transistors per foil. The IGA structures are derived from classical silicon gate array (GA) strategies. In IGAs, by wiring only known good OTFTs (KGOs) using digital printing (inkjet or aerosol), we can obtain high yield circuit at the cost of testing the foils.

As for classical GA or FPGA, circuit implementation consists in two steps: (1) the fabrication of the GA bulk consisting in transistors and general interconnection and (2) the customization of the GA to implement any given function, by wiring transistors and interconnections to produce circuits. These processes have different complexity. Fabrication of GA bulk requires implementing all process steps to build transistors, while GA customization requires only printing metallic layers and related dielectrics that are much simpler, and therefore with simpler equipment. Furthermore, both processing steps can be done in different places and different time frames.

IGA approach differs from classical GA approach in the fact that the direct printing capabilities offered by inkjet processes allow a different personalisation for every circuit that will be used for the personalization processes in order to connect only their own KGOs. Two additional steps are specific for this IGA structures:

Step 1. Testing the OTFTs in the foils produced after bulk fabrication for marking the KGOs. The output of this step will be a file related to each specific foil (both labelled with the corresponding ID) that identifies the OTFTs that work in this foil. These files will reflect the inherent statistical variability given for the fabrication process.

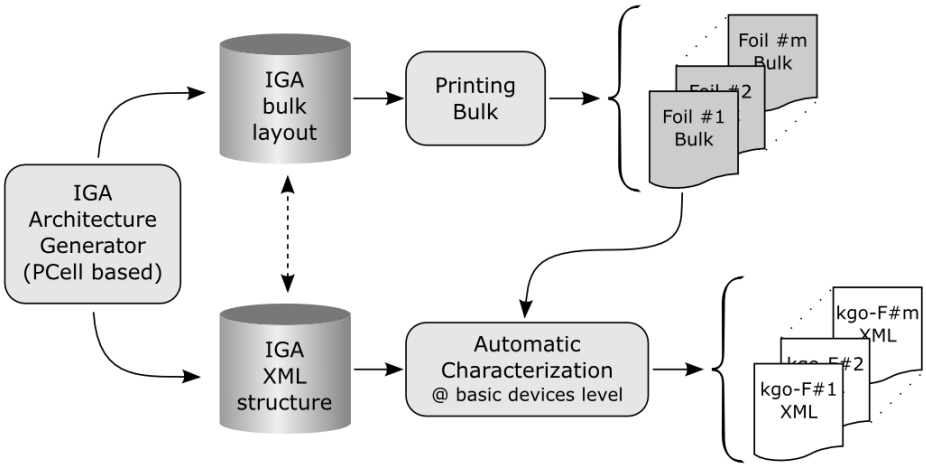


Figure 22. IGA Known Good OTFT (KGO) generation flow

Step 2. Generation of the personalization layers for printing the circuit connectivity in the customization process. Metal layers that implement customization have to take into account both the structural arrangements of groups of OTFTs for building gates and the geometrical topology designed for global placement and routing of the OTFT placed in the foil and its KGO map.

Main difference from the IGA to the current GA strategies refers to the management of the map of KGO coming from foil testing. This would require and differentiated synthesis process for every foil having a different failure map. Since bulk IGA foils and its testing are fabricated and stored. The automatic generation of the wiring on every foil to implement a given circuit can be included to the EDA tool and generate all required files before its final customization, thus becoming a real-time process.

Synthesis steps required for IGA personalization for every foil are reused from current EDA tools. Circuit synthesis from its high level description (i.e. in Verilog) produces a netlist of Boolean functions. Existing technology mapping of Boolean functions to logic gates is implemented according to the available OTFTs. Placement of logic gates of different types can become a complex process depending on the OTFT fabrication yield. Pre-routing to asset on the available connectivity according to the KGO map on p-type OTFTs.

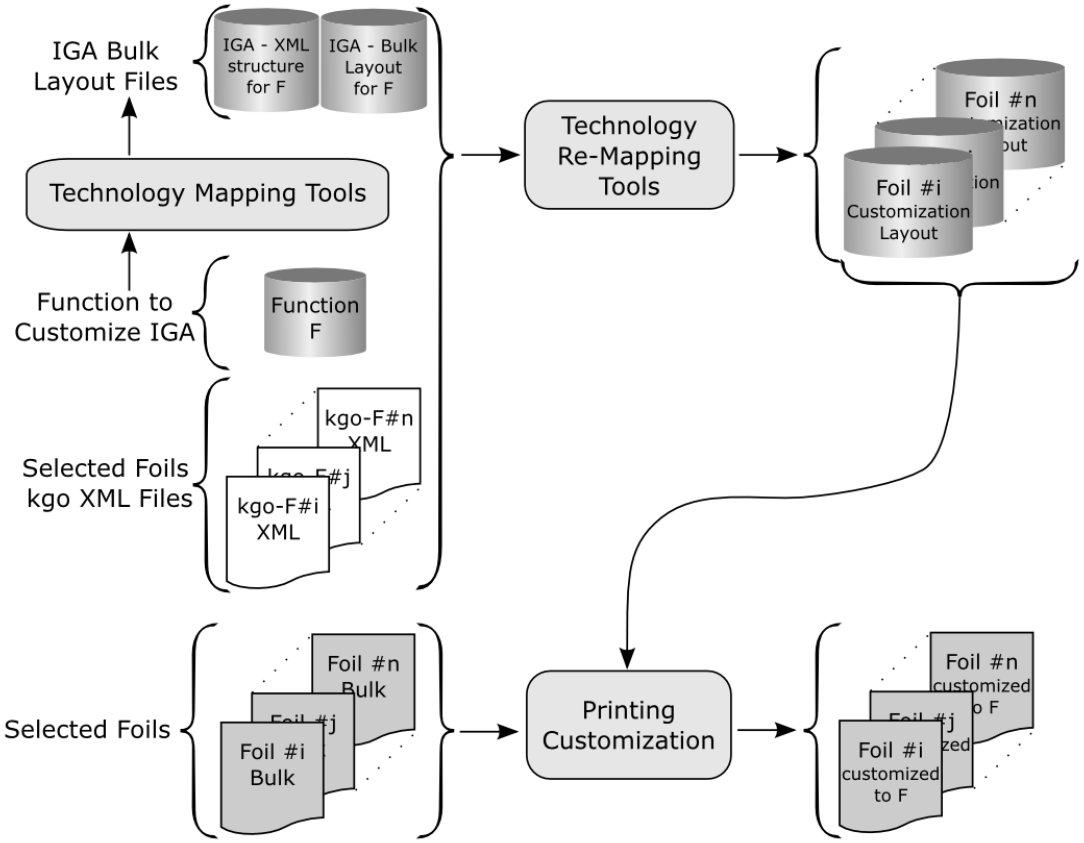


Figure 23. IGA customization steps

Following this strategy we intend to produce high yield circuits from foils that have reduced yield for OTFTs. Of course, this OTFT yield will limit the amount of available transistors and therefore the complexity of the circuit to be implemented. This is equivalent to say that for a given circuit, foils require an overhead of OTFTs. This overhead is related to the mean yield of OTFTs as a multiplying factor to the specific number of OTFTs required for every circuit that can be obtained from logic synthesis. It seems clear that the cost paid for this overhead is compensated by the higher yield obtained.

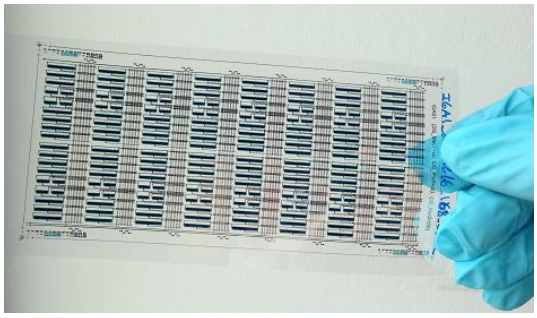


Figure 24. Full inkjet IGA Bulk

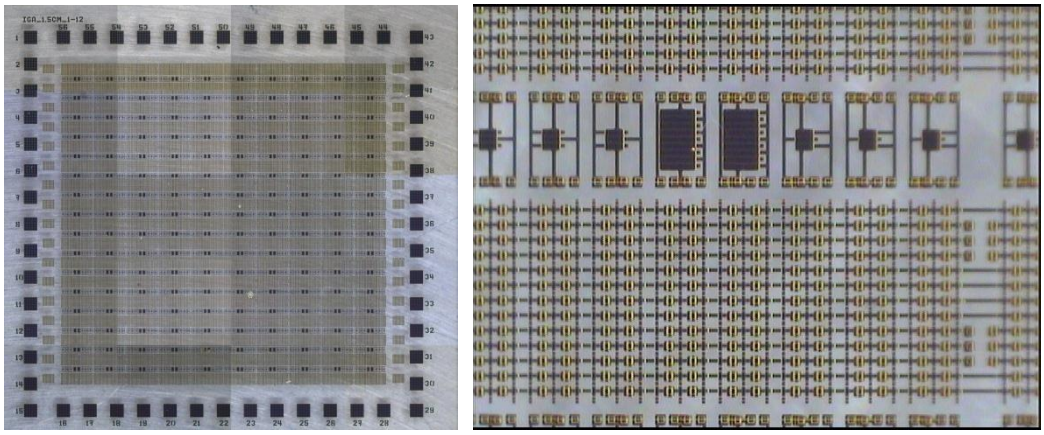


Figure 25. Views of evaporated IGA Bulk (CPI process)

IGA structures have been built for full inkjet process (<200 OTFTs in Figure 24) and evaporation (<2000 OTFTs in Figure 25). The high density of the CPI technology also encouraged us to implement gate array structures. Since the reported yield for CPI is high (all tested foils show yield above 90%) and the processing time is relatively low compared with silicon processes, the gate array approach is also valid since it can also offer shorter personalization times by using 3 different technologies: Mask-based personalization, using 2 further masks for metallization and encapsulation, and Digital printing personalization using either Super-fine inkjet technology (~5 um resolution) or aerosol (~10 um resolution). Having these options in mind we designed 3 different gate array structures with different complexities (presented in D1.2.3, D1.2.4 and D1.2.5).

In order to validate the IGA approach, and therefore the capability to build circuits from arrays of transistors and wires, we inkjet wired series of working inverters so that we can observe the propagation of the digital signal all through the chain. Figure 26 shows the circuits tested for interdigitated transistors.

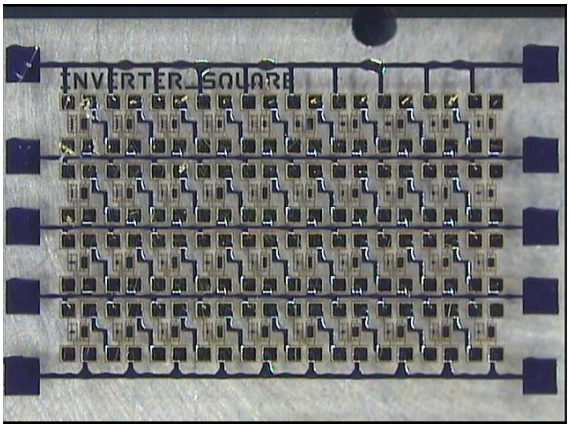


Figure 26. Example of inkjet wiring to build chains of inverters on top of CPI OTFT foils

The series of output DC transfer levels allow us to observe (Figure 27) the signal regeneration in intermediate stages while some of the inverters show non symmetrical DC transfer curve (i.e. inverter #9) due to the inherent process variability.

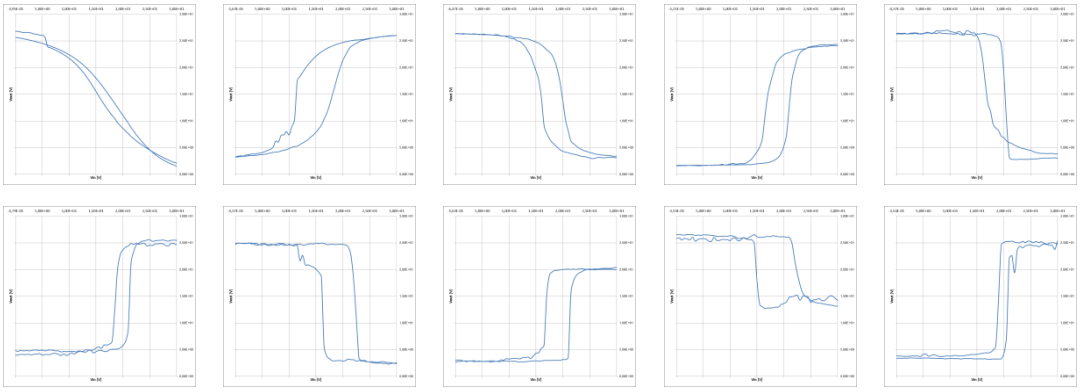


Figure 27. DC transfer characteristic measured for all inverters in the chain

The high variability at transistor level affects the DC behavior (as shown in previous figure) and therefore it is difficult to implement logic gates other than inverters. This is the main reason why only few of the implemented nand/nor2/3 gates have been working properly before the end of the project and also the reason why the any of the fabricated circuits were working properly. This circuit demonstrator implementing the combinational function related to the TicTacToe game (147 OTFTs and 30 I/O pads) that has been designed using our own standard-cell library and fabricated at CPI.

As a global conclusion, the validation of the Technology & Design kit was only achieved at physical and full-custom level but not at cell level where that validation only reached logic inverters and inverter chains.

Furthermore, the TDK4PE philosophy has been promoted and some foundries started announcing design kits but none on them is yet available what, in our opinion, limits the widespread of OLAE technologies.

2. POTENTIAL IMPACT

The impact of the project is strongly linked to the capability of the printed electronics technologies to find a place in the electronics applications market. Several initial applications are being deployed using mainly the systems flexibility as a driver. Different domains are considered as niches for the TDK4PE partners: eHealth and wearable electronics, human interaction, gaming and leisure, automotive and transport. As soon as these success cases increase and the domain attracts new actors that will demand facilities on both technology and design offers. Also the materials and equipment providers are considered as customers of the results obtained at the project.

Every partner approached individually their exploitation model while several of then are pursuing new initiatives to continue progressing in the domain.

2.1. Exploitation of results

2.1.1. UAB

The focus of UAB will be: (i) the support to regional industries, start-ups and public initiatives to build sustainable business models around printed electronics, (ii) the scientific dissemination of the results and the collaboration with the research community and (iii) the training on specialized skills on printed electronics, at all higher education levels (BsC, MsC, PhD) and also to the industry.

At UAB we plan to exploit project results coming from all technical work-packages.

WP2: we plan to continue promoting the methodology to build Technology Design Kits, through:

- Maintaining, evolving and diffusing the full-inkjet TDK.
- Keeping collaboration with CPI and CSEM to maintain, evolve and use their TDK.
- Offer a service, together with CSIC, for building TDKs for any OLAE process interested.
- Continue the standardisation initiative on data formats for technology design kits already proposed in IEC TC 119.
- Programming training events, at least by repeating yearly the OTFT Circuit Design course.

WP3: The knowledge and experience acquired in designing, implementing characterizing and analysing fabrication processes and in materials formulation and validation, will be offered to the industry in terms of consultancy services, R&D projects, IP exploitation and specialized training.

WP4: We plan to exploit the capabilities to build cells, cell libraries and inkjet Gate Arrays in a highly productive way due to its intensive automation for providing IP-cores to end- users in the available technological processes such as TUC, CPI, CSEM, CEA or any other interested.

WP6: We plan to continue building the demonstrator up to its finalization with both technologies full-inkjet and CPI to later analyse their exploitation or the development of similar products (textile-based) by implementing a CoO analysis.

Generally speaking we plan to merge our technological methodology with the model developed and validated in the COLAE framework: Services like CoO analysis, Prototyping, Feasibility Studies, Industrial Design Training or access to external foundries. We also plan to join regional initiatives on entrepreneurship.

2.1.2. ENEA

The exploitation strategy adopted by ENEA is based on the exploration of the printing platform developed within TDK4PE to create products for a wide range of organic electronic applications through the rotes of the Research & Development and the Education.

In the R&D sector for Printed Electronic ENEA focuses on:

- Development of printing process and pre- and post-printing surface treatment technologies for functional layers,
- Advance on new printed buffer-layers to improve the interfaces,
- Progress in definition of new device architectures.

ENEA offered the know-how acquired on these topics to microelectronics based-industry, mainly the local ones, by means of seminaries and laboratory training. The aim is to promote further strengthening and development in printing capabilities to be applied in transversal manner among different application fields. The knowledge on the field of inkjet printed electronics gained in TDK4PE allowed to transfer this technology, in terms of materials, architectures and process, towards other research areas, like photovoltaics sensors and optics.

Moreover, the competences developed in TDK4PE have been the tool to the definition of the contents and objectives related to the printing in currently active national projects.

As future action, ENEA plans to perform an industrial/commercial exploitation of R&D results through the Enterprise Europe Network - database (ENEA Bridgeeconomies - Southern Italy node), a key tool to promote developed technology/processes among interested PMIs and Research organizations.

In the Education area ENEA had and plans to have:

- Specialized courses (Masters/PhD level, open courses) in national academic institutions,
- Specialised training: seminars addressed to industry personnel.
- Courses/seminars in the framework of regional and regional projects developing topics related to solution-processable materials and printed electronics,
- Internal seminars.

ENEA, through these education tools, intends to make known the potentialities of inkjet printing technology to academic and industrial audiences. This dissemination action is aimed to support the students both in the knowledge and the vocational guidance, to guide the industrial realties in the marketing choices.

2.1.3. FXK

Flexink intend to exploit their development of high mobility semiconducting formulations to assist in enabling full colour, flexible display manufacture as well as integrated circuitry. Our new formulations combine high mobility with uniform processing characteristics, which is required for high volume manufacturing, thus opening up a wide range of display applications. We will utilise our expertise, further developed in the project in organic semiconductor synthesis, scale-up and formulation development with respect to both large scale production, and sustainable chemistry. The project has enabled Flexink to custom design inks in direct partnership with the end users in the project, which will accelerate their development processes and ensure the industrial relevance of materials and formulation optimisation. These new Flexink tailored semiconductor inks and formulations are positioned for use in a range of deposition processes, and are expected to be leveraged in a range of reflective display modes and other low performance circuitry.

The directly exploitable outputs from the project included; optimised synthetic routes to the large scale production of high performance semiconducting materials; high volume, high performance polymer semiconductor materials; ready to use ink formulations, optimised and customised for the processes developed by the partners. The accelerated learning curve gained on the ability to scale up semiconductor inks and formulations suitable for high volume manufacturing by Flexink in the project has put Flexink at a strong competitive advantage.

The project has enabled Flexink to additionally ensure the industrial relevance of these materials regarding an appropriate price performance point, and formulation optimisation, creating a materials platform, allowing provision of these materials to the broad scope of the emerging plastic electronics market. Our IP has been protected as confidential know-how, on the basis that we have a freedom to opérate position in this área.

2.1.4. IFS

TDK4PE project was a unique experience to reinforce our know-how of organic and printed modeling. With the different technologies developed and provided during the project, Infiniscale team had to work on modeling on different devices, different technologies and especially on different stages of technology maturity.

The team had to use different techniques and tools and develop new ones. From mathematical modeling to semi-physical modeling and also developing new extractors, Infiniscale has today a rich and unique portfolio of solutions to respond to the industry modeling needs.

Introduction of new modelling solutions on the market

TDK project has allowed us to develop the semi-physical solution.

While mathematical modelling is very powerful, but it is not really accepted by the community. Physical modelling, on other side, needs long time to be achieved especially in case of immature technologies. Semi-physical seems then a very good compromise and very appreciated by partners.

Infiniscale will be able to add this solution to its offer. Thanks to TDK, the company could enhance its GreenLys solution and also develop new modelling extractors that reinforce its commercial offer.

Infiniscale plans to invest to complete the semi-physical solution production and bring to the market in Q4 2015. One and a half man/year effort should be needed for the production and the qualification of this tool.

Commercialization and Expected Revenues

We are expecting to start commercialization of new solutions within Q4 2015.

The company has already WW sales representative, which should help preparing the commercialization process. To be noted that we have already started presenting the different solutions at important conferences in US and Asia.

Our sales department expects revenues about $300k for 2016 with a 50% growth for 2017.

Commercial Barriers

We observe that main barrier for such solutions are financial. Main customers are R&D centres who don't seem to dispose of important funding for EDA tools.

However, we believe that modelling is a critical need and minimum funding should be found.

2.1.5. CSIC

PDK building for third party technologies: Technology characterization, technology files generation, library construction, EDA customization can be implemented for different technologies than TDK4PE. IMB-CNM (CSIC) plan to offer the characterization facilities, SW tools and methodologies developed in the current project to other centres working in OLAE technologies within Europe or across the world. Currently, IMB-CNM (CSIC) is working to integrate modelling of devices in its current characterization and extraction flow.

Build our OLAE technology at CSIC: We have started an internal project to set-up a state of the art OLAE technology taking advantage of our clean room facilities. IMB-CNM (CSIC) has the largest clean room facilities dedicated to micro and nanotechnologies in Spain. In two years, IMB-CNM (CSIC) plans to offer OLAE manufacturing processes in the same way that they are currently offered for silicon-related technologies.

Offer a brokerage service (Europractice-like): Starting from the technology developed in the project and the improvements that planned for the following years, IMB-CNM (CSIC) plans to set up a manufacturing service, and later organize and support

customers in multi-project foils like Europractice MPW IC services open to external processes (i.e. TUC, CPI, CSEM,…).

Participate and promote R&D projects developing TOLAE technologies: With the acquired knowledge and the developed procedures and methodologies, we plan to help industrial partners to initiate R&D projects to implement OLAE technologies in their products.

Currently, several regional, national and EU projects are under discussion in the field of OLAE technologies, both with industries and R&D centres.

2.1.6. PHX

Project TDK4PE has brought to PhoeniX Software, as a software supplier for the micro and nano technology marketplace, additional knowledge and proprietary technology developed for the emerging field of printed electronics. Part of this technology is dedicated to printed electronics indeed, however a large part of the developed new capabilities will be applicable for other areas, like microfluidics and integrated photonics (including silicon photonics). Therefore the new developed modules and routines will leverage the existing knowledge and tools on other field in micro- and nanotechnologies.

Summarizing the advancement of PhoeniX Software as a result of this project delivers the following table:

Product / Module	New capabilities	Application area's
CleWin	- Schematic driven design - PDK compatibility	- PE, Microfluidics, Photonics - PE, Microfluidics, Photonics
MaskEngineer	- Auto-routing	- PE, Photonics
PDAFlow API	- Schematic driven design - Spice modelling - Netlist generation	- PE, Microfluidics, Photonics - PE - PE, Photonics

One can see that most of the newly developed capabilities are applicable in other domains as well. This is good news, as it is increasing the exploitation opportunities. First step is to further develop the results from the project into "real" commercial products, including manuals, examples and marketing material. On the short term focus will be on using the schematic driven design capabilities as developed within CleWin for integrated photonics. As a result of this new capability, a full design flow as demonstrated in this project with CleWin and MaskEngineer will be made available for silicon photonics. It is expected that this will deliver a faster return on investment than in the case for the printed electronics market, as more and more activities are being deployed in this area around the world.

Silicon photonics is today transitioning from R&D into volume manufacturing. Prime target for the developed tools will be at first these R&D environments: universities, institutes, innovative SME's and R&D departments of large companies. In the meanwhile marketing effort will be put onto (large) OEM companies, design houses and fabless companies. Geographically it is worthwhile mentioning that especially in North-America

design teams are gearing up to make use of these technologies and are in need of the developed software solutions.

Strategic positioning is important in a market that is in development and where both large (but new to the field players like EDA companies) and small (new start-ups or companies from other optical technologies like digital imaging or solar) are entering the market place. Experience and knowledge are a key asset of PhoeniX Software, going back to the early nineties as one of the first suppliers of design services and software tools for integrated optics. Building on this knowledge and experience and providing best-in-class support to both customers as well as foundries providing the technology brings added value that is recognized and valued. This unique position is used in the marketing approach of the software solutions, both to potential new users of the software as well as to potential new foundry partners.

As a result of the newly developed capabilities and additional further development in the next 12 months, we expect that we will grow the team with 3 additional persons at the level of PhD or MSc.

For microfluidics and printed electronics, PhoeniX Software will engage in future collaborative projects and use the experience of this project to feed into these areas and further develop the capabilities. Furthermore PhoeniX Software will create a news release and material at its website to disseminate the project results.

2.1.7. STX

SensingTex exploitation strategy will use two project results that have interest for STX:

- By one hand we see that by using TDK Tools for our existing Printed Electronics Portfolio we are going to improve our time to market as the tools will allow us to prototype for customers in a better way reducing the number of trials before reaching the final results. So we see the end of 2014 as the starting point to introduce in our business Offering based on Pressure Sensor & Illuminating Textiles, TDK tools for rapid prototyping and product development.
- By another hand we see that by using of TDK Tools for product development and integration of the TDK project Printed Electronic Solutions with ours. The design of new components by using TDK Tools and materials libraries will allow STX to use them as a Demonstrator Kits that will be sold to boost the business. With those samples our partners/customers will be able to grasp the technology and define their final product specification. This approach has been widely used by STX (Pressure Sensor Tex Development Kit, Smart Mat Development Kit, PrevUlcer Develpment Kit) where customers need touch-and-test the technology first. The large revenue will come from the exclusive licensing of the technology and international partnerships in different sectors. This is our plan:
    a. 2015 first semester: Starting Business in Europe of product integration of passive components: (1) Printing resistances on Switch Sensor Tex. (2) Product for a new 2 wires keypad sensor Solution.
    b. 2015 second semester: Starting Business in Europe of active components:

c. (1) Printing Diodes on Pressure Sensor Tex to avoid the "Ghost Key" effect on piezoresitive Pressure Mapping. (2) Printing Transistors on Pressure Sensor Tex for basic products

Internal IP portfolio and third party portfolio

STX is already working with IP to integrate its technology into different product applications. From the Medical to the Sport Sector, Sensing Tex currently work together with international key partners, the IP is mainly concentrated on its Printed electronics Pressure Mapping technology.

STX owns some patents of Pressure Mapping on touch pressure sensitive textiles:

1. PCT/ES2007/000383 "**Torsion and/or Tension And/or Pressure Textile Sensor**"

2. Patent Granted 201231047 "**A LARGE-AREA EXTENSIBLE PRESSURE SENSOR FOR TEXTILES SURFACES**"

3. P 201331341 "**Textile Piezo-resistive Sensor and Heart rate and respiration rate detection system**"

We know through our patent research of our competitors that there is room on pressure mapping to integrate more components like resistors and diodes in a Large Area Sensor in matrix topology including pressure, temperature and moisture among others based on printed electronics and fully stretchable solutions, this is one of main challenge in this field and there is a freedom to act and operate within this IP. So, in this sense we plan to apply a new patent World Patent Application:

"**PRINTED ORGANIC THIN FILM PRESSURE SENSOR AND LOGIC UNIT**"

Investments, developments and test to bring the solution to market

STX plans some investments that will be needed after the end of the project to bring the intermediate demonstrator kits based on the TDK to on specific market in three different stages:

1. Early stage of Product Commercialization of the Development Kit: In 2015, STX expects to invest € 50k for a first phase of commercialization that will include employment and a commercial budget for commercialization, this commitment will be funded by the capital. It is expected to have sales of around € 150k (As experimented with previous development kits like PevUlcer Development Kit), which would produce a gross profit of € 75k€ that will be reinvested for the next phase. In this phase Partners will pay for the engineering services to integrate our development kit into their products.
2. Product Commercialization: In 2016, the growth is expected to be around 100-200%, giving a gross margin of 50 % that will cover 100% of the initial investment.
3. Maturity Stage of Commercialization: From 2017 is expected to close the first licenses and production batches could be more that € 1M approx. as a starting point.

Expected Revenues and Commercial Barriers

As commented in the previous paragraph revenues are expected the third year after starting commercialization and will be the sixth technology development kit of the company.

The proposed technology Kit may become very complex and so a costly solution. Specific customer solution will probably end up with less sensor areas, less components and more easly to design through TDK with a simplified electronic and limited power consumption respect to first product launch (the Demonstration Kit). For those reasons, it is expected that STX will act as an expertise solution provider able to adapt the needs to the customer targets including price and work together in a long partnership even after the end of this project (including some project partners within the consortium). STX will need to provide quick solution which is one of the strong skills at the company and continue the efforts to reduce power consumption and make those devices applicable in different fields.

Case Study

Considering the range of products possible with the new technology which is equivalent to the current ones, it is expected a 80% of World Wide market share for Pressure Mapping products (with other passive and active printed components) in the first 5 years which will probably decrease later when competition appears. The success of the technology exploitation highly depends on the industrialization phase just after this project ends and the capacity of our company to offer quick customizations.

2.1.8. TUC

For TUC, the gathered experience and knowledge brings an important benefit to the institute's know-how as well as the printed electronics community in Europe. We could demonstrate a manufacturing concept based on solely inkjet printing and manufactured ten thousands of transistors and other electronic devices. This is unique within Europa and increases the competences of TUC. Due to the project, several industrial cooperations were developed. E.g. a research cooperation with Heraeus Noblelight – the leading manufacturer for IR emitters. The cooperation resulted in a joint development of a new drying and sintering strategy for deposited layers within the field of printed electronics. In addition, a new industrial project was established between TUC and Heraeus thanks to the growing inkjet competence of TUC. A cooperation was also developed with the Altana Group Elantas for the development of special dielectric materials for printed electronics and with the company PVnanocell concerning the optimization of silver ink formulation for inkjet printing. All the research cooperations were successfully in terms of the development or optimization of products for customers demands.

The knowledge will be also implemented in the student education. Lectures are in preparation for master students of the course Print and Media Production. Furthermore, parts of the developments within TDK4PE will contribute to the submission of at least two doctoral thesis of involved researchers.

Next to the developed manufacturing approach for S2S technology including pre- and post-treatment methods as well as material knowledge, TUC will finalize the R2R

technology development together with 3DMM. This will improve both the machinery and the competences at TUC and 3DMM. The machinery will be upgraded with inkjet printing resulting in a hybrid system.

TUC will publicly offering fabrication runs based on the developed inkjet process for external partners using the developed design kits and EDA tools. A new webpage was designed (http://bpr.mb.tu-chemnitz.de/ij-technikum/index.php) where we provide services for external partners based on our printing equipment and developed printing process. The offering of fabrication runs for printed electronics will be added soon showing also the link to UAB and CSIC for stressing the design kits and EDA tools. This will allow to continue the close collaboration with UAB and CSIC.

2.1.9. UALG

The knowledge gained with TDK4PE project brought a number of benefits for the organic electronics group based at UAlg, at the academic level and also with Portuguese industry.

TDK4PE contributed strongly for the involvement of the students in the integrated Master course in Electronics and Telecommunication with printing technology to fabricate electronic circuits. Last year, one student concluded his Master thesis entitled "Electrical characterization of electronic circuits produced by inkjet printing". In the current year two students choose to carry their Master Thesis also on the topic. Several internal seminaries and workshops contributed to the dissemination of the technology among undergraduate and postgraduate student community.

The group was also invited to present their results and achievements at the annual meeting of the Organic Electronics Association held in Portugal, Vila-Nova de Famalicão, on March 2013. Contacts were then established with the Center for Nanotechnology and Smart Materials (CENTI) and with other Portuguese companies interested in developing high-tech textiles for the automotive industry. As result of these efforts, a join national research proposal will be submitted in the next call (January 2015) organized by the Portuguese Foundation for Science and Technology (FCT). This contributed to strength our collaboration with companies.

2.1.10. 3DMM

Within TDK4PE the company 3DMM could gather a lot of knowledge in the field of inkjet printed electronics. Although the target of R2R printed transistors could not be realized due to the transfer of efforts towards the S2S based technology the company made significant efforts on the actual integration of inkjet print heads. Especially the development of post-treatment steps such as IR drying optimized for the printed materials was an important advantage for the company. With the experience gained in TDK4PE 3D-Micromac could strengthen its competitiveness and position as one of very few companies, if not the only, fabricating roll-to-roll tools for flexible electronics and offering solutions based on the combination of a multitude of additive and subtractive processes.

To increase the economic impact of the developments the company has started to transfer technologies, including inkjet printing, to further markets such as PV, medical technologies and ophtalmics.

As the further development of printed electronics is not easy to predict 3DMM's sales department takes a conventional approach to this market expecting one machine sale per year adding an average of 1.5 Mio. € to the annual turnover.

Based on the future exploitation of other markets an additional increase of 1 Mio € per year is expected starting on 2016.

2.2. Additional Data

2.2.1. Address of the project public website

The public website is located at http://www.tdk4pe.eu

2.2.2. Relevant contact details

Partner	Web site	Contact Name	Address	Email
UAB (1)	**http://www.uab.cat**	Jordi Carrabina	CEPHIS. Escola d'Enginyeria. Campus UAB. 08193 Bellaterra. Spain	Jordi.carrabina@uab.cat
ENEA (2)	**http://www.portici.enea.it** **http://uttp.enea.it/index.asp?p=7&t=Nanomateriali%20e%20Dispositivi**	Fulvia Villani	ENEA Research Centre Portici P.le E. Fermi, 1 80055 Portici (NA) – Italy	fulvia.villani@enea.it
FXK (3)	**www.flexink.co.uk**	Iain McCulloch	Flexink Dept. of Chem. Imperial College London, SW72AZ, London, UK	Iain.mcculloch@imperial.ac.uk
IFS (4)	**http://www.infiniscale.com**	Firas Mohamed	Infiniscale. 186, Chemin de l'étoile, 38330 Montbonnot St Martin, France	Firas.mohamed@infiniscale.com
CSIC (5)	**http://www.imb-cnm.csic.es/index.php?lang=en**	Lluís Terés	IMB-CNM (CSIC) Til·lers s/n Campus UAB 08193-Cerdanyola (Spain)	Lluis.Teres@imb-cnm.csic.es
PHX (6)	**http://www.phoenixbv.com**	Twan Korthorst	Phoenix BV PO Box 545, 7500 AM Enschede, the Netherlands	info@phoenixbv.com
STX (7)	**http://www.sensingtex.com**	Luis Gomez	SensingTex Passeig Fabra I Puig 474 Local 2 08042 Barcelona (Spain)	Luis.gomez@sensingtex.com
TUC (8)	**https://www.tu-chemnitz.de/mb/DigiTech/professorship.php**	Reinhard R. Baumann	Reichenhainer Str. 70 09126 Chemnitz	Reinhard.baumann@mb.tu-chemnitz.de
UALG (9)	**http://w3.ualg.pt/~hgomes/** **http://w3.ualg.pt/~hgomes/html/Projects/european_projects.htm**	Henrique L. Gomes	Universidade do Algarve, FCT Campus de Gambelas 8000-139 Faro, Portugal	hgomes@ualg.pt
3DMM (10)	http://**www.3d-micromac.com**	Maurice Clair	3D-Micromac AG Technologie-Campus 8, 09126 Chemnitz	clair@3d-micromac.com

3. Use and dissemination of foreground

A plan for use and dissemination of foreground has been executed.

3.1. General Dissemination

All TDK4PE partners have been active in the dissemination of the results obtained in the project to the different stakeholders in organic electronics and related field (textile and smart object industry, electronic design automation industry, etc-).

Partners have been present in many specialized conferences in Europe and worldwide. Industrial partners promoted also activities in specific fairs.

Parts of the format and methodology developed in TDK4PE are promoted as NWI in the TC119 IEC/IEC standardization committee.

This section includes two different tables:

- List of all scientific (peer reviewed) publications relating to the foreground of the project.
- List of all dissemination activities (publications, conferences, workshops, web sites/applications, press releases, flyers, articles published in the popular press, videos, media briefings, presentations, exhibitions, thesis, interviews, films, TV clips, posters).

These tables are cumulative, which means that they show all publications and activities from the beginning until after the end of the project.

LIST OF SCIENTIFIC (PEER REVIEWED) PUBLICATIONS, STARTING WITH THE MOST IMPORTANT ONES										
Nº	**Title**	**Main author**	**Title of the periodical or the series**	**Number, date or frequency**	**Publisher**	**Place of publication**	**Year of publication**	**Relevant pages**	**Permanent identifiers[1] (if available)**	**Is/Will open access[2] provided to this publication?**
1	Geometric Design and Compensation Rules Generation and Characterization for All-Inkjet-Printed Organic Thin Film Transistors	E. Ramon	Journal of Imaging Science and Technology	Volume 57, Number 4,	IS&T	Springfield, VA	2013	40402-1-40402-12(12)	http://dx.doi.org/10.2352/J.ImagingSci.Technol.2013.57.4.040402	No
2	Inkjet Patterning of Multiline Intersections for Wirings in Printed Electronics	E. Diaz	Langmuir	29 (40)	ACS	Washington	2013	12608–12614	DOI: 10.1021/la402101d	No
3	Inkjet-Printed Organic Electronics: Operational Stability and Reliability Issues.	H. Gomes	ECS Transactions	53 (26)	The Electrochemical Society	New Jersey	2013	1-10	DOI: 10.1149/05326.0001ecst	No
4	All-inkjet printed organic transistors: dielectric surface passivation techniques for improved operational stability and lifetime	H. Gomes	Submited to Microelectronics realibility	-	Elsevier	Atlanta, GA	-	-	-	

[1] A permanent identifier should be a persistent link to the published version full text if open access or abstract if article is pay per view) or to the final manuscript accepted for publication (link to article in repository).
[2] Open Access is defined as free of charge access for anyone via Internet. Please answer "yes" if the open access to the publication is already established and also if the embargo period for open access is not yet over but you intend to establish open access afterwards.

LIST OF DISSEMINATION ACTIVITIES								
Nº	**Type of activities[3]**	**Main Leader**	**Title**	**Date**	**Place**	**Type of audience[4]**	**Size of audience**	**Countries addressed**
1	presentations	J. Carrabina	"EDA tools & Design Methods for Printed Electronics"	22/05/2012	IEC-TC119 Stardardisation Commitee, Seul	Scientific Community Industry	<100 participants	International conference
2	meetings	J. Carrabina D. Marin	TDK4PE-Flexibility mutual presentations	30/05/2012	Internet	Scientific Community Industry	<10 participants	International conference
3	posters	C. Martinez	"Inkjet Geometric Design Rules Generation and Characterization"	20/06/2012	LOPE-C 2012	Scientific Community Industry	<1000 participants	International Exhibition and conference
4	posters	J. Carrabina	"Improving Circuit Performance by using Cell-libraries for Application Specific Printed Electronics Circuits"	20/06/2012	LOPE-C 2012	Scientific Community Industry	<1000 participants	International Exhibition and conference
5	presentations	E. Diaz	"Inkjet Resistor Design and Characterization"	26/06/2012	ICOE2012 Tarragona	Scientific Community	<100 participants	International conference
6	posters	F. Villani	"Printed polymer-based p-type OTFTs: study of the aging effect on the transistor performances"	26/06/2012	ICOE 2012 Tarragona	Scientific Community	<100 participants	International conference
7	presentations	J. Carrabina	"TDK4PE: Technology & Design Kits for Printed Electronics"	03/07/2012	ISFOE2012 Thessaloniki	Scientific Community Industry	> 600 participating organizations	International conference
8	presentations	M. Ridao	"Self Iluminating Spaces"	17/04/2012	SMART FABRIC CONFERENCE Miami	Industry		International conference
9	presentations	M. Ridao	"Printed Electronic on Textiles"	25/06/2012	ICOE 2012 Tarragona	Scientific Community Industry	<300 participants	International conference
10	presentations	E. Ramon	"Inkjet Geometric Design & Compensation Rules Generation and Characterization",	09/09/2012	NIP 2012, Quebec	Scientific Community	>100 participants	International conference
11	workshops	J. Carrabina	Session OLAE-Manufacturing, Integration and Devices: Achievements, challenges and future perspectives.	08/10/2012	OLAE 2012 Concertation Meeting, Dresden.	Scientific Community Industry		International conference
12	posters	E. Sowade	"Inkjet-printed electronics: Transfer from lab to fab manufacturing",	13/03/2013	Smart Systems Integration, Amsterdam	Scientific Community Industry	> 200 attendees	International conference
13	posters	F. Vila / J. Pallarès	"A complete suite of open/free EDA tools for PE physical design",	18/03/2013	DATE 2013. Grenoble	Scientific Community Industry	> 50 attendees	International conference
14	posters	E. Díaz	"Greek Cross Test Structure for Inkjet Printed Electronics"	Mar-2013	ICMTS 2013, Osaka	Scientific Community		International conference

[3] A drop down list allows choosing the dissemination activity: publications, conferences, workshops, web, press releases, flyers, articles published in the popular press, videos, media briefings, presentations, exhibitions, thesis, interviews, films, TV clips, posters, Other.
[4] A drop down list allows choosing the type of public: Scientific Community (higher education, Research), Industry, Civil Society, Policy makers, Medias ('multiple choices' is possible.

15	presentations	H. Gomes	Inkjet-Printed Organic Electronics: Operational Stability and Reliability Issues. Presentation at ECS Toronto.	12/05/2013	ECS Toronto.	Scientific Community Industry		International conference
16	presentations	M. Ridao	"Self Illuminating Spaces" Presentation	14/05/2013	Smart Lighting Conference 2013	Industry	6000 attendees	International Exhibition and conference
17	Other	A. Bakker	Foundation pda flow has been launched	31/05/2013				International conference
18	Conference	IFS	Thin Film Transistor Compact modelling with TechModeler	02/06/2013 - 06/06/2013	DAC 2013 Austin	Scientific Community Industry	1600 attendees	International conference
19	conference	F. Mohammed	Infiniscale'll exhibit ICLYS , its innovative variability-aware manager, the new standard of Monte Carlo analysis	04/06/2013	DATE 2013 Austin	Scientific Community Industry	over 1,000 submissions	International Exhibition and conference
20	presentations	E. Sowade	Manufacturing of electronic devices using laboratory inkjet printing and basic approaches towards up-scaling.	11/06/2013	LOPE-C 2013 Munich	Scientific Community Industry	1,800 participants	International Exhibition and conference
21	posters	J. Carrabina/ M. Ridao	Top-down approach for building PE products: hybrid textile-plastic luminous touch sensor.	11/06/2013	LOPE-C 2013 Munich	Scientific Community Industry	1,800 participants	International Exhibition and conference
22	exhibitions	R.Kundt	LOPE-C trade fair 3DMM: Presentation of IR drying results of R2R inkjet printed silver using the Heraeus IR module.	11/06/2013	LOPE-C 2013 Munich	Scientific Community Industry	1,800 participants	International Exhibition and conference
23	posters	F. Villani	Photoresponse of all-inkjet-printed organic transistors realized on flexible substrate	17/06/2013	ICOE2013 Grenoble	Scientific Community Industry	<100 participants	International conference
24	posters	F. Vila	Physical design flow for printed electronics based on open/free EDA tools	17/06/2013	ICOE2013 Grenoble	Scientific Community Industry	<100 participants	International conference
25	web	STX	http://sensingtex.com/projects	June 2013	Web	Industry General public	-	Worldwide
26	conferences	J. Carrabina	"TDK4PE: Technology & Design Kits for Printed Electronics"	03/07/2013	ISFOE2013 Thessaloniki	Scientific Community Industry	> 600 participating organizations	International conference
27	publications	E. Ramon	Eloi Ramon, Carme Martinez, J. Carrabina, "Geometric Design and Characterization for all-inkjet Printed Organic Thin Film Transistors"	01/07/2013	Journal of Imaging Science and Technology	Scientific Community Industry		International journal
28	posters	H. Gomes	Assessment of dielectrics for all-ink-jet printed organic thin film transistors.	03/09/2013	ECME2013	Scientific Community		European conference
29	publications	E. Diaz	Inkjet Patterning of Multiline Intersections for Wirings in Printed Electronics.	04/09/2013	Langmuir	Scientific Community		International journal
30	presentations	E. Sowade	Der Inkjetdruck als Beschichtungstechnologie für funktionale Schichtsysteme.	05/09/2013	Werkstofftechnisches Kolloquium. Chemnitz	Scientific Community Industry	180 participants	Local event

31	conference	R. Baumann	Digital fabrication of smart objects based on printing technologies. Invited opening presentation at IARIGAI 2013	08/09/2013	IARIGAI 2013. Chemnitz	Scientific Community Industry	>100 atendees	International conference
32	presentations	J. Carrabina	Design rules checking for printing electronic devices: concept, generation and usage	08/09/2013	IARIGAI 2013. Chemnitz	Scientific Community	>100 atendees	International conference
33	publication	H. Gomes	Inkjet-Printed Organic Electronics: Operational Stability and Reliability Issues.	01/10/2013	ECS Transactions	Scientific Community Industry		International Journal
34	exhibition	R.Kundt	Presentation of IR drying results of R2R inkjet printed silver using the Heraeus IR module.	18/10/2013	ILACOS Asia	Industry	150 atendees	International exhibition
35	Other	M. Ridao	Meetings with USA tech companies i.e. Polyera	20/10/2013		Industry		
36	conference	M. Ridao	"Self Illuminating Spaces"	29/10/2013	Smart Fabrics Europe 2013. Barcelona	Industry	120 delegates	International conference
37	conference	IFS	"GreenLys: unique tool for Thin Film Transistor Compact Modeling"	20/11/2013 - 22/11/2013	EDS Fair 2013. Yokohama	Industry	22000 visitors	International Exhibition
38		R. Baumann	Digital Manufacturing of printed Smart Objects	21/11/2013	Swiss ePrinting.	Scientific Community Industry		International conference
39	publications	F. Vila	PDK development for Printed/Organic Electronics based on XML	27/11/2013	Proceedings DCIS2013. San Sebastian.	Scientific Community	150 participants	International conference
40	publications	E. Ramon	Pcell based devices & structures for Printed Electronics and related semiautomatic characterization loop	28/11/2013	Proceedings DCIS2013. San Sebastian	Scientific Community	150 participants	International conference
41	conference	R. Baumann	Digital Fabrication of Smart Objects by Printing Technologies (keynote)	04/12/2013	Semicon Japan.	Scientific Community Industry	60000 attendees	International Exhibition and conference
42	presentations	E. Ramon	A standard-cell approach for all-inkjet OTFT digital circuits	23/01/2014	ITC- 2014 program	Scientific Community Industry	150 participants	International conference
43	presentations	J. Carrabina	Contribution to the IEC TC-119 standardization comitee	17/03/2014	Meeting minutes	Scientific Community Industry	>100 atendees	
44	Other	N. Olij	All legal issues of the PDAflow foundation have been finalized	April 2014	Internal report			
45	Other	N. Olij	PHX has intensified cooperation with Mentor Graphics and entered the Open Door program (http://www.mentor.com/company/partner_programs/opendoor/) to further integrate PDAflow activities in the EDA tool chain.	April 2014	Internal report			
46	conference	STX	New Manufacturing Challenge	12/05/2014 – 14/05/2014	W2NYC	Industry		International Conference
47	presentations	J. Carrabina	INKJET GATE ARRAY: Novel concept to implement electronic systems	26/05/2014	Lope-C 2014 Munich	Scientific Community Industry	2,134 visitors	International Exhibition and conference

48	presentations	F. Vila	Semi-automatic PE Technology & Device Library Characterization for PDK Development"	26/05/2014	Lope-C 2014 Munich	Scientific Community Industry	2,134 visitors	International Exhibition and conference
49	presentations	K. Mitra	Inkjet-printed diodes based on metal-insulator-semiconductor (MIS) structure for rectifying application in flexible electronics	26/05/2014	Lope-C 2014 Munich	Scientific Community Industry	2,134 visitors	International Exhibition and conference
50	presentations	D. Weise	Inkjet printing and intense pulsed light sintering of nanoparticle silver patterns – Influence of flashing parameters and substrate	26/05/2014	Lope-C 2014 Munich	Scientific Community Industry	2,134 visitors	International Exhibition and conference
51	posters	E. Sowade	Manufacturing of thin-film transistors using industrial inkjet printheads	26/05/2014	Lope-C 2014 Munich	Scientific Community Industry	2,134 visitors	International Exhibition and conference
52	conference	IFS	Semi-physical TFT compact modelling	02/06/2014	DAC 2014. San Francisco	Scientific Community Industry	1600 attendees	International conference
53	Presentation	E. Sowade	http://www.tu-chemnitz.de/mb/PrintMedienTech/loadframe.php?token=lectures&type=stlect	17/06/2014	Media Technology Colloquium TU Chemnitz	Scientific Community and guests from Industry	30 attendees	Lecture course for international students
54	presentation	K. Mitra	http://www.tu-chemnitz.de/mb/PrintMedienTech/loadframe.php?token=lectures&type=stlect	24/06/2014	Media Technology Colloquium TU Chemnitz	Scientific Community and guests from Industry	30 attendees	Lecture course international students
55	Other	UAB & CSIC, Niels Olij	Course "Organic Thin Film Transistors Circuit Design"	30/06/2014	UAB facilities	Scientific Community Industry	12 attendees	International course
56	presentation	K. Mitra	Potential up-scaling of Inkjet-printed devices for logical circuits in flexible electronics	09/07/2014	ISFOE 2014 Thessaloniki	Scientific Community Industry	> 600 participating organizations	International conference
57	presentation	D. Weise	Inkjet printing (S2S) of Conductive Structures & Functional Devices	09/07/2014	ISFOE 2014 Thessaloniki	Scientific Community Industry	> 600 participating organizations	International conference
58	presentation	K. Mitra	Inkjet Printing of functional devices e.g. organic TFT´s and towards circuits	09/07/2014	ISFOE 2014 Thessaloniki	Scientific Community Industry	> 600 participating organizations	International conference
59	presentation	E. Sowade	Inkjet printing of electronic devices - challenges and achievements;	26/08/2014	Co-Up Workshop	Scientific Community Industry	> 30 attendees	Project Workshop
60	presentation	E. Ramon	Large-Scale Fabrication of All-Inkjet Printed Organic Thin Film Transistors: a Quantitative Study	08/09/2014	NIP30. Canada.	Scientific Community Industry	> 20 attendees	International conference
61	Presentation	R. Zichner	Inkjet printing and sintering techniques of functional layers for electronic applications	30/09/2014	TheIJC.com	Scientific Community Industry	300 attendees	International Exhibition and conference

3.2. Section B

This section specifies exploitable foreground and provides the plans for exploitation. All these data is public (except the marked confidential in tables) and intended to demonstrate the added-value and positive impact of the project on the European Union.

3.2.1. Part B1

The applications for patents, trademarks, registered designs, etc. is listed.

B1: LIST OF APPLICATIONS FOR PATENTS, TRADEMARKS, REGISTERED DESIGNS, ETC.					
Type of IP Rights[5]	**Confidential Click on YES/NO**	**Foreseen embargo date dd/mm/yyyy**	**Application reference(s) (e.g. EP123456)**	**Subject or title of application**	**Applicant (s) (as on the application)**
1	YES	Q4 2015		Semi-physical compact modelling for printed electronics	Infiniscale
2	YES	Q4 2015		Printed circuitry on textile backing with logic components	SensingTex

[5] Note to be confused with the "EU CONFIDENTIAL" classification for some security research projects

3.2.2. Part B2

Type of Exploitable Foreground[6]	Description of exploitable foreground	Confidential Click on YES/NO	Foreseen embargo date	Exploitable product(s) or measure(s)	Sector(s) of application[7]	Timetable, commercial or any other use	Patents or other IPR exploitation (licences)	Owner & Other Beneficiary(s) involved
Commercial exploitation	Schematic drive layout capability	YES	31.03.2015	CleWIn Schematic / CleWin_DK	Printed electronics, Microfluidics, Integrated Photonics	Q3-2015 and onwards	-	Phoenix
Commercial exploitation	Auto-routing	NO	-	MaskEngineer and OptoDesigner auto-routing module	Printed Electronics, Integrated Photonics	Q2–2015 and onwards	-	Phoenix
Possible commercial exploitation of R&D results	Printed electronics circuitry and components	NO	-	Printed textile sensors	C.13.9.6 Textile electronics	Q4 2015	Possible patent on printed electronic textiles	SensingTex
Possible commercial exploitation of R&D results	Printed electronics compact modleing	NO	-	GreenLys XL	Organic devices compact modelling	Q4 2015	Intend to submit a patent on semi-physical modeling	Infiniscale
Technical expertise	Service of build-on-demand Technology Design Kits	NO	-	Service to OLAE process interested	Printed electronics, LASS, SIO	>2015	-	UAB, CSIC
Technical expertise	OTFT electrical characterization, Parameter extraction, statistical analysis & modelling	NO	-	Service to Industry and R&D (university and RTO) , education	Fabless designers, LASS and SIO	>2015	-	UAB
Technical expertise	Standardization on data formats for TDKs (proposed IEC TC 119)	NO	-				-	UAB

[6] A drop down list allows choosing the type of foreground: General advancement of knowledge, Commercial exploitation of R&D results, Exploitation of R&D results via standards, exploitation of results through EU policies, exploitation of results through (social) innovation. 20

[7] A drop down list allows choosing the type sector (NACE nomenclature) : http://ec.europa.eu/competition/mergers/cases/index/nace_all.html

General Advancement of knowledge	Organization of specialized training and courses, masters, thesis,..	NO	-	Service to Industry and R&D (university and RTO) , education		>2015	-	UAB, ENEA, UAlg, TUC
Single process development	Maintaining, evolving and diffusing the full-inkjet TDK	NO	-	Dissemination and promotion of TDK tools.			-	UAB, Phoenix
Technical expertise	Fabrication of RUNs, prototypes or specific devices using the developed design kits and EDAs	NO	-	Service to R&D (university and RTO). Technology transfer to Industry		>2015	-	UAB, TUC, ENEA
Technical expertise	Provide IP-cores to end-users	NO	-	Service to R&D.		>2015	-	UAB
Technical expertise	Consultancy/Brokerage services about PE	NO	-	Service to Industry and R&D (university and RTO)		>2015	-	UAB, CSIC, ENEA, TUC, SensingTex
Possible commercial exploitation of R&D results	Manufacturing of suitable printing materials for PE	NO	-	OSC, dielectric inks.	Printed Electronics manufacturers market	>2015	-	Flexink
General Advancement of knowledge	Optimization and customization of synthetic routes, OSC, dielectrics and processes	NO	-	Material benchmarking		>2015	-	Flexink
Planned Investments	Build an OLAE technology unit	NO	-	Facilities improvement and/or company/group expansion.		>2015	-	CSIC
General Advancement of knowledge	Participate and promote R&D projects developing OLAE technologies	NO	-	R&D projects, contract research		>2015	-	CSIC, ENEA, UAB, TUC, UAlg, Phoenix
Commercial exploitation / promotion	Develop project results into commercial or promotional products: marketing material, demos…	NO	-	Promotion and dissemination		>2015	-	UAB, Phoenix, SensingTex

Planned Investments	Expected increase in workforce	YES	-	Facilities improvement and/or company/group expansion.		>2015	-	Phoenix
Possible commercial exploitation of R&D results	Use TDK tools for optimizing prototype manufacturing	NO	-	TDK tools for rapid prototyping and product development		2014	-	SensingTex
Planned Investments	Needed for bringing TDK demonstrator kits to specific market	NO	-	Facilities improvement and/or company/group expansion.		2015-2017	-	SensingTex
General Advancement of knowledge	Maintaining industrial cooperations initiated during project	NO	-	Material benchmarking	Specific providers and industries.	>2015	-	TUC
Single process development	R2R technology development	NO	-	R2R machinery		>2015	-	TUC, 3D-Micromac
General Advancement of knowledge	High-tech texiles	NO	-	R&D projects, contract research	Automotive industry	Will be submitted January 2015	-	UAlg

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