CARBON BASED SMART SYSTEM FOR WIRELESS APPLICATION

Start Date : 01/09/12
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Topic addressed : Very advanced nanoelectronic components: design, engineering, technology and manufacturability

WORK PACKAGE 2 : Design and simulation activities

DELIVERABLE D2.1

Report on design of the distributed amplifier based on CNT FET including the PA design and graphene based LNA, mixer and detector

Due date : T0+12 **Submission date : T0+13**

Lead contractor for this deliverable : UNIVPM

Dissemination level : PU – Public

WORK PACKAGE 2 : Design Activities

PARTNERS ORGANISATION APPROVAL

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1 INTRODUCTION

According to the DoW, the main objectives of Task 2.1 to which D2.1 refers to, are described in the following:

The target of the work is given by the analysis and design of broadband distributed amplifier CNT-FETs (Carbon nanotube field effect transistors), including prospects for LNA, PA, mixer and detectors. The CNT-FET, with a top-gate configuration and high-k dielectric, is explored in this task to realize a core microwave device and amplification at high frequency over wide-band. Single CNT channels and CNT-arrays are considered. Mixing operation and detection are thus demonstrated, as produced by the non linearities exhibited by the CNT-FET.

Driven by technology and market requirements, semiconductor electronics already has found its way into nanoscale dimensions. Beyond this, radio-frequency (RF) nanoelectronics represents an emerging branch of nanotechnology with possibilities for microwave, millimeter-wave and THz devices and systems. To alleviate the silicon technology limits, numerous alternative approaches have been pursued (Si-Ge, III-V high mobility semiconductors) but it seems that the major breakthrough may come from materials exhibiting room temperature ballistic transport [1-19], namely CNTs [1,2], graphene and graphene nanoribbon [3,4].

Semiconducting CNTs are unique electronic materials with room temperature carrier mobility of > 100,000 $cm^2/V/s$, three times larger than InAs, and a band gap of -0.6 eV, which is close to that of silicon. Some of the key semiconducting properties of CNTs are compared with other materials in Table 1. The high mobility makes CNT FETs attractive for low power amplifiers and the high-saturated electron velocity leads to projected operation into the THz rangex. Single wall nanotubes (SWNTs) are inherently small, ~1 nm in diameter. This ultra small diameter enables effectively 1- dimensional conduction with the potential for ultra-low shot-noise performance and improved linearity. An additional benefit of small size is extremely low capacitance [2], which translates into high operating speeds without the need for extreme lithography.

	Bandgap eV	Electron mobility $cm^2/V/s$	Saturated electron velocity 10^7 cm/s	Thermal conductivity W/cm/K
CNT	~0.9	100000	> 10	> 30
InAs	0.36	33000	0.04	0.27
Si	1.1	1500	0.3	1.5
GaAs	1.42	8500	0.4	0.5
InP	1.35	5400	0.5	0.7
4H-SiC	3.26	700	2	4.5
GaN	3.49	900	3.3	20

Table 1 : Electronic and thermal properties of CNT as compared to other materials

We design and simulate the fundamental sub-component of the nano T/R module, namely the CNT channel for charge transport in FET: full-wave techniques in the frequency (energy)-domain are applied for investigation of the combined electromagnetic-coherent transport problem. The quantum transport, modeled by a multichannel approach, is self-consistently coupled with the solution of the Poisson equation [2,5]. Charges transport is affected by the self-generated electrostatic field, in addition to the electrostatic potential applied by external electrodes. We show the use of this approach in dealing with FET, but basic concepts are shared with a wide class of devices: amplifiers, rectifiers, harmonic generators, switches and logic elements.

In order to characterize, synthesis, and optimize the patterning of nano-devices, new numerical and analytical tools are used [7-15]: these are capable of simulating, simultaneously and consistently, the charge transport phenomena at the nanoscale and the electromagnetic behavior of nanostructures. This is needed to address the items of "beyond CMOS" research, that explores the possibility of new types of devices, like, for instance, electron-spin, electron-valley-, and superconductor-based devices. We focus on modeling of devices based on the ballisticity of carrier transport in CNT.
In general, the analysis can be carried out by discrete models such as tight binding (TB), and continuous models, such as effective mass and *k·p* approximations, which stems from the approximation of TB around particular points of the dispersion curves. Another popular approach for the calculation of quantum transport is given by the use of the Green's function of a CNT region. This method is closely related to another approach, which breaks up the system into layers perpendicular to the transport direction. Beside the above, *ab initio* methods requires high computational resources, and can hardly include the effect of i) self-generated electromagnetic (EM) field, ii) impinging external EM fields.

Recently, we have introduced, and now employed in the present NANO-RF project, full-wave techniques both in the frequency (energy)-domain [4], and the time-domain [7], for the investigation of new devices based on CNT, single and multiwall. In both the approaches, the quantum transport is described by the Schrödinger equation. The electromagnetic field provides driving terms for the quantum transport equations, that, in turns, provides charge and current sources for the electromagnetic field. The analogy between quantum transport and microwave propagation problems leaves open the possibility of a systematic application of well-established microwave techniques for the synthesis, analysis, and calibration of quantum devices [10,11].

The accurate investigation of the CNT-FET component is the building block for the qualitative and quantitative design of i) CNT FET-based distributed amplifier (including the PA), ii) graphene-based LNA, iii) mixer and detector.
Demonstration, progress and feedback of the presented full-wave techniques and design methods will be related to the dynamics and interaction to the incoming WP3 and WP4.
In the following, general rules for the design of CNT-based amplifiers are reported.
Further improvements and refinements will be achieved once experimental results and measures of the fabricated components/devices (e.g. S-parameters) will be available.

2 CNT-FET

2.1 CNT TRANSPORT CHARACTERIZATION

2.1.1 Basic CNT-FET theory

The multi-band carrier transport (Schrödinger equation) and the electrostatic potential (Poisson equation) throughout the cylindrical device of the figure below (right) are simultaneously solved by numerical iteration (Fig. 1, left).

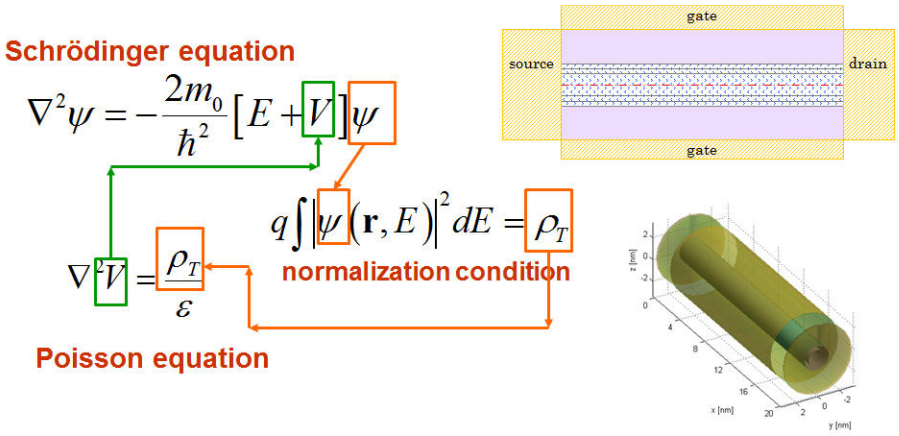

Figure 1 : Computational scheme of the iterative Poisson-Schroedinger (SP) system of equations (left), and single-wall CNT FET (right): the electrodes are modeled so as to preserve the cylindrical symmetry.

The quasistatic electromagnetic field provides sources terms for the quantum transport equations that, in turns, provides charges and currents for the Poisson equation.

The CNT-FET modelling includes control of geometry (channel size, gate radius), as well as quantistic parameters (number of electronic bands, transfer energies among carbon atoms, etc.), electrical parameters (applied voltages, electrical permittivity of the medium around CNT, etc.), and numerical parameters (space refinement in the CNT for Schrödinger solution, energy refinement in calculating the current and charge integrals, the number of modes in potential solution, etc.).
The Schrödinger equation is written for each individual (wall and/or sub-band) transport channel

$$\frac{d^2\Psi_{h,e}^{n,m}}{dz^2} = -\frac{2m_{h,e}^{n,m}}{\hbar^2}\left(E - U_{h,e}^{n,m}(z)\right)\Psi_{h,e}^{n,m}$$

where *m* indicates the *m*th wall and *n* indicates the *n*th subband. All quantities related to electrons (*e*) and holes (*h*) are kept distinct. The potential energy *U* appearing in the above equation is defined as

$$U_{\mathrm{e}}^{n,m}(z) = \tilde{U}_{\mathrm{e}}^{n,m}(z) - eV(R+\delta_m, z)$$
$$U_{\mathrm{h}}^{n,m}(z) = \tilde{U}_{\mathrm{h}}^{n,m}(z) + eV(R+\delta_m, z)$$
$$\tilde{U}_{\mathrm{e}}^{n,m}(z) = E_{\mathrm{vac}} - e\chi_T^{n,m}$$
$$\tilde{U}_{\mathrm{h}}^{n,m}(z) = \tilde{U}_{\mathrm{e}}^{n,m}(z) - E_{\mathrm{g}}^{n,m}$$

where *R* is the radius of the smallest of the CNT walls, E_{vac} is the vacuum energy, χ is the CNT-electron-affinity for the carriers of the (*n,m*)-channel, E_{g} is the *n*th energy gap of the *m*th wall and *V* is the electrostatic potential satisfying the Poisson equation:

$$\frac{d^2V}{d\rho^2} + \frac{1}{\rho}\frac{dV}{d\rho} + \frac{dV}{dz^2} = -\frac{Q}{\varepsilon}$$

where Q is the charge dentisty in the CNT channel and V is evaluated at $\rho = (R + \delta m)$, that is, the radius of the mth wal of the CNT. The boundary conditions for V are given by

$$V(R_G, z) = V\mathrm{g} - \phi\mathrm{g}$$

$$V(R + \delta m, 0) = V\mathrm{s} - \phi\mathrm{s}$$

$$V(R + \delta m, L) = V\mathrm{d} - \phi\mathrm{d}$$

where R_G is the radius of the gate electrode, ϕg, ϕd, ϕs, are the work functions of the gate, drain and source respectively, and Vg, Vd, Vs, are the voltages applied at drain and source respectively. At this step, each nanotube wall has been treated as if it was an independent nanotube. As a consequence, the dispersion curves of the mth wall are computed by means of a tight-binding (TB) approach, neglecting the interaction with the other walls. In the absence of external bias, the Fermi level, then the work function, is the same for the metal and the CNT: this assumption is extended to all the CNT walls. A different choice could be made just by redefining χ and ϕ.
A solution of the wave functions for constant V is:

$$\Psi_{\mathrm{h,e}}^{n,m} = \begin{cases} A_{\mathrm{h,e}}^{n,m} \mathrm{e}^{-\mathrm{j}\beta_{\mathrm{h,e}}^{n,m,\mathrm{S}} z} + B_{\mathrm{h,e}}^{n,m} \mathrm{e}^{\mathrm{j}\beta_{\mathrm{h,e}}^{n,m,\mathrm{S}} z} \\ C_{\mathrm{h,e}}^{n,m} \mathrm{e}^{-\mathrm{j}\beta_{\mathrm{h,e}}^{n,m,\mathrm{D}} z} + D_{\mathrm{h,e}}^{n,m} \mathrm{e}^{\mathrm{j}\beta_{\mathrm{h,e}}^{n,m,\mathrm{D}} z} \end{cases}$$

where the normalization amplitudes are chosen accordingly to the condition that the current associated to each individual transport channel is given by (Landauer):

$$I_{h,e}^{n,m} = \frac{4e}{h} \int (f_{h,e}^{S} - f_{h,e}^{D}) T_{h,e}^{n,m} \, dE$$

The actual wavefunctions, solution of the Schroedinger eaquation, are obtained by connecting the solutions of piecewise continuous (discretized) potential. The total current is calculated as the sum of all channel contributes:

$$I = \sum_{n,m} \left(I_h^{n,m} + I_e^{n,m} \right)$$

The total charge in the CNT channel is given by the sum of all holes and electrons injected from the metal contacts:

$$q_{\mathrm{e}}^{n,m} = \int |\Psi_{\mathrm{e}}^{n,m,\mathrm{D}}(z)|^2 + |\Psi_{\mathrm{e}}^{n,m,\mathrm{S}}(z)|^2 \mathrm{d}E$$

$$q_{\mathrm{h}}^{n,m} = \int |\Psi_{\mathrm{h}}^{n,m,\mathrm{D}}(z)|^2 + |\Psi_{\mathrm{h}}^{n,m,\mathrm{S}}(z)|^2 \mathrm{d}E$$

$$q^{n,m} = q_{\mathrm{e}}^{n,m} - q_{\mathrm{h}}^{n,m}, \qquad Q = \frac{e}{2\pi} \frac{\delta(\rho - R - \delta_m)}{\rho} \sum_{n,m} q^{n,m}.$$

The capacitance associated to the gate electrode should account for the quantum capacitance related to the charge in the channel form source and drain, i.e. Q_{ST} and Q_{SD} respectively.

$$C_{SG} = C_{SE} + C_{ST} = -\frac{dQ_{SG}}{dv_{gs}} = -\frac{dQ_{SE}}{dv_{gs}} - \frac{dQ_{ST}}{dv_{gs}}$$

$$C_{DG} = C_{DE} + C_{DT} = -\frac{dQ_{DG}}{dv_{gs}} = -\frac{dQ_{DE}}{dv_{gs}} - \frac{dQ_{DT}}{dv_{gs}}$$

Please refer to section 2.3.2 for more detail on lumped circuit analysis and meaning,

2.1.2 Some modeling results

The CNT FETs based on SWNTs have been extensively characterized at DC in the literature. The state of the art is the direct measurement of a current gain cut-off frequency of 4 GHz and an intrinsic value of 30 GHz (calculation by removing access and parasitic capacitances) on a transistor composed of a large number of CNTs. As a quasi-one-dimensional (1-D) conductor, a CNT channel resistance is limited by the fundamental quantum resistance (RQ) of 6.5 kOhm per tube. The simplest idea is to deliver to this quantum resistance (ignoring metallic versus semiconducting behavior) a 1 V operating voltage, which will give a current of about 150 µA/nanotube. With all its non-idealities like poor contacts, scattering as well as existence of tunneling barriers, the state-of the-art CNT FETs can deliver around 20 µA/nanotube at about 1 V. This is roughly confirmed by a simulation example, where the band mismatch between CNT reduce2 the current delivered by a single channel down to less than 10 µA. Simulation detail is shown in the following:

CNT Length=50nm,
CNT Diameter =1.25nm,
Drain to source voltage =1V,
Gate radius = 3nm,
Relative dielectric permittivity = 25,
Gate to source voltage =0.5V,
Metal work function =4.2V.

Considering a transistor with a width of 1 µm and nanotubes arranged in a 500 CNT array, as it is the case in NANO-RF project, the current scales up of the same factor.
The capacitance per nanotube is ~2-5 aF, which corresponds to ~1 fF/µm, not far from a silicon transistor. This is verified in the following simulation example, where the capacitance of a double-wall CNT, and that of two single-wall CNTs, are reported and compared.

Simulation detail:
CNT Length=20nm,
Drain to source voltage =0.35V,
Gate radius = 3nm,
Relative dielectric permittivity = 25,
Metal work function =4.5V.

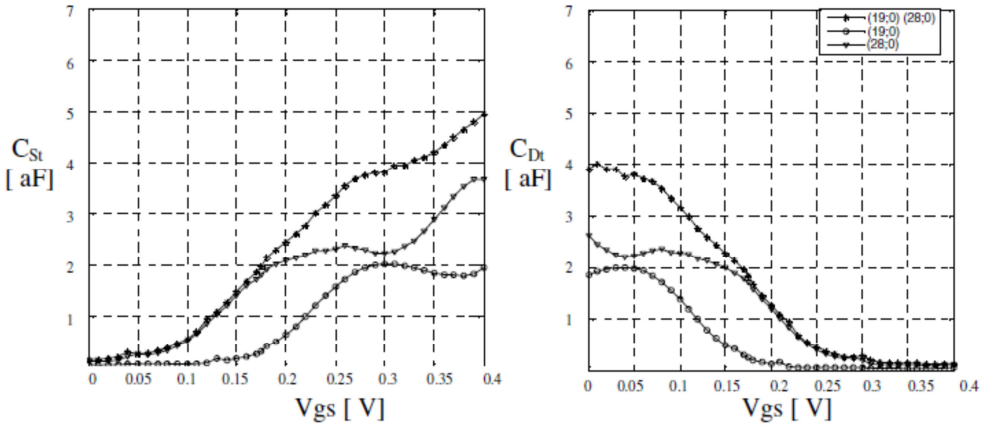

Figure 2 : CNT contribution (by means of injected charge) to the Gate-Source (left) and Gate-Drain (right) capacitance of a (19,0)-(28,0) double-wall CNT, compared with those of a (19,0) sw-CNT and a (28,0) sw- CNT; all quantities vary with Vgs, for Vds fixed to 0.35 V; the CNT length is 20nm

The charge injected from the electrodes into a (19,0)-(28,0) double-wall CNT is reported in the following figure, and is compared with that of a (19,0) single-wall CNT and of a (28,0) single-wall CNT.

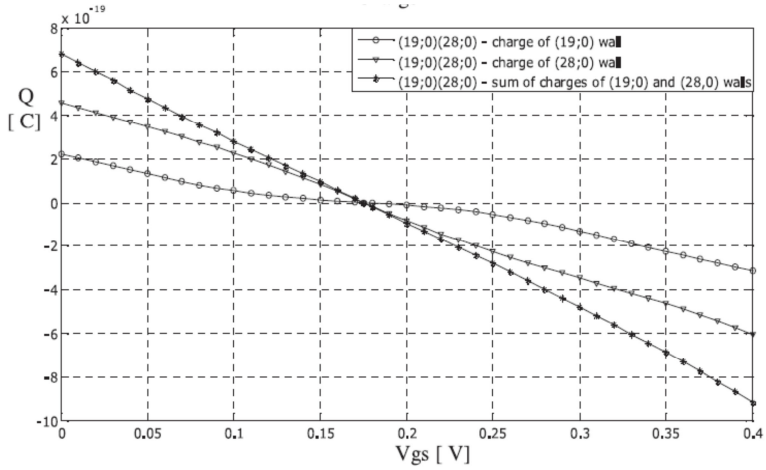

Figure 3 : Example of charge injected in a (19,0)-(28,0) double-wall CNT, compared with charge injected in its individual walls; all quantities vary with Vgs, for Vds fixed to 0.35 V; the CNT length is 20nm.

The transistor performances are actually dominated by the Source/Drain-Gate parasitic capacitance which is in the order of tens of fF, depending on the actual Gate - Source/Drain overlap, as indicated by simulations.

As a further example of application of the application of the described model, the analysis of the contribution of sub-bands in the CNT transport has been carried out for a (28, 0) sw-CNT. In this case, in addition to the fundamental band, two sub-bands have to be included in the numerical simulation: this is due to the fact that the relatively large diameter of the (28, 0) CNT yields a small band gap and dense dispersion curves. Beside the total current we show, in fig. 3, for both the (19, 0) and (28, 0) CNTs, the contribution of each sub-band: the contribution to the current of the first sub-band is not negligible, while the contribution of the third sub-band is not significant here.

Simulation detail:
CNT Length=20nm,
Gate radius = 3nm,
Relative dielectric permittivity = 25,
Metal work function =4.5V.

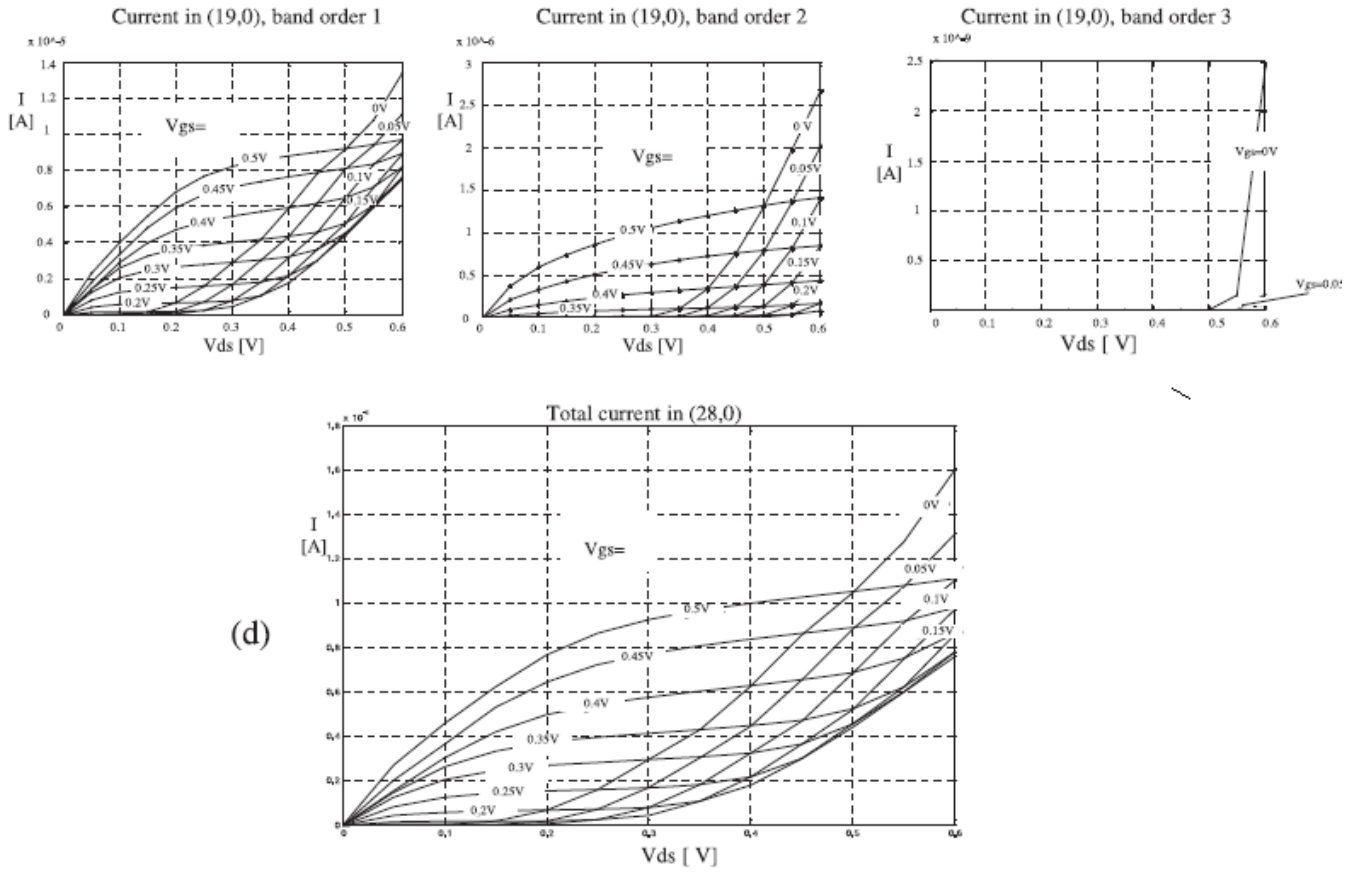

Figure 4 : Current flowing in a (28, 0) CNT versus Vds, for different values of Vgs. (a) Current contribution of the fundamental band. (b) Current contribution of the first sub-band. (c). Contribution of the second sub-band. (d) Total current

2.1.3 Effect of the metal work function in the properties of the CNT-metal contact.

In order to show the basic properties of CNT-FET device, we report the following I-V curves, that are typical of a FET device with a semiconducting CNT channel. In this example, the CNT is 50nm long, and is surrounded by a cylindrical gate of radius 15nm. Current saturation and non-linear response are highlighted.

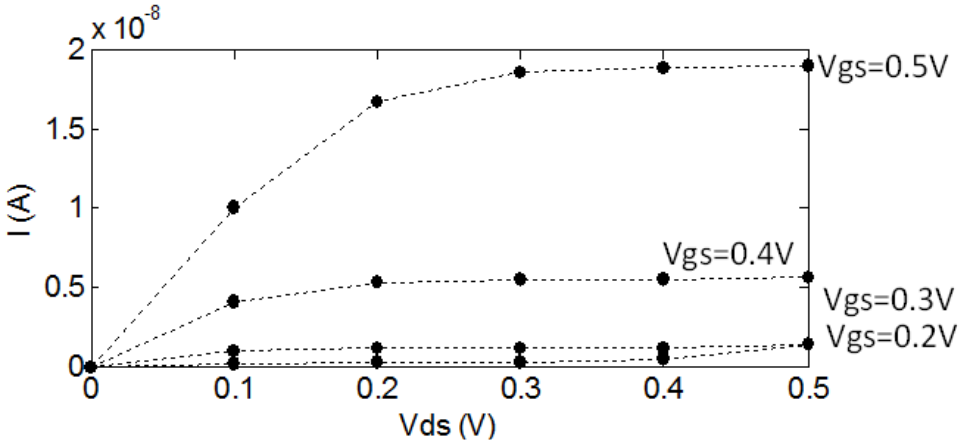

Figure 5 : I-Vds characteristics for different applied gate voltages. The metal work function is 4.5eV,equal to that of CNT.

In the Fig. 5 above, the dependence of current (I) on drain voltage (Vds) is reported: different curves are related to different gate voltages (Vgs). All voltages are referred to a zero source voltage.
The metal and CNT work-functions (Wf) are assumed to have the same value, i.e. 4.5 eV. The role played by the metal work-function in determining the transistor operation is of fundamental importance as it affects the Shottky barrier height and the CNT/GNR metal doping. This is evident from Fig. 6, where we show that setting a nonzero difference, U_0, between the Fermi level of CNT and metal,
i.e. $Wf_{metal}=Wf_{CNT}-U_0$,
strongly affects the quality of the contact, as the height of the Shottky barrier changes. As a matter of fact, shifting the Fermi level of just a fraction of eV brings about a current difference of even one or two orders of magnitude, in the case of a semiconducting CNT (16,0) having a band gap of about 0.56eV.

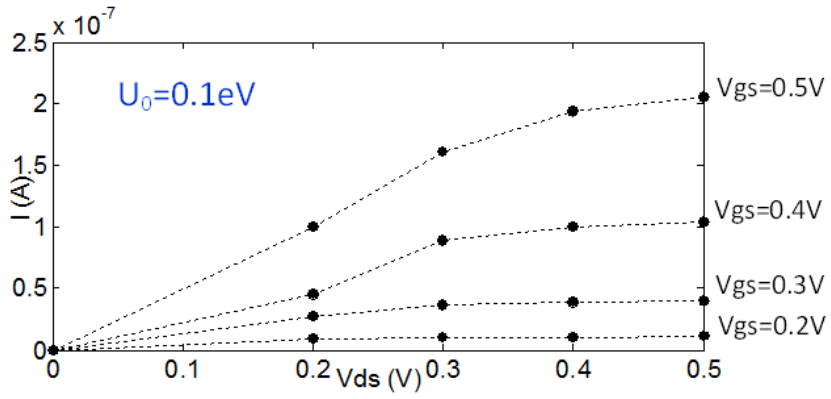

Figure 6 : I-Vds characteristics for different applied gate voltages. The metal work function is 4.4eV, that means n-doping of the contacted CNT

The comparison between the currents delivered by the two CNT-FET above, with metal work function equal to 4.5eV and 4.4eV, is reported in Fig. 7. A current difference as high as one order of magnitude is obtained: as a matter of fact, in case of relatively long CNT, tens or hundreds

nanometers, the contact resistance due to the Shottky barrier has a strong impact on the device performance.

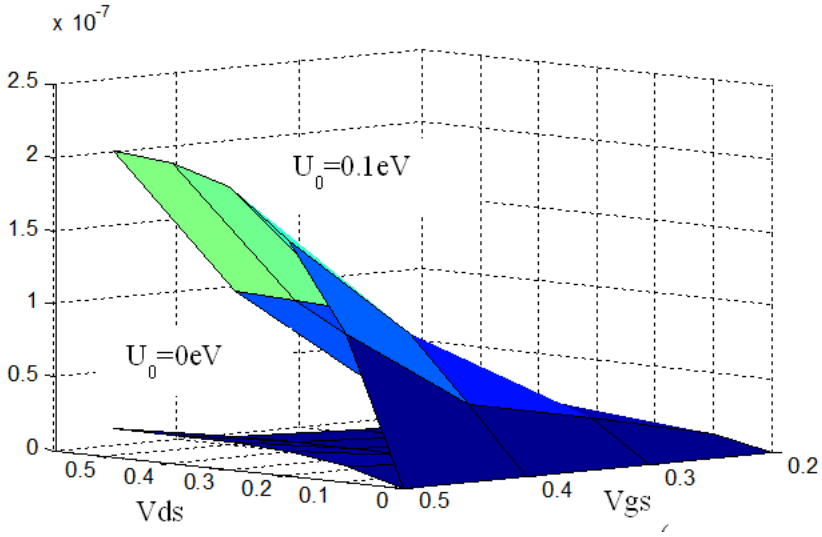

Figure 7 : I-Vds characteristics for different applied gate and drain voltages. The upper and lower surface are obtained with a metal work function of 4.4eV and 4.5eV respectively

Further decreasing of the metal work function yield the current curves of Fig. 8 below.

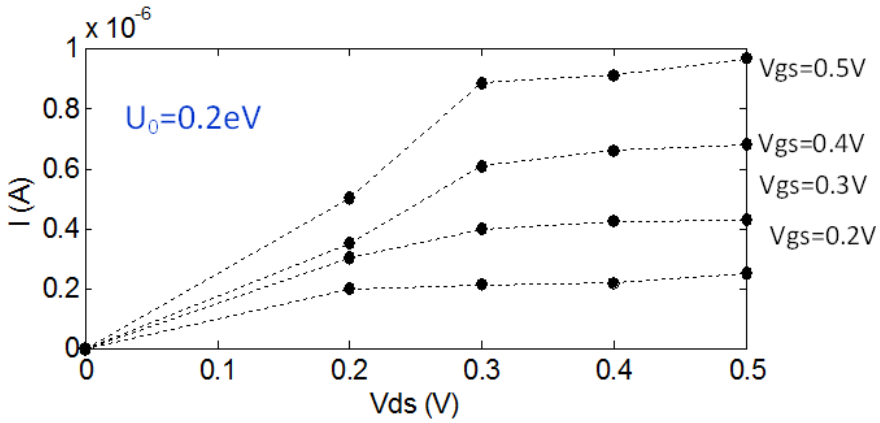

Figure 8 : I-Vds characteristics for different applied gate and drain voltages; the metal work function is 4.3eV

2.2 NUMERICAL CONSIDERATIONS AND USER FRIENDLY-INTERFACE

2.2.1 Numerical Convergence of the model

For completeness, an example of numerical convergence of the iterative SP solution has been reported in Fig. 9: the potential along the CNT converges to a stable curve after a few numerical iterations.

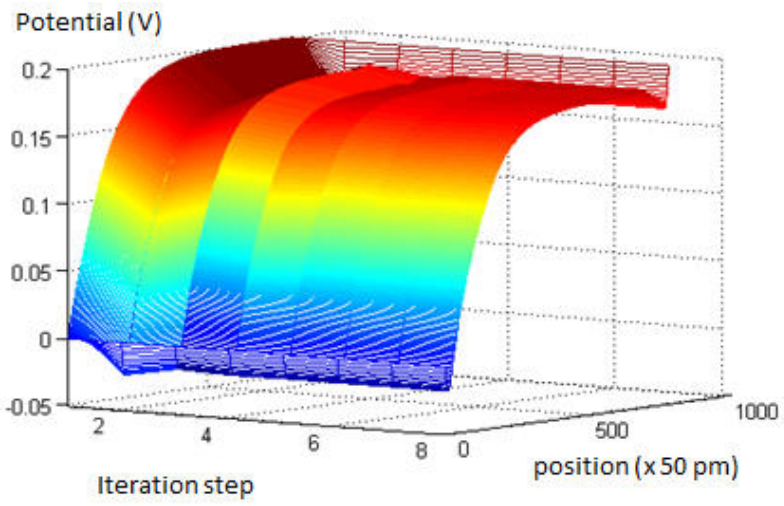

Figure 9 : Potential along a 50nm (16,0) CNT, with Vgs=0.2 V, Vds=0.2 V, and U0=0.2eV, as a function of the computational step of the iterative SP system

An interesting aspect of our numerical simulations is shown in the following figure: we report the number of steps needed to ensure the convergence of the SP system, for several couples of external voltages (*V*ds, *V*gs). It is noted that it may be very difficult to find a solution for such a system as it may require a large number of iterations, especially for high values of *V*gs and small values of *V*ds. Basically, this is due to the fact that in the latter conditions a relatively large amount of charge can be injected in the CNT from the metal electrodes.

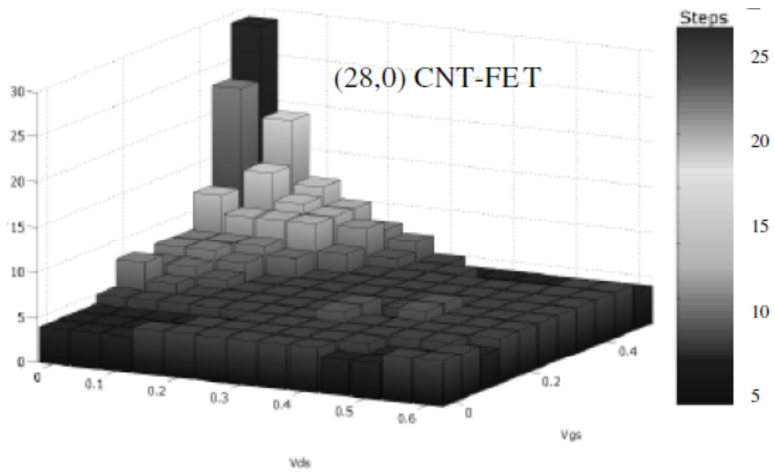

Figure 10 : Number of iterations made to achieve the solution of the Poisson–Schroedinger system, as a function of Vds and Vgs, for a 20nm CNT

2.2.2 Setting up a CNT-FET simulation

The basic steps in setting up a CNT-FET simulation, by means of the user-friendly simulator that has been developed in-house, are listed below in chronological sequence.

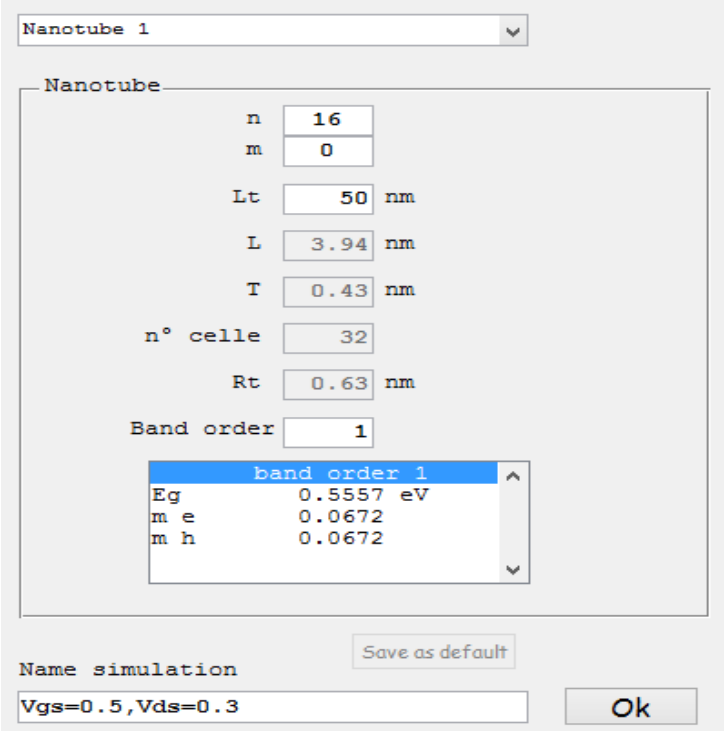

Figure 11 : Step 1: setting CNT chirality, length, and number of sub bands

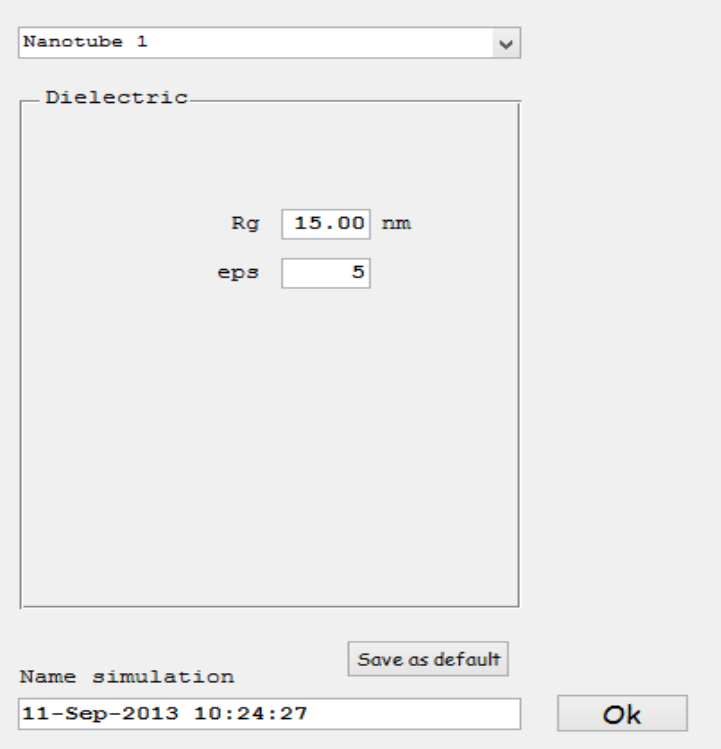

Figure 12 : Step 2: setting the Gate radius and relative dielectric permittivity

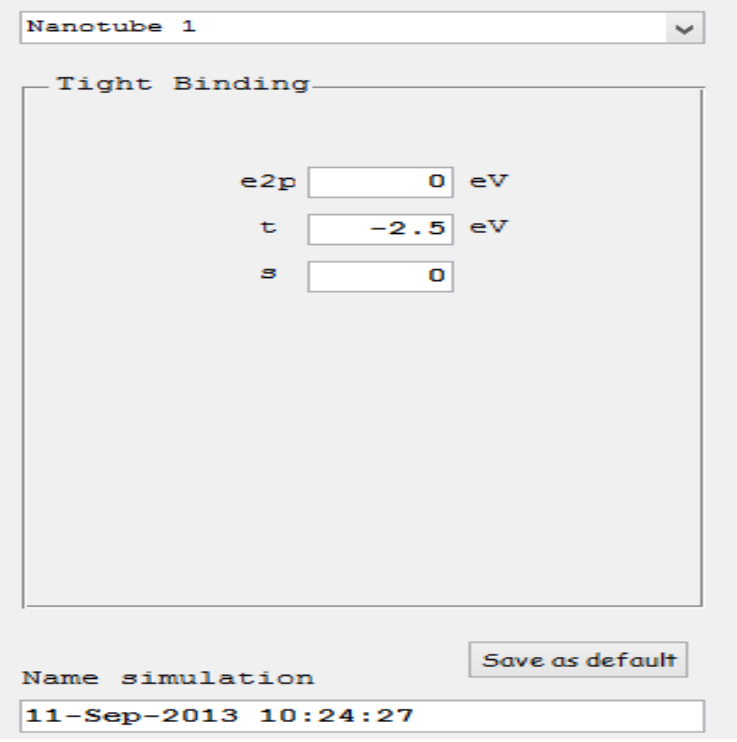

Figure 13 : Step 3: setting the quantum parameters

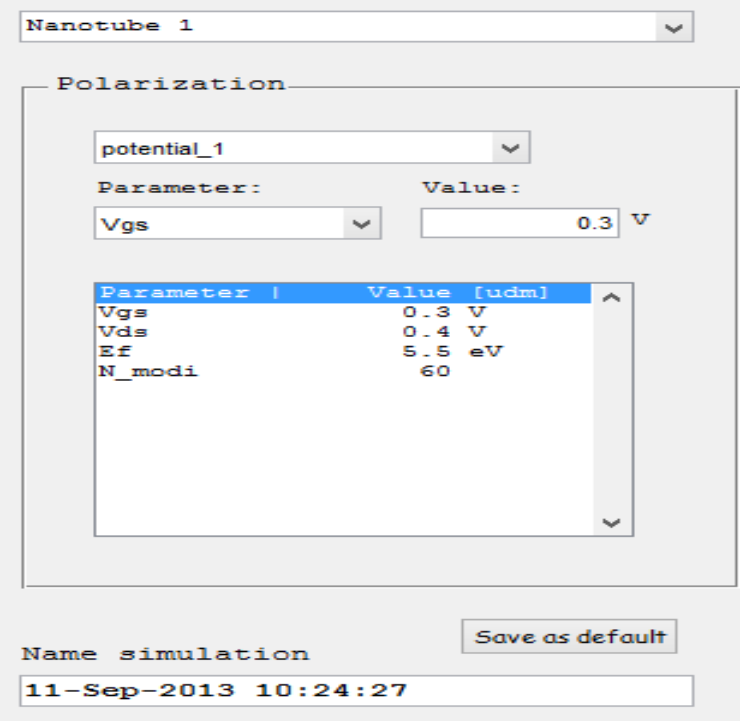

Figure 14 : Step 4: setting the external potential and the metal Fermi energy

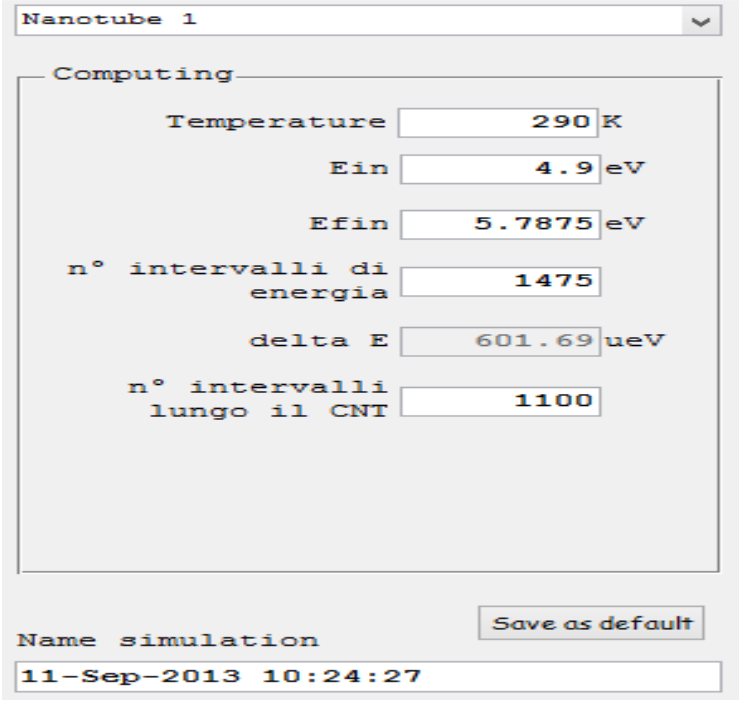

Figure 15 : Step 5: setting temperature and computing parameters

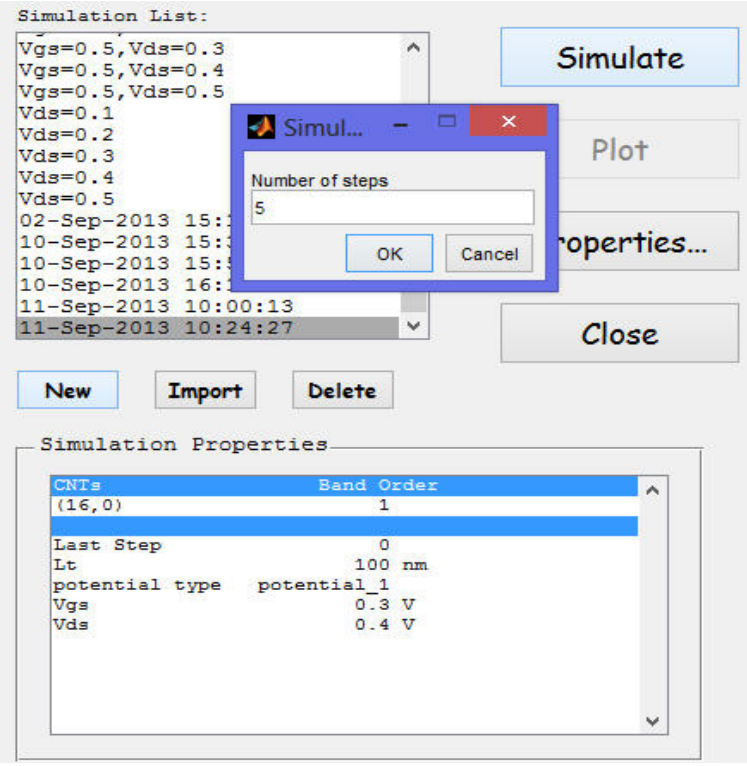

Figure 16 : Step 6: setting the number of iterations of the SP system to be performed, and run

2.3 GENERAL RULE FOR CNT AMPLIFIERS

2.3.1 Transistor characterization

The general rules and potential limitations for the design of CNT-FETs are established by means of simulators and tools are made available within the consortium.
The LNA and PA will be designed using EM simulators taking into account the values established: once the basic CNT-FET component has been electrically characterized, the dual gate system embedded in coplanar waveguide CWG technology will be a relatively easy task to be performed by standard EM tools, like HFSS.
Various configurations will be tested as a starting point for the final fabrication and test.

- *Effects of CNT length and size,*
- *CNT-FET parallel configuration*
- *CNT-FET parallel configuration*

As it is shown in the following, differently from conventional transistor, current is not inversely proportional to the CNT length,

$$I_{D,Sat} = \frac{W}{L}\mu C_{inv}\frac{(V_G - V_{th})^2}{2}$$

As a matter of fact, owing to the balisticity of charge transport, changing the length of the CNT channel does not provide significant change in the transconductance. Considering, for instance, three different CNT-FETs as in the following,

- ✓ *L=50nm*
- ✓ *L=100nm*
- ✓ *L=200nm*

It is found that the channel transmittivity strongly changes, as it is shown in the following picture, but the transconductance is almost the same, about 2.5-3 µS.

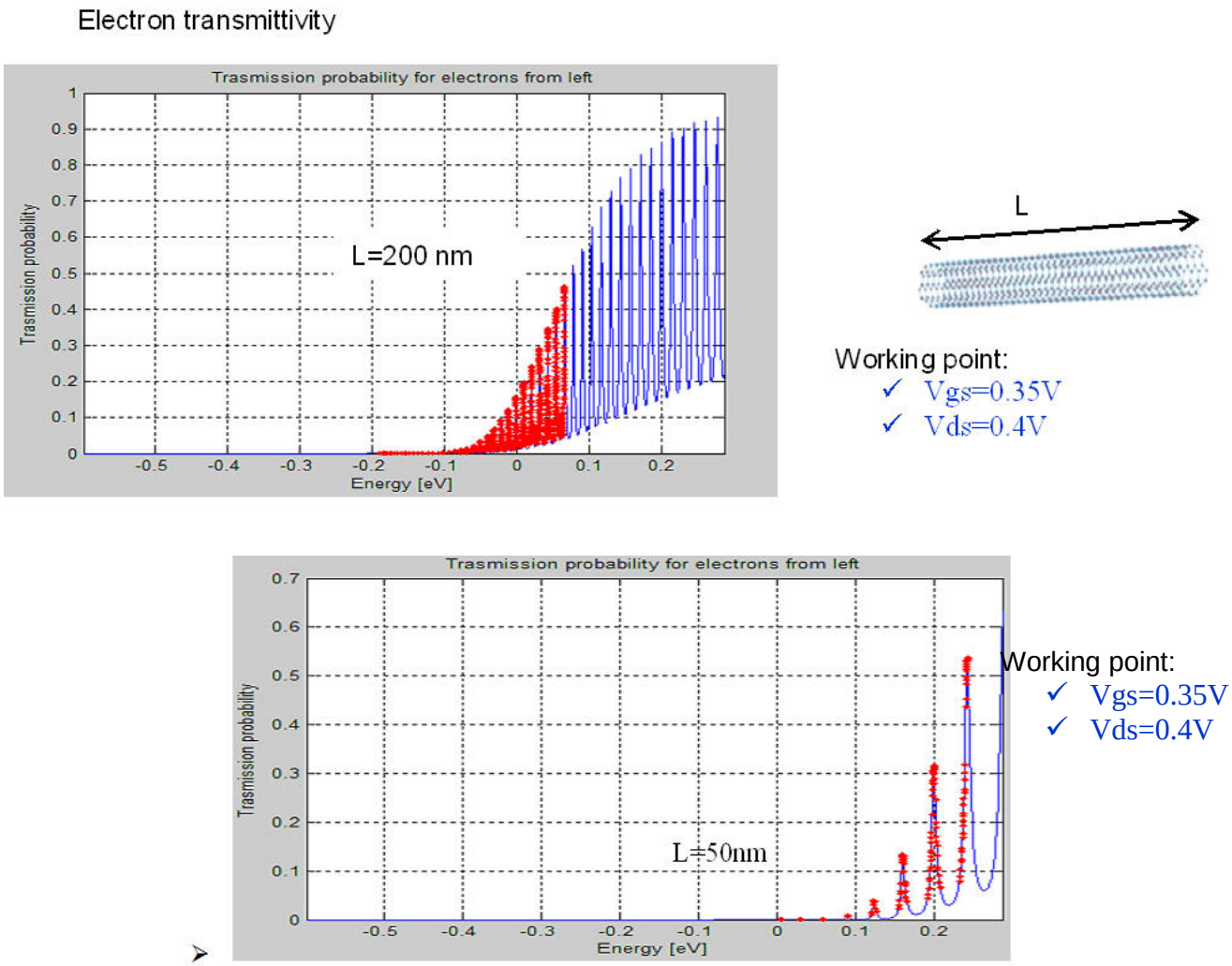

Figure 17 : Comparison between the transmission probabilities for electrons in the conduction band of two CNTs of different lengths: 200nm (up) and 50nm (down). Energies are referred to the Fermi level, Vgs = 0.35 V, Vds = 0.4

In Table 2, we outline the calculated transconductances of several CNT-FETs, i.e. dI/dVgs (with Vds=0.5V), for different values of U_0,

Simulation detail:
CNT Length = 50nm,
Gate radius = 15nm,
Relative dielectric permittivity = 5,
Working point: Vgs = 0.4V, Vds=0.5V.

Simulated transconductance	
U_0 (eV)	**g_m (µS)**
0	**0.13**
0.1	**1**
0.2	**3**
0.3	**5**

Table 2 : Simulated transconductance of a 50nm CNT with a DC voltage of 0.4V applied to the Gate electrode, for different metal work functions

2.3.2 Circuit model

A small signal analysis is performed by varying the applied voltages around a working point, defined by a pair (*V*ds, *V*gs). The following equivalent circuit can be used in order to characterize the frequency response of the transistor:

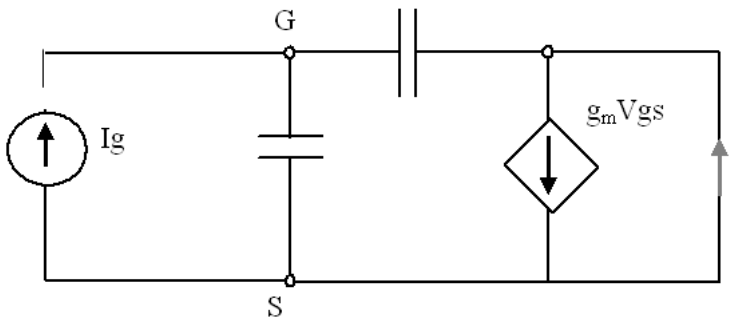

Figure 18 : Equivalent circuit of the CNT-FET. Labels G, S and D stand for the gate, source and drain contacts, respectively.

The parameters of figure 18 are defined as follows:

$$g_m = \left.\frac{\mathrm{d}i_\mathrm{D}}{\mathrm{d}v_\mathrm{gs}}\right|_{(V_\mathrm{gs}, V_\mathrm{gs})}$$

$$C_\mathrm{SG} = -\frac{\mathrm{d}Q_\mathrm{S}}{\mathrm{d}v_\mathrm{gs}}, \qquad C_\mathrm{DG} = -\frac{\mathrm{d}Q_\mathrm{D}}{\mathrm{d}v_\mathrm{gs}}$$

where $C_{SG} = C_{SE} + C_{ST}$ and $C_{DG} = C_{DE} + C_{DT}$, whose meaning is clarified in the following.
Q_S (Q_D) is given by the sum of the charges of the source (drain) electrode, related to C_{SE} (C_{DE}), and the charges diffused from the source (drain) in the CNT, related to C_{ST} (C_{DT}). The charge on the drain and the source may be calculated as integrals of the electric field flux through appropriate surfaces around the electrodes. On the other hand, the nanotube charge is obtained as a space integral of the linear charge, as for the curves of figure 3. Typical results for CNT capacitances were shown in figure 2.
The transconductance of a single-wall or double-wall CNT is obtained by applying the definition above. The results are shown in figure 19.
As it was previously mentioned, the capacitance of the electrodes is estimated to be an order of magnitude greater than C_{ST} and C_{DT}. The unitary gain frequency f_T , derived from the equivalent circuit of figure 18, is

$$\left|\frac{g_m}{(C_\mathrm{SG}+C_\mathrm{DG})}\frac{1}{\mathrm{j}\omega_T}\right| = 1 \Leftrightarrow \omega_T = 2\pi f_T = \left|\frac{g_m}{(C_\mathrm{SG}+C_\mathrm{DG})}\right|$$

In practice, the above equation shows that f_T increases as the diameter and/or the number of walls increase. Basically, the electrode capacitance here dominates with respect to the CNT capacitance. Then, the use of large or multi-wall CNTs, or, *as in NANO RF, of CNT arrays*, affects the transconductance more than the total capacitance: the increased transconductance leads to a higher f_T. This is true until the increased number of CNT (in case of an array) requires a larger Gate electrode, for a correct bias of all of them.

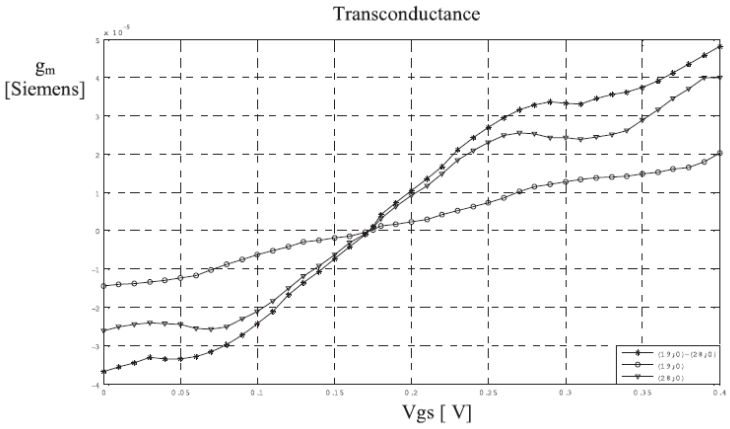

Figure 19 : Transconductance of a (19, 0)–(28, 0) double-wall CNT, compared with those of a (19, 0) sw-CNT and a (28, 0) sw-CNT.

2.3.3 CNT-array CNT-cascade FET

The 1-D CNT array technology can potentially deliver a very high current in the same area and for identical gate capacitance, which leads to increased current density and lower delay at higher integration density.
It is reasonable assumed that the mutual CNT interaction is almost negligible: in practice, it is possible to simulate an array by integrating the results of the individual CNT as if they were separately gated (see Fig. 2).
As shown in the previous section, an equivalent lumped circuit model of the CNT-FET is made available after the numerical simulation. The following qualitative key issues stem from the quantitative analysis:

o simulating CNT transistors of different length shows that, in the ballistic regime, the length of the CNT channel just sligthly affects the I-V characteristics; this was esemplified in section 4.3.1.

o The transconductance increases with the CNT diameter, the number of walls, and, in case of a CNT-array-FET, the number of CNTs, i.e.:

$$I_{array} = N \cdot I_{CNT} \rightarrow g_{array} = N \cdot g_{CNT}$$

o In general, the quantum capacitance of a CNT has a small impact to f_T, because the electrode capacitance dominates: ideally, increasing the number of CNTs in a large CNT-array-FET should leave unchanged f_T, but with the benefit of a higher transconductance.

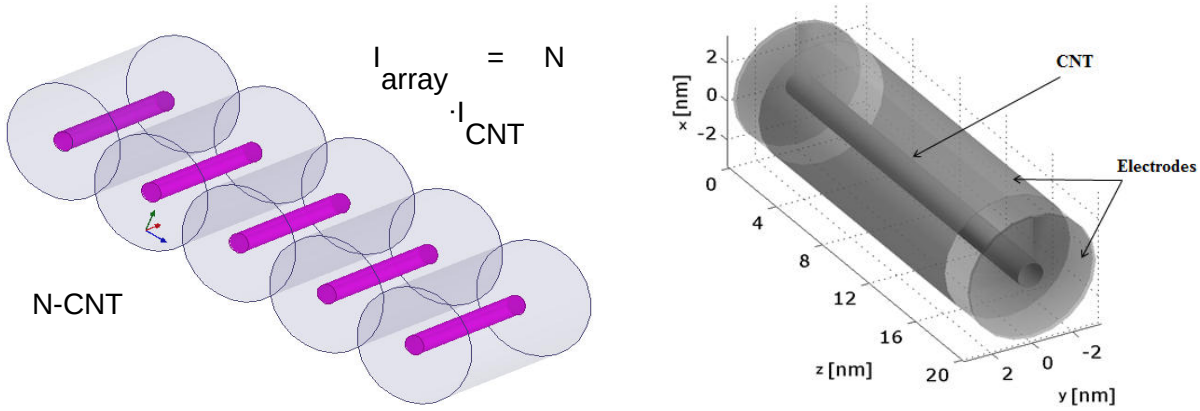

Figure 20 : CNT-FET (right), and CNT-array-FET (left)

Let consider the cascade of two CNT-FETs, and try to derive the behaviour of the whole device in terms of transconductance and f_T. All parasitics and contact resistances, as well as mismatch between the two stages, are not considered in the idealized picture below. Or, as equivalent concept, we can assume a matching network between two neighbour cascade CNTs, that is T=1, R=0, being T the transmittivity and R the reflectivity of the matching network. This is an operative condition that can

be achieved by inserting an appropriate ladder network, as a combination of L, C and R passive components, once the S-parameters of the CNT-FET will be available.
The output impedance is set to zero in order to evaluate the current gain Id_{out}/Ig.

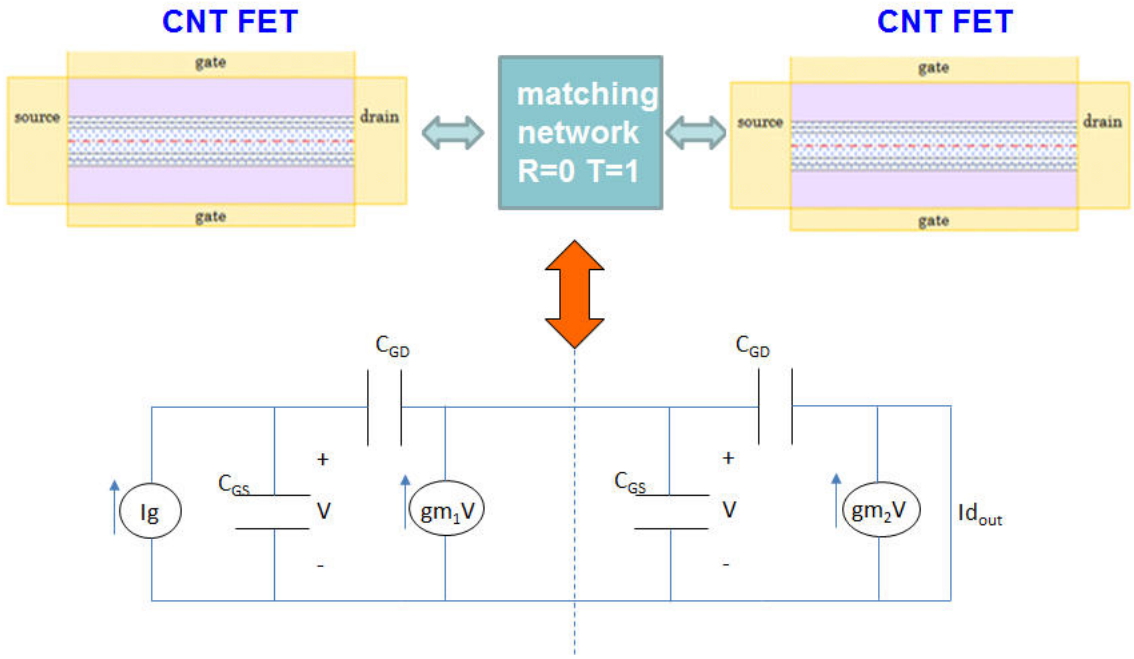

Figure 21 : Cascade of CNT-FETs.

As a result, if the operating frequency of each transistor operates below the unit gain frequency of the *single transistor*, then it is verified that the total gain is roughly proportional the product of the individual transconductances. Moreover, it is found that the unit gain frequency does not substantially change with respect to that of the single transistor. The gain current is calculated as:

$$\frac{Id_{out}}{Ig} = 1/\left[\frac{-\omega^2\left(C_{GS}+2C_{GD}\right)\left(C_{GS}+C_{GD}\right)}{\left(gm_1+j\omega C_{GD}\right)\cdot\left(gm_2+j\omega C_{GD}\right)}-\frac{j\omega C_{GD}}{\left(gm_2+j\omega C_{GD}\right)}\right]$$

assuming

$$C_{GS}=C_{GD}=C \quad and \quad g_{m_1}=g_{m_2}$$

yields:

$$Id_{out}/Ig \approx g_m^{\,2}$$

which means that the current gain is proportional to the product of the individual current gains. Imposing $Id_{out}/Ig=1$, yields:

$$\omega_T \approx g_m/2C$$

which is the same as the single CNT-FET.

3 CONCLUSIONS

A self-consistent analysis of multichannel carrier transport in multi-wall CNTs is performed with the aim of characterizing CNT-FET (carbon nanotube field effect transistors) of different size and under different Bias condition. CNTs are embedded in FETs as conduction channels: the analysis is carried out by self-consistent Poisson-Schroedinger approach, suitable for structures of realistic size, and takes into account the contribution of all electron and hole sub-bands. Typical current-voltage characteristics, together with calculated trans-conductances, are reported.

Results not only show quantitatively the characteristics of multichannel transport, but also highlight qualitative aspects and design rules of the CNT-FET. For instance, considerations about the cut-off frequency of multiple CNT FETs, in array or cascade configuration, have been reported. In particular, the equivalent circuit model of two cascaded CNT-FETs, whose lumped elements are derived by numerical simulation, features a multiplication of their individual current gains, with an unchanged operation bandwidth.

The model is enriched by an accurate investigation of the effects of metal and CNT work function in the contact quality, and, consequently, in the current delivered by the FET. All calculations are performed by a user friendly solver, developed in house, whose main characteristics have been shown schematically.

The above investigation is the qualitative and quantitative basis for the design of i) CNT FET-based distributed amplifier (including the PA), ii) grapheme-based LNA, iii) mixer and detector.
The further development and feedback of the presented techniques related to the design (i), (ii), (iii), will be achieved once experimental results and measures (e.g. S-parameters) of the fabricated components/devices (WP3 and WP4) will be available.

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