



## CARBON BASED SMART SYSTEM FOR WIRELESS APPLICATION



Start Date : 01/09/12  
Project n°318352

Duration : 36 months

Topic addressed : Very advanced nanoelectronic components: design, engineering, technology and manufacturability

### WORK PACKAGE 7 : Project management

#### DELIVERABLE D7.15


#### Progress Activity Report #1 Covered period: T0 – T0+6

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	<b>D7.15 - Progress Activity Report #1 (T0 – T0+6)</b>	2/30
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## WORK PACKAGE 7: Project management

### PARTNERS ORGANISATION APPROVAL

	Name	Function	Date	Signature
Prepared by:	S.Xavier	R&D Engineer	05/08/13	
Approved by:	Afshin Ziaei	Research Program Manager	05/08/13	

### DISTRIBUTION LIST

QUANTITY	ORGANIZATION		NAMES
1 ex	Thales Research and Technology	TRT	Afshin ZIAEI
1 ex	Chalmers University of Technology	CHALMERS	Johan LIU
1 ex	Foundation for Research & Technology - Hellas	FORTH	George KONSTANDINIS
1 ex	Laboratoire d'Architecture et d'Analyse des Systèmes	CNRS-LAAS	George DELIGEORGIS
1 ex	Université Pierre et Marie Curie	UPMC	Charlotte TRIPON-CANSELIET
1 ex	National Research and Development Institute for Microtechnologies	IMT	Mircea DRAGOMAN
1 ex	Graphene Industries	GI	Peter BLAKE
1 ex	Thales Systèmes Aéroportés	TSA	Yves MANCUSO
1 ex	SHT Smart High-Tech AB	SHT	Yifeng FU
1 ex	Universita politecnica delle Marche	UNIVPM	Luca PIERANTONI
1 ex	Linköping University	LiU	Rositsa YAKIMOVA
1 ex	Fundacio Privada Institute Catala de Nanotecnologia	ICN	Clivia SOTOMAYOR
1 ex	Tyndall-UCC	Tyndall	Mircea MODREANU

	<b>D7.15 - Progress Activity Report #1 (T0 – T0+6)</b>	3/30
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## CHANGE RECORD SHEET

REVISION LETTER	DATE	PAGE NUMBER	DESCRIPTION
v0	07/2013	10	Initial version
v1	08/2013	25	All partners contributions
v2	08/2013	29	Final version

# CONTENTS

<b>1</b>	<b>PROJECT OBJECTIVES AND MAJOR ACHIEVEMENTS DURING REPORTING PERIOD (T0 – T0+6)</b>	<b>6</b>
<b>2</b>	<b>MANAGEMENT ACTIVITIES (WP7)</b>	<b>7</b>
2.1	GRANT AND CONSORTIUM AGREEMENTS	7
2.2	MANAGEMENT STRUCTURE	8
2.3	MEETING	9
<b>3</b>	<b>PROGRESS IN THE ACTIVE THECNICAL WORKPACKAGE 1, 2 &amp; 3</b>	<b>10</b>
3.1	WP1 : SYSTEM AND APPLICATIONS SPECIFICATIONS	10
3.1.1	<i>WP OBJECTIVES</i>	10
3.1.2	<i>PROGRESS TOWARD OBJECTIVES : STATUS OF ACTIVES TASKS IN REPORTING PERIOD</i>	10
3.1.2.1	Task 1.3 : Identification of CNT interconnect specifications (CHALMERS)	10
3.2	WP2 : DESIGN AND SIMULATION ACTIVITIES	11
3.2.1	<i>WP OBJECTIVES</i>	11
3.2.2	<i>PROGRESS TOWARD OBJECTIVES : STATUS OF ACTIVES TASKS</i>	11
3.2.2.1	Task 2.1: Design of broadband distributed amplifier CNT FET; prospects for LNA, PA, and mixer (IMT/LAAS)	11
3.2.2.2	Task 2.2: Design of the CNT based RF switch (TRT)	12
3.2.2.3	Task 2.4: Design the CNT based antenna (UPMC)	13
3.2.2.4	Task.2.5 Design and simulation of RF graphene devices	15
3.3	WP3 : FABRICATION ACTIVITIES	18
3.3.1	<i>WP OBJECTIVES</i>	18
3.3.1.1	CNT and graphene growth technology	19
3.3.1.2	CNT and graphene material characterization (ICN/FORTH)	23
3.3.1.3	Fabrication of CNT FET (SHT/LAAS)	26
3.3.1.4	Development of carbon nanotube interconnects	27
<b>4</b>	<b>DISSEMINATION AND EXPLOITATION ACTIVITIES (WP6)</b>	<b>29</b>
4.1	PROJECT LOGO	29
4.2	PROJECT WEBSITE	29

## FIGURES

Figure 1 : NANO-RF Timetable.....	7
Figure 2 NANO-RF Management Structure .....	8
Figure 3: Schematic of CNTFET active are detail .....	12
Figure 4 : 4 electrodes concept for tweezer configuration.....	13
Figure 5 : Example of a CNT-based dipole antenna integrated on quartz substrate: (a) 3D desing – (b) Input complex impedance – (c) 3D radiation pattern .....	14
Figure 6: Schematic of GHALL mask period (a) and a single HALL device (b) .....	15
Figure 7 : graphene coplanar antenna geometry .....	16
Figure 8 : substrate used for the graphene coplanar antenna.....	16
Figure 9 : Radiation fields of the graphene coplanar antenna .....	17
Figure 10 : Graphene diode devices using for the simulation.....	17
Figure 11 : simulated I(V) characteristic.....	18
Figure 12 : CNT forest samples grown by TCVD .....	19
Figure 13 : CNT forest samples grown by PECVD.....	20
Figure 14 : Graphene grown on Cu.....	20
Figure 15 : Raman spectra of graphene grown on Cu. ....	20
Figure 16 : Growth of graphene on SiC .....	21
Figure 17 : Surface orientation of the substrate .....	21
Figure 18 : Three pages from the datasheet for sample S8111 .....	23
Figure 19 : Raman characterization from ICN compare with Forth.....	24
Figure 20 : Raman measurement on graphene provided by GI .....	25
Figure 21 : Single-walled semiconductive CNT growth for FET fabrication .....	26
Figure 22 : Image of randomly CNT deposition.....	27
Figure 23. CNT Via growth process illustration .....	28
Figure 24. Growth result of CNT vias. ....	28
Figure 25 : Nano-RF website homepage .....	30

## TABLES

Table 1 : General Assembly Representatives .....	9
Table 2 : Executive Board members .....	9
Table 3 : Summary of the CNT based via specification.....	11

	<b>D7.15 - Progress Activity Report #1 (T0 – T0+6)</b>	6/30
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## 1 PROJECT OBJECTIVES AND MAJOR ACHIEVEMENTS DURING REPORTING PERIOD (T0 – T0+6)

According to the timetable (see Figure 1), the project objectives over the reporting period are:

- Within the framework of WP 1 ‘Systems and Applications Specifications’ : precisely determine the component specifications based on the system requirements established by all the partners.
- Within the framework of WP 2 ‘Design and simulation activities’ : design and simulate all the CNTs and graphene based sub-components forming the nano T/R module to be demonstrated in WP5 comprising filters/oscillators, switches, mixers, LNAs and PAs and finally an antenna. The main technical objectives are:
  - Design and modelling of CNT and graphene based FET and then design and modeling of LNA,PA and mixer based on either CNT or graphene
  - Design and modelling of CNT switch;
  - Design and modelling of CNT filter/oscillator and graphene mixer
  - Design and modelling of CNT antenna.
  - Design and modelling of LNA based graphene
  - Design and modelling of a graphene loaded antenna.
- Within the framework of WP 3 ‘Fabrication activities’ to: all the CNT and graphene based sub-modules that have been designed in the work package 2. The principal objective of this work package is to fabricate the test structures and also final components based on the results of WP2
- Within the framework of WP 6 ‘Dissemination and exploitation’: to implement the elementary project tools necessary for the widest dissemination of the project results among scientific communities and industries. These tools are:
  - Project Logo
  - Project Website
- Within the framework of WP 7 ‘Project Management’ : to establish durable basis for the project management and monitoring all along the project duration, through the following actions:
  - Establishment of the Consortium Agreement governing the relations between the partners;
  - Set-up of the management structure: General Assembly, Executive Board and WP management teams;
  - Regular project and technical meetings;

As described in the following sections, all these objectives have progressed between T0 and T0+6.

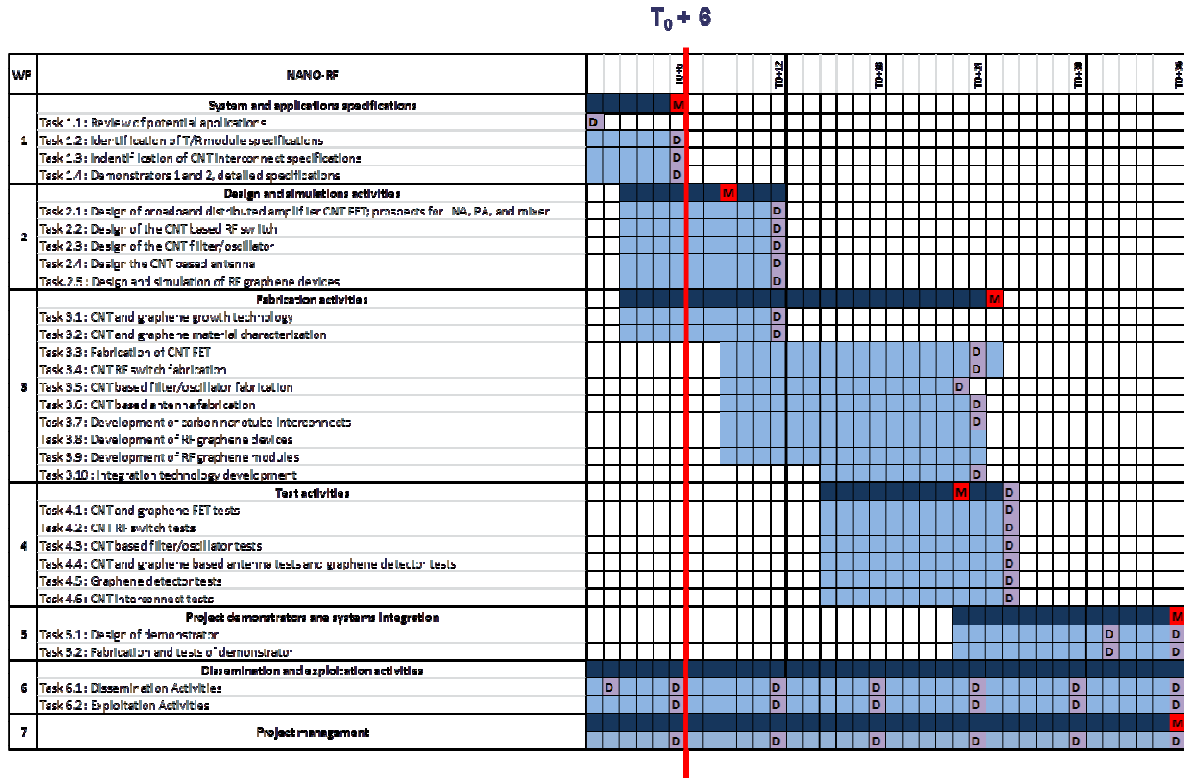


Figure 1 : NANO-RF Timetable

## 2 MANAGEMENT ACTIVITIES (WP7)

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
TRT	TRT, CHALMERS, FORTH, LAAS, IMT, TSA, SHT, UNIVPM, ICN, Tyndall	T <sub>0</sub> – T <sub>0</sub> +36	D7.1 to D7.21 M7.1	-	On-Going

### 2.1 GRANT AND CONSORTIUM AGREEMENTS

After 4 rounds of negotiation, conciliation on the consortium agreement has been found between all partners on 24th March 2013. The final version of the consortium agreement has been validated by the European Commission, returned to TRT and, as deliverable D7.1, is now downloadable on the private area of the website.

According to its article 2, “the purpose of the Consortium Agreement is to specify:

- the internal organization of the Consortium including the decision making procedures
- the rules on dissemination, use and access rights;
- the distribution of the Community financial contribution;
- the settlement of disputes between the Parties;

- Liability, indemnification and confidentiality arrangements between the Parties.”

The contract between TRT and the European Commission has been signed on 1st September 2012. Consequently to the conciliation found on the Consortium Agreement, TRT has received all the Accession Forms and the Grant Agreement is now completed.

## 2.2 MANAGEMENT STRUCTURE

As announced in the DoW, the NANO-RF consortium has set up a management structure adapted to the project complexity and to the work to be performed. This management structure (represented Figure 2), the role, rights and duties of each participant are described in detail in the consortium agreement.

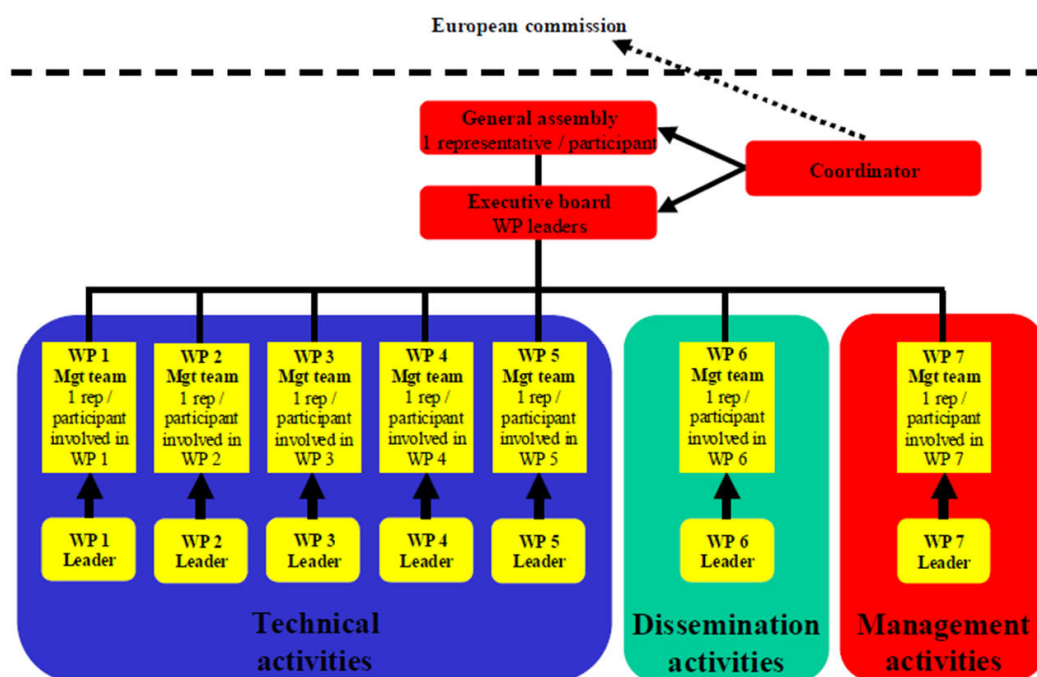


Figure 2 NANO-RF Management Structure

The consortium organisation is based on three main types of project bodies:

- The General Assembly consists of one representative of each partner. Its role is to be in charge of the overall direction and major decisions with regard to the project based on recommendations made to it by the Executive Board;
- The Executive Board consists of the work-package leaders. It is in charge of managing the project;
- The work-package management teams consist of one representative of each partner carrying out a part of the given work-package. It is in charge of managing the work-package.

Consequently, at the conclusion of the Kick-Off meeting, the consortium has designated the members of these bodies for the duration of the project (see Table 1 and Table 2).



Participant		General Assembly Representatives	
1	TRT	Afshin ZIAEI	afshin.ziaei@thalesgroup.com
2	CHALMERS	Johan LIU	johan.liu@chalmers.se
3	FORTH	Georges KONSTANDINIS	aek@physics.uoc.gr
4	LAAS	George DELIGEORGIS	gdeligeo@laas.fr
5	UPMC	Charlotte TRIPON-CANSELIET	charlotte.tripon-canseliet@upmc.fr
6	IMT	Mircea DRAGOMAN	mircea.dragoman@imt.ro
7	GI	Peter BLAKE	peter@grapheneindustries.com
8	TAS	Yves MANCUSO	yves.mancuso@fr.thalesgroup.com
9	SHT	Yifeng FU	yifeng@sht-tek.com
10	UNIVPM	Luca PIERANTONI	l.pierantoni@univpm.it
11	LIU	Rositsa YAKIMOVA	roy@ifm.liu.se
12	ICN	Clivia SOTOMAYOR	clivia.sotomayor@icn.cat
13	TYNDALL	Mircea MODREANU	mircea.modreanu@tyndall.ie

**Table 1 : General Assembly Representatives**


WP		WP Leaders		
1	Systems and applications specifications	TAS	Yves Mancuso	yves.mancuso@fr.thalesgroup.com
2	Design and simulation activities	IMT	Mircea Dragoman	mircea.dragoman@imt.ro
3	Fabrication activities	FORTH	Georges Konstantinidis	aek@physics.uoc.gr
4	Test activities	CNRS-LAAS	George Deligeorgis	gdeligeo@laas.fr
5	System integration and tests	ICN	Clivia Sotomayor	clivia.sotomayor@icn.cat
6	Dissemination and exploitation	TRT	Afshin Ziaei	afshin.ziaei@thalesgroup.com
7	Project Management	TRT	Afshin Ziaei	afshin.ziaei@thalesgroup.com

**Table 2 : Executive Board members**

## 2.3 MEETING

In order to ensure a correct progress and a high coherence of the collaborative project, during the reporting period, numerous meetings were organized:

- 3 project meetings, where all the partners are represented
  - Kick-Off Meeting, held in Paris, France, on 25<sup>th</sup>-26<sup>th</sup> September 2012;
  - 3-Month Meeting, held in Barcelona on 31<sup>th</sup> January- 01<sup>st</sup> February 2013;
  - 6-Month Meeting, held in Cork on 14<sup>th</sup> May 2013;

	<b>D7.15 - Progress Activity Report #1 (T0 – T0+6)</b>	10/30
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- 2 technical meetings for WP 2, where only the partners involved in the given WP are represented:
  - Technical Meeting, held in Amsterdam on 30<sup>th</sup> october 2012;
  - Technical Meeting, held in Ancona on 18<sup>th</sup> march 2013;
- 1 conference call (WP 2) were planned and occurred

The agendas, minutes and presentations made for these meetings are downloadable on the private area of the website.

### 3 PROGRESS IN THE ACTIVE THECNICAL WORKPACKAGE 1, 2 & 3

#### 3.1 WP1 : SYSTEM AND APPLICATIONS SPECIFICATIONS

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
TSA	TRT, CHALMERS, FORTH, LAAS, IMT, TSA, SHT	T <sub>0</sub> – T <sub>0</sub> +6	D1.1 to D1.4 M1.1	T1.1 to T1.4	<b>On Going</b>

##### 3.1.1 WP OBJECTIVES

The objective of WP1 is to precisely determine the component specifications based on the system requirements established by all the partners. In a first step, all the partners will define the applications that can be addressed by the devices developed in NANO-RF. Among the applications foreseen, we have already identified onboard weather radar systems and automotive radars systems as potential applications

##### 3.1.2 PROGRESS TOWARD OBJECTIVES : STATUS OF ACTIVES TASKS IN REPORTING PERIOD

###### 3.1.2.1 Task 1.3 : Identification of CNT interconnect specifications (CHALMERS)

In this work, the specifications of CNT interconnect will be benchmarked with previous researches on CNT based interconnects, and the electrical and thermal performance will be set so as to be able to match that of the metals as close as possible. Specifications for CNT interconnect are summarized in the Table 3.

	<b>D7.15 - Progress Activity Report #1 (T0 – T0+6)</b>	11/30
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Properties	State-of-the-art CNT vias	This work's specification
CNT interconnect diameter	~ 30 $\mu\text{m}$	20 $\mu\text{m}$
CNT interconnect aspect ratio	~ 3:1	5:1
Electrical resistivity	$10^{-4} \sim 10^{-5} \text{ Ohm.m}$	$10^{-6} \text{ Ohm.m}$
Thermal conductivity	13-17 W/mK	40 W/mK
Thermal cycling life time (Reliability performance)	N/A (No report on thermal cycling)	200 cycles at -20°C to 150°C accelerated stress.
High frequency performance	N/A (No report on detailed HF performance analysis of real CNT vias)	The CNT interconnect resistance and inductance is expected to remain constant at frequencies up to 1 GHz . The skin effect should be ignorable at 1 GHz.

**Table 3 : Summary of the CNT based via specification**

### 3.2 WP2 : DESIGN AND SIMULATION ACTIVITIES

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
IMT	TRT, UPMC, IMT, TSA, UNIVPM, LiU, ICN	$T_0 + 3 - T_0 + 13$	D2.1 to D2.5 M2.1	T2.1 to T2.5	<b>On Going</b>

#### 3.2.1 WP OBJECTIVES

In this WP, we will design and simulate all the CNTs and graphene based sub-components forming the nano T/R module to be demonstrated in WP5 comprising filters/oscillators, switches, mixers, LNAs and PAs and finally an antenna. The main technical objectives are:

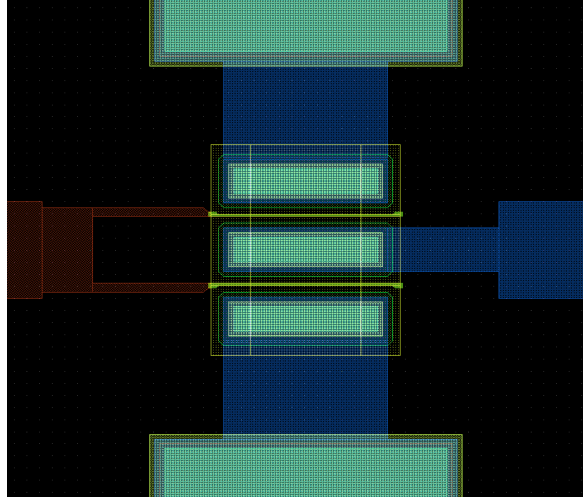
- Design and modeling of CNT and graphene based FET and then design and modeling of LNA, PA and mixer based on either CNT or graphene
- Design and modeling of CNT switch
- Design and modeling of CNT filter/oscillator and graphene mixer
- Design and modeling of CNT antenna
- Design and modeling of LNA based graphene
- Design and modeling of a graphene loaded antenna.

#### 3.2.2 PROGRESS TOWARD OBJECTIVES : STATUS OF ACTIVES TASKS

##### 3.2.2.1 Task 2.1: Design of broadband distributed amplifier CNT FET; prospects for LNA, PA, and mixer (IMT/LAAS)

For the CNT FET, preselected semiconducting CNT's need to be utilized to achieve the highest CNT current control. This puts increasing limitations as to the Source – Drain separation of the CNT FET fabricated since during the selection process (Density Gradient Ultracentrifugation) CNT length is

reduce to an average of below  $1\mu\text{m}$ . The circuit design has to be provided with detailed results regarding the effect of D-S separation and channel length in order to achieve the optimum FETs. A series of test transistors have been designed to study those parameters (**Figure 3**).



**Figure 3: Schematic of CNTFET active area detail**

In short the designed mask incorporates:

- Source Drain separation (between  $2\mu\text{m}$  and  $100\text{nm}$ )
- Gate fingers (2 – 6)
- Gate length ( $10 - 40\mu\text{m}$ )
- Gate width ( $1\mu\text{m} - 50\text{nm}$ )

### 3.2.2.2 Task 2.2: Design of the CNT based RF switch (TRT)

The design of the RF switch has been based on a 4-electrode design as shown in Figure 4 below. This design consists of two pairs of electrodes: a voltage  $V_1$  will be applied to the inner pair of electrodes responsible for the connection of the CNTs and a voltage  $V_2$  will be applied on the outer pair of electrodes in order to force the electrodes to contact. This particular design has been devised in order to apply a lower voltage between the “contact CNTs”.

For this particular design to work, the distance between the electrodes with CNTs,  $Int_{elec}$ , has to be as close as possible and from a technological point of view, this will depend on the electron beam lithography step and in this case, has been assumed to be **100nm**. Another parameter that needs to be considered is the length of contact between the CNTs,  $L_{cont}$ . Upon actuation, the CNTs can be connected either by “*tip contact*” or by “*side contact*”. For this preliminary simulation studies, the length of the contact upon “side-contact” connection is assumed to be of the order of **116nm**. This parameter has been obtained in the literature and it has been included in a MATLAB simulation pack at TRT.

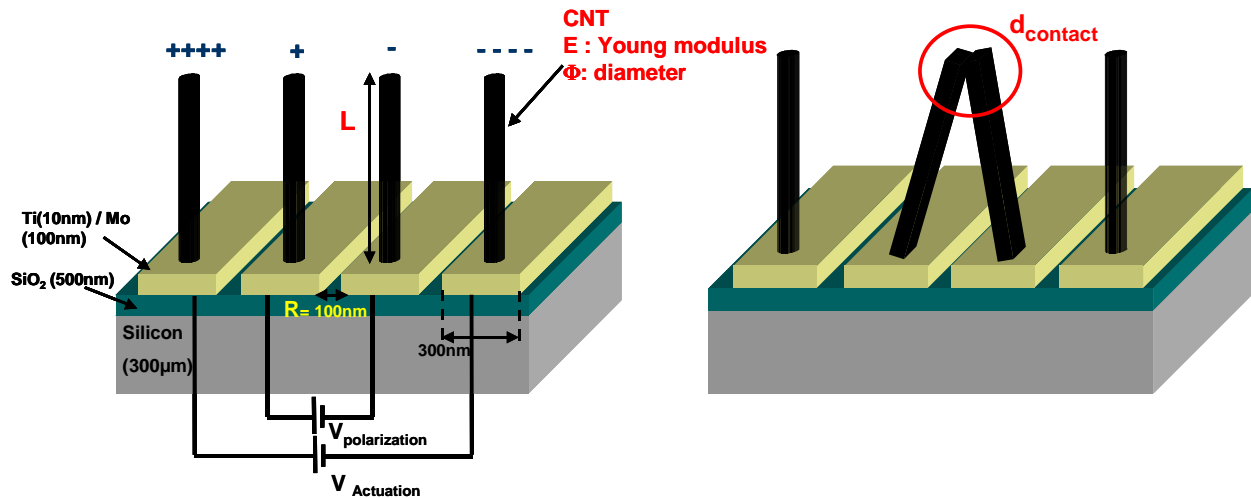


Figure 4 : 4 electrodes concept for tweezer configuration

The key parameters identified for simulation purposes were :

- ✓ Young's modulus for the CNTs,  $E$
- ✓ Diameter of the carbon nanotubes,  $\phi_{cnt}$
- ✓ Length of the CNTs,  $L$
- ✓ Interspacing between the electrodes with CNTs,  $Int_{elec}$
- ✓ Interspacing between the CNTs,  $Int_{cnts}$

Based on the simulation carried out, the dimensions to be used have been obtained and the process flow established.

### 3.2.2.3 Task 2.4: Design the CNT based antenna (UPMC)

During these 6-months first time period, UPMC was involved in three main actions dedicated to WP 2 in order to reach CNT-based antenna design with specific innovative operational criterii such as high degree of miniaturization, working frequency around 20 GHz, very low insertion losses, maximum exploitation of CNT material advantages compared to standard integrated semiconductor technologies.

- *Experimental SW/MW material parameters identification in microwave domain*

Exceptional theoretical work on CNT material parameters already published in a unique, bundle or dispersed in liquid solution configuration demonstrate exceptional complex conductivity and permittivity behavior of this material in frequency as a function of its chirality (zigzag, armchair or chiral) and diameter and length as in <sup>1</sup>for example.

In order to validate these hypotheses, UPMC in cooperation with IEMN (sub-contractor) has set up an experimental probe test environment dedicated to vertical SW/MW CNT layer characterization with a 0.04-110 GHz working frequency. Homemade modeling tool taking into account coplanar multilayered configuration as in <sup>2</sup>, leading permittivity extraction in microwave frequency were developed in order to qualify vertical CNTs delivered material for this project, ie from technological

<sup>1</sup> A. M. Attiya, Lower Frequency limit of carbon nanotube antenna, Progress In Electromagnetics Research, PIER 94, 419{433, 2009

<sup>2</sup> Erli Chen and Stephen Y. Chou, Characteristics of Coplanar Transmission Lines on Multilayer Substrates: Modeling and Experiments, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 45, NO. 6, JUNE 1997

process from SHT/Chalmers partners. By complementary CNT electrical properties extraction, such as lineic inductance/capacitance, contact resistance, CNT-based antenna design procedure becomes functional.

## ▪ Optimization of CNT-based antenna design procedure

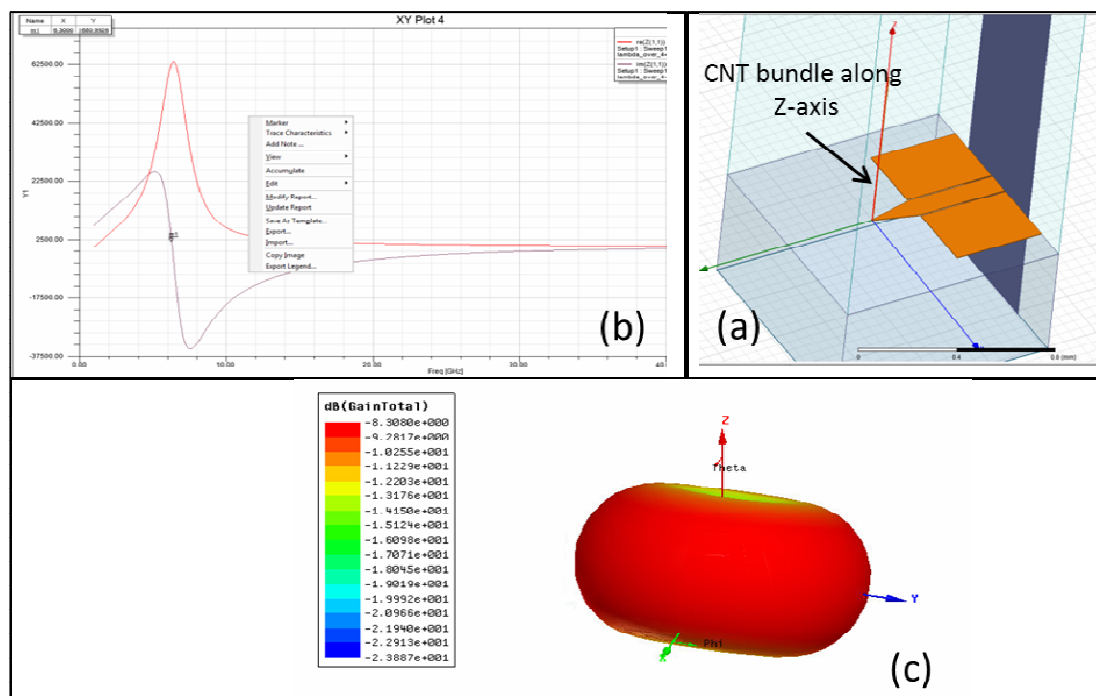
CNT-based antenna design work relies on use of 3D FDTD electromagnetic analysis from HFSS software. Free space (monopole/dipole) and integrated on usual substrate (quartz, Si) CNT-based antenna topologies have been investigated by UPMC in order to validate potential antenna miniaturization by this innovative material thanks to the existence of a negative imaginary conductivity leading to high inductive behavior compared to classical metals in microwave domain.

CNT-based antenna design is optimized in terms of resonant frequency / frequency bandwidth, Input impedance and radiation patterns. CNT-based material part is assumed by a parametric conductive tube with specific impedance surface and diameter in order to model a vertical SW/MW metallic CNT bundle.

First simulations results revealed an efficient radiation at 6.3 GHz of a 750 $\mu$ m-length CNT bundle based quarter-wave dipole although the same topology demonstrates a resonant frequency ( $\lambda/2$ ) at 100 GHz for a metallic wire of the same length (cf Figure 5). Others antenna configurations (slot-wired antenna) are under study to match antenna expected performances to its topology.

## ▪ Operational layouts delivery with technological process compatibility (TRT/SHT/Chalmers)

First layouts of vertical CNT layer-based test samples for microwave material qualification from TRT/SHT/Chalmers process have been set up. First CNT-based quarter-wave length monopole layouts are under design process finalization.



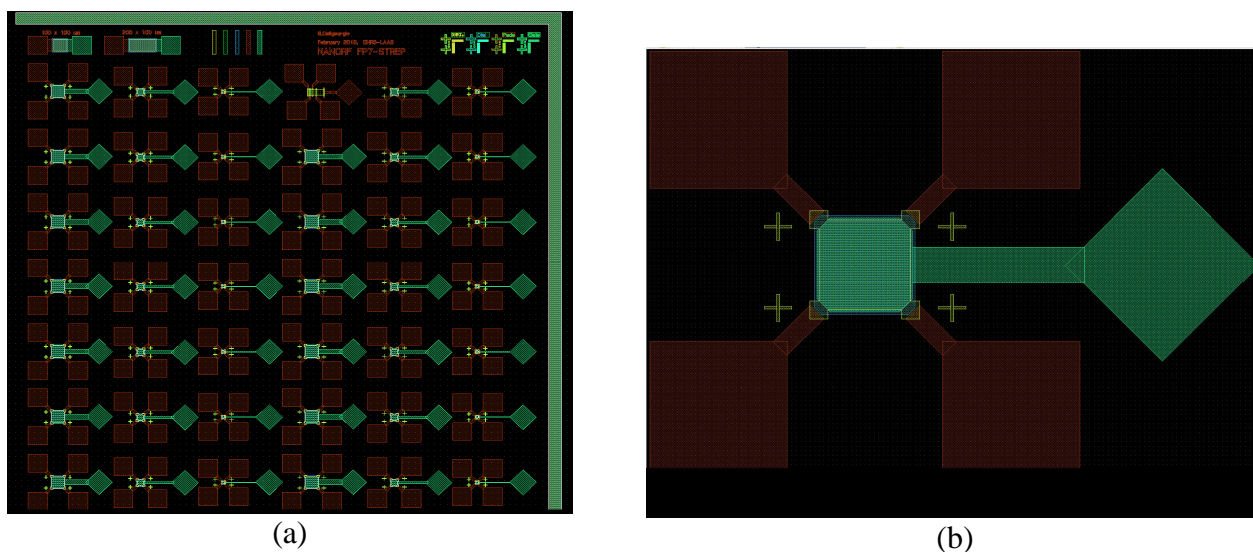
**Figure 5 : Example of a CNT-based dipole antenna integrated on quartz substrate: (a) 3D desing – (b) Input complex impedance – (c) 3D radiation pattern**

### 3.2.2.4 Task.2.5 Design and simulation of RF graphene devices

- Graphene FET design (LAAS/FORTH)

The initial step is to evaluate the effect of dielectrics to graphene mobility. To this end, the Hall Effect will be used on graphene. A set of masks has been designed to facilitate comparative studies (**Figure 6**).

Specifically, HALL, resistivity and gated HALL measurements before and after gate dielectric deposition will allow measuring the graphene behavior and gating dielectric impact. Ability to also measure resistivity by the TLM method and Gate capacitance to measure effective dielectric coefficient in case of composite stacks has been incorporated into the design.



**Figure 6: Schematic of GHALL mask period (a) and a single HALL device (b)**

In short the design incorporates:

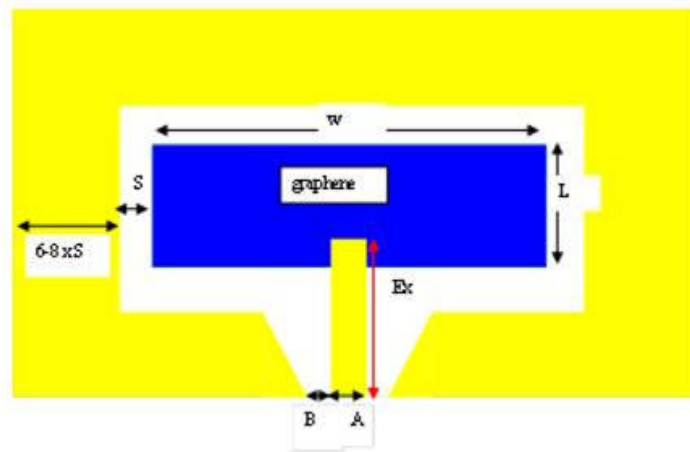
- Different Van der Paw gated structures to measure mobility degradation and dielectric performance over graphene (41 device per period, 3 different sizes)
- Test capacitors to evaluate gate dielectric and breakdown (2 per period)
- TLM measurement device to verify graphene sheet resistance measurements (1 per period)

These masks have been fabricated and initial fabrication of test devices has started.

- Graphene Antenna (UNIVPM & IMT)

We have started to design the graphene antenna which is a device not still reported and we have chosen a slot antenna in coplanar geometry depicted in the Figure 7 below:

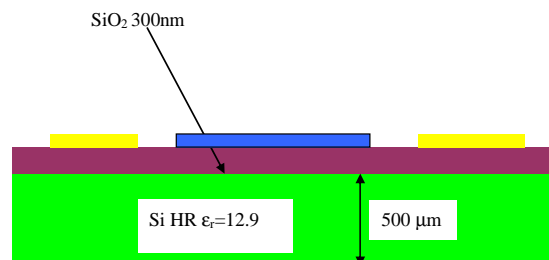




**Figure 7 : graphene coplanar antenna geometry**

Considering  $W = \lambda_g/2 = 0.9$  cm,  $L = 0.1\lambda_g = 0.18$  cm,  $S = 450$   $\mu$ m

The CPW ground electrodes width  $6 \times 0.045 = 2.7$  mm,  $A = 100$   $\mu$ m,  $B = 50$   $\mu$ m and  $\lambda_g = 1.8$  cm. The graphene antenna is deposited on a Si/SiO<sub>2</sub> substrate having the thicknesses displayed in the Figure 8 below:

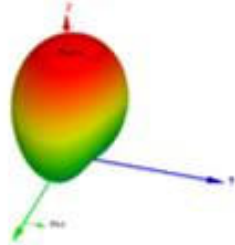
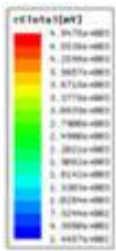


**Figure 8 : substrate used for the graphene coplanar antenna**

The resistance of graphene monolayer is considered 700 ohms typically for graphene grown by CVD to be used for the fabrication of such big antenna.

For this antenna the radiation field at 13 GHz is displayed below, as well as the antenna parameter showing a good efficiency.



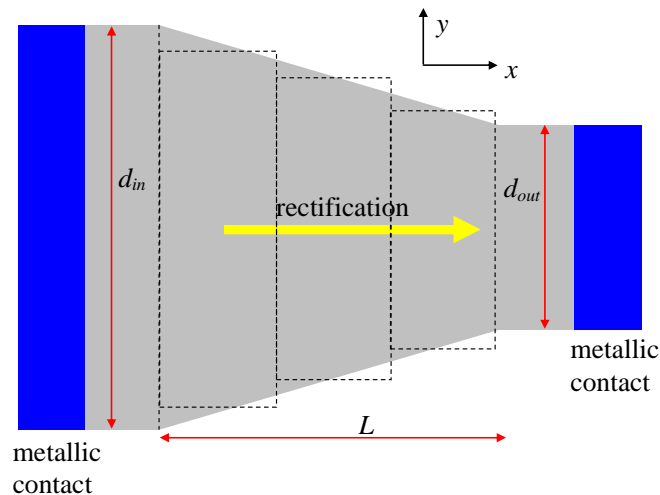


Max U	0.0311	W/sr
Peak directivity	3.1862	
Peak gain	3.057	
Peak Realized gain	0.3916	
Radiated Power	0.122	W
Accepted power	0.128	W
Incident Power	1	W
Radiation Efficiency	0.959	

**Figure 9 : Radiation fields of the graphene coplanar antenna**

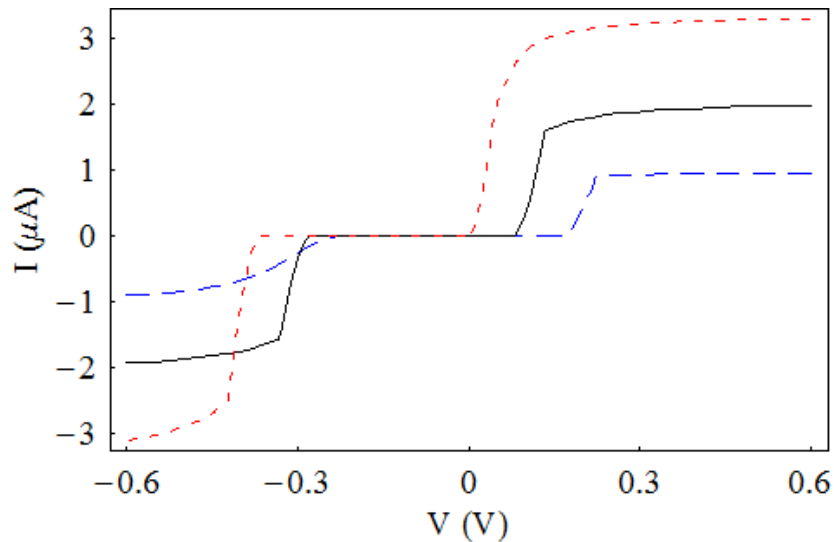
The radiation field is well confined and with low lobes, while the efficiency is very good (Figure 9). Better results could be obtained by biasing the with a dc voltage the graphene and the ground electrode of the antenna. In this case, the resistance is reduced to 10-20 ohms and the radiation parameters are still improved without degrading S11 and keeping at the VSWR<3.

The second device that we have simulated is a geometric graphene diode where the rectification mechanism is done using only the geometry of the diode itself in the ballistic regime (Figure 10).



**Figure 10 : Graphene diode devices using for the simulation**

The Dirac equation was solved in each rectangle and the continuity conductions were imposed at each boundary. The simulated I(V) characteristic is displayed below (Figure 11):



$E_F = 0$  (blue dashed line), 0.1 eV (solid black line) and 0.2 eV (red dotted line).

**Figure 11 : simulated I(V) characteristic**

We will see in the I(V) above the ambipolar transport property of graphene, as well the behavior of the diode.

## 3.3 WP3 : FABRICATION ACTIVITIES

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
FORTH	TRT, CHALMERS, FORTH, LAAS, UPMC, IMT, GI, SHT, LiU, ICN, Tyndall	$T_0 + 3 - T_0 + 25$	D3.1 to D3.8 M3.1	T3.1 to T3.10	<b>On Going</b>

### 3.3.1 WP OBJECTIVES

In this work package we will fabricate all the CNT and graphene based sub-modules that have been designed in the previous work package. The principal objective of this work package is to fabricate the test structures and also final components based on the results of WP2. The manufacturing process in this WP will be optimised and the products will be delivered to WP4. The technical objectives for this work package are:

- To develop CNT growth technology to achieve the desired structure following results of the design activities. CNT growth must be compatible with all the substrate technology to achieve the desired RF components as specified in Work-package 1.
- To develop graphene growth techniques either based on exfoliation for proof of concept RF graphene devices and at the wafer scale for graphene circuits to be used in the sub-modules
- To set-up a pilot line for manufacturing CNT for microwave applications.
- To fully characterize the CNT that have been grown by thermal CVD or plasma enhanced CVD . The characterization of graphene via exfoliation or epitaxial growth on SiC. The goal

will be to verify that physical, structural, etc. properties will be compatible with the RF functions we want to achieve.

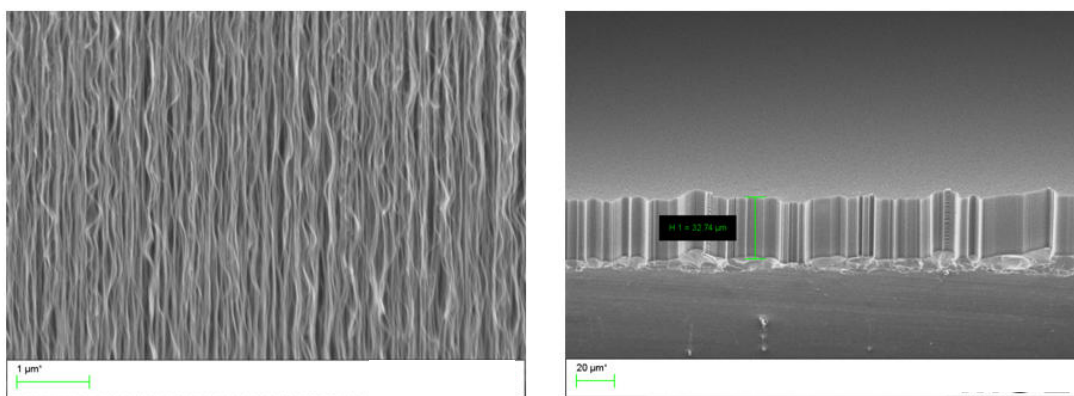
- To fabricate the RF submodules designed in the previous work package: CNT FET (LNA, PA and mixer), the RF switch, the RF filter/oscillator and the antenna, LNA based on graphene, graphene antenna, graphene mixer and graphene detector
- To develop various technologies that will allow for the integration of the sub-modules produced within this work package to be integrated on a single Si carrier wafer.
- To supply other work packages with CNT and graphene for characterization, modeling, simulation and demonstration and to optimize CNT and graphene according to their feedbacks.

## 3.3.1.1 CNT and graphene growth technology (SHT/CHALMERS)

### • CNT growth (SHT)

In this period, we have developed various recipes to grow CNTs in difference conditions and morphology for different applications in this project. Both thermal chemical vapour deposition (TCVD) and plasma enhanced chemical vapour deposition (PECVD) method have been used to grow CNTs on different substrates.

In the TCVD method, common silicon wafer is used as the substrate. A layer of catalyst which is consisted of  $\text{Al}_2\text{O}_3$  and Fe is then deposited onto the substrate by an electron beam evaporator. In this case a 1 nm thick Fe is evaporated as the catalyst and 10 nm thick  $\text{Al}_2\text{O}_3$  is used as diffusion barrier layer. By using a TCVD system, CNTs are grown from the catalyst particles, forming the forest morphology on the chip, as shown in Figure 12 below. The synthesis process is carried out under a pressure of about  $1 \times 10^{-6}$  mbar and the temperature of roughly 700 °C. A mixture of  $\text{C}_2\text{H}_2$  and  $\text{H}_2$  in proportions 1:9 to a pressure of 11 mbar is supplied as the gas source. During the growth the chamber is flowed with the mentioned gas mixture, while maintaining a constant pressure. The length of the CNT forests is controlled by the growth time.



**Figure 12 : CNT forest samples grown by TCVD**

In the PECVD method, the growth process is similar to the TCVD method, and the same carbon precursor and reduction gas have been used. What is different is that plasma is introduced after the pre-heating process is finished therefore the CNTs grown in this manner brings better alignment in the vertical direction, especially for individually aligned CNTs. An example of the CNTs grown by this method is shown in Figure 13as below.

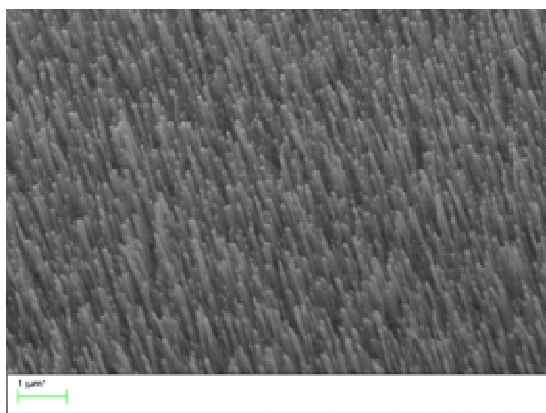


Figure 13 : CNT forest samples grown by PECVD

## • Graphene growth

There are several ways to obtain graphene material and we started to study the different graphene synthesis methods.

### ▪ Graphene CVD growth on metals (SHT/CHALMERS)

In the past half year, the monolayer graphene was optimized and fabricated. A thermal CVD was used for graphene synthesis. The 25µm copper foil substrates were cleaned with acetone, IPA and DI water. They were then placed on the heating stage with a thermocouple attached on the stage surface. C<sub>2</sub>H<sub>2</sub> and Ar were chosen respectively as the carbon precursor and the gas carrier. The reactor chamber was initially pumped down to a base pressure of 0.5 mbar. 1000sccm Ar and 20sccm H<sub>2</sub> were then introduced into the furnace. The temperature was raised at a rate of 300 °C/min to about 900 °C and maintained for 10 min to anneal the Cu films. 5 sccm C<sub>2</sub>H<sub>2</sub> was introduced at a flow rate of 5sccm to start the graphene growth. The growth lasted for 10 min. Finally, all the gas supplies were turned off, and the residual gas was pumped to a pressure of ~0.1 mbar. The reactor chamber was subsequently naturally cooled to room temperature with 1000sccm Ar and 20sccm H<sub>2</sub>. An example of the graphene grown by this method is shown as below in Figure 14 and Figure 15.

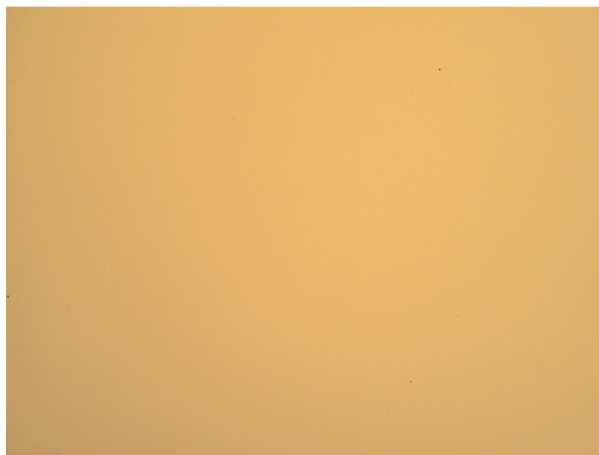


Figure 14 : Graphene grown on Cu

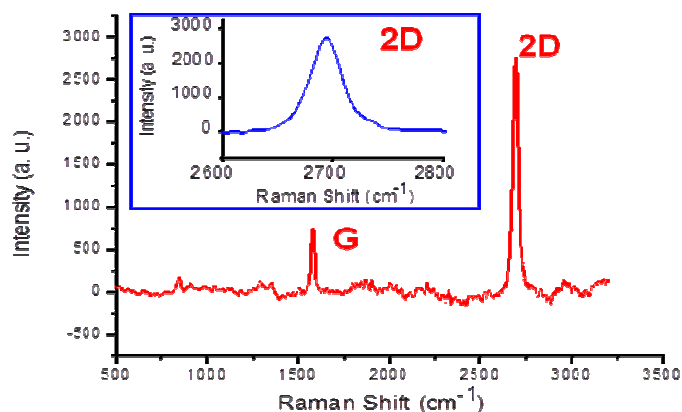


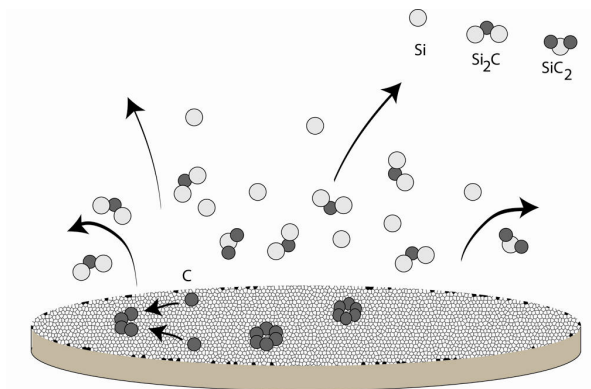
Figure 15 : Raman spectra of graphene grown on Cu.

## ▪ SiC decomposition (LiU)

The graphene on silicon carbide has focused on growth of monolayer graphene on different polytypes.

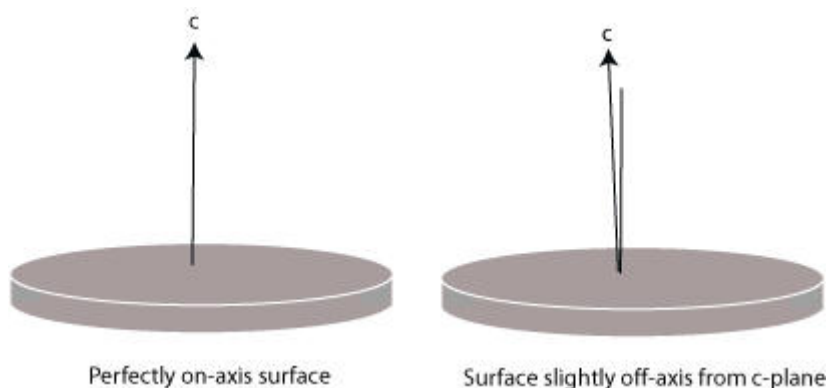
The conventional polytypes that are commercially available are 6H-SiC and 4H-SiC. The chemical composition is the same with silicon and carbon atoms building up the crystals, but they distinguish in the stacking order of the atoms. In 6H-SiC the stacking results in a unit cell that is 15 nanometers in height, while the stacking in 4H-SiC results in a unit cell that is 10 nanometers in height.

The process for growth of graphene on SiC is based on sublimation of a wafer (Figure 16). The top surface is heated, and the silicon atoms leave the surface with remaining carbon atoms that form graphene. In an optimized case the carbon atoms will form a monolayer of graphene. In case of sublimation we have a scenario which is now related to decomposition/erosion of Si–C bilayers from the lattice stack. In this act, since Si has the highest vapor pressure, Si leaves the surface while C nominally rests and migrates on the surface.



**Figure 16 : Growth of graphene on SiC**

At locations on the surface where the surface orientation is not planar, for example at macroscopic defects, there is an enhanced probability for formation of bilayer graphene, or even few layer graphene. In addition, when the SiC crystals that are produced in boule growth is cut to produce wafers on which graphene may be grown, the cutting is typically not perfect along the low index surface of SiC. In case of 6H-SiC and 4H-SiC this surface is the (0001) surface. As a result, there is a nominal off orientation from the (0001) on-axis surface. This off-axis surface is characterized by steps (Figure 17).



**Figure 17 : Surface orientation of the substrate**

When heated, the surface undergoes a surface reconstruction. This reconstruction process is a natural habit for SiC. Surface restructuring after heating up SiC results in formation of steps and terraces and they may have an impact on the doping uniformity (graphene conductance) or bilayer formation. The main effect behind the surface restructuring is the phenomenon of step bunching which is different in the different SiC polytypes due to energetical reasons. Understanding this process may facilitate the choice of optimal substrates. It has been shown that the graphene resistance increases with step heights, step density, and step bunching. Therefore it is possible to speculate that spatial control of step configurations can be used to concentrate current into specific regions of a graphene sheet for a new device design

In case of the two polytypes, the 6H-SiC and 4H-SiC, the difference in stacking will be a factor to consider during the sublimation. To date, the graphene formation has not been discerning for any given polytype.

In addition, the availability of 6H and 4H-SiC wafers is not similar. Until now both polytypes have been available for research and development. Lately, we found that the 6H-SiC is less readily available with such wafers that have a surface finish that is suitable for graphene growth. The two major suppliers of high quality wafers are Cree Research Inc., and SiCrystal AG (Germany). Since 1-2 years Cree stopped producing 6H-SiC wafers, and SiCrystal has no longer a final polishing of 6H-SiC wafers that is typically applied for epitaxy (so called epi-ready polishing). The optical polish in wafers from SiCrystal has remaining surface scratches, and these are highly unfavorable for monolayer graphene formation.

In comparison of polytypes, we found some difference when epitaxial graphene growth was performed on the Si-terminated face of 4H-, 6H-, and 3C-SiC substrates by silicon sublimation from SiC in argon atmosphere at a temperature of 2000°C. The graphene surface morphology, thickness and band structure was thoroughly studied using atomic force microscopy, low-energy electron microscopy, and angle-resolved photoemission spectroscopy. Differences in the morphology of the graphene layers on different SiC polytypes is related mainly to the minimization of the terrace surface energy during the step bunching process. The uniformity of silicon sublimation is a decisive factor for obtaining large area homogenous graphene. It is also shown that a lower substrate surface roughness results in more uniform step bunching with a lower distribution of step heights and consequently better quality of the grown graphene.

Three samples have been supplied to partners. The size of the samples is 7x12 square millimeter. The substrate is nominally on oriented (0001) semi-insulating 4H-SiC (supplied by Cree Research Inc.). By the growth regime it is expected to have at least 75% of 1 ML graphene on the surface area.

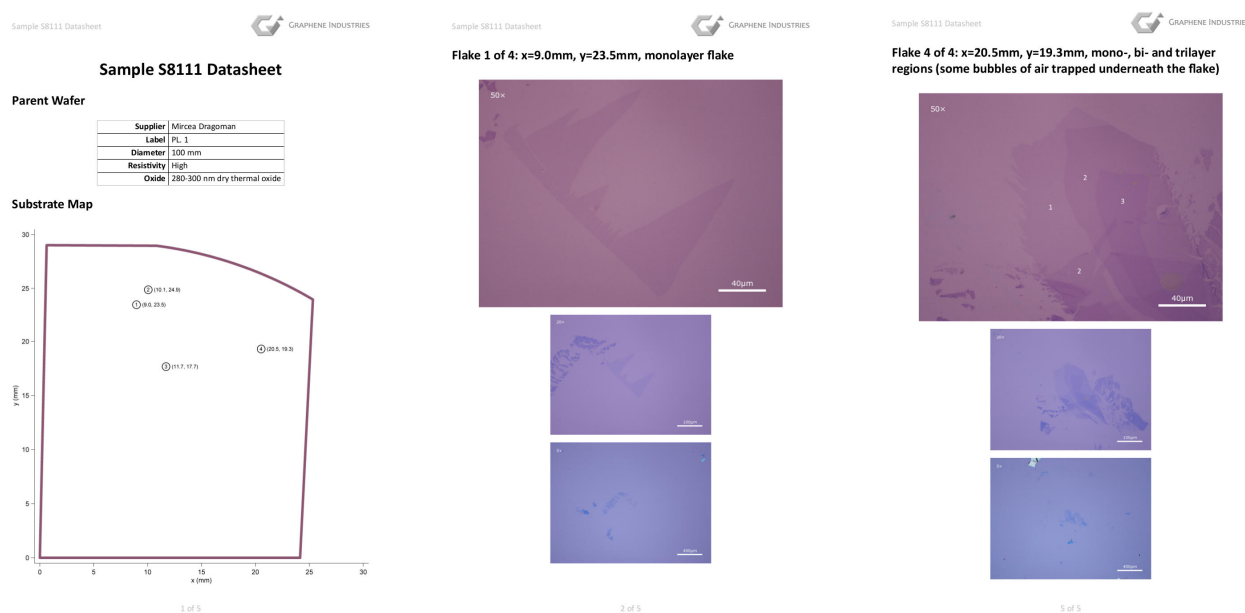
### ▪ Graphite ex-foliation (GI)

During the first period, different samples containing mono-crystalline graphene flakes produced using high resistivity silicon wafers provided by consortium partner IMT :

- Silicon dioxide (SiO<sub>2</sub>) layers grown via chemical vapour deposition (CVD) tested as an alternative to thermally grown SiO<sub>2</sub>.
  - Graphene yields significantly lower on CVD oxide: <10% compared to thermally grown. CVD oxide has a rougher surface, reducing graphene flake adhesion and therefore yields.
  - Since poor adhesion also reduces device fabrication yields, we recommend thermal oxide growth for new wafer batches.
- Three samples (on thermal oxide) sent to consortium partner FORTH. >12 flakes produced, mixture of mono-, bi- and trilayers of graphene



- Datasheets provided for each sample, showing location and number of graphene layers for each flake (Figure 18). The number of layers was determined using optical contrast measurements at an illumination wavelength of 560 nm (filter bandwidth: 10nm).
- Additional graphene flakes are now being prepared on SiO<sub>2</sub> and hexagonal boron nitride (hBN). Graphene on hBN will allow higher carrier mobilities.



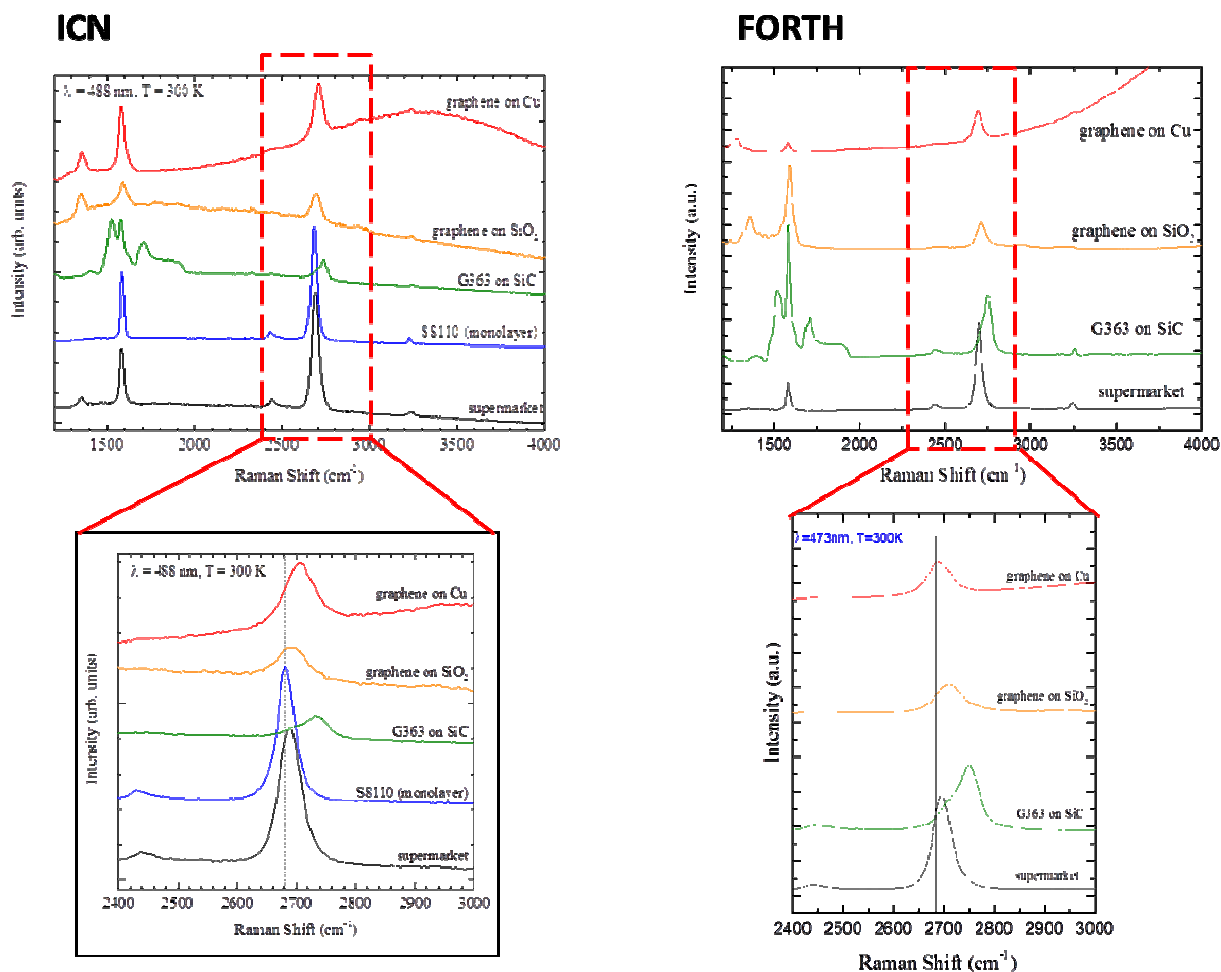
**Figure 18 : Three pages from the datasheet for sample S8111**

### 3.3.1.2 CNT and graphene material characterization (ICN/FORTH/Tyndall)

Graphene can be highly complex materials and substrate morphology and growth conditions are of paramount importance to the final material quality. During the first period, we performed a full characterization of these materials, allowing the use of appropriate material features for the intended goals of NANO-RF.

Different samples provided by LiU (SiC decomposition), SHT/CHALMERS (CVD on metal) and Graphene Industries were analyzed by Raman spectroscopy.

Raman characterization are presented on Figure 19

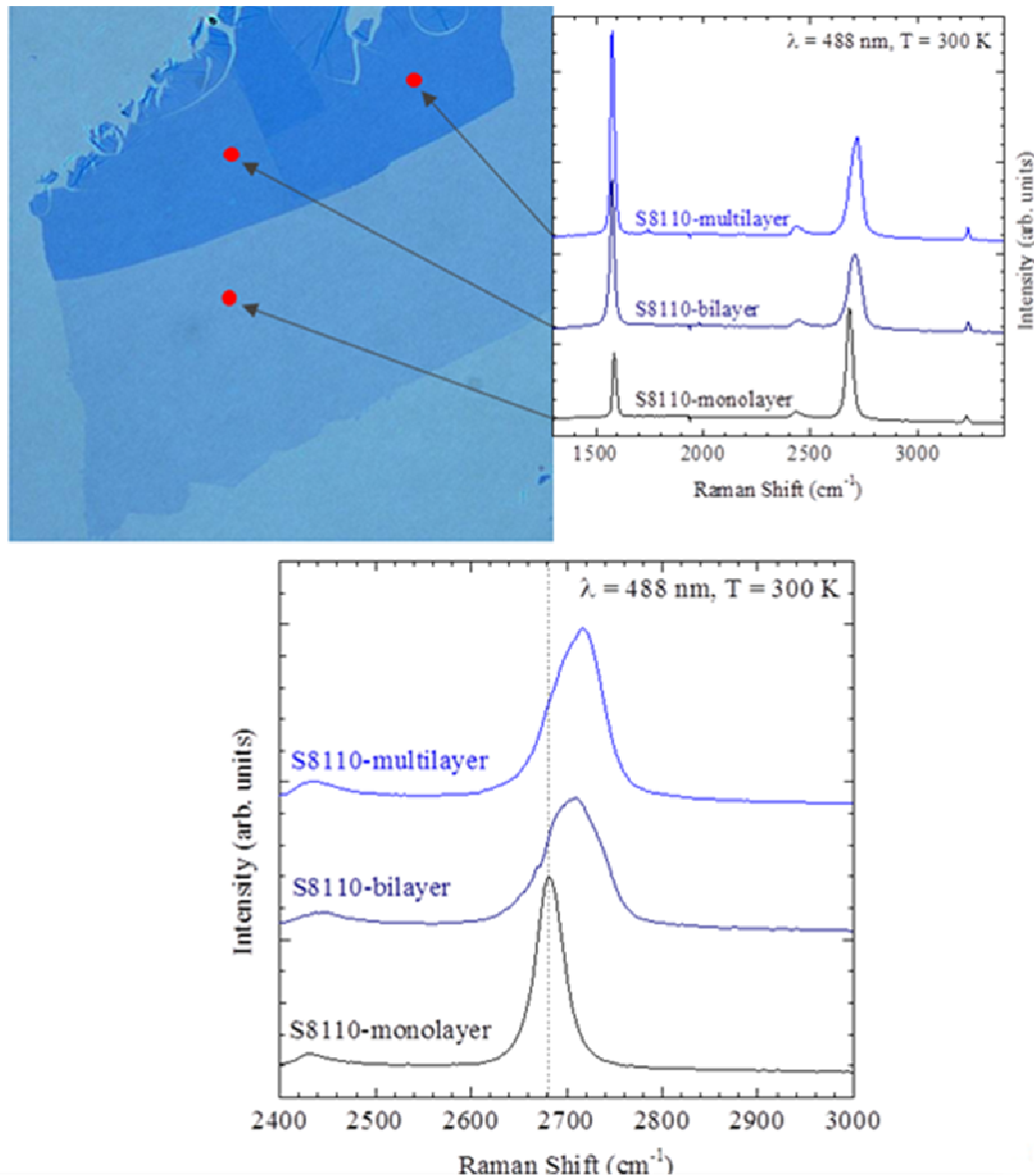


**Figure 19 : Raman characterization from ICN compare with FORTH**

The results obtained by ICN and FORTH are comparable and can demonstrate the high quality of graphene provided by Graphene Industries.

Complementary measures have been carried out on the Graphene provided by GI (sample S8110) and the results are presented in Figure 20. In case of the S8110 sample, ICN measured Raman spectra at three different positions of an isolated graphene flake with different contrast in the optical microscope (red dots in the attached image indicate the positions of the laser).





**Figure 20 : Raman measurement on graphene provided by GI**

To summarize the work done during the first period:

- A variety of graphene samples was produced or acquired from different sources (delivered by FORTH)
- Micro-Raman spectroscopy was conducted at different position of the samples. Based on detailed analysis of the line shape, line width, mode intensity and spectral position, the first set of graphene samples was characterized.
- The analysis of these features allowed a detailed classification of the different samples regarding the presence of defects, graphene layer numbers, and the influence of different substrates.
- Additional graphene samples were recently send from FORTH to ICN for continued investigations.
- Design specifications for isolated and bundled vertical and horizontal CNTs were developed and defined.

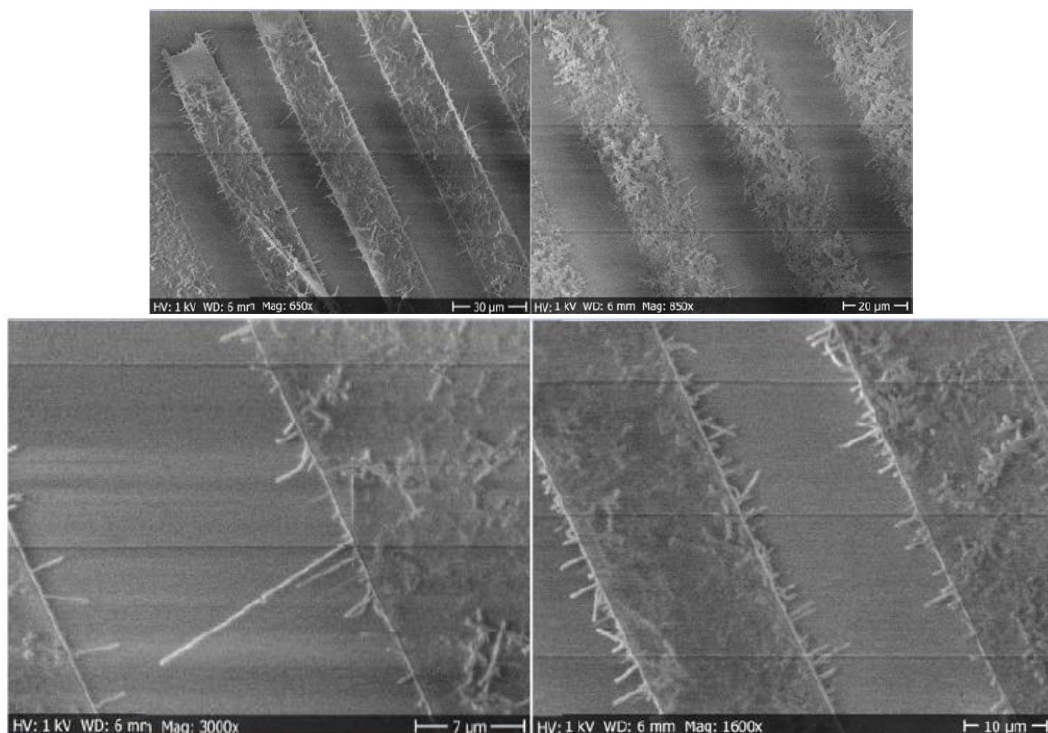
- An experimental method (two laser Raman thermometry) was developed aiming towards the determination of the thermal conductivity of covalently and non-covalently bound horizontal CNTs which are currently under development at SHT.

### 3.3.1.3 Fabrication of CNT FET (SHT/LAAS)

In order to fabricate a FET, the CNTs should also be semiconductive in order to keep a bandgap. Two ways are studied to obtain semiconducting CNTs :

- Horizontally single wall CNTs :

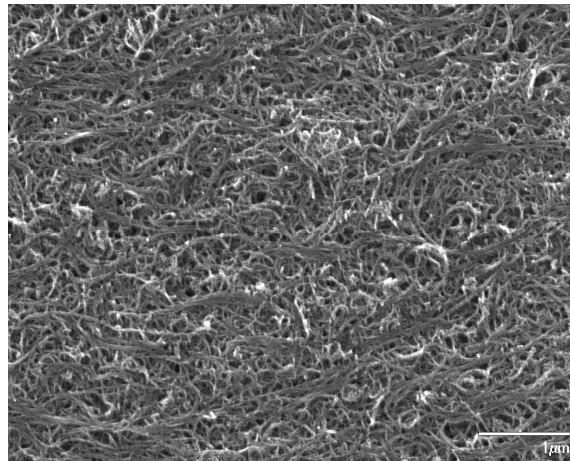
We try to grow horizontally aligned single-walled CNTs on ST-cut quartz, which could have a better control of CNT spatial position and orientation for the integration of CNT FET. Based on the previous research, first of all, the 4 inch quartz was annealed at 900°C for 8 hours in air; thereafter through standard lithography process the patterned strip structures were fabricated. After that the 2Å thickness of Fe as catalyst was deposited into the patterned line structure by E-beam evaporation; then we diced the whole quartz wafer into small pieces and have a lift-off to remove the residual photoresist. The CNT growth was conducted by the TCVD method with acetylene as carbon precursor. We have obtained some preliminary results as shown in the picture below. The length and density of CNTs is not high enough at the moment, therefore right now what we're trying to do is to perform the CNT growth under different process parameters conditions, in order to map out the process window, furthermore getting more uniform, longer and higher density of semiconductive single-walled CNTs. SEM pictures are presented on Figure 21



**Figure 21 : Single-walled semiconductive CNT growth for FET fabrication**

- Aligned CNT deposition

CNT are one dimensional structure and deposition in solution makes a randomly oriented carpet (Figure 22).



**Figure 22 : Image of randomly CNT deposition**

To obtain maximum conductivity in the channel of a CNTFET aligned CNTs need to be fabricated. Given the choice of preselected semi-conducting CNTs which come in solution, the capillary forces alignment method is explored to obtain aligned CNT bundles that will enable superior CNT performance.

Experiments using dip coating and capillary forces are planned to measure and optimize the following parameters:

- CNT alignment
- Density of deposited CNTs
- Carpet thickness

The realized carpets will be characterized by SEM and then electrically to measure their current carrying ability.

### 3.3.1.4 Development of carbon nanotube interconnects (CHALMERS)

In this task, Chalmers is supposed to develop the interconnect technology using CNTs as the building block. In this period, fabrication flow for making CNT-filled through silicon vias (TSVs) has been designed. Preliminary fabrication of the in-situ CNT growth in vias has been demonstrated.

The vias in this work were etched in Si by a standard DRIE process. The CNT bundles were directly grown by thermal chemical vapor deposition (CVD) from a pre-deposited catalyst layer on the bottom of the vias (Figure 23a). The CNT forests were grown from a 10/1 nm thick Al<sub>2</sub>O<sub>3</sub>/Fe catalyst layer, deposited by electron beam evaporation on Si substrates and patterned by standard photolithography and lift-off processes. The catalyst layer was firstly annealed on a heater heated to 500 °C in a flow of 692 standard cubic centimeters (sccm) H<sub>2</sub> for 3 minutes. After that, the heater temperature was raised to 700 °C at a rate of 300 °C/min and a flow of 200 sccm C<sub>2</sub>H<sub>2</sub> was introduced into the reactor for growing CNTs. The temperature at which C<sub>2</sub>H<sub>2</sub> was input was varied from 500 °C to 700 °C to

grow forests with different CNT volume fractions. Different growth time was applied to produce CNT forests of different heights. Typical growth rate was in the range of 1  $\mu\text{m/s}$ .

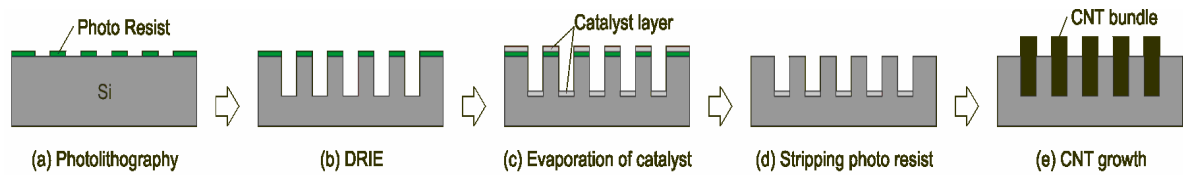


Figure 23. CNT Via growth process illustration

The growth of CNT in the TSV vias shows good results (Figure 24). The next step will be to characterize these interconnects. However, the growth condition (750  $^{\circ}\text{C}$  in hydrogen and acetylene) is not compatible with semiconductor active devices. Therefore, transfer technologies should be developed in parallel to solve the compatibility issues.

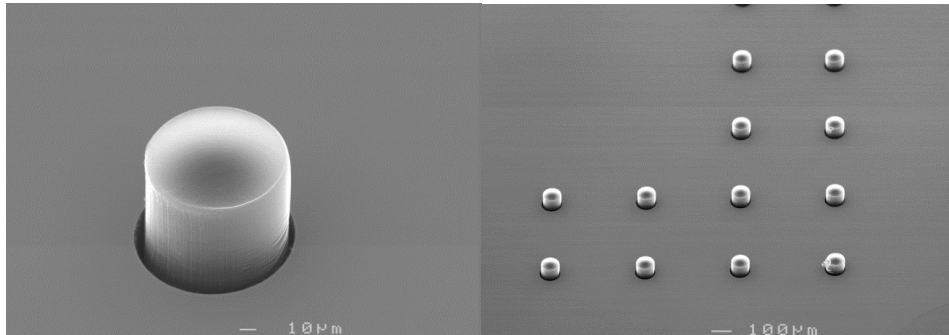



Figure 24. Growth result of CNT vias.

	<b>D7.15 - Progress Activity Report #1 (T0 – T0+6)</b>	29/30
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## 4 DISSEMINATION AND EXPLOITATION ACTIVITIES (WP6)

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
TRT	TRT, ICN	T <sub>0</sub> +0 – T <sub>0</sub> +36	D6.1 to D6.6	-	On Going

### 4.1 PROJECT LOGO

A few drafts of the project logo had been presented to the partners during the Kick-Off meeting of the project. Following the remarks and comments made during this meeting, the following final logo has been chosen. It corresponds to the deliverable D6.1, due date T<sub>0</sub>+3.

The “hexagonal structure” represents graphene or carbon nanotube that will be used in the realization of the different devices during the project.

This logo will be applied to any support of dissemination used by any member of the consortium to communicate on project related activities: presentations, papers, posters, newsletter, website, etc.




### 4.2 PROJECT WEBSITE

Corresponding to the deliverable D6.1, the NANO-RF website has been activated online on 12 February 2013 and is available at the following address: <http://www.project-nanorf.com>. The missions of the website are:

- (i) To provide visibility to the project and disseminate the scientific/technical achievements to the international communities interested in our activities. This mission is fulfilled by the public area of the website.
- (ii) To provide an efficient mean for communication inside the project consortium for all organizational issues and to allow the partners to exchange, store and retrieve technical data and information. This mission is fulfilled by the private area.



	<h1>D7.15 - Progress Activity Report #1</h1> <h2>(T0 – T0+6)</h2>	<p>30/30</p>
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**Figure 25 : Nano-RF website homepage**