



CARBON BASED SMART SYSTEM FOR WIRELESS APPLICATION



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Project n°318352

Duration : 45 months

Topic addressed : Very advanced nanoelectronic components: design, engineering, technology and manufacturability

WORK PACKAGE 7 : Project management

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WORK PACKAGE 7: Project management

PARTNERS ORGANISATION APPROVAL

	Name	Function	Date	Signature
Prepared by:	S.Xavier	R&D Engineer	26/10/15	
Approved by:	Afshin Ziaei	Research Program Manager	27/10/15	

DISTRIBUTION LIST

QUANTITY	ORGANIZATION		NAMES
1 ex	Thales Research and Technology	TRT	Afshin ZIAEI
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1 ex	National Research and Development Institute for Microtechnologies	IMT	Mircea DRAGOMAN
1 ex	Graphene Industries	GI	Peter BLAKE
1 ex	Thales Systèmes Aéroportés	TSA	Yves MANCUSO
1 ex	SHT Smart High-Tech AB	SHT	Yifeng FU
1 ex	Universita politecnica delle Marche	UNIVPM	Luca PIERANTONI
1 ex	Linköping University	LiU	Rositsa YAKIMOVA
1 ex	Fundacio Privada Institute Catala de Nanotecnologia	ICN	Clivia SOTOMAYOR
1 ex	Tyndall-UCC	Tyndall	Mircea MODREANU

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CHANGE RECORD SHEET

REVISION LETTER	DATE	PAGE NUMBER	DESCRIPTION
v0	07/2015	10	Initial version
v1	26/10/2015	23	All partners contributions
v2	27//10/2015	23	Final version

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1 PROJECT OBJECTIVES AND MAJOR ACHIEVEMENTS DURING REPORTING PERIOD (T0+30 – T0+36)

1.1 PROJECT OBJECTIVES DURING THE REPORTING PERIOD (T0+30-T0+36)

According to the timetable (see Figure 1), the project objectives over the reporting period are:

- Within the framework of WP 2 ‘Design and simulation activities’ : according to the first review meeting, the work for WP2 continues in parallel of WP3 during the second year of the project
- Within the framework of WP 3 ‘Fabrication activities’ to: all the CNT and graphene based sub-modules that have been designed in the work package 2. The principal objective of this work package is to fabricate the test structures and also final components based on the results of WP2
- Within the framework of WP 4 ‘Test activities’: the different manufactured CNT components will be tested, consisting of the following test:
 - CNT FET and graphene electrical characterization: DC to RF
 - CNT RF switch tests
 - CNT based filter/oscillator tests§ CNT based antenna tests
 - RF graphene device (LNA ,mixer, detector)
 - Calibration of basic equivalent circuit models (parameter extraction based on experimental data)
- Within the framework of WP 6 ‘Dissemination and exploitation activities’ : dissemination information and results of the project within the partners and youside the project, as well as proposing exploitation transfer plans and managing the Intellectual
 - List of publication and conference
 - Explotation activities
- Within the framework of WP 7 ‘Project Management’ : to establish durable basis for the project management and monitoring all along the project duration, through the following actions:
 - Regular project and technical meetings;

As described in the following sections, all these objectives have progressed between T0+24 and T0+30.

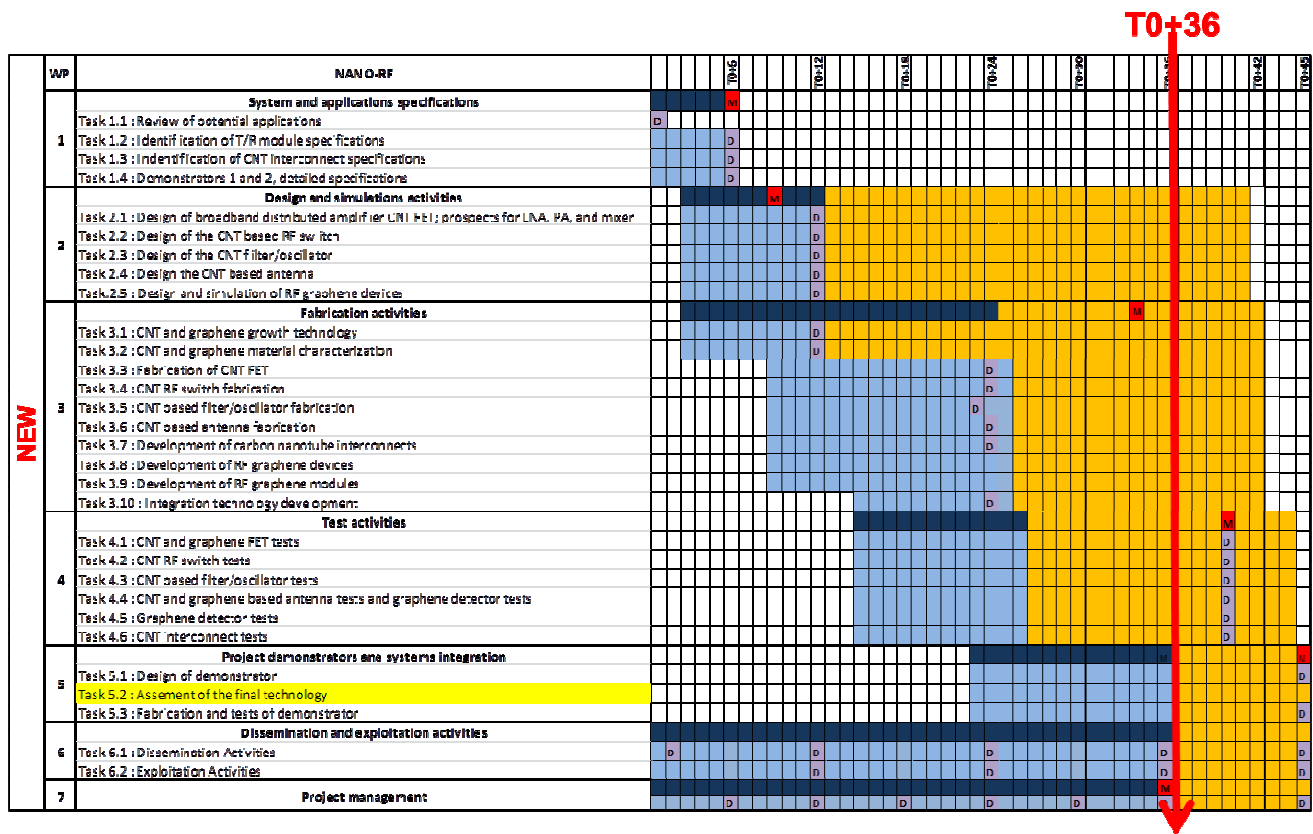


Figure 1 : New NANO-RF Timetable

1.2 MAJOR ACHIEVEMENTS DURING THE REPORTING PERIOD (T0+30-T0+36)

1.2.1 WP2 : Design and simulation activities

In the reporting period (T0+30-T0+36), different devices of the project have been redesigned:

- New design of graphene antenna
- Design of passive RF component

1.2.2 WP3 : Fabrication activities


Regarding the development of the technology for the CNT and graphene growth, some achievements have been obtained:

- Improvement of the quality of CVD graphene after growth condition modification

Several CNT and graphene samples are also prepared and delivered to the consortium.

During the period, some devices have been also fabricated:

- New run of fabrication for CNT and Graphene FET
- Fabrication of test sample for evaluate the RF performance concerning the TSV CNTs
- Passive RF component fabrication
- Optimization of the dielectric layer (HfO2) deposition for CNT and Graphene FET

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1.2.3 WP4 : Test activities

The different manufactured graphene components fabricated in WP3 are measured:

- Characterization of CNT filter
- electrical characterization of dielectric layer (HfO₂) necessary for CNT and Graphene FET

1.2.4 WP6 : Dissemination and exploitation activities

There are several publication and conference from the consortium.

1.2.5 WP7 : Management activities

During the period several meeting were organized:

- 1 project meetings, where all the partners are represented

2 MANAGEMENT ACTIVITIES (WP7)

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
TRT	TRT, CHALMERS, FORTH, LAAS, IMT, TSA, SHT, UNIVPM, ICN, Tyndall	T ₀ – T ₀ +45	D7.1 to D7.21 M7.1	-	On-Going

2.1 MEETING

In order to ensure a correct progress and a high coherence of the collaborative project, during the reporting period, numerous meetings and teleconference were organized:

- 1 project meetings, where all the partners are represented
 - 36-Month Meeting, held in Linköping (Linköpings University) on 13 September 2015;

The agendas, minutes and presentations made for these meetings are downloadable on the private area of the website.

3 PROGRESS IN THE ACTIVE THECNICAL WORKPACKAGE 2

3.1 WP2 : DESIGN AND SIMULATION ACTIVITIES

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
IMT	TRT, UPMC, IMT, TSA, UNIVPM, LiU, ICN	T ₀ +3 – T ₀ +41	D2.1 to D2.5 M2.1	T2.1 to T2.5	Postpone

All the deliverable for WP2 are submitted at T₀+13.

3.1.1 WP OBJECTIVES

In this WP, we will design and simulate all the CNTs and graphene based sub-components forming the nano T/R module to be demonstrated in WP5 comprising filters/oscillators, switches, mixers, LNAs and PAs and finally an antenna. The main technical objectives are:

- Design and modeling of CNT and graphene based FET and then design and modeling of LNA, PA and mixer based on either CNT or graphene
- Design and modeling of CNT switch
- Design and modeling of CNT filter/oscillator and graphene mixer
- Design and modeling of CNT antenna
- Design and modeling of LNA based graphene
- Design and modeling of a graphene loaded antenna.

3.1.2 PROGRESS TOWARD OBJECTIVES : STATUS OF ACTIVES TASKS

3.1.2.1 Task 2.5 : Design and simulation of RF graphene devices (UNIVPM/FORTH/IMT)

IMT has finalized the design of a graphene antenna which is vertically DC polarized for an electrostatic doping of the graphene antenna to reduce the sheet resistance.as it is presented in Figure 2

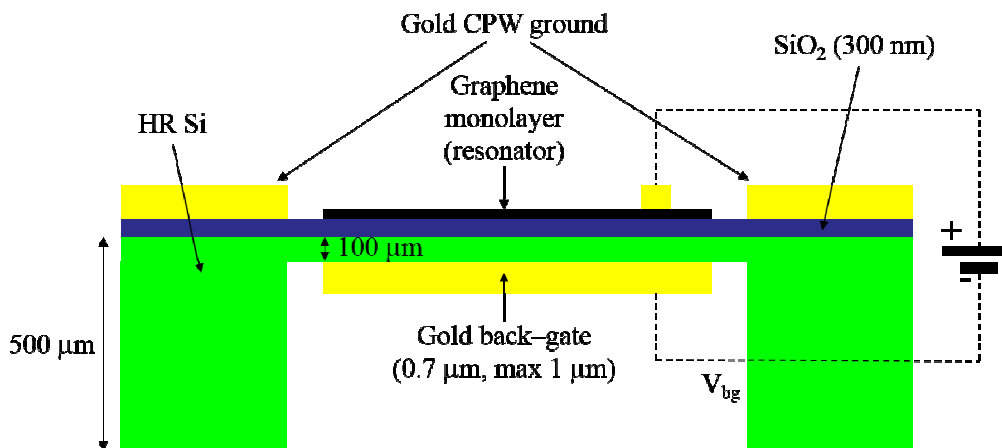


Figure 2 : designe of graphene antenna

The simulated electromagnetic properties are presented below in Figure 3 @10 GHz for a surface resistance of 100 Ω :

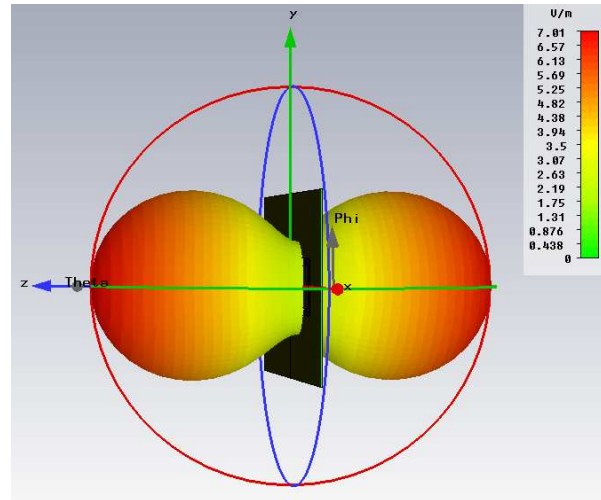
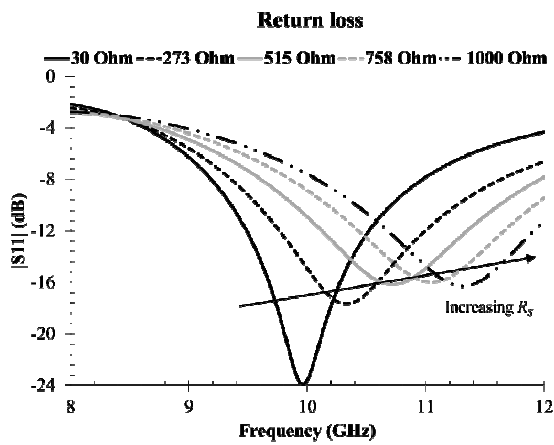


Figure 3 : simulated electromagnetic properties

The antenna is now in fabrication process.

Design of passive RF components

In order to complete the circuits corresponding to the modules of Nano-RF a series of passive components need to be used to realise the matching circuits. To obtain a detailed measurement set of passive components, a series of passive devices were designed.

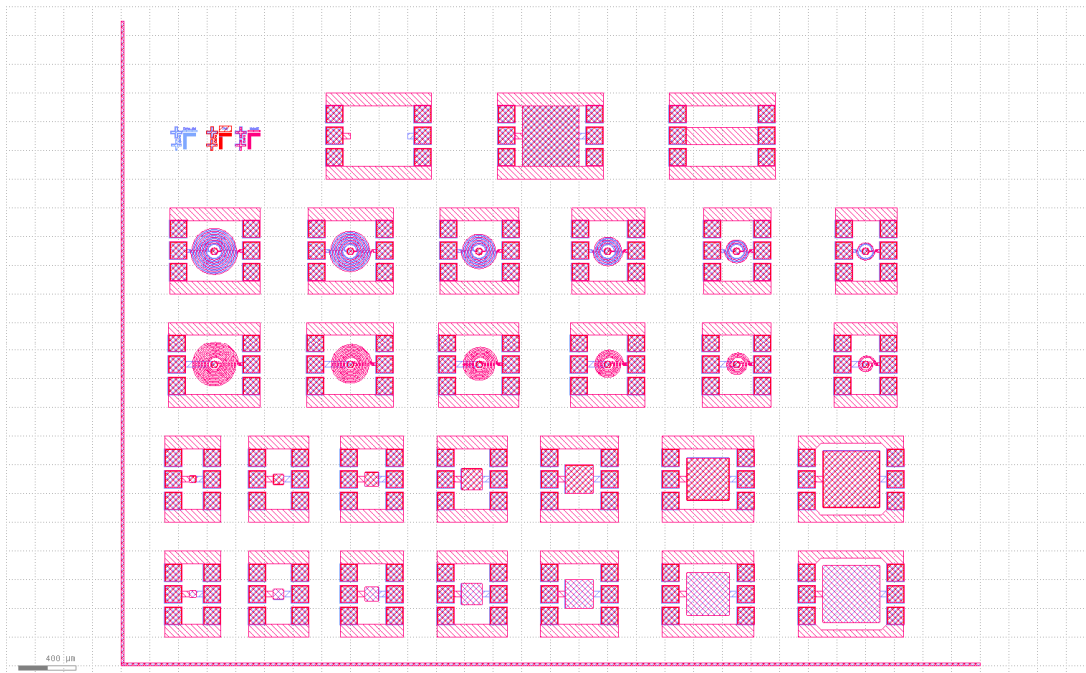


Figure 4: Schematic of the designed period of passive components mask

Figure 1 shows a complete period of the passive components. It contains the following categories of components organised in rows:

Simple inductors, 1 to 6 turns (Low values)

Stacked Inductors 1 to 6 turns on each metallization (High values)

1 μm thick Polyimide capacitors 50x50 to 400x400 μm (Low value)

100nm thick Si_3N_4 capacitors 50x50 to 400x400 μm (High values)

The period also contains a set of de-embedding devices to complete the RF-measurements and data analysis by removing the pads effect. The de-embedding devices are situated in the top row next to the alignment marks and are a) Open b) Short and c) Through.

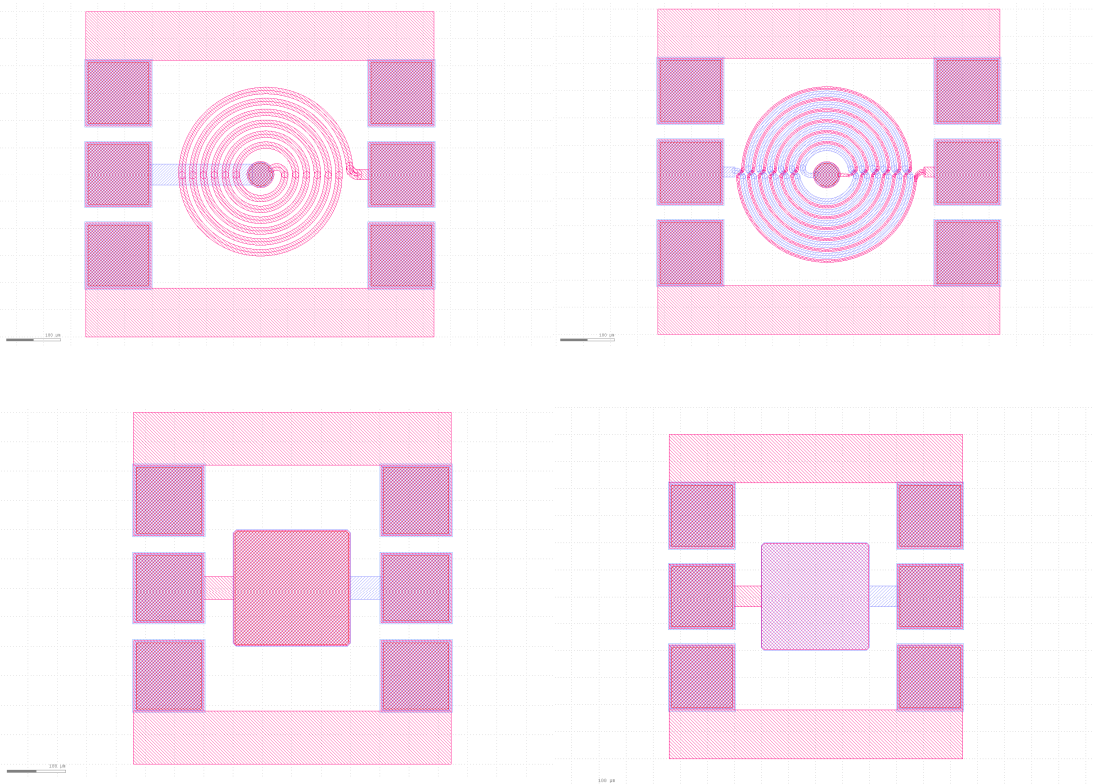



Figure 5: Schematic images of the Inductors (top row) showing the simple (left) inductor and the stacked (right) inductor. The bottom row shows the two types of capacitors Si_3N_4 on the left and polyimide on the right

4 PROGRESS IN THE ACTIVE THECNICAL WORKPACKAGE 3

4.1 WP3 : FABRICATION ACTIVITIES

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
FORTH	TRT, CHALMERS, FORTH, LAAS,	$T_0 + 3 - T_0 + 42$	D3.1 to D3.8 M3.1	T3.1 to T3.10	On Going

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	UPMC, IMT, GI, SHT, LiU, ICN, Tyndall				
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4.2 WP OBJECTIVES

In this work package we will fabricate all the CNT and graphene based sub-modules that have been designed in the previous work package. The principal objective of this work package is to fabricate the test structures and also final components based on the results of WP2. The manufacturing process in this WP will be optimised and the products will be delivered to WP4. The technical objectives for this work package are:

- To develop CNT growth technology to achieve the desired structure following results of the design activities. CNT growth must be compatible with all the substrate technology to achieve the desired RF components as specified in Work-package 1.
- To develop graphene growth techniques either based on exfoliation for proof of concept RF graphene devices and at the wafer scale for graphene circuits to be used in the sub-modules
- To set-up a pilot line for manufacturing CNT for microwave applications.
- To fully characterize the CNT that have been grown by thermal CVD or plasma enhanced CVD . The characterization of graphene via exfoliation or epitaxial growth on SiC. The goal will be to verify that physical, structural, etc. properties will be compatible with the RF functions we want to achieve.
- To fabricate the RF submodules designed in the previous work package: CNT FET (LNA, PA and mixer), the RF switch, the RF filter/oscillator and the antenna, LNA based on graphene, graphene antenna , graphene mixer and graphene detector
- To develop various technologies that will allow for the integration of the sub-modules produced within this work package to be integrated on a single Si carrier wafer.
- To supply other work packages with CNT and graphene for characterization, modeling, simulation and demonstration and to optimize CNT and graphene according to their feedbacks.

4.2.1 PROGRESS TOWARD OBJECTIVES : STATUS OF ACTIVES TASKS

4.2.1.1 Task.3.1 CNT and graphene growth technology

➤ Graphene growth

There are several ways to obtain graphene material and we started to study the different graphene synthesis methods.

▪ SiC decomposition (LiU)

Based on work aims of LiU in Nano RF project, we have explored the role of buffer layer and growth parameters for having a full control on the epitaxial graphene growth process on SiC to obtain cm scale continuous coverage of monolayer graphene (MLG). During the graphene growth process on the Si-face of SiC the first grown carbon layer, is covalently bonded to the SiC substrate. This so-called buffer layer lacks the π bands of graphene and only the second carbon layer (known as

monolayer graphene (ML)) shows the properties of graphene. The buffer layer is a precursor for graphene formation and can strongly influence its quality; depending on the buffer layer integrity the graphene may contain defects which may work as scattering centers for carriers and decrease their mobility.

Graphene samples were grown on the Si face of different SiC polytypes in an inductively heated furnace at a temperature ranging from 1700 - 1950°C and at argon ambient with a pressure range from 750 - 950 mbar at different growth times. Graphene surface morphology, thickness, structure and electronic properties have been assessed by using AFM, LEEM, Reflection map, Raman spectroscopy, and EFM respectively.

To improve the uniformity of the growth process and access to large scale growth up to 4 inch (Figure 6), besides the existing growth cell we have made graphene growth in the recently constructed growth set-up which has some beneficial characteristics. The new system is fully automatic and just need a growth recipe to start and end up the growth process without any operator. It has also longer RF-coil with uniform distance between the pipes and also the possibility to move coil up and down to change the temperature gradient for both etching the SiC substrates and epitaxial graphene growth.



Figure 6 : Newly operated 4 inch growth system.

AFM height and phase images show that formation of the buffer layer (growth temperature 1850 °C and argon pressure 950 mbar) can start at any place on the substrate, but preferable place is the kink of the steps as shown in Figure 7a. The C atoms coalesce and nucleate into graphene islands on the kink part of a step (marked by circle) and these islands act as a sink for other C atoms. As the edge of steps act as a C source, the growth rate is higher along the step edge and for this reason a buffer layer first covers like a ribbon the edge of steps (Figure 7b). Then growth continues from the edge of a step to in forward direction. Our study shows that buffer layer first covers the steps with larger terrace (Figure 7c).

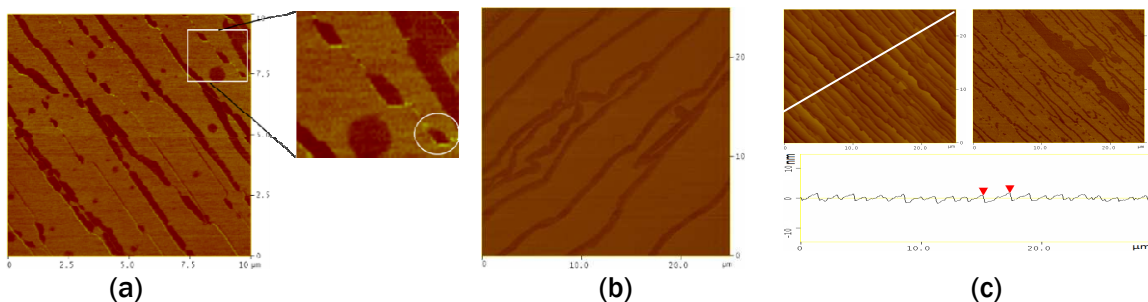


Figure 7 : - AFM images of a) Initial stage of buffer layer formation, b) Ribbon like growth of buffer layer, c) Full coverage of large terraces.

We have shown that reflectance mapping can be used for rigorous determination of the number of layers in G/SiC. [I.G. Ivanov et al., Carbon, 77, 492, (2014)]. The reflection map (Figure 8a) in this study shows full coverage of a buffer layer before starting the ML graphene growth. The good quality of buffer layer was confirmed by LEEM (Figure 8b) and LEED (Figure 8c) pattern, the pattern is similar all over the surface.

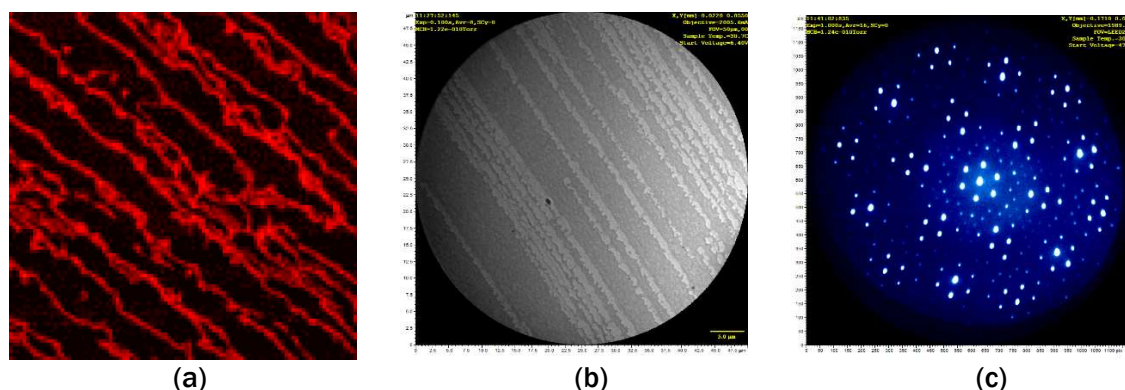


Figure 8 - a) Reflection map (30μm×30μm) of buffer layer (black) and ML (red) graphene, b) LEEM images, and c) LEED pattern of buffer layer.

We have also found that the Raman spectra of bare BL differ substantially from the spectra of BL with one layer graphene (Figure 9a, b with subtraction of the spectrum of the SiC substrate). While the former resemble the well-known spectra of amorphous carbon (a-C) films (however, with pronounced structure in the 2D band in contrast to a-C, Figure 9a), the latter exhibit well-pronounced structure visible around the D and G bands (Fig. 4b). In particular, the Raman spectra of BL under one graphene layer (1LG) show a distinct peak at ~1235 cm⁻¹ previously associated with sp³-bonding [E. Rzepka et al., Diam. Relat. Mater., 8, 481, (1999)], which most likely results from the fact that 1/3 of the C-atoms in the BL are bound to the substrate. The BL spectrum observed in some spots of hydrogenated graphene (not shown) also has its particular appearance, which suggests that the structures of the three types of BL mentioned above are all different.

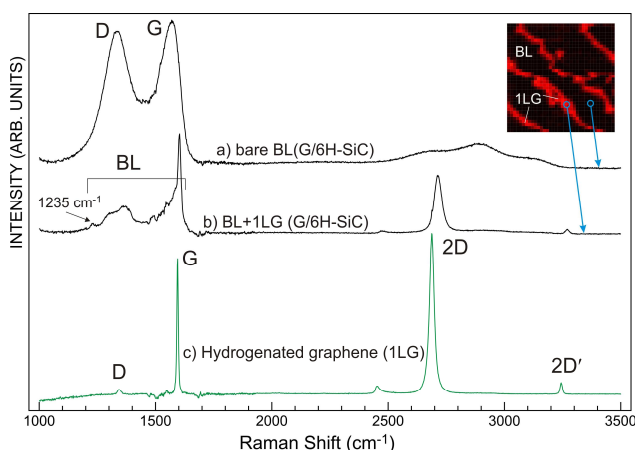



Figure 9 : - Typical Raman spectra of (a) bare BL, (b) BL with 1LG, and (c) H-intercalated graphene. The insert shows the accompanying reflectance map with the points from which the spectra in (a) and (b) are taken. The vertical scale is the same for all spectra.

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- Graphite ex-foliation (GI)

Based on requirements from consortium partners, particularly Tyndall, we have concentrated on producing graphene flakes on oxidised silicon wafers (thermally grown oxide) for this period. In total, >15 mono-crystalline graphene flakes have been prepared across 3 samples (T+30M → T+36M). The table below contains more information about the samples.

Sample Ref #	Substrate material	Flakes	Delivered to
S8170	High resistivity Si with 300 nm of SiO ₂ (dry thermal growth)	4 monolayers, 3 mixed (mono-, bi-, tri)	Mircea Modreanu, TYNDALL
S8171	High resistivity Si with 300 nm SiO ₂ (dry thermal growth)	2 monolayers 2 mixed (mono-, bi-, tri)	Mircea Modreanu, TYNDALL
S8172	High resistivity Si with 300 nm of SiO ₂ (dry thermal growth)	3 monolayers 2 mixed (mono-, bi-)	Mircea Modreanu, TYNDALL

Datasheets for the samples can be found at: <http://grapheneindustries.com/datasheets/NanoRF>

Each sample contains homogeneous regions >20µm wide that are suitable for a range of characterisation techniques and device fabrication needs.

4.2.1.2 Task.3.3 Fabrication of CNT FET

A series of runs (3 runs) have been realised for both graphene and CNT FET's. All 3 runs focused on implementing the high-k HfO₂ dielectric layers on the final devices to optimize for operating speed and achievable gain. Furthermore, the source drain distance has been downscaled to improve the operating characteristics of the devices. Those FET's are now sent to characterization to obtain their RF performance in order to facilitate the design of the circuit modules.

4.2.1.3 Task.3.7 Development of carbon nanotube interconnects (SHT/CHALMERS)

One of the important issues in Nano-RF is the RF performance of the TSV developed to interconnect the various modules and sub-modules. To properly account for that in the RF design, a set of test devices was designed and the respective mask was prepared. The test devices enable measurement and de-embedding of the TSV RF properties.

Since the required submodules are going to be implemented on Silicon (CNT modules) but some modules may be realised on lower permittivity substrates, the mask is separated in two areas. One optimised for Silicon substrate and one for polymeric substrates.

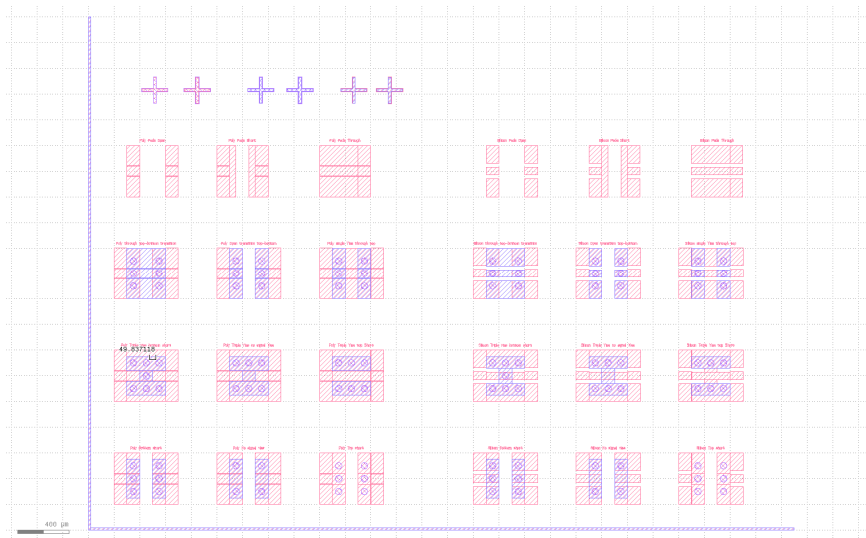


Figure 10: Schematic of the designed period of Vias performance test-bed

Figure 1 shows a complete period of the test Vias structures. It contains two areas one optimized for Silicon and one for lower permittivity substrates.

In each area there is a set of 9 devices plus three reference (short, open and through) devices as well as different number of Vias.

The performance will be compared to similar devices fabricated using copper vias fabricated following the same design.

Passive RF components

To facilitate accurate fabrication of the LNA and HPA circuits required for NANO-RF, a foundry of passive components namely inductors and capacitors need to be used. In the previous months a set of passive components have been designed. That design has been put to fabrication leading to a set of inductors and capacitors that were measured to obtain foundry data for the circuit fabrication.

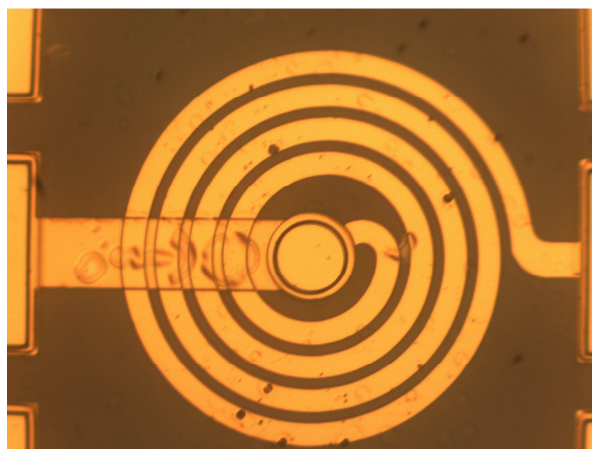



Figure 11: Optical image of a 4 turn non stacked inductor fabricated on SiC.

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The following devices have been fabricated:

- Single level inductors 1 – 6 turns
- Stacked inductors 1 – 6 turn
- Si₃N₄ capacitors (high C values) with size 50x50 to 400x400 μm²
- Polyimide capacitors (low C values) with size 50x50 to 400x400 μm²

Those components have been characterized in a VNA setup to measure their S-parameters and the component performance has been simulated by IMT to extract their behaviour.

4.2.1.4 Task.3.8 Development of RF graphene devices

Dielectrics (Tyndall, ICN, FORTH)

In particular during this period, Tyndall-UCC has continued his work towards developing a room temperature e-beam process for the growth of high-k metal oxides (HfO₂) suitable as gate oxides for graphene (GFET) and CNT FET devices that will be developed in Task 3.3 and Task 3.8.

During reporting period, Tyndall-UCC work have concentrated on the characterisation of the high-k dielectrics growth impact on the CVD single layer graphene corresponding to growth batches NANO RF 36 and NANO RF 37(see Table 1 for details)

Table 1. Summary of Tyndall-UCC high-k dielectrics growth activity during the reporting period ((i.e.T0+30-T0+36)

Sample reference	Material	Substrate	Bottom electrodes	Thickness(nm)	Growth process	Deposition temperature
NANO RF-36	HfO ₂ /HfO ₂	CVD Graphene/SiO ₂ /Si	No	1.5 /4	E-beam/ALD	23 °C/250 °C
NANO RF-37	HfO ₂ /HfO ₂	CVD Graphene/SiO ₂ /Si	No	2.5 /4	E-beam/ALD	23 °C/250 °C

In order to assess the overall impact growth of high-k dielectrics growth on the CVD single layer graphene Tyndall-UCC propose a new approach that involves the use of ultra-high resolution Micro Raman mapping down to 200nm.

The two samples from batches NANO RF 36 and NANO RF 37 have been analysed by the Micro Raman mapping, several areas of 50μmx50μm have been analysed with a step of 200nm. The main results are presented below in Figure 12 to 17.

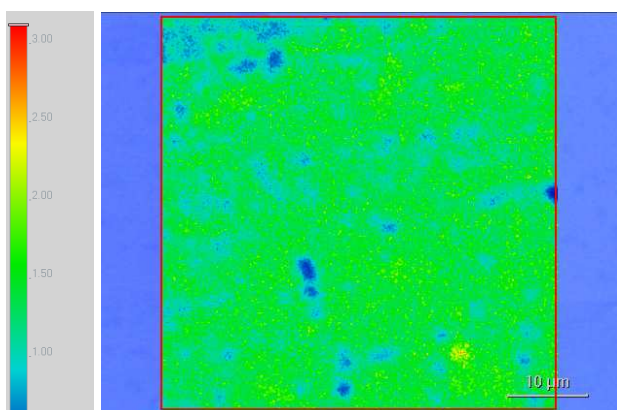


Figure 12 : Peak Height Ratio I_{2D}/I_G :NANO RF 36, CVD SLG Graphene, 1.5nm HfO₂ E-beam/4nm HfO₂ ALD; 50µmx50µm scanned area, 200nm step; 60000 scans

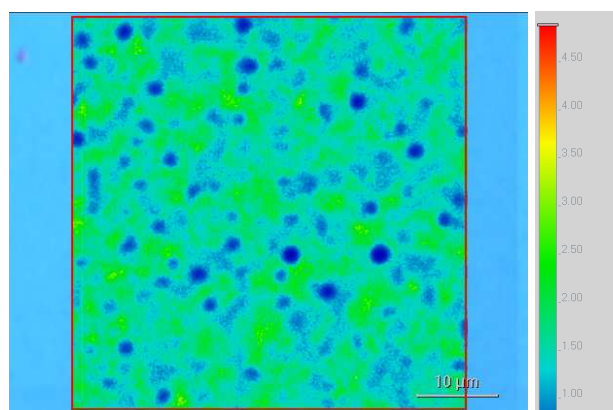


Figure 13 : Peak Height Ratio I_{2D}/I_G :NANO RF 37, CVD SLG Graphene, 2.5nm HfO₂ E-beam/4nm HfO₂ ALD; 50µmx50µm scanned area, 200nm step, 60000 scans

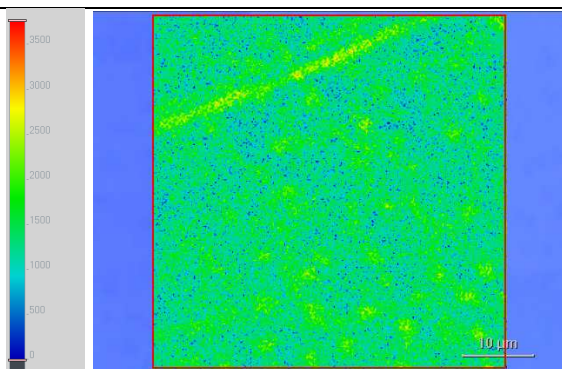


Figure 14 : Defect Peak Area (A_D):NANO RF 36, CVD SLG Graphene, 1.5nm HfO₂ E-beam/4nm HfO₂ ALD; 50µmx50µm scanned area, 200nm step, 60000 scans

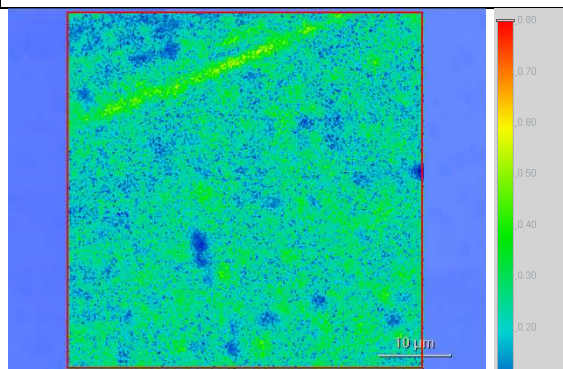


Figure 15 : Peak Area Ratio A_D/A_G :NANO RF 36, CVD SLG Graphene, 1.5nm HfO₂ E-beam/4nm HfO₂ ALD; 50µmx50µm scanned area, 200nm step, 60000 scans

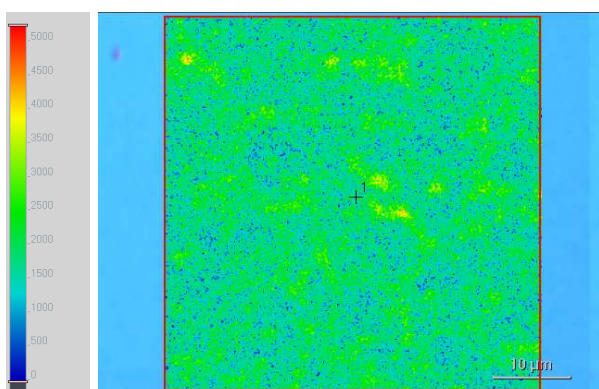


Figure 16 : Defect Peak Area (A_D):NANO RF 36, CVD SLG Graphene, 2.5nm HfO₂ E-beam/4nm HfO₂ ALD; 50µmx50µm scanned area, 200nm step, 60000 scans

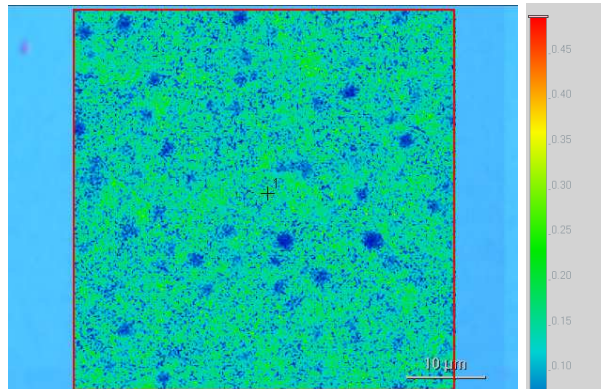



Figure 17 : Peak Area Ratio A_D/A_G :NANO RF 36, CVD SLG Graphene, 2.5nm HfO₂ E-beam/4nm HfO₂ ALD; 50µmx50µm scanned area, 200nm step, 60000 scans

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In Figure 12 and Figure 13 are showed the correlation maps for the I2D/IG graphene phonon modes (peak height ratio) for samples NANO RF 36 and NANO RF 37. The ratio I2D/IG is indicative for the quality of the SLG and a lower ratio is indicative for a decrease in the graphene carrier mobility. We can see that a lower HfO2 E-beam buffer leads to retaining good quality graphene while increasing HfO2 E-beam buffer leads to a worsening of graphene quality mainly around the grain boundaries of the CVD graphene.

In Figure 14 and Figure 15 are presented the correlation maps for sample NANO RF 36; in Figure 13 is shown the correlation map for AD (Peak Area for the D phonon mode) and in Figure 4 is shown the correlation map for the ratio AD/ AG (Peak Area Ratio for the D and G phonon modes). These results outline the presence of defects that are located mainly at the grain boundaries of the CVD graphene.

In Figure 16 and Figure 17 are presented the correlation maps for sample NANO RF 37; in Figure 16 is shown the correlation map for AD (Peak Area for the D phonon mode) and in Figure 6 is shown the correlation map for the ratio AD/ AG (Peak Area Ratio for the D and G phonon modes). As for sample NANO RF 36, these results outline the presence of defects that are located mainly at the grain boundaries of the CVD graphene.

As a main conclusion it can be outline that a lower HfO2 E-beam buffer preserves the electronic quality of CVD single layer graphene while increasing the thickness of the HfO2 E-beam buffer may lead to a slight decrease of the electronic quality of CVD single layer graphene. The new methodology propose by Tyndall-UCC allows a meaningful qualification of high-k dielectrics/SL graphene stack for the GFET devices.

5 PROGRESS IN THE ACTIVE THECNICAL WORKPACKAGE 4

5.1 WP4 : TEST ACTIVITIES

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
LAAS	TRT, CHALMERS, FORTH, LAAS, UPMC,IMT, GI, SHT,UNIVPM, LIU,TYNDALL	T ₀ +15 – T ₀ +44	D4.1 to D4.7 MS4	T4.1 to T4.6	On Going

5.2 WP OBJECTIVES

This work package is dedicated to the electrical characterization (DC to RF) of all the devices fabricated in WP3. The results obtained will be compared with the results obtained through simulations in WP2 and basic equivalent circuit models will be calibrated following parameter extraction from static (DC) to high-frequency (HF) measurements. A strong interaction is planned with WPs 2 and 3, in order to take into account all the fabrication available parameters as well to feedback into fabrication and application design the needed optimization

5.3 PROGRESS TOWARD OBJECTIVES : STATUS OF ACTIVES TASKS

5.3.1 Task.4.3 CNT based filter/oscillator tests

The second fabrication of CNT filter was measured and the results is presented in Figure 18

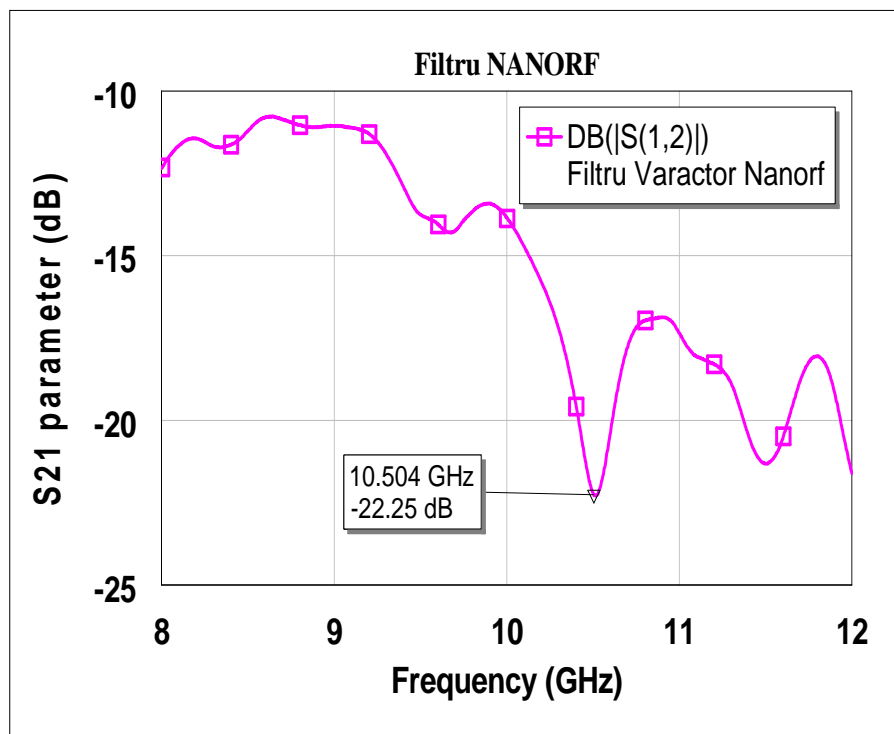
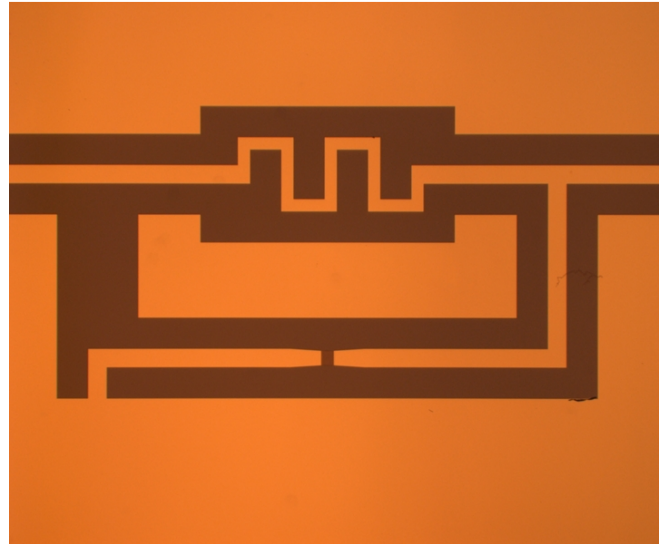
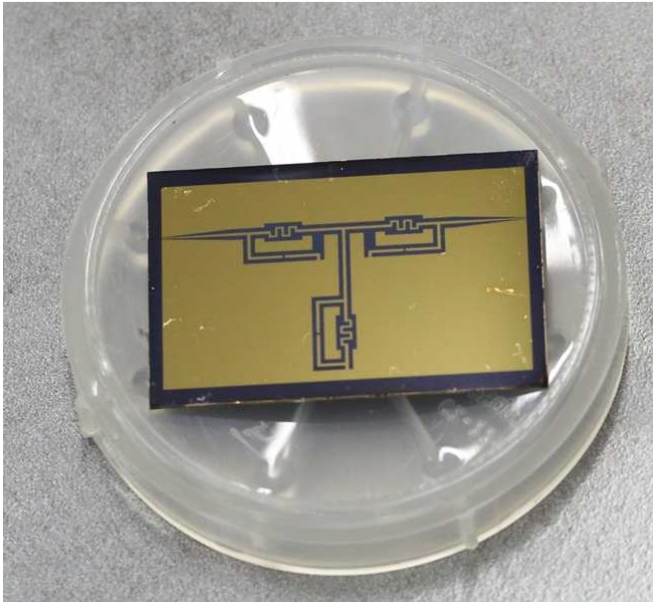


Figure 18 : RF Measurement of CNT filter

The measurement validates the design and the technological process. The filter two terminals fits with probe tips of 150 microns pitch and we were able to measure the filter. The molybdenum deposition is compatible with the filter.

Measurements shows filter resonance at 10 GHz which is compatible with the specification and losses due to Mo

The CNT are shorter than required, they are missing in many points. You cannot actuate them. For the next run a special attention to CNT growth is necessary.

5.3.1 Task.4.1 CNT and Graphene FET test

To test and optimize the HfO₂ stack deposited on the FET transistors, two fabrication runs were realised. One is a metal insulator metal structure (MIM) using Pt electrodes and the entire stack (both e-gun and ALD deposited HfO₂) and the second one was a Graphene insulator metal structure (GIM) resembling the actual gate structure.

For the initial MIM structures, a series of varying high-k thickness HfO₂ layer with thickness of 5, 10 and 15nm has been realised on a Pt continuous layer covered with a thin (1.5-2nm) layer of HfO₂ used for ALD nucleation. The structure was completed by a top Pt electrode. The leakage current as a function of Voltage between the top and bottom electrode has been measured and is depicted in the following plots.

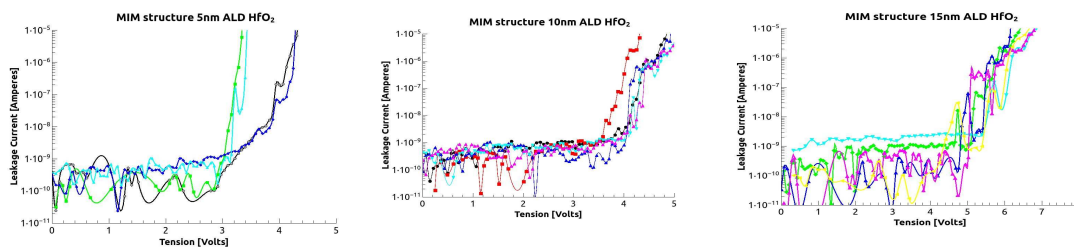


Figure 19: I-V characteristics of test MIM structures, notice the increasing breakdown voltage as the thickness of HfO₂ is increased from 5 to 15nm

To verify the validity of the results, a second run using graphene as the bottom electrode was realised. The top electrode was Pt and the system leakage is depicted in the following figure.

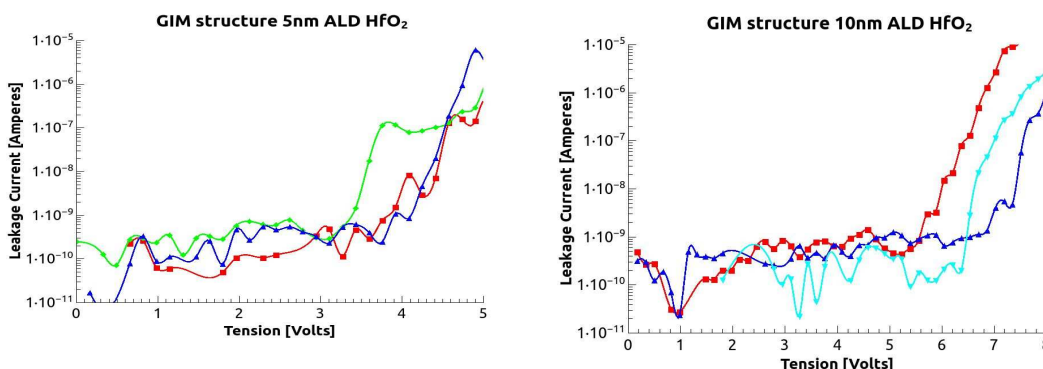



Figure 20: I-V characteristics of test GIM structures. The breakdown is larger compared to the MIM case shown in Figure 18

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The results show good dielectric performance with a HfO₂ thickness of only 7-12nm (including the e-gun deposited nucleation layer) which is expected to lead to better transconductance.

Development of technique for the measurement of thermal properties:

ICN has focused in this period on the development of two novel techniques for the measurement of thermal properties of the modules and the demonstrators, both in passive mode as well as under operation conditions. These are scanning thermal microscopy (SThM) and frequency domain thermoreflectance (FDTR). The combination of these two techniques provides several advantages for the envisioned thermal measurements of the modules in the project. SThM can achieve unprecedented spatial resolution for the mapping of thermal properties down to 30 nm, whereas FDTR gives direct access to the quantity of the thermal diffusivity. Another advantage of the later technique is the contactless fashion of the measurements.

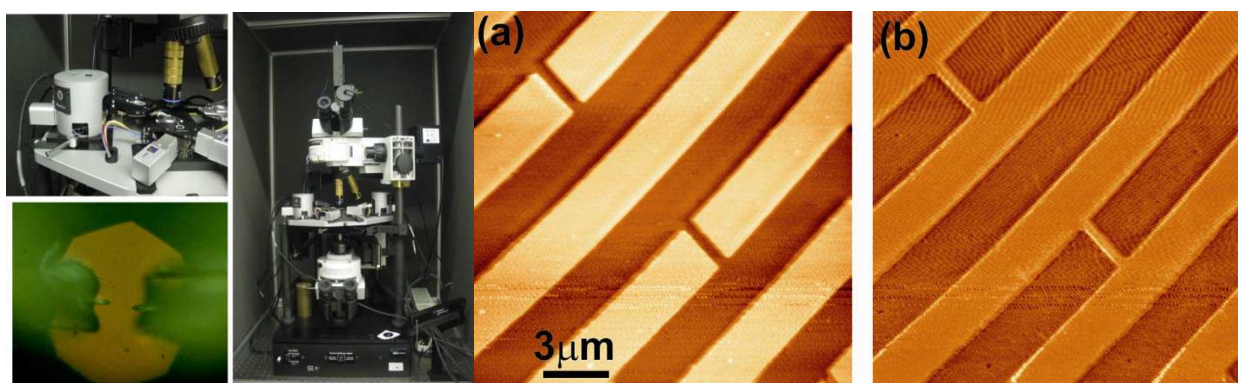


Figure 21: left: SThM setup, middle: AFM image, right: corresponding thermal image.

Figure 21 shows detailed pictures of the scanning thermal microscope and test measurements on a calibration sample in AFM mode and the corresponding thermal image. In the following period of the project, this technique shall be used to map the temperature distribution in CNT and graphene based modules and to identify local hotspots and high temperature gradients for device optimization. In addition, the design, construction and programming of the FDTR setup is well advanced and first measurements of the thermal diffusivity with this technique are expected in the coming months.

6 DISSEMINATION AND EXPLOITATION ACTIVITIES (WP6)

WP leader	Involved Partners	Duration	Deliverables Milestones	Active Tasks	Status
TRT	TRT, ICN	T ₀ +0 – T ₀ +36	D6.1 to D6.6	-	On Going

6.1 PUBLICATIONS & CONFERENCE

➤ Publications

- M. Dragoman, A. Cismaru, M. Aldrigo, A. Radoi, and D. Dragoman, Switching microwaves via semiconductor-isolator reversible transition in a thin-film of MoS₂, JOURNAL OF APPLIED PHYSICS 118, 045710 (2015).

- M.Dragoman, Carbon-based nanodevices routes: inks, flakes, spaghetti, wafers-invited papers 8th International Conference on Advanced Materials, ROCAM 2015.
- M.Dragoman, Receiving microwave signals with graphene-invited paper , WOCSDICE ,Smolenice, 2015.
- Conference
 - M.Dragoman, Carbon-based nanodevices routes: inks, flakes, spaghetti, wafers-invited papers
 - 8th International Conference on Advanced Materials, ROCAM 2015.
 - M.Dragoman, Receiving microwave signals with graphene-invited paper , WOCSDICE ,Smolenice, 2015.