

SEA4KET PROJECT – BULLETIN

SP3 - SWCC450 Single Wafer Critical Cleaning 450

AT A GLANCE

Assessment of a new 300mm integrated cleaning system with low O₂ processing capability.

Minimized substrate loss to meet wafer processing requirements.

SEA4KET SP3 – PARTNERS

Lam Research
 Fraunhofer IISB
 Intel

Advances proposed in SP3

- Spin Clean Systems are being used for high volume production in FEOL, MOL and BEOL for 1x nm technology on 300mm wafers
- New technology nodes of 10nm and smaller require improved control of process parameters for critical cleans.
- Lam developed an integrated system concept with Plasma Etch and Wet-Spin Clean process modules combined in one system. This unique combination allows transfer between etch and clean process chambers without exposure to the clean room and/or FOUP ambient. The wet etch and clean module with ECC (Environment Controlled Chamber) technology enables processing of corrosion sensitive materials as all process steps take place in an inert N₂ environment.



Lam Spin Clean System

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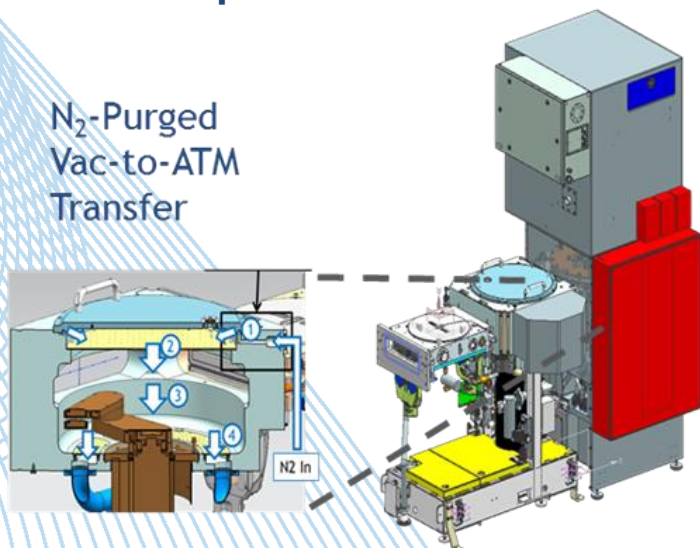
SP3 - SWCC450

Single Wafer Critical Cleaning 450

Project Results

- **Advantages of low O₂ processing to minimize CD loss demonstrated for several FEOL applications**
- **New Point-Of-Use chemical mixing provides flexible control of process parameters directly at the point of use on the wafer**
- **Particles, metal contamination and uniformity within specification**
- **Stable and reliable handling between process modules in the cluster platform**

N₂-Purged
 Vac-to-ATM
 Transfer



SEA4KET PROJECT MANAGEMENT

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Integrated Etch-Clean system installed at imec

SEA4KET PROJECT – BULLETIN

SP4: Advanced Batch Processing

AT A GLANCE

Assessment of 450mm Batch Oxidation System for future 450mm production requirements

Optimization of equipment and process parameters to meet wafer processing requirements

Advances proposed in SP4

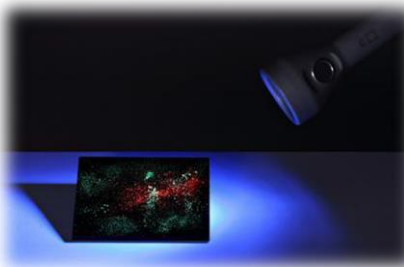
- Prove general ability of 450mm Batch Oxidation System for future 450mm production requirements in G450C pilot line, with respect to process capability, repeatability, cleanliness, equipment reliability, physical tool performance and system internal contamination
- Specific improvements are expected in the areas of reduction of logistics overhead time, contamination performance, efficient mini-environment purging, and isolation and uniform heat distribution of heating element and flange area.
- After validation several of the expected improvements can be considered for 300mm batch equipment

SEA4KET SP4 – PARTNERS



TNO innovation for life

Fraunhofer
IISB

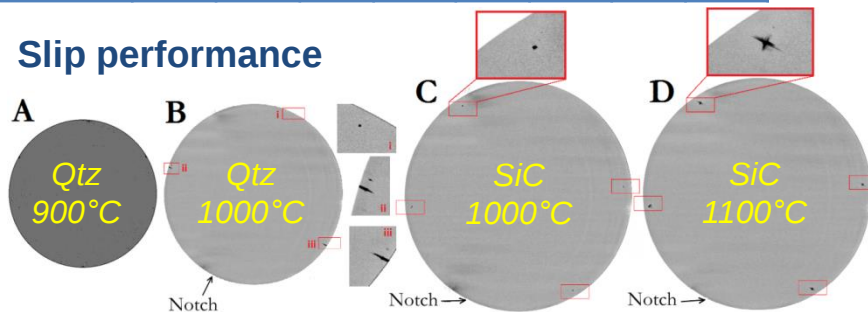


SEA4KET PROJECT – BULLETIN

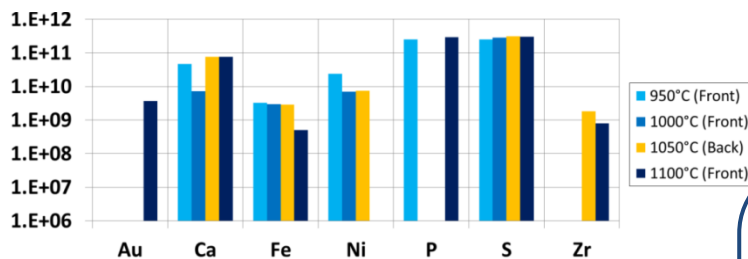
Final process results

Quantity	<d>		WiW		WtW		RtR	
Unit	nm		3σ %		3σ %		3σ %	
Process	Dry	Wet	Dry	Wet	Dry	Wet	Dry	Wet
Bottom			3.3	2.1				
Center	10.3	44.8	1.8	0.6	1.4	0.6	0.7	1.0
Top			0.4	0.4				

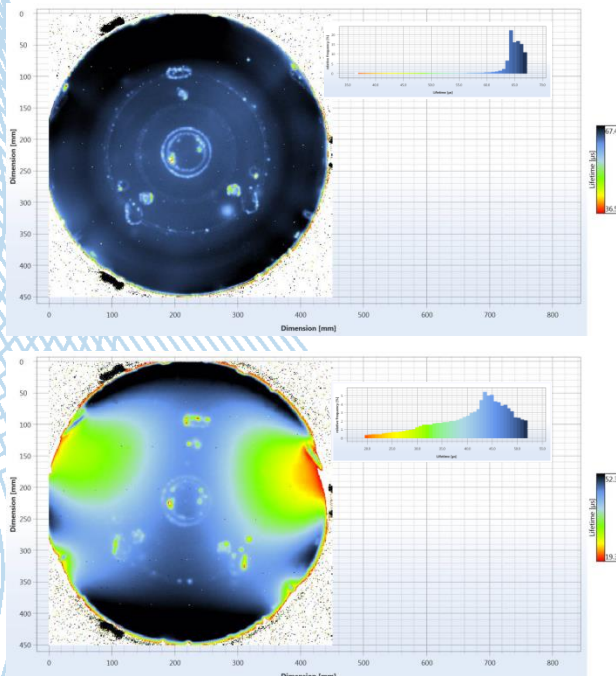
Slip performance



Metal contamination performance



SP04/08 collaboration: carrier lifetime



SEA4KET PROJECT

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SUBPROJECT SP4 - CONTACT

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Conclusions batch furnace

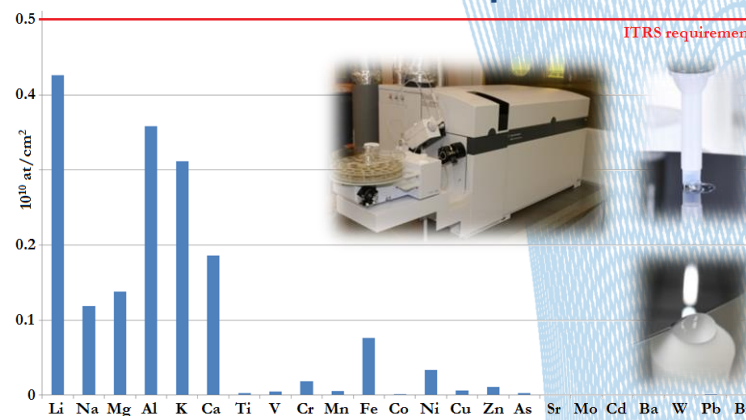
All specifications met but **three**:

- Wet-ox particles (→ improve wafer quality)
- Ca/S level (→ Ca: “human”; S: investigate)
- MTTR: Many “developmental” interventions

Conclusions contamination measurements

- Organic & Inorganic equipment available
- 450 mm ready
- Outperforms ITRS requirements

VPD-ICPMS 450 mm tool performance



SEA4KET PROJECT – BULLETIN

SP5 – CWH

Critical Wafer Handling

AT A GLANCE

Assessment of different end-effectors for handling of ultra-thin and 450 mm wafers

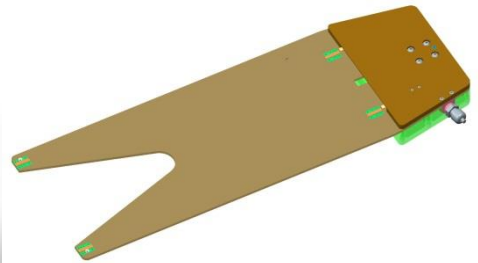
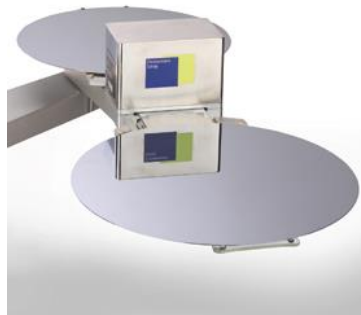
Contamination examination (particles, metallic and organic compounds) on the handled wafers

SEA4KET SP5 – PARTNERS

Fraunhofer IISB
 ZS – Handling
 Mechatronic
 HAP (Fabmatics)
 Freiberg Instruments

Advances proposed in SP5

- Clean and safe handling of ultra thin 300 mm wafers and 450 mm wafers
- Enabling contact free handling for 450 mm wafers and thinned wafer substrates with smaller wafer diameters
- Adapting end-effectors on a 450 mm cluster platform
- Comparison between the four different end-effectors relating to particle generation, organic and metallic contamination
- Testing end-effectors with regard to industrial applicability



SEA4KET PROJECT – BULLETIN

SP5 – CWH

Critical Wafer Handling

Project Results

Different handling technologies were compared regarding:

- Particle contamination
- Organic contamination
- Metallic contamination
- Longtime tests

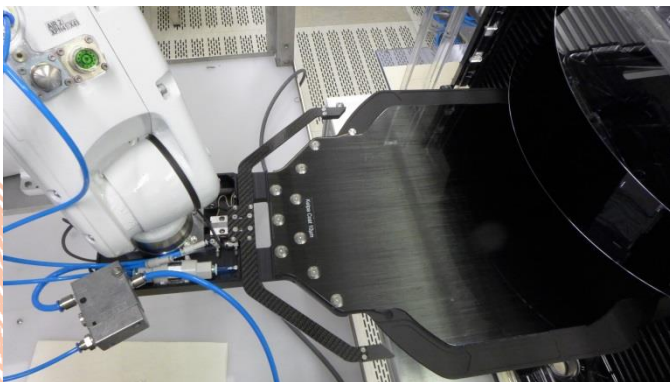
Established systems for measuring organic and metallic contamination on 450 mm wafers

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Freiberg Instruments
Inline Metrology



FABMATICS
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ZS-Handling

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Fraunhofer
IISB

SEA4KET PROJECT – BULLETIN

SP6- AMLL450
Vacuum transportation
interface for 450mm
architecture

AT A GLANCE

Assessment of vacuum carrier technology for handling of 300-450mm wafers

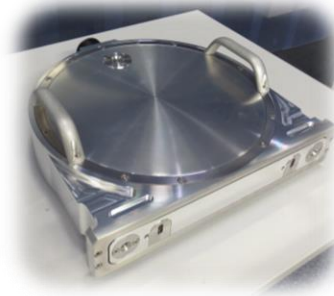
Optimization of carrier parameters to meet wafer transport and storage requirements

SEA4KET SP6 –
PARTNERS

Fraunhofer IISB
 Pfeiffer Vacuum (PV-F)
 ASM

Advances proposed in SP6

- Development & manufacturing of 450mm carrier and interface
- Attachment of the system to the 300/450mm cluster at FhG IISB
- Assessment of the tool/process in this 300/450mm cluster platform



SEA4KET PROJECT – BULLETIN

SP6- AMLL450

Vacuum transportation interface for 450mm architecture

Project Results

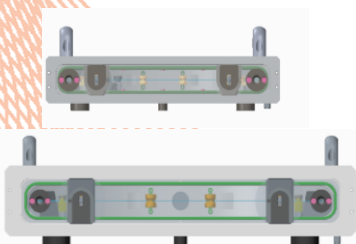
- Market need evaluation: R&D
- Assessment of 300 mm carrier cleanliness by IISB, in the 300/450mm cluster platform /
 - Development of tests methodology
 - Validation of cleaning process
- Study of 450mm carrier
- Material investigation
- Material assessment for future carrier (no added contamination)

SEA4KET PROJECT MANAGEMENT

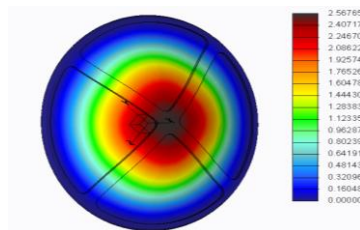
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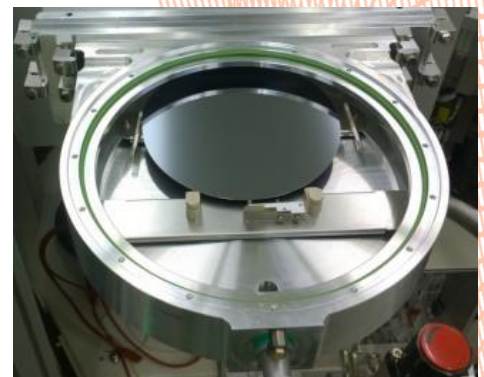
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300 carrier vs 450 mm



450 mm plate strain 2.5mm



300 mm attached to platform
for assessment

SEA4KET PROJECT – BULLETIN

SP007 – 450DM
450mm defects metrology

Advances proposed in SP07

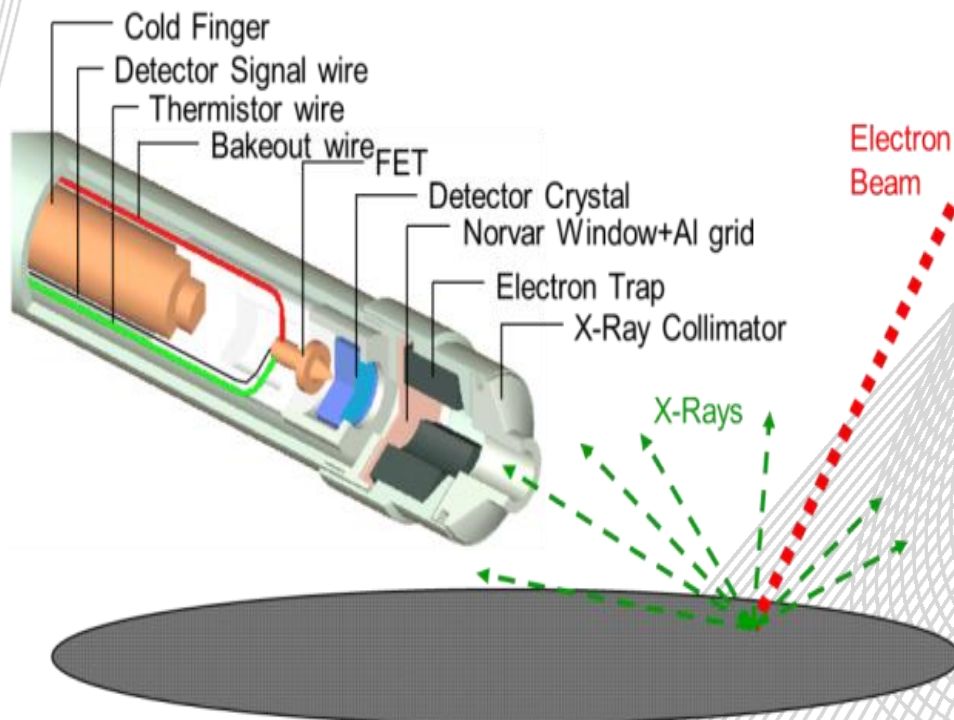
- An assessment of SDD EDX module integration with AMIL's 450mm defect review tool
- Establish a defectivity protocol and a baseline for imec's 450mm/10nm technology node pilot line

AT A GLANCE

New AMIL's SDD EDX material
 characterization capabilities
 assessment for imec's
 450mm/10nm pilot line

SEA4KET SP07 PARTNERS

AMIL
 FhG
 imec
 Intel



SEA4KET PROJECT – BULLETIN

SP07 – 450DM

450mm defects metrology

Project Results

initial status	achieved	final target	Competition	ITRS	Value
defectivity					
yes	yes	1000-2000	NAv	720	>1000
yes	yes	7	NAv	7	15
yes	yes	1	NAv	1	1
yes	yes	>95	NAv	NAv	>95
yes	yes	<5	NAv	NAv	<5
yes	yes	>1000	NAv	NAv	>1000

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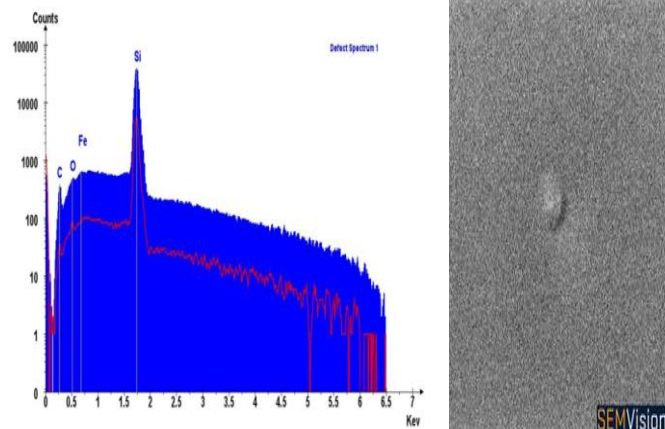
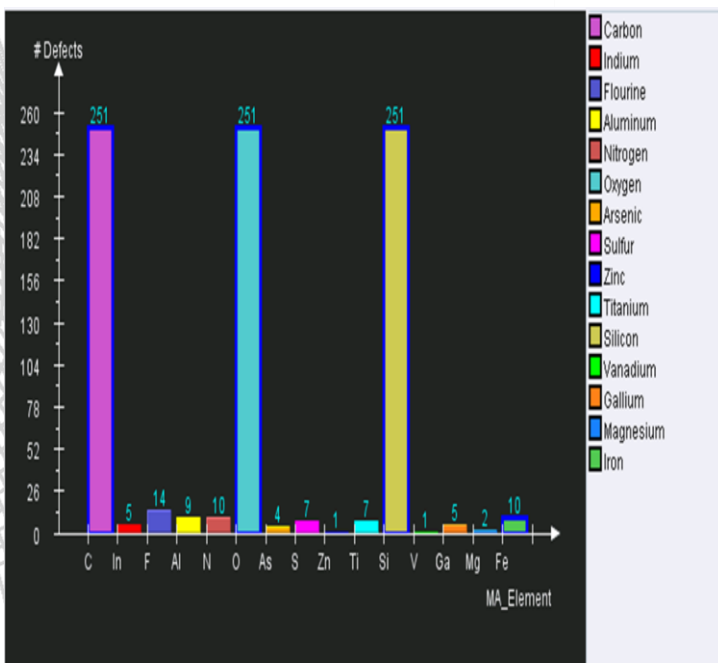
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imec



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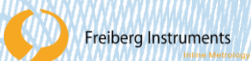
Sub-project 8 - MetroCom Metrology Components

AT A GLANCE

Availability of a flexible platform that provides an automated, industry compliant environment for metrology component evaluation

PARTNERS

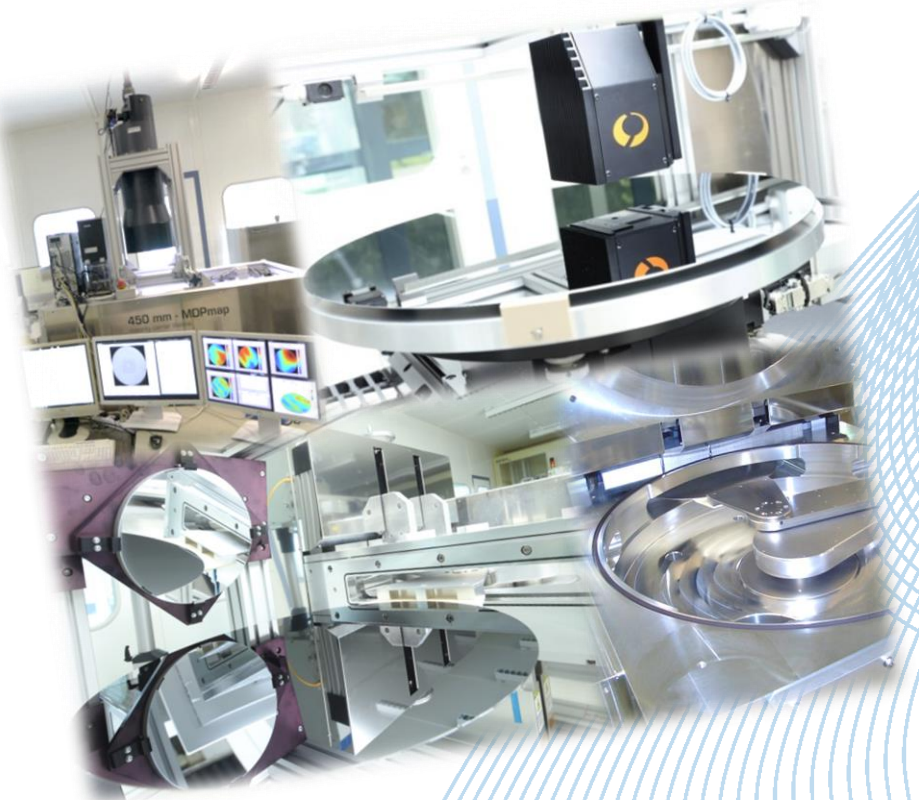
Fraunhofer IISB
Freiberg Instruments
MFA Budapest
E+H Metrology



Main achievements

- An open 300/450 mm platform is now available to support metrology companies in testing their sensors.
- A sensor for carrier lifetime measurement for silicon wafer characterization at low injection levels (high sensitivity to below 1×10^9 Fe atoms/cm³) has been developed further.
- A line-based spectroscopic ellipsometer for fast mapping of 450 mm wafers (throughput of up to 60 wafers/hr) has been devised and built.
- A topography sensor for 450 mm wafers (Makyoh-based, field-of-view ≥ 300 mm + stitching) has been implemented.

See activity-related project-bulletins for the results of individual metrology component evaluation within sub-project "MetroCom".



SEA4KET PROJECT – BULLETIN

Sub-project 8 - MetroCom Metrology Components

Benefits

- A versatile metrology module including a high-quality 3D-positioning system and a communication interface is attached to a 300/450 mm cluster handling platform.
- An automated industry compliant evaluation stand for different metrology components is built. It meets the specification and requirements for component testing of industrial partners.
- SMEs are enabled to test and subsequently transfer innovative measurement technologies to the market without prior cost and effort for automation.
- Feasibility studies for various sensors are successfully performed by using the versatile metrology module, thus demonstrating its potential and benefit for optical and electrical characterization of wafers up to 450 mm diameter.

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Figure: Open platform for metrology component evaluation that comprises a 300/450 mm transport tool and a versatile metrology module

SEA4KET PROJECT – BULLETIN

Assessment of carrier lifetime metrology within Sub-project 8 – MetroCom

AT A GLANCE

Contactless, spatially resolved and high-sensitive detection of electronic material properties of 450 mm Silicon wafers by applying carrier lifetime measurements.

PARTNERS

Freiberg Instruments GmbH,
Fraunhofer IISB

CONTACT

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Achievements

- MDP sensor development enabling contact-less carrier lifetime measurement of eg-Silicon up to 450 mm wafer diameter at low injection levels.
- Enabling contamination monitoring and thin epitaxial layer characterization through an increased MDP measurement sensitivity and resolution, which excel those of competitive measurement techniques.
- Sensor inherent possibility to switch between MDP and common μ PCD measurement conditions, thus allowing for straight comparison of respective measurement results.
- Demonstration of repeatable characterization of Si wafers up to 450 mm diameter with respect to
 - Impact of different wafer annealing conditions
 - Detrimental effects of handling tools and wafer support systems on electronic material properties
 - Metal impurity determination
 - Trap density distribution
- Sensor application not restricted to Silicon, but also adaptable to wide bandgap semiconductor (esp. SiC and GaN) characterization.

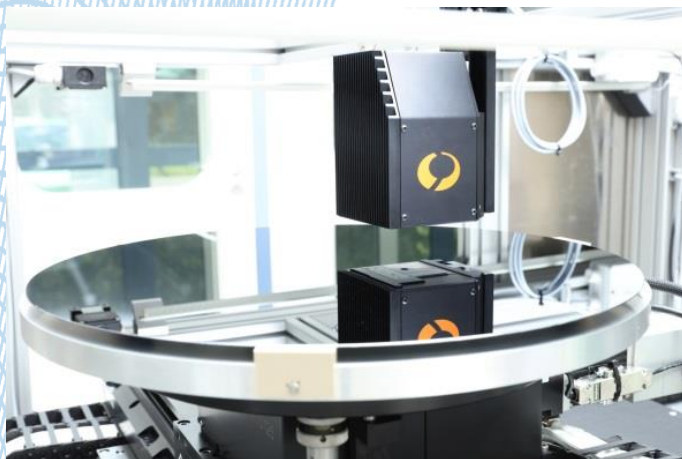


Figure 1: MDPmap sensor enabling carrier lifetime measurement of 450 mm Si wafers

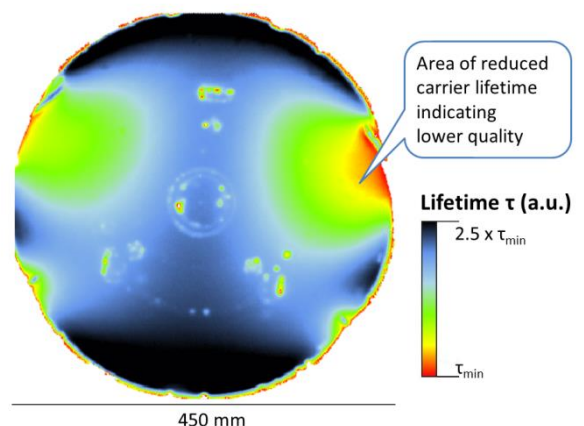


Figure 2: Carrier lifetime map of a 450 mm Si wafer obtained by MDP measurement

SEA4KET PROJECT – BULLETIN

Assessment of a high-speed optical mapping and monitoring tool within Sub-project 8 – MetroCom

AT A GLANCE

Contactless, spatially resolved, high-speed and high-sensitive detection of thin film properties on 450 mm Silicon wafers by applying expanded beam ellipsometry measurements.

PARTNERS

MFA, Fraunhofer IISB, IMEC

CONTACT

MFA - Research Centre for
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 Academy of Sciences
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 Dr. Péter Petrik
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Achievements

- MFA developed a high-speed optical mapping and monitoring tool for 450 mm wafer diameter.
- Its speed is 1800 points within 1 minute on a 450 mm wafer. Continuous measurement and evaluation is possible.
- Optical models for the measurement of lateral homogeneity of dielectric, metal and implanted layers were developed.
- Native oxide covered 450 mm Si wafer, NiSi covered 300 mm Si-wafers and Plasma Immersion Ion Implanted (PIII) 300 mm Si-wafers were successfully measured in Erlangen (IISB) in a clean-room environment
- Determine thickness with sub-nm precision.
- Determine refractive indices or composition with sub-% precision.
- Application not restricted to Silicon, but also adaptable to wide bandgap semiconductor (esp. SiC and GaN) characterization.



Figure 1: High-speed optical mapping and monitoring tool for 450 mm wafer diameter

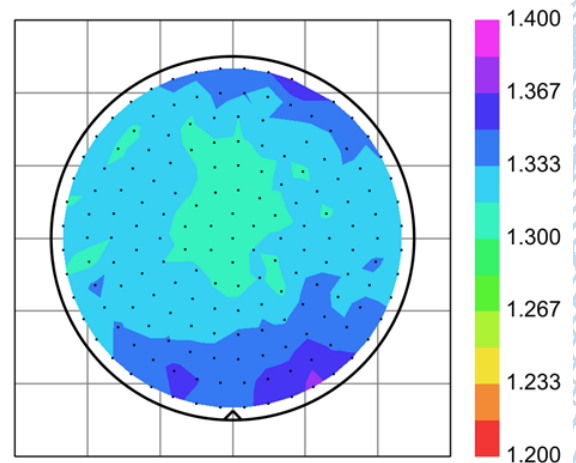


Figure 2: Native oxide thickness-map of a 450 mm Si wafer

SEA4KET PROJECT – BULLETIN

Feasibility study of topography metrology within Sub-project 8 – MetroCom

AT A GLANCE

Development of a topography sensor for 450 mm silicon wafers and proof of applicability

PARTNERS

Fraunhofer IISB,
E+H Metrology GmbH

CONTACT

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 www.iisb.fraunhofer.de

Achievements

- Successful set-up and performance test of a novel topography sensor based on surface-slope measurement
- Development of related control, evaluation and analysis software for automated and reliable topography measurements
- Quick nanotopography and global shape (bow and warp) measurements of wafers with up to 300 mm diameter possible within one shot
- Successful demonstration of topography and nanotopography measurements of 450 mm silicon wafers by applying stitching procedures that are specially adapted for this purpose
- Measurement results in good agreement with state-of-the-art equipment, but also providing additional information
- Sensor applicability not restricted to silicon wafer technology but also applicable for the investigation of various plain surfaces

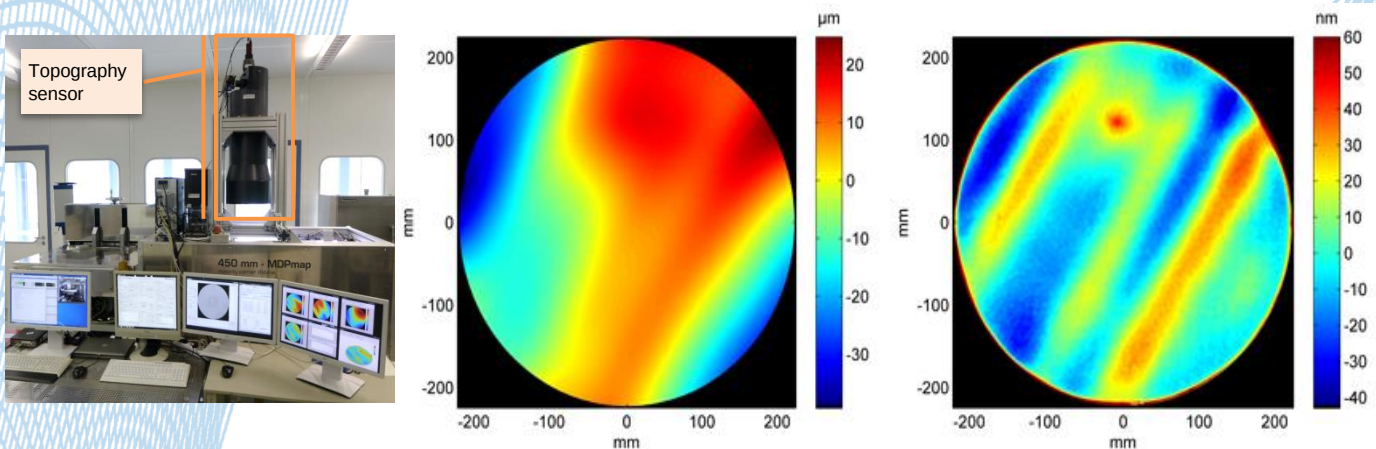


Figure: Feasibility study of the topography sensor using the metrology module provided by the sub-project: The measurement set-up (left) and the respective results of topography (center) and nanotopography measurements (right) of a 450 mm double-side polished silicon wafer

SEA4KET PROJECT – BULLETIN

SP9 – 3DIMS

AT A GLANCE

Assessment of a versatile integrated test system for 300mm wafers for 3D stacking applications:

- Probing large-array fine-pitch micro-bumps
- Automatic D2D stack testing
- Probing ultra-thinned Ø300mm wafers on tape frame

SEA4KET SP9 – PARTNERS

Cascade Microtech
 imec
 GLOBALFOUNDRIES

3D Integrated Measurement System

- Cascade Microtech CM300 full-automatic dual-configuration probe station
- National Instruments PXI test instrumentation in STS hard-docking test head
- Cascade Microtech Pyramid Probe® RBI advanced MEMS-type probe cards/cores



SEA4KET PROJECT – BULLETIN

SP9 – 3DIMS

3D Integrated Measurement System

Project Results

- Probing large-array (1,200) fine-pitch (40µm) micro-bumps: WIO1 and WIO2
- First successful attempts to probe ultra-fine-pitch (20µm) micro-bumps
- Automatic re-align and probing of matrices of pick-n-placed die-to-die stacks
- Probing of ultra-thinned (50µm) Ø300mm wafers on dicing tape on tape frames

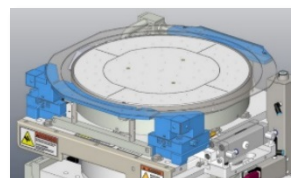
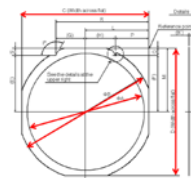
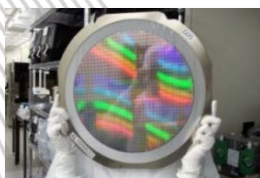
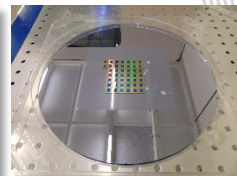
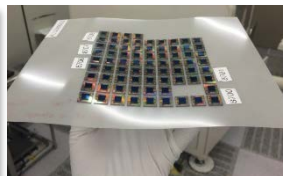
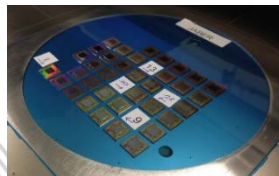
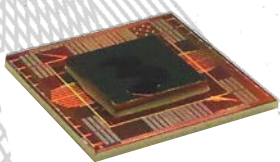
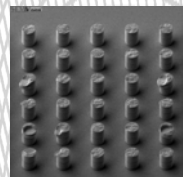
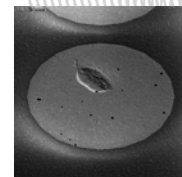
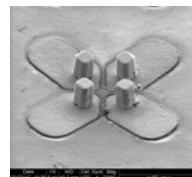
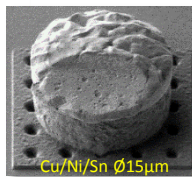
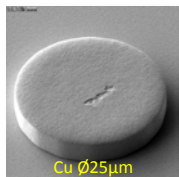
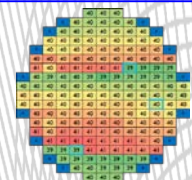
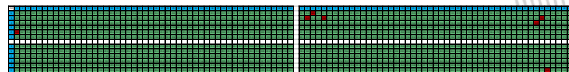
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SEA4KET PROJECT – BULLETIN

SP10 - COVBOND

Direct Covalent Bonding at Room Temperature

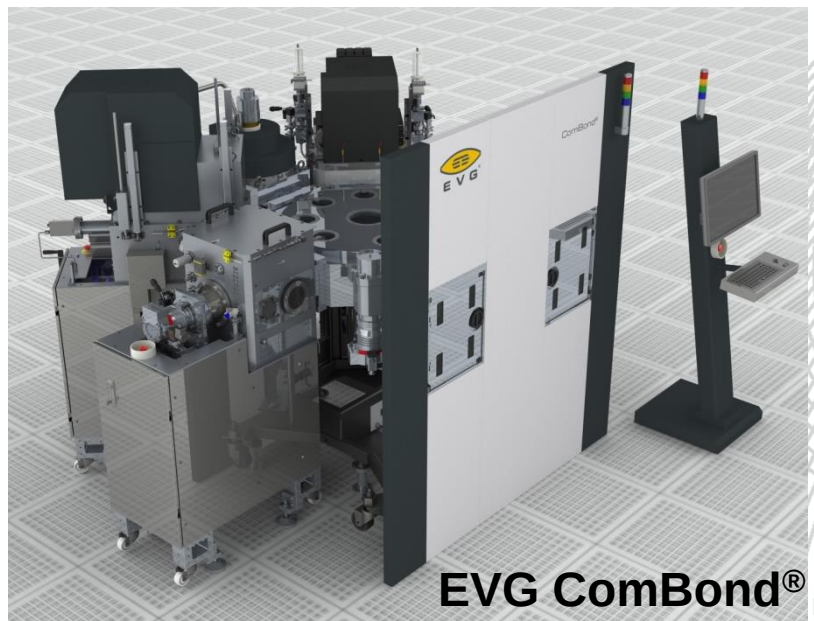
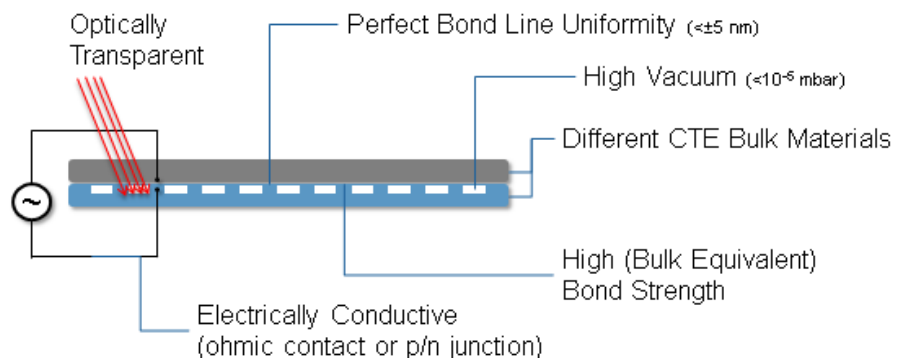
AT A GLANCE

Assessment of room temperature covalent wafer bonding technology.

SEA4KET SP10 –
PARTNERS
 EVG
 CEA LETI
 ST Microelectronics

Advances proposed in SP10

- Development of a surface preparation method for enabling room temperature covalent bonding.
- Characterization of the process for various combinations of materials/surface qualities
- Implementation of the newly-developed equipment and processes into volume manufacturing environment.



EVG ComBond®

SEA4KET PROJECT – BULLETIN

SP10 - COVBOND

Direct Covalent Bonding at Room Temperature

Project Results

Equipment and process technology assessed based on:

- Functionality
- Contamination (particles/metals)
- Wafer Bonding process results

Room temperature fusion bonding was achieved for Si-Si, Si-GaAs, Si-SiC, SiC-SiC, GaAs-InP but also for Al-Al and Cu-Cu.

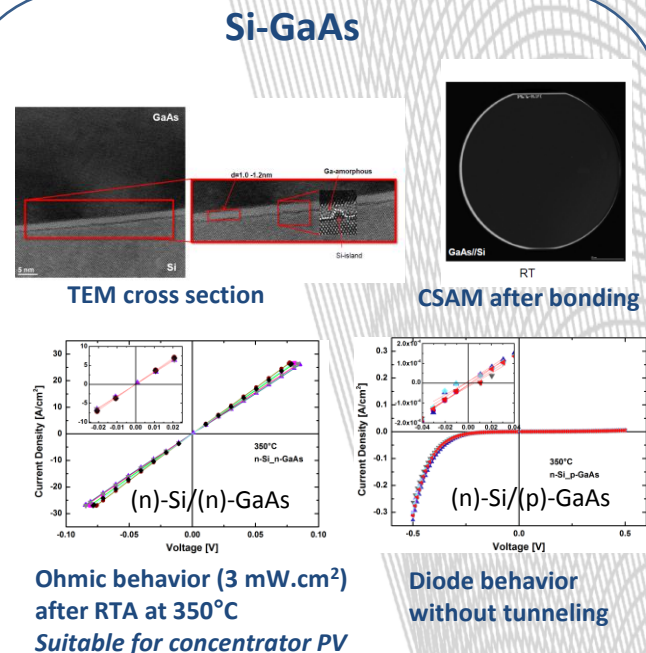
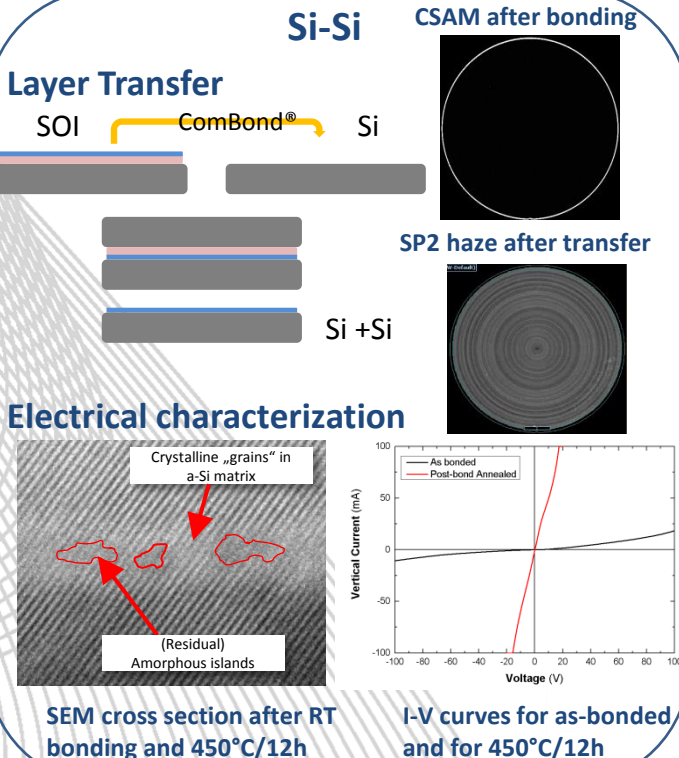
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Results Highlights



SEA4KET PROJECT – BULLETIN

SP11 – 3DIPiCs
**Inspection for 3D Integrated
Photonics Circuits**

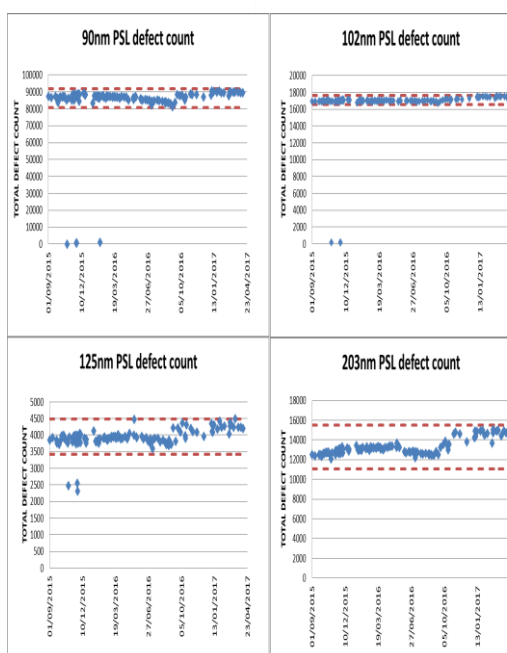
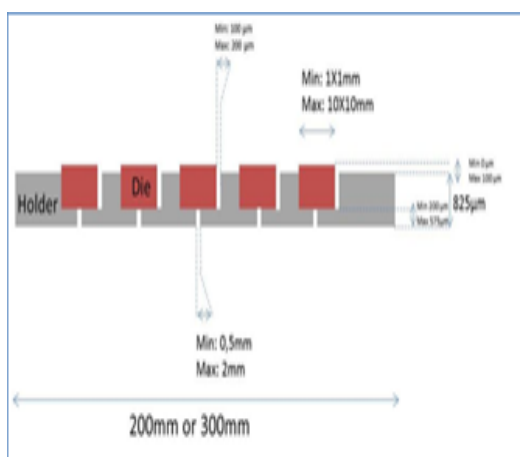
AT A GLANCE

Novel defect inspection of 3D
heterogeneous integration of
hybrid photonics devices
compatible with CMOS
technology

**SEA4KET SP11 –
PARTNERS**
STMicroelectronics
AMIL
CeaLeti

Advances proposed in SP11

- Adaptation of AMIL's Complus inspection tool
for single photonic dies inspection using
special die holders



SEA4KET PROJECT – BULLETIN

SP11 – 3DIPiCs

Inspection for 3D Integrated Photonics Circuits

	Initial status	achieved	Final target
Analysis Metrology			
Measurement application (e. g. sheet resistance ...)	Defectivity		Defectivity
Wafer type (n, p, patterned, unpatterned, pn junction)	Patterned, unpatterned and stickers	Demonstrated on unpatterned stickers, on going on patterned stickers	Patterned, unpatterned and stickers
Measurement type (Non-Contacting, Non-destructive, contacting, destructive)	Non contact, non destructive	achieved	Non contact, non destructive
Wafer preparation	NA		NA
Wafer postprocessing (possible, cleaning needed ...)	No		No
Measuring Time			
Time for evaluation of raw measurement			
Measurement speed (Seconds/point)			
Measurement Range	0 - 50 000 defects	0-100 000 defects demonstrated	0 - 50 000 defects
Detectable species (what is actually measured)	Particles, holes, ...	All defect types captured	Particles, holes, ...
Sensitivity	Please see sensitivity table below		
Precision / Accuracy	"±/- 4µm for GF30 and above (per AMAT ATP)	±/- 4µm for GF30 achieved	
Detection Limit	PSL 0,09µm	Demonstrated with PSL spheres	PSL 0,09µm
Repeatability	>97% on OTW and >95% on product wafer (by defect count only)	Achieved	
Reproducibility	>97% on OTW and >95% on product wafer (by defect count only)	Achieved	
Wafer Map Resolution	NA		
Wafer Map Edge Exclusion	3 mm	Achieved	3 mm
Spot/measurement point size	Depends on the magnification used.		
Removal of material (etch/sputter rate; uniformity)	NA		NA
Equipment special feature (uniqueness ...)	NA		NA

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SEA4KET PROJECT – BULLETIN

SP12 - XMeCK
X-ray Metrology

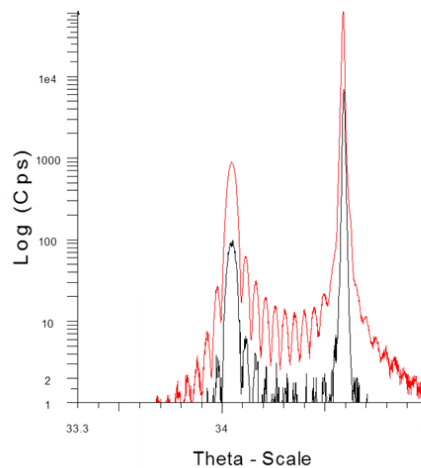
AT A GLANCE

Assessment of X-ray metrology on thin to ultrathin films and on small measurements spots

SEA4KET SP12 –
PARTNERS
 Bruker
 STMicroelectronics
 CEA-Leti

Advances proposed in SP12

- Availability of high brightness X-ray sources which will result in an improvement in throughput of a factor of ~ 10.
- Improved usability and algorithms targeted to advanced materials, photonics, and their heterogeneous integration
- Complete prototype
- Improved analytical software for HRXRD



Ten times more intensity and better resolution High Brightness X-ray source



SEA4KET PROJECT – BULLETIN

SP12 - XMeCK X-ray Metrology

Project Results

D8 Fabline automated diffractometer

The D8 Fabline is a highly versatile automated diffractometer for 300 mm wafers, with snap lock optics and automatic recognition of components. It was installed and accepted at CEA-LETI starting from Mar 2015. The tool is in a so called D8 Fabline-HR configuration, for HRXRD, XRR and GIXRD measurements. The tool has been used for measurements on a range of different samples of interest to CEA-Leti and therefore also representative of the interest of the broad semiconductor industry.

Strain in SiGe in small metrology pads

Patterned samples with SiGe finFET in small metrology pads have successfully been measured in Bruker Karlsruhe on the D8 Fabline-MH tool using a High Brilliance rotating anode (Turbo X-ray Source) with a $100 \times 100 \mu\text{m}^2$ spot size as shown in Fig. 2. Typical measurement times are minutes per site. Capability to measure in small spots at high throughput is an enabler for further adoption of X-ray metrology in the semiconductor high volume manufacturing.



Fig. 1 D8 Fabline tool

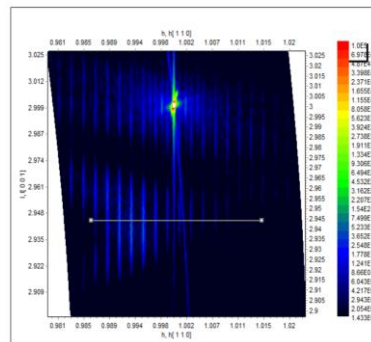


Fig. 2 An RSM on the 113 asymmetrical reflection of a small finFET pad, showing starting relaxation of the epitaxial layer

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SEA4KET PROJECT – BULLETIN

SP12 - XMeCK X-ray Metrology

Project Results

Strain and concentration in III-V materials for photonics and power devices

A range of III-V materials find applications in photonics and power devices. Gallium arsenide has a wider bandgap than silicon. It is therefore used in LEDs, for its efficient light emission. To the same family belong InGaAs and AlGaAs.

(Al)GaIn and (Al)InN are typically used in power devices. Its bandgap can be tailored as a function of the aluminium concentration in the alloy.

The strain and concentrations in these alloys are important parameters for the product quality and can be determined by the D8 Fabline in HRXRD analysis mode as shown in Fig. 3.

Thickness and crystallinity of ultrathin films

Titanium nitride (TiN) films are used as diffusion barrier layers in microelectronic devices. The performance and stability of such barrier is related to the crystallinity and grain size in the film. Thin polycrystalline TiN samples of 7 nm and 3 nm were measured using XRR to analyze thickness and roughness (Fig. 4). GIXRD was used to analyze the crystalline phase (Fig. 5).

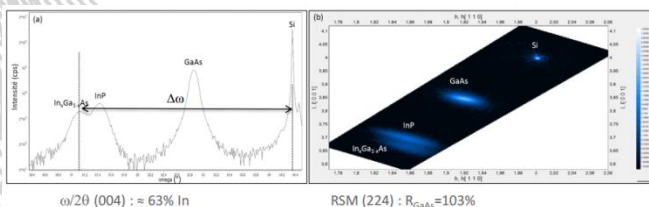
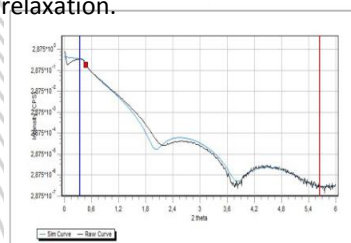


Fig. 3 RSM of 224 Bragg reflection; the position of InGaAs and InP is a measure for the relaxation.



N	R	Material	Cell input	Thickness	Conc X Top, %	Conc X Bot, %	Relax. Top	Relax. Bot	Density T	Roughness
1	1	TiN_a	density	4.7046	0.0000	0.0000	0.000	0.000	5.49499	0.3961
SUB	1	Si	density	0.0000	0.0000	0.0000	0.000	0.000	2.32910	0.0000

Fig. 4 XRR scan of 5nm TiN sample.

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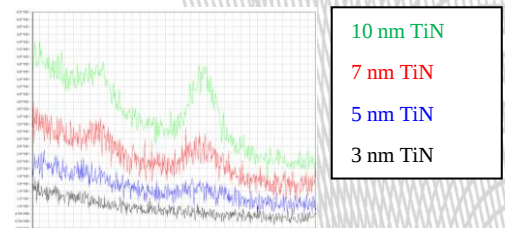


Fig. 5 The peaks at 43° and 62° that are typical for TiN are present in the 7 nm and 5 nm sample, but have disappeared in the 3 nm sample.

SEA4KET PROJECT – BULLETIN

SP13 - REPSiC

Rapid Electrical Field Driven Processing of Gate Dielectrics on Silicon Carbide

AT A GLANCE

Assessment of plasma
oxidation and nitridation tool
for SiC gate oxide formation

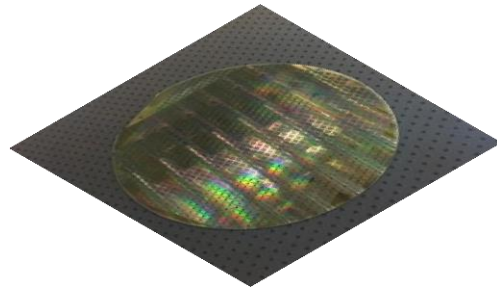
Optimization of chamber and
process parameters to
optimize oxide quality on SiC

SEA4KET SP13 – PARTNERS

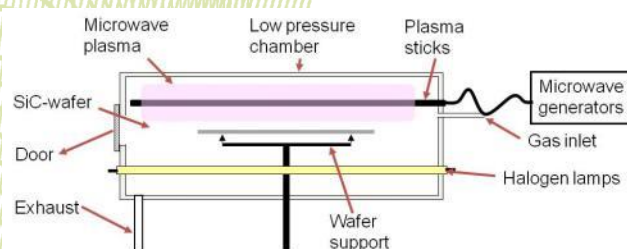
Fraunhofer IISB
HQ – Dielectrics
Infineon Technologies

Advances proposed in SP13 - REPSiC

- Proposed concept uses a new electron charge driven method for enhanced oxidation rate of SiC without oxide damage.
- Process has been demonstrated on Si wafers and SiC samples before
- Remarkable reduction of oxidation temperature and thermal budget by 500 °C
- Oxide growth independent from crystal orientation (now oxidation anisotropy)



150 mm SiC MOSFET wafer on SiC susceptor in the plasma oxidation equipment



Schematic of the high-density microwave plasma oxidation and in-situ post plasma anneal apparatus

- Concept enables free combination and sequence of oxidation and nitridation in order to establish user defined nitrogen profiles
- New methodology to influence the SiC-oxide interface, including its electrical characteristics

HQ-Dielectrics

SEA4KET PROJECT – BULLETIN

SP13 - REPSiC

**Rapid Electrical Field Driven Processing of
Gate Dielectrics on Silicon Carbide**

Project Results

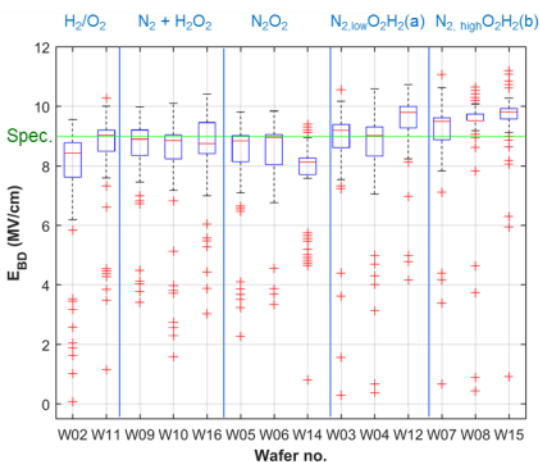
**Multiplied oxide growth rate on SiC at
low temperature (< 1000 °C)**

**Excellent conformality of oxide
growth, i.e. very little anisotropy**

**Oxide thickness > 10 nm
demonstrated, potentially up to 20 nm**

**MOSCAP and MOSFET Device grown
with plasma oxide base gate dielectric**

Promising first electrical results



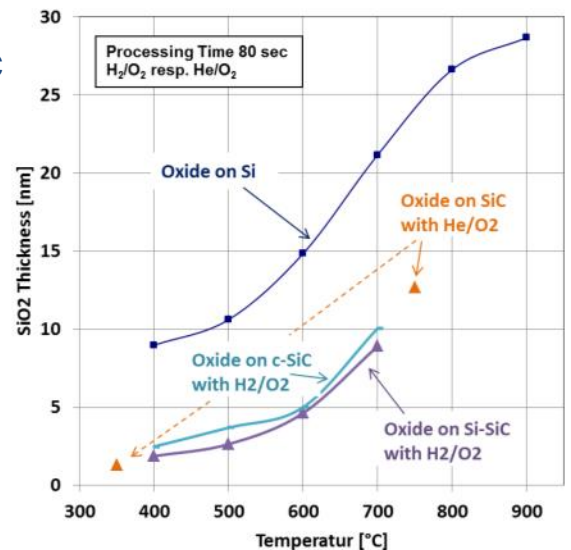
Break down field satisfies technological requirements

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Oxide growth rate on SiC compared to Si:
0.9 nm/min @ RT/350 °C, 9 nm/min @ 750 °C

HQ-Dielectrics

SEA4KET PROJECT – BULLETIN

**SP14 – TLS4SiC
Thermal Laser Separation
for Fast High Quality
Silicon Carbide Dicing**

AT A GLANCE

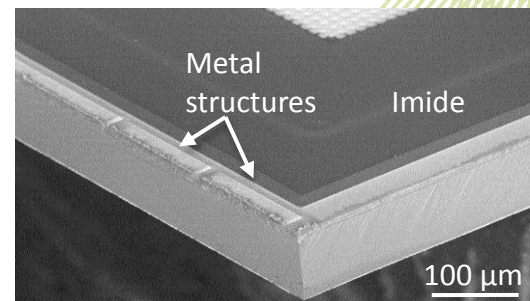
Assessment of an innovative dicing technology able to fulfill the requirements of SiC volume production.

**SEA4KET SP14 –
PARTNERS**

Fraunhofer IISB
Fraunhofer CSP
3D-Micromac AG
Infineon Technologies

Advances achieved in SP14 – TLS4SiC

- Assessment of the kerf free dicing technology for Silicon Carbide product wafers with regard to throughput, reliability, edge quality and electrical characteristics of separated chips and handling issues.
- Increased feed rate up to a factor of 100 compared to state of the art dicing technology.
- Very high edge quality – no chipping, smooth side walls and no delamination of backside metal – leads to good electrical characteristic and promises long-term stability of separated chips.
- High throughput and no tool wear results in a significantly reduction of process costs compared with state of the art dicing technology.
- TLS4SiC will be an enabler for SiC volume production by providing a separation technology allowing for high quality results with high throughput far beyond state of the art.



SEA4KET PROJECT – BULLETIN

SP14 – TLS4SiC

Thermal Laser Separation for Fast High Quality Silicon Carbide Dicing

Project Results

- Tape assessment prove that a standard dicing tape for blade dicing can be used for TLS-Dicing™.
- Developed shipping strategy for zero kerf diced wafers guarantees damage free transportation.
- Development of a process simulation model.
- Successful dicing of up to 150 mm SiC diode wafers with chips sizes down to 0.96 mm² demonstrated.
- SEM and TEM measurements proofed high chip sidewall quality with no micro cracks.
- TLS diced wafers assembled using Infineon's production lines in Malaysia.
- Electrical measurements proof good die attach, good electrical characteristics and long term stability of TLS diced chips.
- Next generation TLS-Dicing™ tool microDICE™ developed and built up.

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