Grant Agreement No. 619572

COSIGN

Combining Optics and SDN In next Generation data centre Networks

Appendix to D2.1

Confidential additional information to provide some background and detail not to be published outside the confines of the COSIGN project

Tim Durrant
Venture Photonics Ltd
August 2015

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Summary

This pack of information is to provide additional information regarding the Deliverable 2.1

"Integration of OpenFlow SW Interface with
Polatis System and Venture 4x4 OXS"

The main focus of this appendix is the Venture switch technology. It provides some history of the technical development over the span of COSIGN so far, and also some recent testing that is directly or indirectly in support of D2.1.

There is technical information on the product and processing under development that is to be treated as Confidential, only for members of the consortium (including the Commission Services).

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Intent of Task 2.2.2 activities

The fundamental intent of the Venture Photonics part of the COSIGN project is the development of a fast solid state single mode InP Optical CrossPoint Switch (OXS)

Key target characteristics are

- Optical switching 5 ns
- Wavelength window 1530-1560 nm
- Polarisation dependent loss 1 dB
- Insertion loss < 7 dB
- Cross talk -50 dB

Device to be capable of integration with driver circuit to be driven by OpenFlow software

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Partner roles

The structure of the OXS project is such that

- Much of the chip development effort is channelled through UNIVBRIS, though much of the materials spend is from Venture
- The packaging effort is provided by Venture
- The driver and software integration effort is provided by DTU and UNIVBRIS
- Additional support from TUE

There is a chip and package development, a driver development and an integration of optics with driver and software

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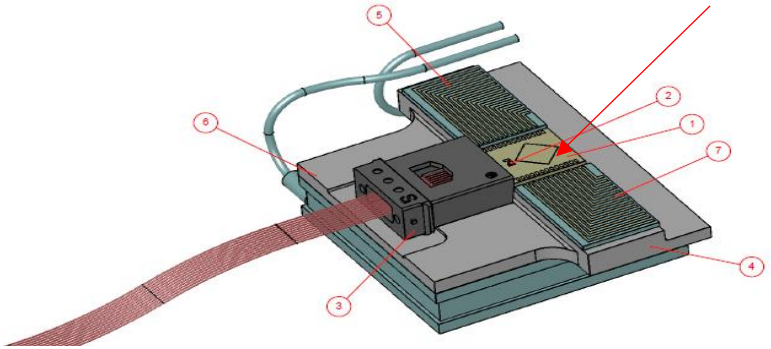
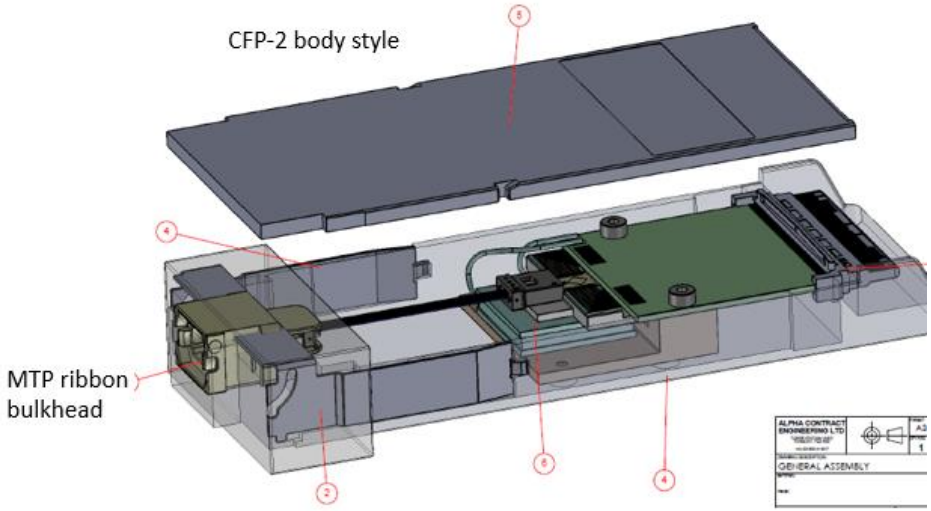
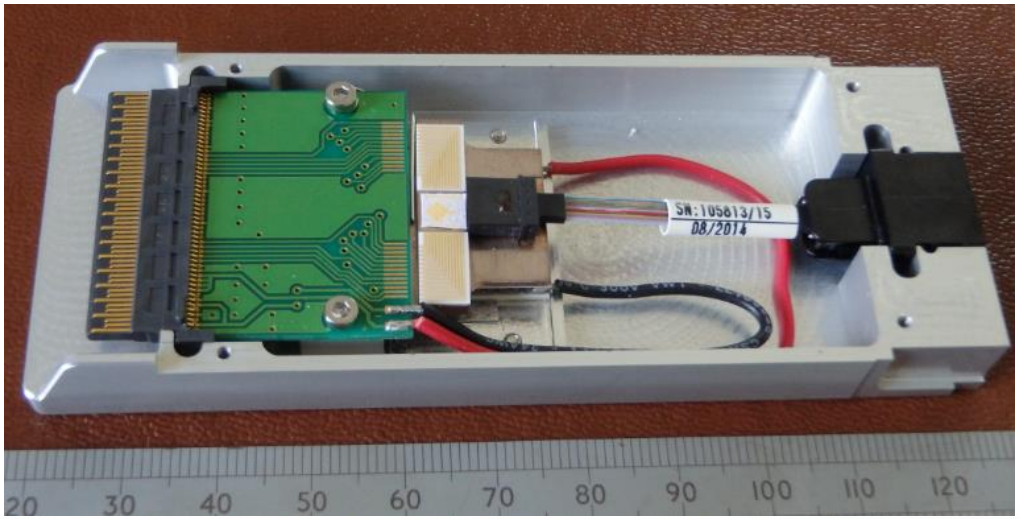
The packaging solution developed using the CFP2 module style

Chip





Ribbon fibre/chip interface



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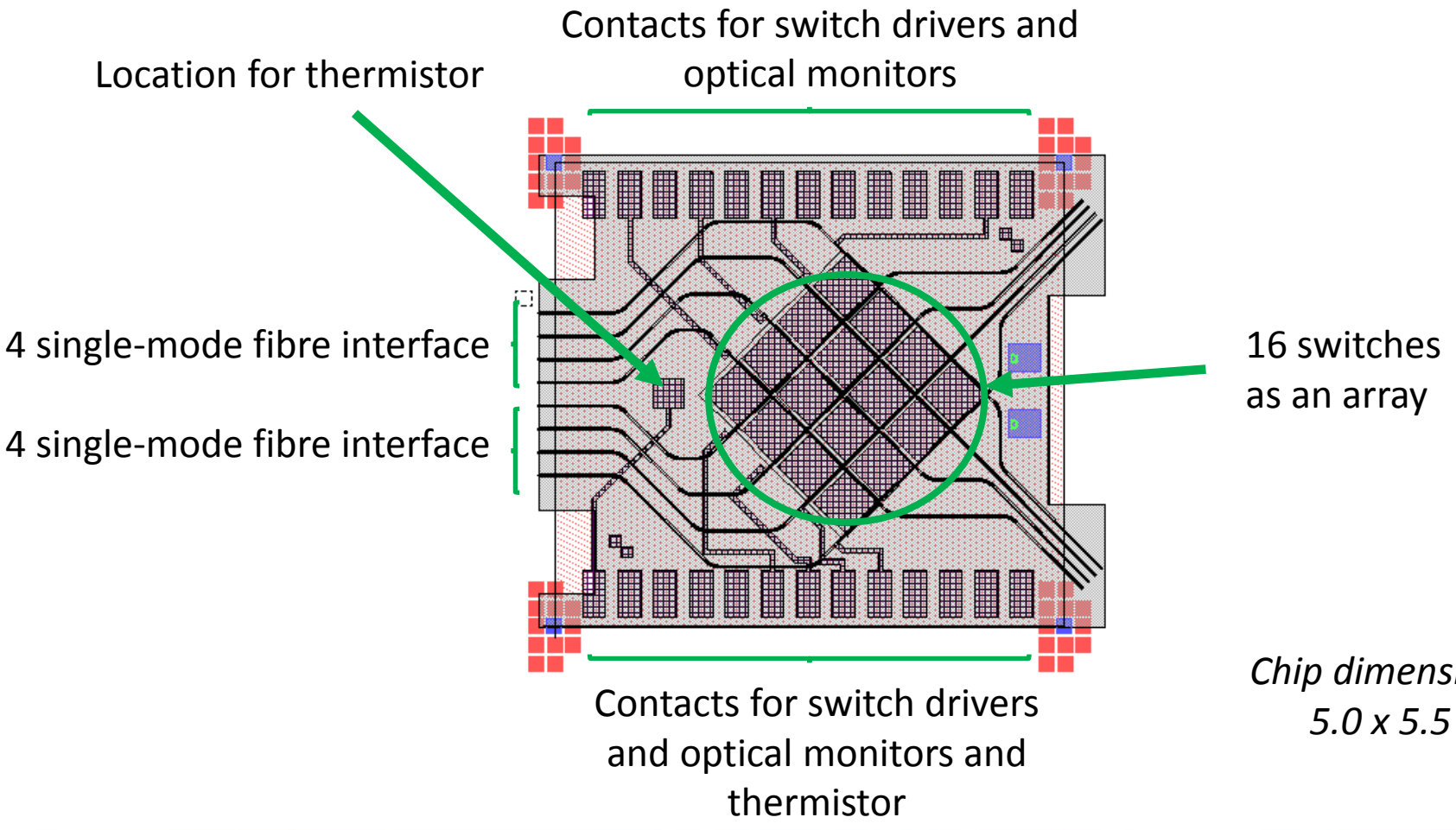
Functionality of a 4x4 InP OXS chip



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Individual switch function

The basic principle of operation is by Active Vertical Coupling (AVC)
Epi layers designed so that light passes straight through the switch with bias off.
Switching occurs by carrier injection induced index matching change (bias on).
This 'lifts' the optical path 'up', to then be internally reflected, then 'dropped' back to a different waveguide

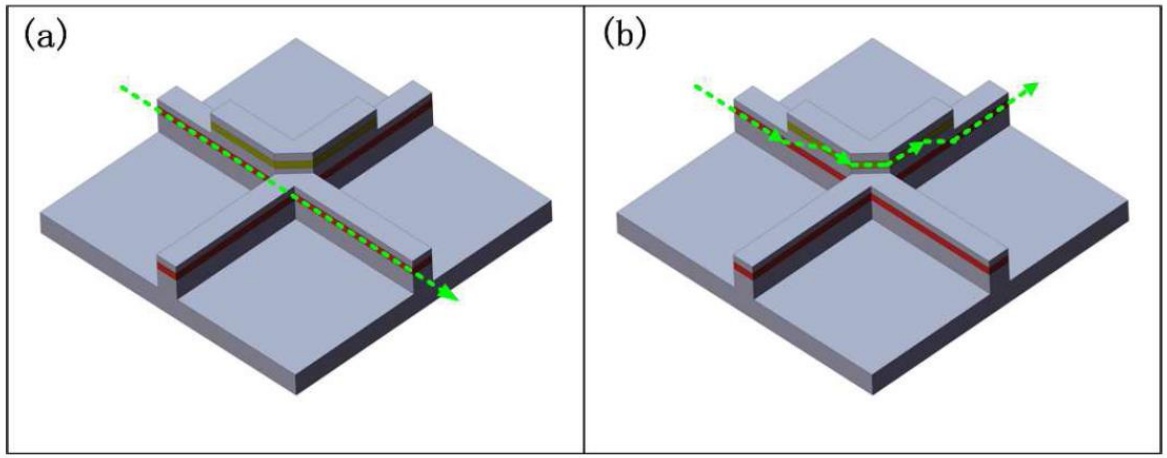

Fig.2. (a): "Off" state under Zero bias and (b): "On" state under forward bias in one single AVC cell

In addition Semiconductor Optical Amplifiers (SOA) and optical monitors are built into the waveguide to be able to give individual control of light conditions through the switch

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Epi structure

These features demand a complex chip structure.

The epi layer, simplistically consists of 28 doped layers

Repeats	Thickness (A)	Material	Dopant	type	Concentration (cm^{-3})
1	2000	$In_{0.53}$ GaAs Cap	Zn	p	1E+19
1	500	Q1.1	Zn	p	1E+18
1	13000	InP	Zn	p	4-6E+17
1	3000	Q1.1	Zn	p	4-6E+17
1	500	InGaAlAs(Al=0.42)	-	i	
1	250	Q1.3	-	i	
1	1000	Q1.55	-	i	
1	250	Q1.3	-	i	
1	1000	Q1.1	-	i	
1	5000	InP	Si	n	4-6E+17
1	800	InGaAlAs(Al=0.22)	Si	n	4-6E+17
1	5000	InP	Si	n	4-6E+17
1	1800	Q1.35	Si	n	4-6E+17
1	3000	InP buffer	Si	n	4-6E+17
1	1600	Q1.35	Si	n	4-6E+17
1	3000	InP buffer	Si	n	4-6E+17
1	1400	Q1.35	Si	n	4-6E+17
1	3000	InP buffer	Si	n	4-6E+17
1	1400	Q1.35	Si	n	4-6E+17
1	3000	InP buffer	Si	n	4-6E+17
1	1400	Q1.35	Si	n	4-6E+17
1	3000	InP buffer	Si	n	4-6E+17
1	1400	Q1.35	Si	n	4-6E+17
1	3000	InP buffer	Si	n	4-6E+17
1	1600	Q1.35	Si	n	4-6E+17
1	3000	InP buffer	Si	n	4-6E+17
1	1700	Q1.35	Si	n	4-6E+17
1	10000	InP buffer	Si	n	4-6E+17
1		InP Sub			

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Wafer processing

Processing the wafer requires (in simplified form) 34 process steps, many needing very accurate alignment with previous activities.
This is not including the cleaving and Anti-Reflection (AR) coating stages.

1) *n-contact*: clean (solvents, O2 ash, dHCl), e-beam deposit PdGeAuPdAu (20+50+10+50+240nm) on n-InP substrate
2) *e-beam 1*: spin 2 layers PMMA resist, align precisely to cleaved flat, define pattern in PMMA bilayer for e-beam markers, cleave markers, labelling text
3) *marker lift-off*: develop, ash, dHCl, deposit NiCrAuNiCr, solvent soaks & cleans
4) *ICP SiNx dep*: O2 RIE ash, dHCl, dNH4OH, DI, 0.4um ICP SiNx dep
5) *e-beam 2*: spin ZEP resist, define pattern in ZEP for mirror etch mask (over-sized)
6) *SiNx RIE*: ZEP develop, ash, CHF3/O2 RIE etch (IF1) through SiNx onto III-V (ZEP mask)
7) *strip resist*: MF319, O2 ash, solvents, O2 RIE, dHCl
8) *e-beam 3*: MF319, ash, spin HSQ resist, e-beam to define pattern in HSQ for mirror mask
9) *III-V ICP etch*: develop, ash, dHCl, CH4/H2/Cl2 ICP etch (IF1) mirror just short of 2nd ($Al_{0.22}$-Q) etch-stop (HSQ+SiNx mask)
10) *Post-ICP cleans*: O2 RIE, dHCl
11) *III-V RIE etch*: CH4/H2/O2 RIE etch mirror down onto 2nd ($Al_{0.22}$-Q) etch-stop (HSQ+SiNx mask)
12) *SiNx/SiO2 etch*: MF319, O2 RIE, solvents, O2 ash, BHF etch
13) *ICP SiNx dep*: O2 RIE ash, dHCl, dNH4OH, DI, *0.7um* ICP SiNx dep
14) *e-beam 4*: *2x* spin ZEP resist, define pattern in ZEP preparing for HSQ shallow ridge mask
15) *SiNx RIE*: ZEP develop, ash, CHF3/O2 RIE etch (*IF2*) remaining SiNx mask down onto III-V (ZEP mask) *pattern change and trials required to obtain dose/bias*
16) *strip resist*: MF319, O2 ash, solvents, O2 RIE, dHCl mask
17) *e-beam 5*: MF319, ash, spin HSQ resist, define pattern in HSQ for shallow ridge mask & mirror trench in-fill
18) *III-V RIE etch*: HSQ develop, O2 ash, CH4/H2/O2 RIE etch (*IF2*) to 1st etch-stop with small over-etch (SiNx+HSQ masks)
19) *cleans*: MF319, O2 RIE ash, solvents, O2 barrel ash
20) *e-beam 6*: MF319, ash, spin HSQ resist, define pattern in HSQ for XWG deep etch
21) *III-V ICP etch*: HSQ develop, O2 ash, CH4/H2/Cl2 ICP etch (*IF2*) XWG (HSQ & SiNx masks)
22) *SiNx/SiO2 etch*: MF319, O2 RIE, solvents, O2 ash), BHF etch
23) *PECVD*: O2 barrel ash, dNH4OH, DI, deposit 0.1um PECVD SiO2
24) *HSQ*: ash, spin HSQ resist, oven
25) *PECVD*: O2 barrel ash, deposit 0.1um PECVD SiO2
26) *e-beam 7*: spin 4 layers PMMA resist, define pattern in PMMA to remove SiO2 planarisation over cleave markers & text labels
27) *SiO2 RIE*: PMMA develop, ash, CHF3/Ar RIE etch (*IF3*) SiO2 planarisation through onto NiCr-Au-NiCr features
28) *strip resist*: MF319, O2 ash, solvents, O2 ash
29) *e-beam 8*: spin 4 layers PMMA resist, define pattern in PMMA for *p*-contact window
30) *SiO2 RIE*: PMMA develop, ash, CHF3/Ar RIE etch SiO2 planarisation through onto III-V shallow ridge cap layer
31) *strip resist*: MF319, O2 ash, solvents, O2 ash
32) *e-beam 9*: spin 4 layers PMMA resist, define pattern in PMMA for *p*-contact lift-off
33) *p-contact lift-off*: PMMA develop, O2 ash, dHCl, e-beam deposit *p*-ohmic TiPdAu (20+40+240nm), solvent soaks & cleans
34) *contact anneal*: barrel ash, RTA at 380C to anneal ohmic contacts

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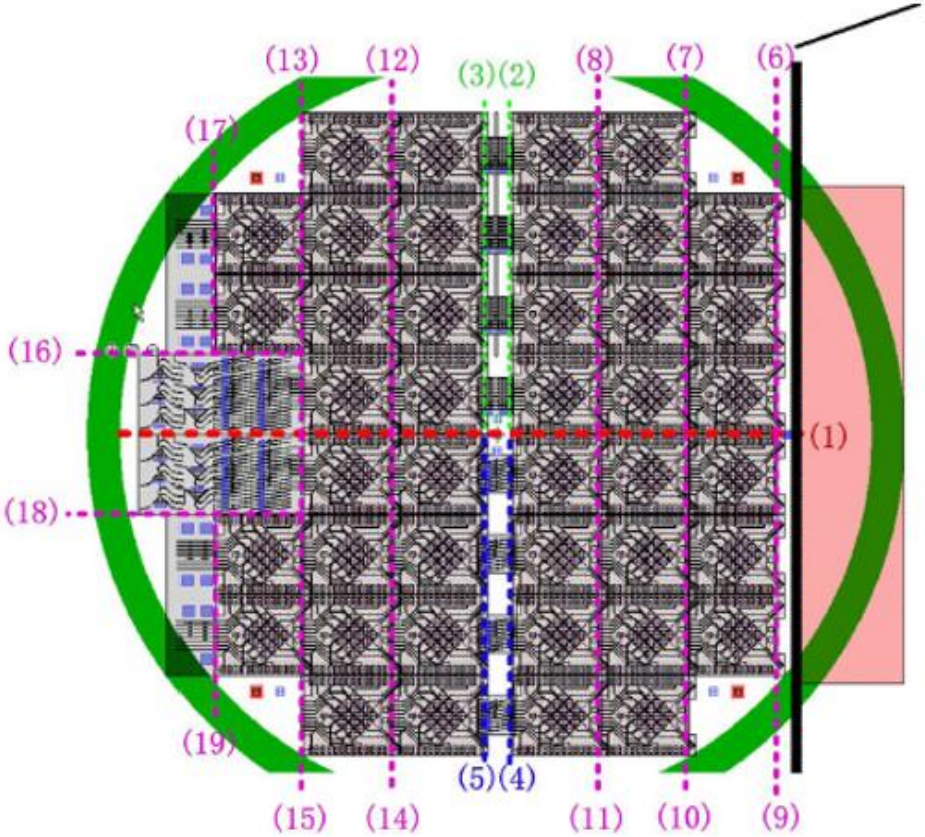
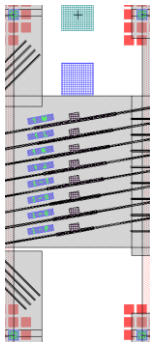
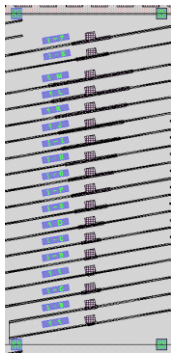
Wafer design

As part of the risk mitigation approach for the wafer fabrication, test pieces are designed into the mask in addition to the OXS chips

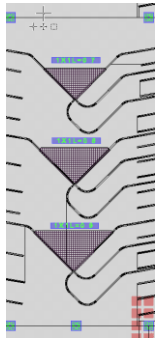




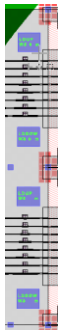
S-inclined SOA Chip
2 mm*5 mm



L-inclined SOA Chip
2.2 mm*5 mm



1X1 OXS Chip
2 mm*5 mm



Laser Chips
1.1 mm*5 mm

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More risk mitigation

After a substantial process development phase, resulting in iterations to the design, two wafers were committed to processing.

Part of further risk mitigation was to separate the two wafers by several steps so that any issues revealed would not affect both wafers (ice-breaker and follow-up wafer). In addition the last few critical steps have been halted on the follow up wafer until results become clear.

There has been much continued learning regarding the design and processing with the activities on these wafers.

The ice-breaker has made it through all processes, but the follow-up wafer is being held back at about the 75% complete stage until substantial characterisation has been performed.

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Disaster on one of the last steps of the ice-breaker wafer

Due to some fab recipe imperfections, the lower passive waveguide was etched away and could not be used in these regions.

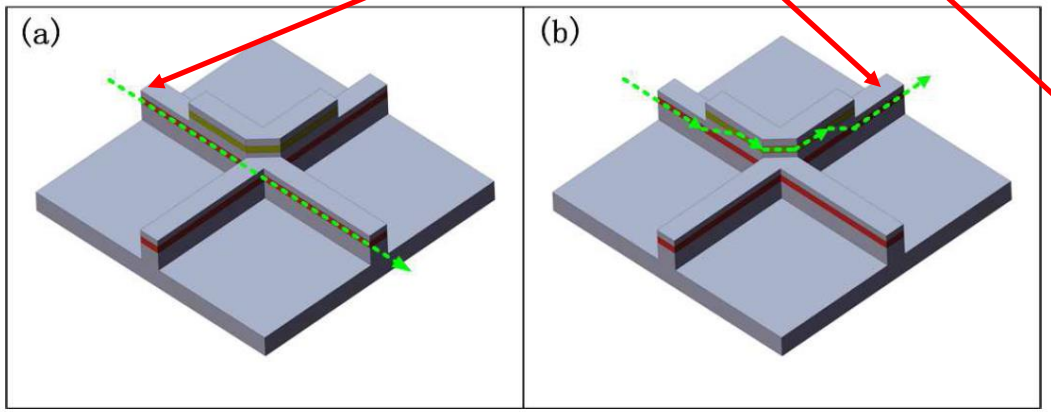
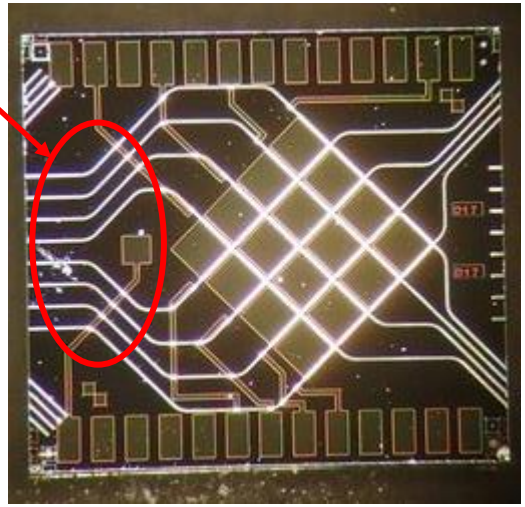


Fig.2. (a): "Off" state under Zero bias and (b): "On" state under forward bias in one single AVC cell



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Hope

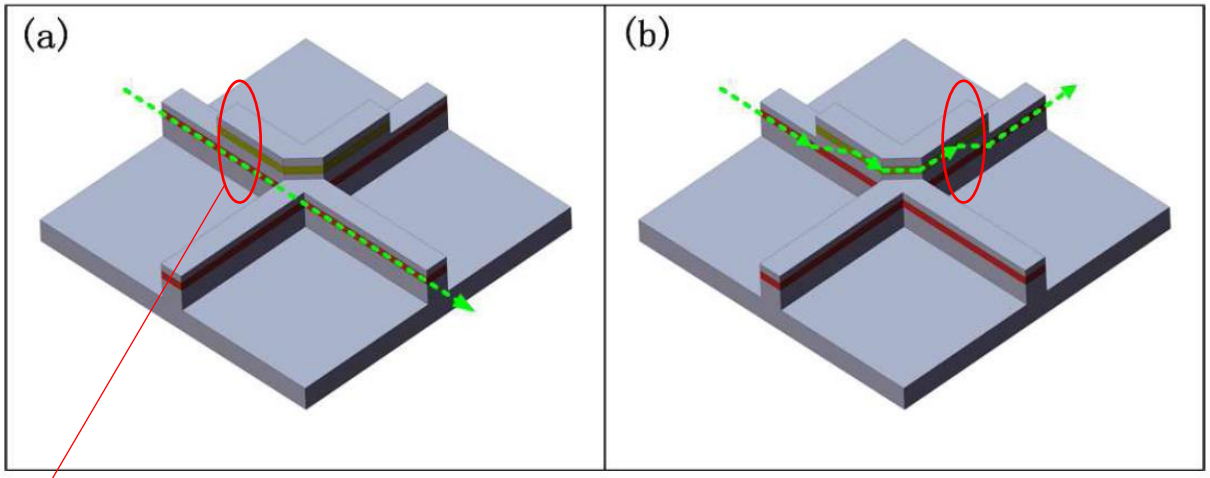
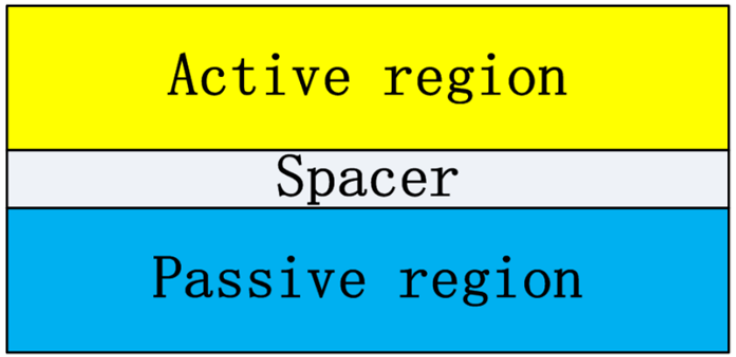


Fig.2. (a): "Off" state under Zero bias and (b): "On" state under forward bias in one single AVC cell

However the region with upper active and lower passive structure is still intact in the Active Vertical Coupling (AVC) structure.
This is true for all such layers present across the wafer.



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Logical consideration

- The material structure across the wafer is the same
- This means that by cleaving the wafer carefully in a slightly different way we can use some of the test pieces to perform characterisation of optical and integration performance in a representative way
- The key and only significant difference to a full OXS chip is that it is a single linear switch rather than a 4x4 switch with all the optics on one face
- The result of this is that the developed packaging cannot be used for this early characterisation work
- So the characterisation work is done on a lab alignment rig with reduced temperature control opportunities
- This has resulted in some of the measurements being done with ~50 mA rather that the planned ~250 mA
- Control of the chip switching function is the same regardless of the optical interface
- There will not be opportunity for very fast switching characterisation as a result of the packaging and jigging considerations. But full integration can be demonstrated under controlled conditions.

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Parts of the wafer being used

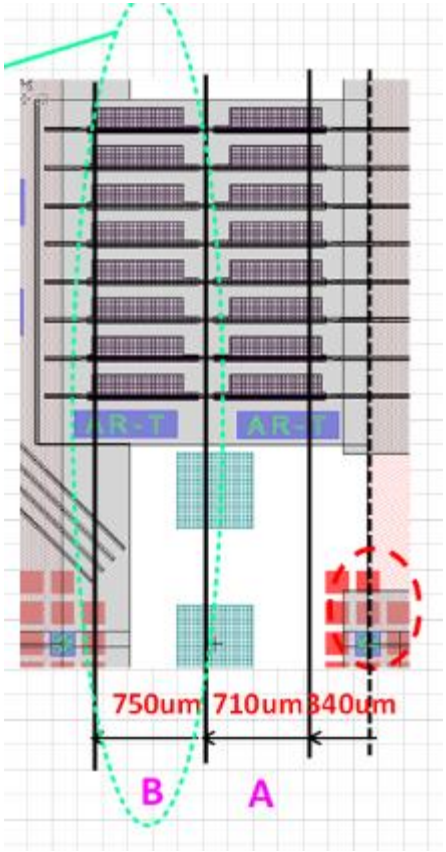
697 µm

Good Facet

Good Facet

Fresh
Good Facet

Bad Facet



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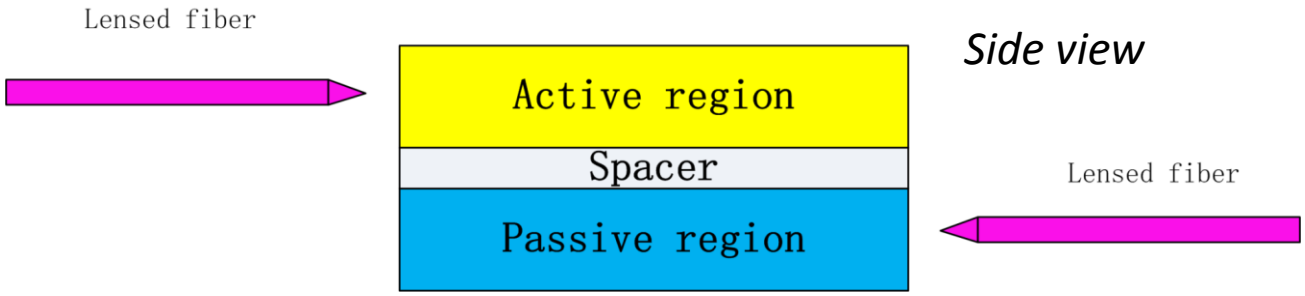
Recovery
To test the switch on and off



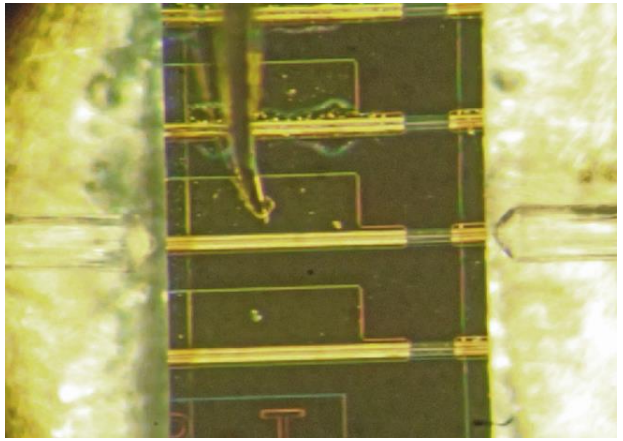
Side view

1) Align the lensed fibre to the upper active region from the facet in the left hand side

2) Align the lensed fibre to the lower passive region from the facet in the right hand side

3) Inject light to the chip from the left lensed fibre, and detect the light power from the right lensed fibre

4) In this method, when the chip is under current injection, the light transmitted in the upper active waveguide injected from the left lensed fibre will be coupled into the lower passive waveguide.



Top view

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The switch “Off” state can be defined with no power output in the right lensed fibre while the switch “On” state is defined with power detected in it; and the switch extinction ratio is defined as the 10*log10(Power_on/Power_off)
The whole OXS extinction ratio is estimated to be 2*10*log10(Power_on/Power_off)
Thus we can treat these test pieces as a switch
In addition a number of other characteristics can be gathered.

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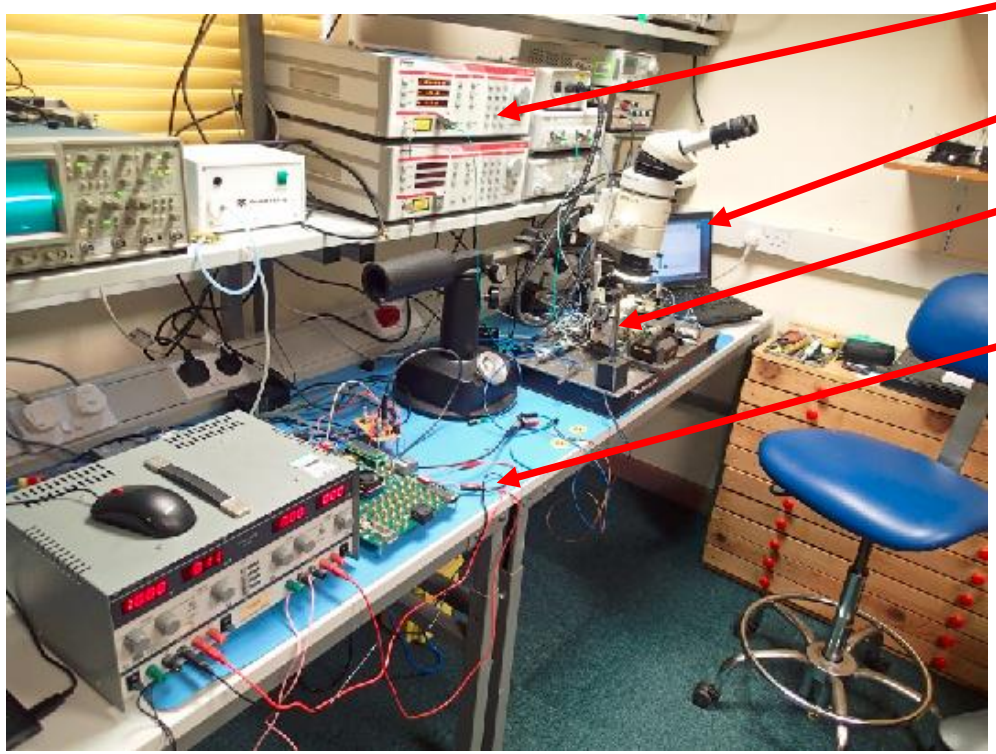
Lab set up for integration testing



Laser light source

Detector system

Alignment rig and Device under test (Venture)

FPGA/Driver (DTU)

Open Flow software (UNIVBRIS)

With help from Bob Musk of Entroptix Ltd

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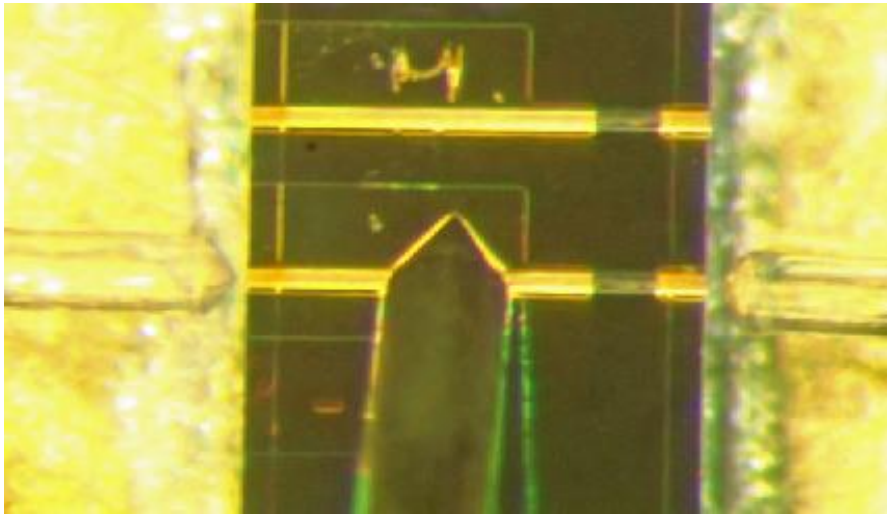
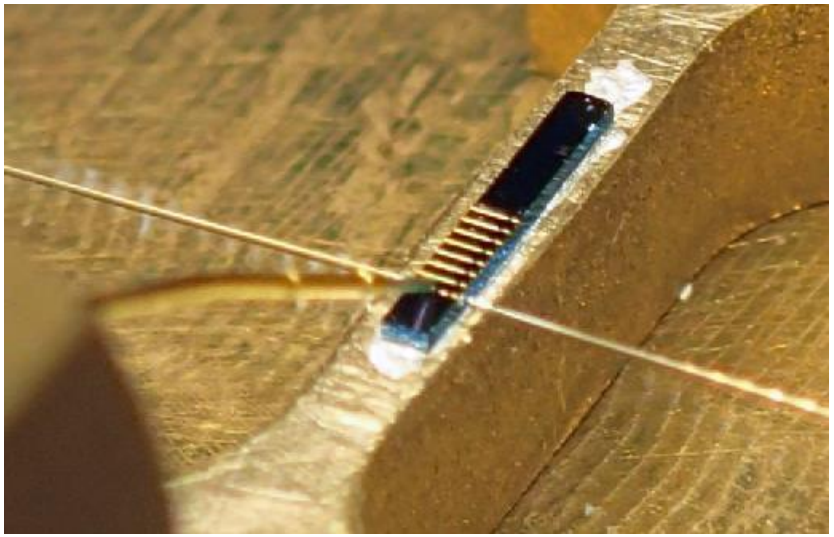
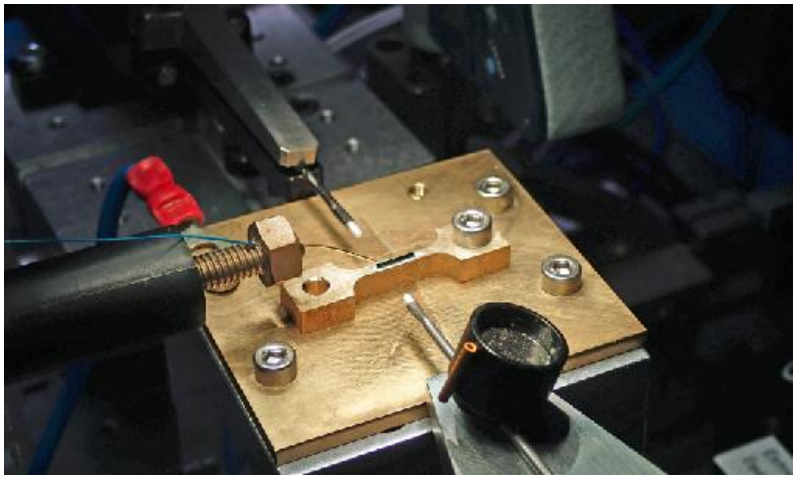
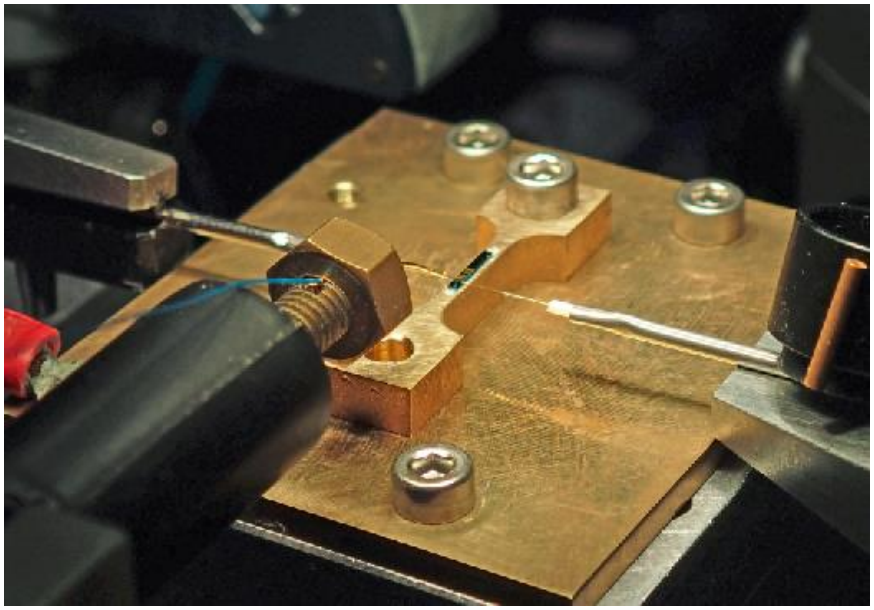
Optical alignment









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Ethernet Frame specification for communication between OF agent and FPGA control board

Ethernet Frame for Veture Switch Configuration (byte for each column)																													Ethernet Frame lines (Captured by Wireshark)
ADDR\BYTE	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			sequesnce number		Source MAC Address									Destination MAC Address						0
00	RESERVED																																10,20
01	Keep alive message length								Time-slice duration												frame size		Time-slice numbers				Mode						30,40
02	1 to 32 time slot: fast switch control commands for port 1																																50,60
03	33 to 64 time slot: fast switch control commands for port 1																																70,80
04	64 to 96 time slot: fast switch control commands for port 1																																90,a0
05	1 to 32 time slot: fast switch control commands for port 2																																b0,c0
06	33 to 64 time slot: fast switch control commands for port 2																																d0,e0
07	64 to 96 time slot: fast switch control commands for port 2																																f0,100
08																																	110,120

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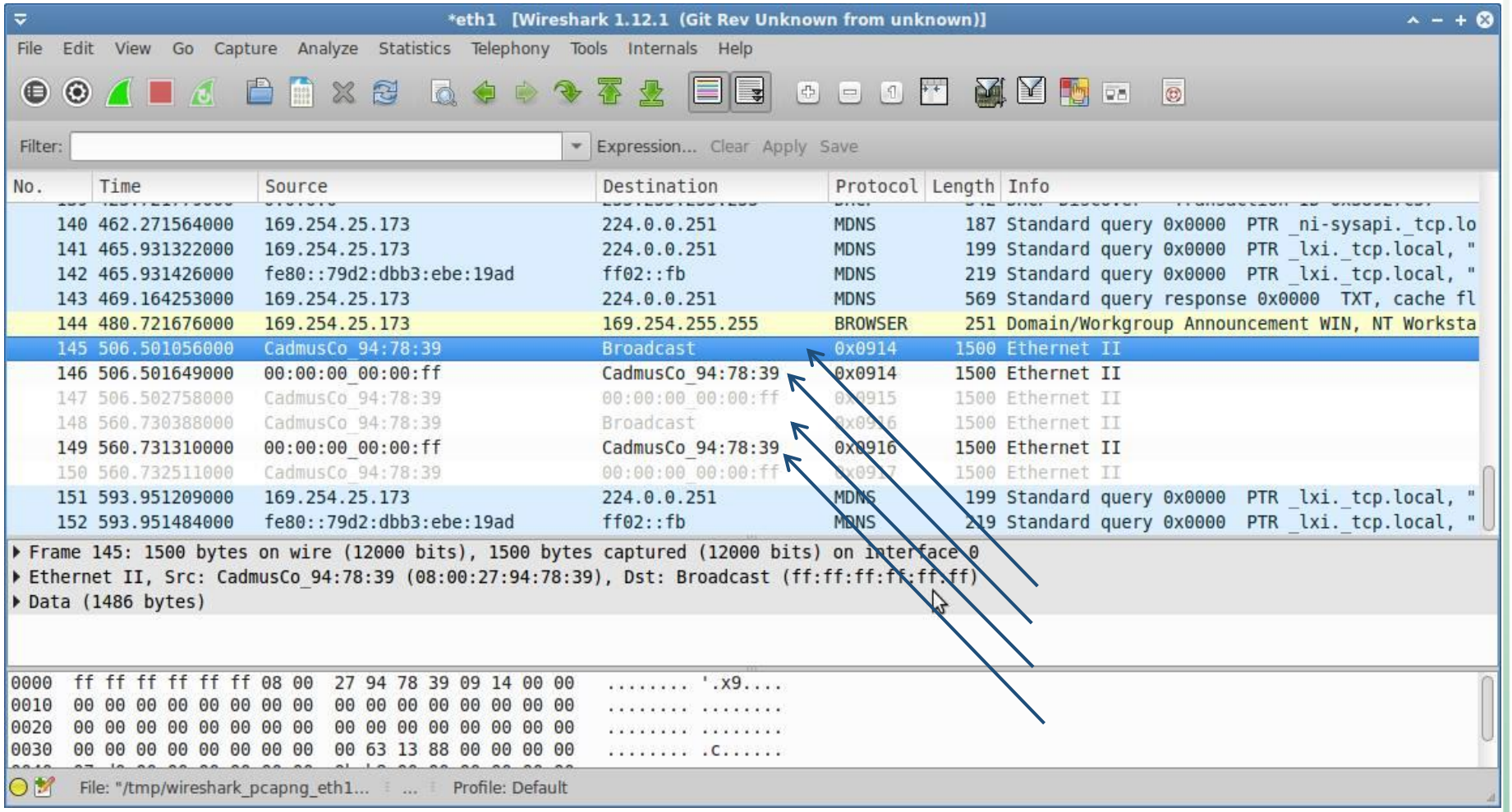
Wireshark snapshots of frames between Agent and FPGA



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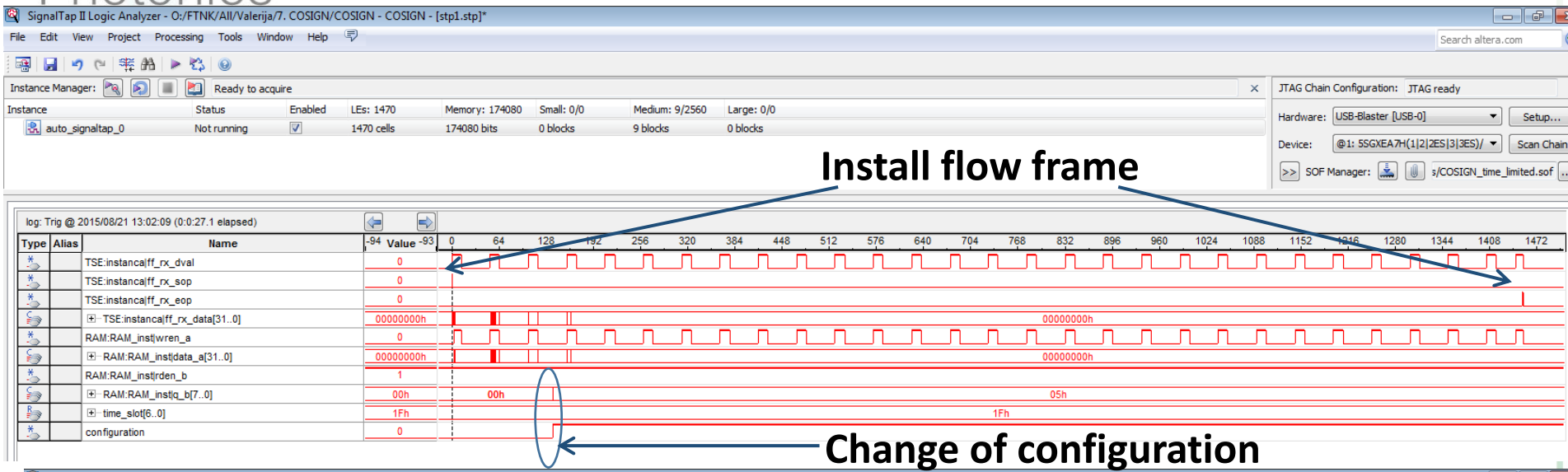
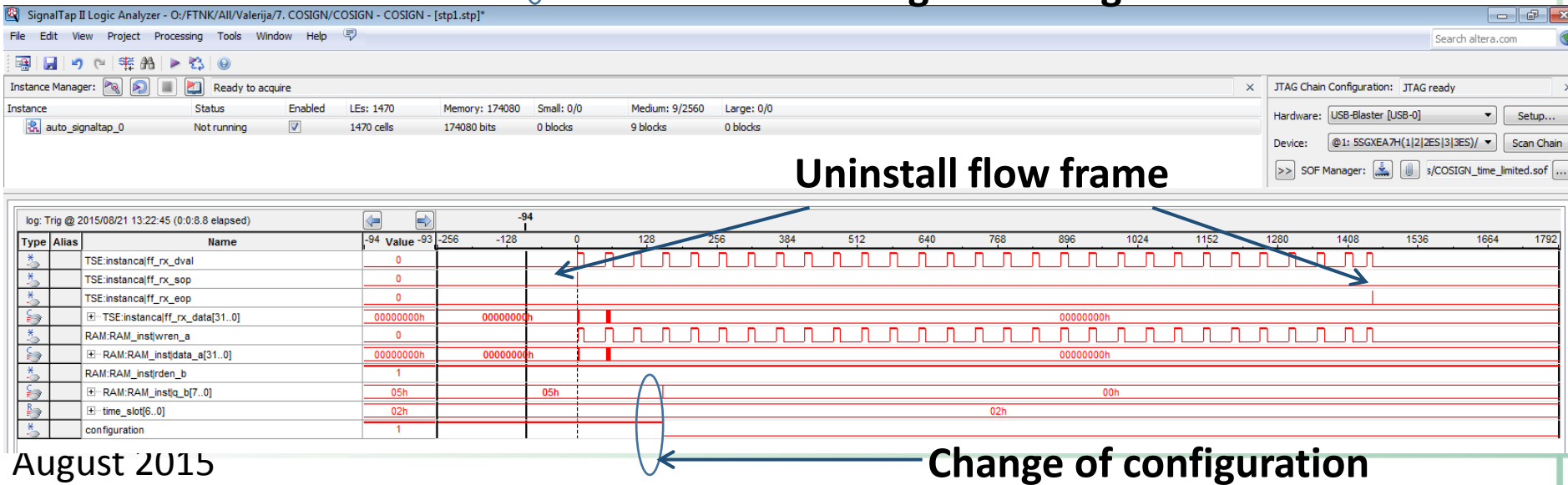
Signal Tap snapshots of frames received by the FPGA





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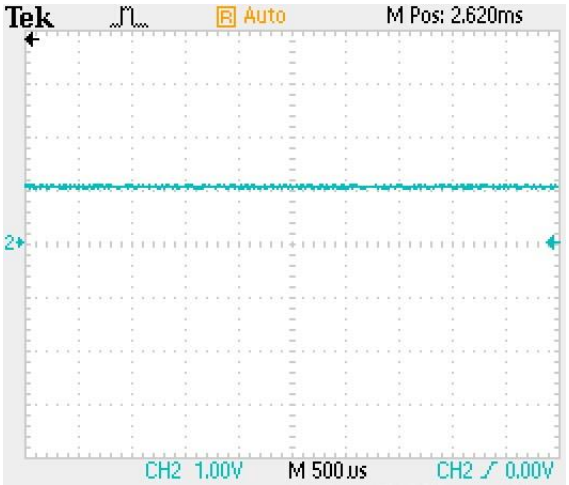
Configuration signals generated from the FPGA

At FPGA output

Standard 0 V and 2.5 V outputs

At driver output



Adjusted to 0 V and 1 V outputs to satisfy switch requirements

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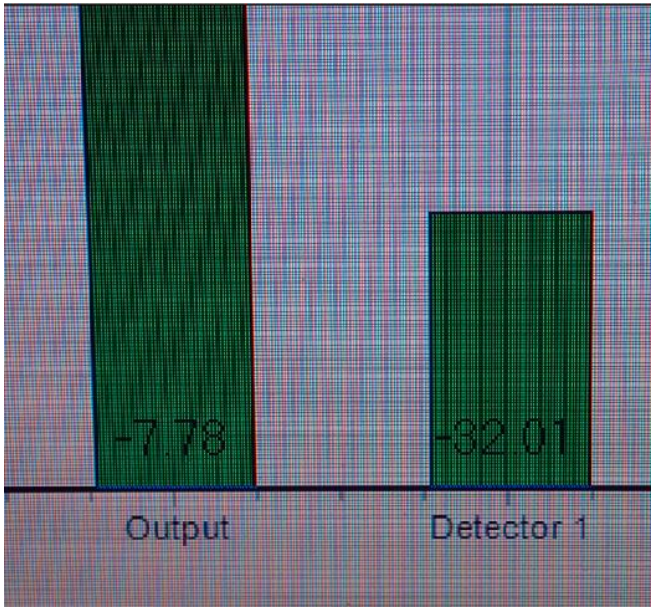
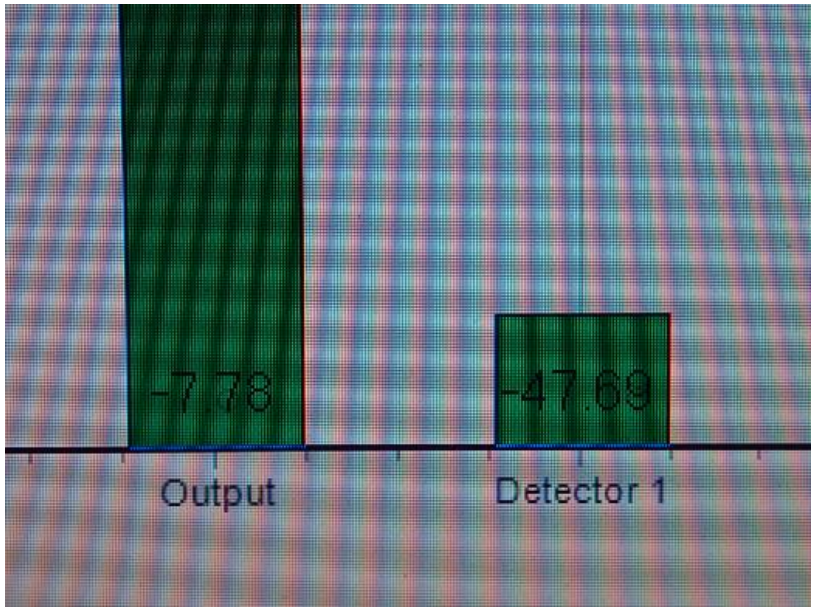
Output showing 15 dB of switching at 50 mA under OpenFlow control





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In addition to the work required for D2.1 there has been substantial additional characterisation work undertaken. The next few pages show some of this data.

This is not part of D2.1 but provides considerable additional confidence in the direction of development for the fast switch.

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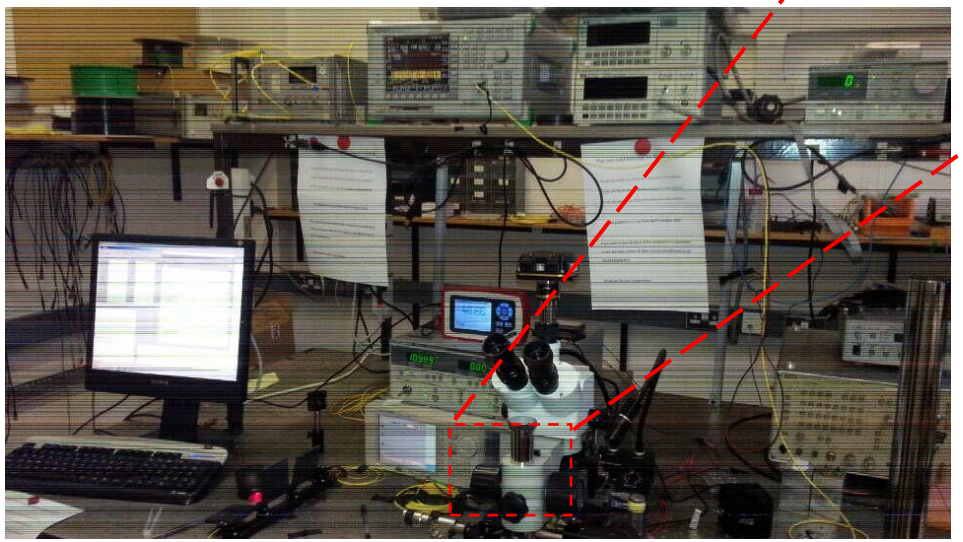
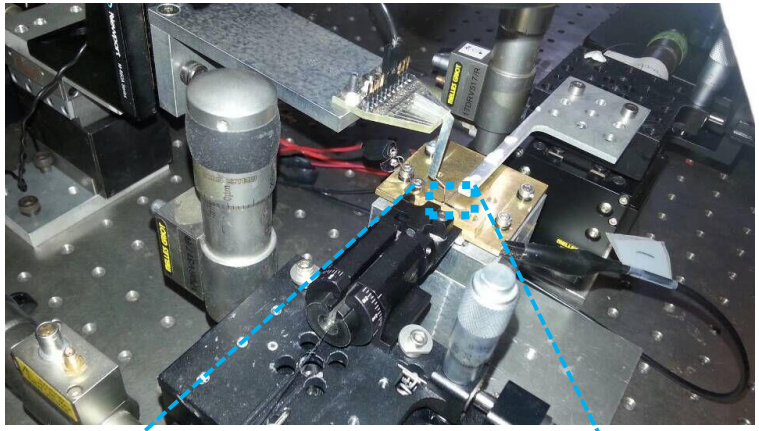
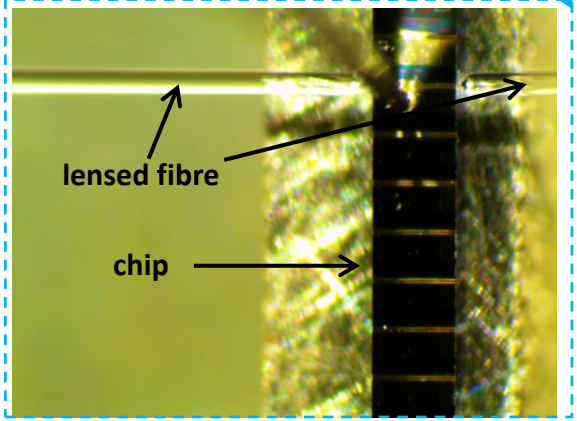
Additional testing of polarisation independence v wavelength

- Feedback-loop constant temperature control module is included in the test bed
- Polarisation control method is proposed, verified and used to study the polarisation-independent switching performance
- Computer-assisted sweeping measurement via GPIB is also established in the test bed.







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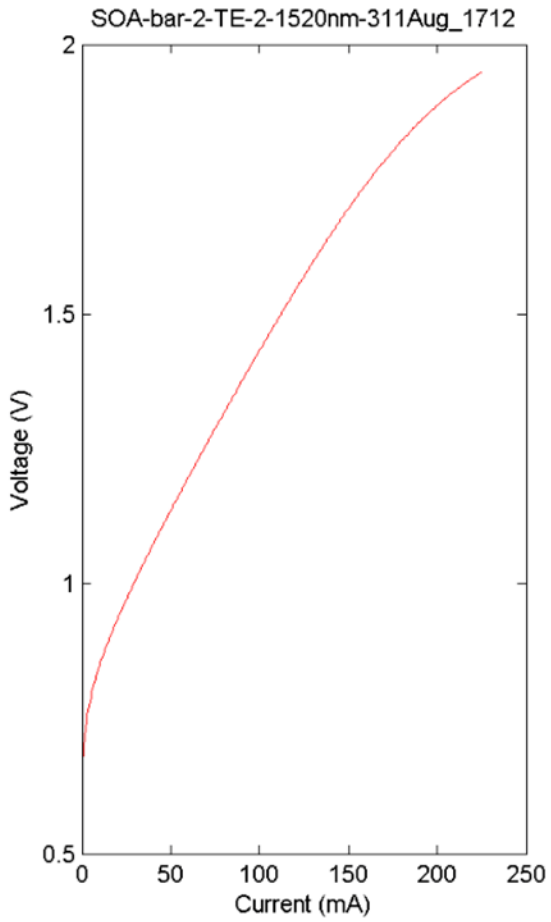
Electrical characterisation of OXS chip

Smooth V-I curve indicates the good current injection and diode junction design, matching the simulation result.



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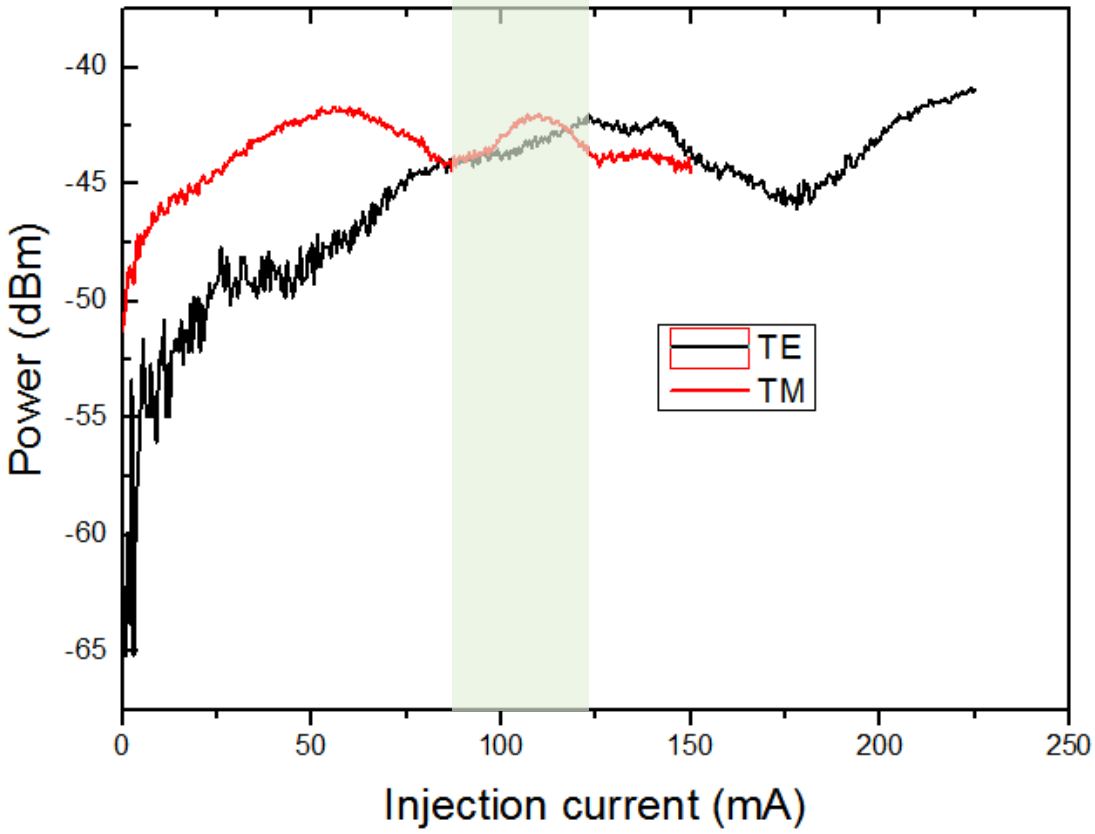
Comparison between TE and TM switching

At λ=1520 nm



Polarisation independent switching (PDL< 1 dB) could be realized with injection current ranging from 80 mA to 120 mA at λ=1520 nm

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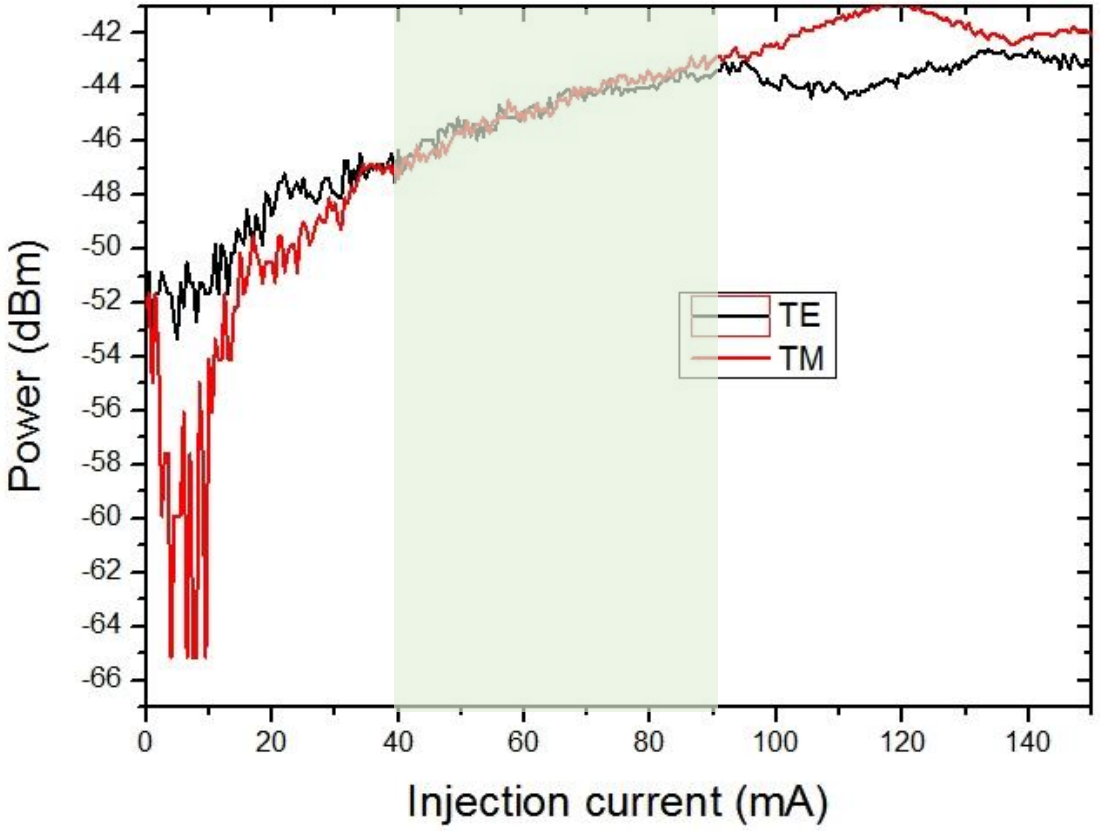
Comparison between TE and TM switching

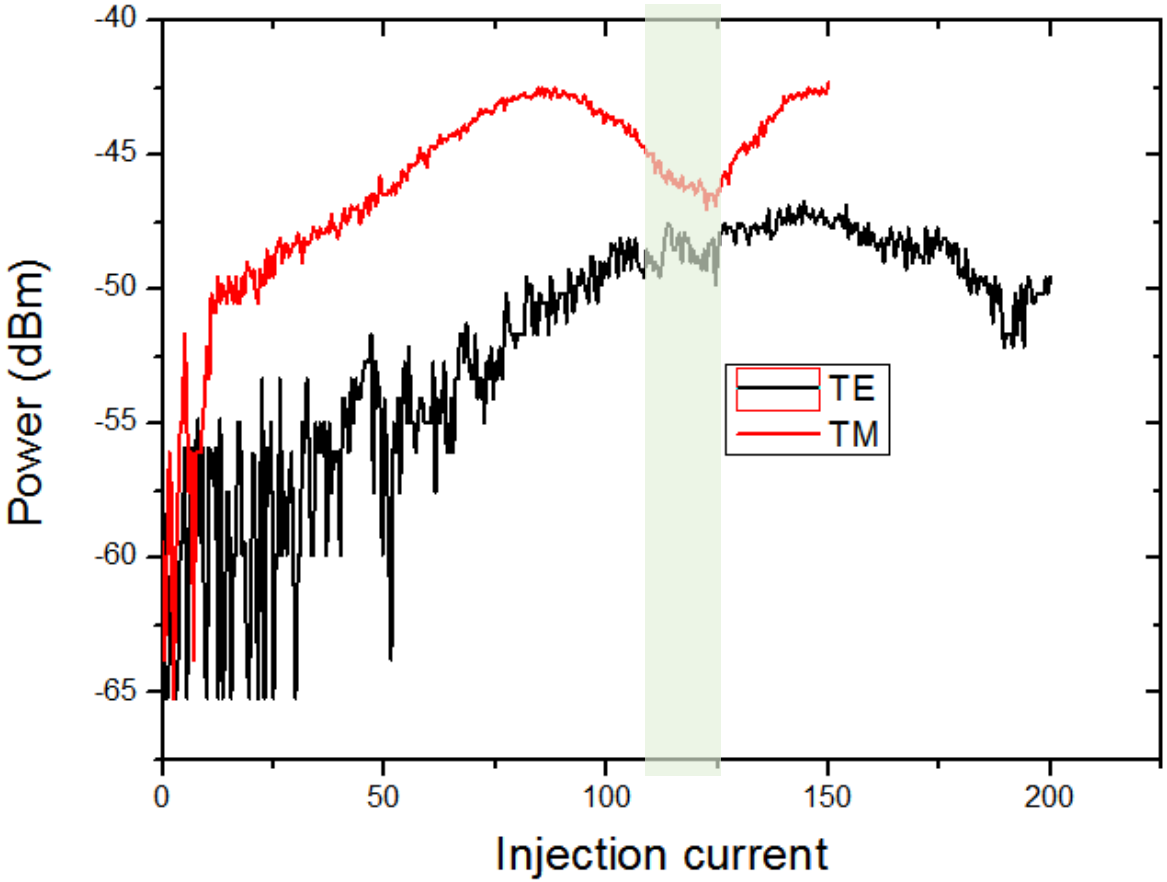
At 1540 nm



Polarisation independent switching (PDL< 1 dB) could be realized with injection current ranging from 40 mA to 90 mA at λ=1540 nm

Comparison between TE and TM switching

At λ=1565nm



Polarisation independent switching (PDL~ 2 dB) could be realized with injection current ranging from 80 mA to 120 mA at λ=1560 nm

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Conclusions

- D2.1 provides a summary of the demonstration that the integration of OpenFlow software with the driver circuit successfully controls the OXS. That report does not go into details of the chip and jigging issues addressed in order to provide that demonstration.
- This Appendix provides confidential technical background to that deliverable report.
- In addition the Appendix provides data to show that the electrical and optical results from the switch characterisation exhibit very encouraging optical performance metrics across the C-Band. These include polarisation independent switching to within a very few dB to better than 40 dB.
- Fast switching characterisation is planned to be demonstrated in the next few months with the completion of the follow-up wafer.
- After this there will be a substantial review of the data set before committing new materials into processing further development switches.