IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Workpackage Report for Year 4

Jointly-executed Programme of Integrating Activities (JPIA) Report

With input from all clusters.

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Policy Objective (abstract)

Each ArtistDesign research activity has work within both the JPIA and the JPRA workpackages. The JPIA activities are carried out on a global, NoE level, transcending the clusters. They form the supporting background for integration of the NoE, and are executed in phase and in interplay with the JPRA research activities. For instance, funds for staff mobility will be allocated taking into account the needs for research.

The activities listed here will promote integration of geographically dispersed teams. All these activities will have long-lasting effects, well beyond the duration of the initial EC funding.

These activities include Joint Technical Meetings, Staff Mobility and Exchanges, Tools and Platforms.

Versions

number	comment	date
1.0	First version delivered to the reviewers	February 1st 2012

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1. Overview of the Workpackage

1.1 ArtistDesign Participants and Affiliated Partners

Each ArtistDesign research activity contributes to achieving both research and integration goals. Thus, each has work within both the JPIA and the JPRA workpackages, and all partners and affiliated partners participate in the Joint Programme of Integration Activities.

1.2 Starting Date, and Expected Ending Date

These activities are intimately related to the JPRA (Joint Programme of Research Activities) and run for the entire duration of the NoE.

1.3 Policy Objective

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-- Changes wrt Y3 deliverable --

No changes to the above text with respect to Year 3.

2. Joint Technical Meetings

Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

They are often organized around the annual General Assembly and Review, or around some of the main conferences in the area (most of which are piloted by a majority of ArtistDesign partners).

Depending on the context and in particular on the maturity of the topics under discussion, these Joint Technical Meetings may be open to the public, or by invitation (which implicitly includes all interested ArtistDesign partners).

-- All new text: this entire chapter pertains only to activity in Year 4.--

2.1 Modelling and Validation cluster

Conferences Organised

Conference: The European Conference on Computer Systems (EuroSys 2011), University of Salzburg, Salzburg, Austria
10-13 April 2011
The EuroSys conference series brings together professionals from academia and industry. It has a strong focus on systems research and development: operating systems, data base systems, real-time systems and middleware for networked, distributed, parallel, or embedded computing systems. EuroSys has become a premier forum for discussing various issues of systems software research and development, including implications related to hardware and applications.
EuroSys 2011 followed the pattern established by the previous EuroSys conferences, by seeking papers on all aspects of computer systems. EuroSys 2011 also included a number of workshops to allow junior and senior members of the systems community to explore leading-edge topics and ideas before they are presented at a conference.
The general chair was Christoph Kirsch from the University of Salzburg.
http://eurosys2011.cs.uni-salzburg.at

Conference: ACM/IEEE Ninth International Conference on Formal Methods and Models for Codesign (Memodode 2011)
Verimag has co-chaired this conference which had taken place in Cambridge. Memocode attracts researchers and practitioners who create methods, tools, and architectures for the design of hardware/software systems. These systems face increasing design complexity including tighter constraints on timing, power, costs, and reliability.
http://www.memocode-conference.com

Conference: The 6th IEEE International Symposium on Industrial Embedded Systems (SIES 2011), Mälardalen University, Västerås, Sweden.
June 15-17, 2011.
TRENTO has co-chaired this conference, which is concerned with all aspects related to modelling and developing embedded systems, with particular emphasis on their application in

a variety of industrial environments. The considered applications range from SoCs, which are making inroads in to the area of industrial automation, to automotive and safety-critical systems.
In particular, at this year conference, TRENTO and IST-Austria have organized a special session dedicated to various aspect of robust design with a keynote speech by Jean-François Raskin on the Synthesis of Robust Controller and Games With Imperfect Information, and a set of three invited papers on specification, control and design methodologies.

Conference: 9th International Conference on Formal Modeling and Analysis of Timed Systems, FORMATS 2011, Phønix Hotel, Aalborg, Denmark, 21-23 September 2011 http://formats2011.cs.aau.dk/

Timing aspects of systems from a variety of computer science domains have been treated independently by different communities. Researchers interested in semantics, verification and performance analysis study models such as timed automata and timed Petri nets, the digital design community focusses on propagation and switching delays, while designers of embedded controllers have to take account of the time taken by controllers to compute their responses after sampling the environment.

Organizers: Alexandre David, Kim G Larsen, Claus Thrane, Rikke W. Uhrenholt

Workshop Organizations

3rd Workshop on Games for Design, Verification and Synthesis.

Co-located with CONCUR'11, Aachen (Germany), 10 September 2011

http://www.lsv.ens-cachan.fr/Events/gasics10/

The aim of this workshop was to bring together researchers working on game-related subjects, and to discuss on various aspects of game theory in the fields where it is applied. The workshop was composed of two invited talks, together with contributed talks on the following (non-exhaustive) list of relevant topics:

- Adapted notions of games for synthesis of complex interactive computational systems
- Games played on complex and infinite graphs
- Games with quantitative objectives
- Game ith incomplete information and over dynamic structures
- Heuristics for efficient game solving.

Organizers: Kim G. Larsen, Nicolas Markey, Jean-François Raskin, Wolfgang Thomas.

INRIA Rennes Gipsy Workshop on Games, Logic and Security in Nov. 2011 (http://www.irisa.fr/prive/pinchina/GIPSy/gipsy11.html).

Workshop: Design framework -- concept and tool
Hristina Moneva, Teade Punter, Roelof Hamberg – ESI workshop for industry with participation from companies Océ, ASML, Philips Healthcare, and Vanderlande, Eindhoven, the Netherlands, November 11, 2011

Workshop: A Design Framework for Model-based Development of Complex Systems Hristina Moneva, Roelof Hamberg, Teade Punter – AVICPS (Analytic Virtual Integration of Cyber-Physical Systems Workshop), Vienna, Austria, November 29, 2011

Workshop: Synchron Workshop 2010 and 2011
INRIA organized through its Aoste team the 17th edition of Synchron in Frejus. The seminar is a rather informal event, of one-week duration, meant to gather international experts together with junior researchers and PhD/postdoc students in a studious while festive atmosphere. Days are given to formal presentations, and evenings may be spent in further talks and informal demos. In 2010 the Synchron seminar attracted over 50 participants, and acknowledged the active support of Artist-Design. The 2011 edition of Synchron has been hold in Fontainebleau in December 2011
http://www.artist-embedded.org/artist/Synchron-2010,2206.html

Workshop: ACESMB 2011, 4th International Workshop on Model Based Architecting and Construction of Embedded Systems
October 18th, 2011, Wellington (New-Zealand, held in conjunction with MoDELS 2011) .
The objective of this workshop was to bring together researchers and practitioners interested in model-based software engineering for real-time embedded systems. Contributions related to this subject at different levels, and ranged from modelling languages and semantics to concrete application experiments, from model analysis techniques to model-based implementation and deployment. Due to the criticality of the application domain, a particular focus was on model-based approaches yielding efficient and provably correct designs.
http://www.artist-embedded.org/artist/Overview,2337.html

Workshop: UML&FM'2011, Fourth IEEE International workshop UML and Formal Methods
June 20th, 2011, Lero, Limerick, Ireland (held in conjunction with FM 2011)
For more than a decade now, the two communities of UML and formal methods have been working together to produce a simultaneously practical (via UML) and rigorous (via formal methods) approach to software engineering. UML is the de facto standard for modelling various aspects of software systems in both industry and academia, despite the inconvenience that its current specification is complex and its syntax imprecise. The fact that the UML semantics is too informal have led many researchers to formalize it with all kinds of existing formal languages, like OCL, Z, B, CSP, VDM, Petri Nets, UPPAAL, HOL, Coq, PVS etc. This fourth workshop was meant to be open to various subjects as the main objective was to encourage new initiatives of building bridges between informal, semi-formal and formal notations.

http://www.artist-embedded.org/artist/Overview,2271.html

Workshop: UML&AADL'2011, Sixth IEEE International workshop UML and AADL

April 27th, 2011, Las Vegas, USA (in conjunction with ICECCS 2011)
New real-time systems have increasingly complex architectures because of the intricacy of the multiple interdependent features they have to manage. They must meet new requirements of reusability, interoperability, flexibility and portability. These new dimensions favour the use of an architecture description language that offers a global vision of the system, and which is particularly suitable for handling real-time characteristics. Due to the even more increased complexity of distributed, real-time and embedded systems (DRE), the need for a model-driven approach is more obvious in this domain than in monolithic RT systems. The purpose of this workshop was to provide an opportunity to gather researchers and industrial practitioners to survey existing efforts related to behaviour modelling and model-based analysis of DRE systems.
http://www.artist-embedded.org/artist/Overview,2195.html

Workshop: Rigorous Embedded Design 2011 organised and funded by ARTIST

April 10th, 2011 Salzburg, Austria (within EuroSys 2011)

The objective of this workshop organised by VERIMAG was to discuss new methodologies for the rigorous design of embedded systems. Through a series of invited talks, the workshop surveyed some of the challenges and emerging approaches in the area. A series of design flows have been presented. The workshop mainly discussed performance analysis, correctness (high confidence and security), code generation, and modelling aspects (including timed scheduling and software/hardware interactions). Those concepts are illustrated with examples coming from the aeronautic, automotive, and robotic areas. Interactions between industrials and academic researchers have been facilitated through a series of open discussion sessions.

http://www.artist-embedded.org/artist/Programm,2288.html

Workshop: VVPS. Verification and Validation of Planning and Scheduling Systems organised and funded by ARTIST

June 13, 2011, Freiburg, Germany (within ICAPS)

The VVPS workshop organised by VERIMAG aimed at enhancing a stable forum on relevant topics connected to contaminations between V&V and P&S. The workshop intended to deepen the debate on relevant aspects of interactions between V&V methods and P&S-based systems. It investigated new solutions and identified open issues.

Workshop: ICES Seminar: Formalisms for Description and Visualization of Embedded Systems Architectures – Current State of Practice, Needs and Research Topics

Stockholm, Sweden, April 12th, 2010

This ArtistDesign workshop was carried out as part of CPS Week at KTH, 12 April 2010, with approx. 50 participants from industry and academia.

http://www.artist-embedded.org/artist/Overview,1937.html

Workshop: TiMoBD, Time Analysis and Model-Based Design, from Functional Models to Distributed Deployments

ESWeek, Taiwan, October 9-14, 2011

Model-based and Model-driven design flows are very popular in the industry because of the possibility of analysis and verification by simulation or model checking and because of the availability of automatic code generation tools that provide a path to implementation. However, in most flows, the timing behavior of the system depends on features of the computation and communication architecture that are modelled late or not modelled at all, bringing the possibility for an inappropriate selection of the computing platform (over- or underperforming) and possibly an incorrect software implementation of the functional model. To this end, timing analysis techniques can provide support for the analysis of architecture solutions and system configurations and also define analytical methods for the synthesis of feasible/correct solutions. Hence, there is a need for a better integration of timing analysis technologies, methods and tools in model-based and model-driven flows. The workshop attempted at bridging the gap between the three communities of model-based design, real-time analysis and model-driven development, for a better understanding of the ways in which new development flows that go from system-level modelling to the correct and predictable generation of a distributed implementation can be constructed leveraging current and future research results.

Workshop Green and Smart Embedded System Technology: Infrastructures, Methods and Tools at the Cyber-Physical System Week

Stockholm, Sweden, April 12th, 2010

Organizing committee, general chairs: Alberto Sangiovanni Vincentelli, Huascar Espinoza, Marco Di Natale, Roberto Passerone

Efficient production, transmission, distribution and use of energy are fundamental requirements for our modern society and the challenge of a green, low carbon economy. Embedded systems have an important role to play in increasing the energy efficiency and in reducing carbon emissions to sustainable growth. Indeed, most systems for monitoring and control of energy production, distribution and use are today interconnected and controlled by embedded devices, in areas such as industrial manufacturing, transportation systems, building automation, domestic appliances and more. This offers the opportunity for the creation of new integrated systems offering new products, processes and services with greater efficiency and better situation awareness to end-users and service and infrastructure owners.

http://www.artist-embedded.org/artist/Overview,1928.html

PhD School ARTIST Quantitative Model Checking Winter School 2012.

IT University, Copenhagen, Denmark, February 27th – March 1st, 2012.

Opgazing committee: Kim G. Larsen, Axel Legay and Andrzej Wąsowski (program co-chairs), Louis-Marie Traonouez and Fabrizio Biondi (local organizers).

The PhD school on quantivative model checking, QMC 2012, is organized by the European Network of Excellence ARTIST Design, the Danish VKR Center of Excellence MT-LAB and the IDEA4CPS research centre and takes place at the IT University Copenhagen from the 27 of February to the 1st of March 2012. It features lectures and other activities by world-renowned experts within the areas of real-time, probabilistic, and hybrid model checking.

Keynotes and Invited talks

Keynote: Twan Basten
The disappearing computer
Devlab Café, Development Laboratories, Eindhoven, the Netherlands, 29 April 2011

Keynote: Jeroen Voeten
Performance prediction and optimization for Wafer Scanners
Dutch Model Checking Day 2011, Delft, the Netherlands, 17 June 2011

Keynote: Jozef Hooman
Using a Commercial Model Checker at Philips Healthcare
System Validation seminar, University of Twente, the Netherlands, 23 May 2011

Keynote: Jozef Hooman
Compositional Model Checking using Verum's ASD:Suite at Philips Healthcare
MBSD seminar, Radboud University, Nijmegen, the Netherlands, 1 July 2011

Keynote: Jozef Hooman
Experiences with a Compositional Model Checker in the Healthcare Domain
International Symposium on Foundations of Health Information Engineering and Systems (FHIES 2011), Johannesburg, South Africa, 30 August 2011

Keynote: *Sara Tucci*
AUTOSAR Timing Extension and a Case Study for Schedulability Analysis
ArtistDesign Workshop on Real-Time System Models for Schedulability analysis University of Cantabria 7-8 February 2011

Keynote: *Sara Tucci*
Applying Model Driven Engineering to RTES: Technologies, Standards and Experiences
ES-week Workshop on Time Analysis and Model-Based Design, from Functional Models to Distributed Deployments, Taipei, 2011

Keynote: *Wang Yi*
The Digraph Real-Time Task Model, invited talk, Workshop on Rigorous Embedded Design 2011, April 10th, 2011, Salzburg, Austria (within EuroSys 2011).

Keynote Lecture*: Thomas A. Henzinger*
Computational Science versus Computer Science, Ninth Basel Computational Biology Conference (BC2), Basel, Switzerland, June 2011.

Keynote Lecture*: Joseph Sifakis*
Trustworthy Software Systems, int conf on Sensornetworks Sensornets February 2012, Rome

Keynote Lecture*: Joseph Sifakis*
Rigorous System Design*, VLSI-SoC, October 3–5, 2011, Hong Kong, China*

Keynote Lecture*: Joseph Sifakis*
Methods and tools for component-based system design, DATE 2011, Grenoble

Key Note*: The Major Challenges of the EDA Industry in the Next 5 Years*
Tel Aviv, May 3, 2011
Alberto Sangiovanni Vincentelli gave the key note address at the Israel Executive Forum addressing the future directions of the EDA industry.
http://www.israelexecutiveforum.com/agenda.aspx

Key Note*: 1,000 Electronic Devices Per Living Person: Dream Or Nightmare?, 4th IEEE International Workshop on Advances in Sensors and Interfaces*
Borgo Egnazia, June 9th, 2011
Alberto Sangiovanni Vincentelli gave the opening key note talking about the potential offered by the myriad of sensors, controller and actuators that will be soon available.
http://iwasi2011.poliba.it/programme.html

Key Note*: 1000 electronic devices per person, dream or nightmare, International Electronic Forum, Future Horizon*
Seville, October 7th, 2011
Alberto Sangiovanni Vincentelli delivered this talk to an audience consisting of CEO, COO and CTO of the semiconductor industry.

***Key Note**: Application Driven Design – New Directions Require New Tools!*
Tel Aviv, May 4, 2011
Alberto Sangiovanni Vincentelli gave the key note at this conference stressing the need for new tools for system level design. He was awarded at the Conference with the ChipEx Award for exceptional contribution to the semiconductor industry delivered by the Science and Technology Minister of Israel Professor Daniel Hershkovitz (see picture below).

Key Note: DAC Workshop
San Diego, June 5th, 2011
Alberto Sangiovanni Vincentelli chaired and gave the opening key note talk at the DAC Workshop on Intra and Inter-Vehicle Networking.

Key Note and Workshop: DAC Workshop on Design Analysis and Implementation of Real-Time Systems with Time-Triggered and Event-Triggered Applications
San Diego, June 5th , 2011
Alberto Sangiovanni Vincentelli chaired and presented the Key Note opening address

***Invited Lecture*:**
Haifa, March 8, 2011
Alberto Sangiovanni Vincentelli gave a distinguished seminar talk at Haifa IBM Research attended by all researchers on System and Contract-Based Design.

Invited Lecture:
Lausanne, March 11, 2011
Alberto Sangiovanni Vincentelli gave a distinguished seminar series talk on Interconnect Everywhere at EPFL.

Invited Lecture:
Rome April 28, 2011
Alberto Sangiovanni Vincentelli gave a *lectio magistralis* (500 people attending) at the University of Rome on Innovation, Funding New Enterprise and the Importance of a Rich Ecosystem.

Lectio Magistralis: What is Important in the Design of Systems
Politecnico di Bari, December 2nd , 2011
Alberto Sangiovanni Vincentelli delivered the Lectio Magistralis at the Commencement of Politecnico di Bari about the importance of research in and teaching of system design.

***Invited Lecture:** Christoph Kirsch,*
Virtualizing Time, Space, and Power for Cyber-Physical Cloud Computing, ARTIST Workshop on Rigorous Embedded Design, Salzburg, Austria, April 2011.

Invited Lecture: Thomas A. Henzinger,
From Boolean to Quantitative Synthesis, Eleventh Annual Conference on Embedded Software (EMSOFT), Taipei, Taiwan, October 2011.

Invited Lecture: Thomas A. Henzinger
Ten Years of Interface Automata, ACM SIGSOFT Impact Paper Award Lecture, 19th Annual Symposium on Foundations of Software Engineering (FSE), Szeged, Hungary, September 2001.

Invited Lecture: Thomas A. Henzinger
Quantitative Reactive Models, Workshop on Synthesis, Verification, and Analysis of Rich Models (SVARM), Saarbrucken, Germany, April 2011.

Invited Lecture: Thomas A. Henzinger
Formal Methods for Composing Systems, Design Automation and Test in Europe (DATE),Grenoble, France, March 2011.

Invited Lecture: Christoph Kirsch,
Virtualizing Time, Space, and Power for Cyber-Physical Cloud Computing, ARTIST Workshop on Rigorous Embedded Design, Salzburg, Austria, April 2011.

Invited talk: Kim G Larsen
RED, Rigorous Embedded Systems, Salzburg, Austria, April 10, 2011. www.artist-embedded.org/artist/Programm,2288.html/

Invited talk: Kim G Larsen
The 9th International Workshop on Java Technologies for Real-time and Embedded Systems - JTRES 2011, York 26-28 October 2011. Timing and Performance Analysis of Embedded Software Systems Using Model Checking.

Invited talk, Kim G Larsen
PDMC, 10th International Workshop on Parallel and Distributed Methods in verifiCation, July 14, 2011, Cliff Lodge, Snowbird, Utah.
www.pdmc.cz/PDMC11

Invited talk, Kim G Larsen
iWIGP, International Workshop on Interaction, Games and Protocols, Saarbrücken, Germany, March 27, 2011.
www.etaps.org/programme/76-programmeiwigp

Invited talk, Kim G Larsen
ROCKS, Rigorous Dependability Analysis using Model Checking Techniques for Stochastic Systems, Workshop, March 26, Saarbrücken, 2011. www.etaps.org/programme/66-programmerocks/

Invited talk, Kim G Larsen
World Conference, Development Tools Sessions, Nürnberg, March 3, 2011.

Invited Lecture: Christoph Kirsch,
Virtualizing Time, Space, and Power for Cyber-Physical Cloud Computing, ARTIST Workshop on Rigorous Embedded Design, Salzburg, Austria, April 2011.

Invited talk, Kim G Larsen
De 17e Nederlandse Testdag, 29 November 2011. University of Twente, Enschede, The Netherland.

Tutorials and Panels

Panelist: *Christoph Kirsch,*
Vehicular Wireless Networks: What should the future hold? International Symposium on Wireless Vehicular Communications (WiVeC), San Francisco, California, September 2011.

Invited Panelist: Kim G. Larsen
Microsoft Software Summit , Paris, France, April 14, 2011, research.microsoft.com/en-us/events/ss2011

Invited Lecture: Kim G. Larsen
ARTIST Summer School in China, IOS/ISCAS, Beijing, August 8-12, 2011.
www.artist-embedded.org/artist/Overview,2239.html

Invited Lecture: Kim G. Larsen
ARTIST Summer School, Aix-les-Bains, France, September 4-9, 2011

Tutorial: Twan Basten
Designing Next-Generation Real-Time Streaming Systems.
9th IEEE/ACM International Conference on Hardware/Software-Codesign and System Synthesis, CODES+ISSS 2011. Embedded Systems Week. Taipei, Taiwan, October 9, 2011.
http://esweek.acm.org/ and http://www.es.ele.tue.nl/~sander/tutorials/esweek-2011/.

Summer School Speaker: *Christoph Kirsch*
Virtualizing Time, Space, and Power for Cyber-Physical Cloud Computing, Georgia Tech Summer School on Cyber-Physical Systems, Atlanta, Georgia, USA, June, 2011.

Tutorial Speaker: *Christoph Kirsch*
The Logical Execution Time Paradigm, Tutorials on Time-Predictable and Composable Architectures for Dependable Embedded Systems, ESWEEK, Taipei, Taiwan, October 2011.

Invited Tutorial: Thomas A. Henzinger
Applications of Games in Quantitative Verification and Synthesis, invited tutorial, Annual GAMES Workshop, Paris, France, September 2011.

-- The above is new material, not present in the Y3 deliverable --

2.2 SW Synthesis, Code Generation and Timing Analysis cluster

Course: Retargetable Compilation

Lugano, Switzerland, Feb. 16-19 & Feb 23-25, 2011

Objectives: Spreading excellence in memory-architecture aware compilation and processor retargetability beyond ArtistDesign partners.
Presenters: Peter Marwedel (TU Dortmund), Heiko Falk (TU Dortmund), Rainer Leupers (RWTH Aachen)
Other participants: about 20 students
Conclusion: The new format (extended even if compared to 2010) turned out to be very useful.
http://www.alari.ch

Tutorial: Mnemee design flow: a framework for memory management and optimization of static and dynamic data in MPSoC system

ARCS 2011, Lake Como, Italy, February 22, 2011

Speakers: P. Marwedel, D. Soudris. S. Stuijk, A. Mallik, D. Cordes, S. Collet, D. Kritharidis
This tutorial addressed the Mnemee tool flow that performs source-to-source transformations to automatically optimize the original source code and map it on the target platform. The optimizations aim at reducing the number of memory accesses and the required memory storage of both dynamically and statically allocated data. Moreover the Mnemee tool flow performs optimal assignment of all data on the memory hierarchy of the target platform.

Tutorial: MPSoC hardware/software architectural and design challenges/solutions

DATE 2011, Grenoble, France, March 15th, 2011

Speakers: G. Vanmeerbeeck, K. Tiensyrja, A. Jantsch, D. Soudris, B. Candaele

Mapping software onto multi-processor platforms requires efficient parallel programming techniques while achieving non-functional requirements. The fundamentals, design steps and alternative programming models to implement such embedded applications onto multi-cores were discussed in the tutorial. The need to accommodate a large number of applications on these massively parallel computing platforms requires the system engineer to quickly evaluate the performances of application mappings. The tutorial reviewed mainstream evaluation techniques based on simulation, abstract workload and processing capacity models. On-chip and in-package memory organization and efficient data management are key to high performance. The tutorial reviewed various memory architectures and techniques to address space management, cache coherency, memory consistency, and dynamic application specific memory allocation techniques.

Industrial Workshop Bringing Theory to Practice: Performance and Predictability in Embedded Systems,

Grenoble, France, March 18, 2011

Philipp Lucas, Lothar Thiele, Benoit Triquet, Theo Ungerer, Reinhard Wilhelm

The PPES workshop was concerned with critical hard real-time systems that have to satisfy both efficiency and predictability requirements. For example, an electronic controller for a safety-critical system in an automobile needs to react not only correctly to external inputs such as rapid deceleration or loss of grip, but also provably within a given time-span. This topic of reconciling predictability and performance has received much interest in recent years, in particular considering its growing relevance and complexity with the advent of multi-core systems with shared resources.

Workshop: Software & Compilers for Embedded Systems (SCOPES) 2011

St. Goar, Germany – June 27-28, 2011

Objectives for the meeting: SCOPES focuses on the software generation process for embedded systems.
Organizer: Sander Stuijk, Henk Corporaal (TU Eindhoven)
Conclusions: One of the conclusions was to further integrate the MAP2MPSoC and SCOPES workshops in 2011.

http://www.scopesconf.org/scopes-11

Meeting: 4th Workshop on Mapping Applications to MPSoCs, 2011

St. Goar, Germany – June 28-29, 2011

Objectives for the meeting: This is the flagship workshop of this cluster. The goal of this workshop is to establish links between leading researchers in the area and to stimulate advanced research. Consistent with recommendations of the reviewers, this workshop included presenters from other cluster as well, for example from ETH Zürich and TU Denmark. In this way, the inter-cluster coordination concerning MPSoCs took place.
Organizer: Peter Marwedel (TU Dortmund)
Other participants: About 50
Conclusions: We are reaching out far beyond the ArtistDesign network. The workshop is now a key forum for discussions in this area. Attendees expressed their strong interest to continue this series of informal workshops as a platform for discussions.

http://www.artist-embedded.org/artist/Program,2298.html

Workshop: 11th International Workshop on Worst-Case Execution Time Analysis, 2011

Porto, Portugal – July 5th, 2011, in connection with ECRTS 2011

Objectives for the meeting: To present and discuss recent work in WCET analysis of all kinds of systems by static or dynamic methods.
Organizers: Chair: Chris Healy (Furman University), Steering Committee: Peter Puschner (TU Vienna), Jan Gustafsson (MDH), Guillem Bernat (Rapita)
Other participants: About 35
Conclusions: this year's workshop had several contributions addressing the industrial fitness and certification issues in WCET analysis, as well as coding and compiler support and timing analysis, in addition to the more traditional timing analysis topics. As a highlight the workshop featured an invited talk by Francisco Cazorla from Barcelona Supercomputing Center, on hardware support for composable critical real-time embedded systems. Earlier workshops have featured invited talks from ETH Zürich, and Linköping University, thus fostering inter-cluster communication.

http://www.artist-embedded.org/artist/-WCET-2011-.html.

Keynote: Energy-Efficient Embedded Computing
Energy-Aware Computing (EACO) Workshop
Bristol, United Kingdom – July 13-14, 2011

P. Marwedel presented an overview of his group's work on energy models for embedded software, on the life cycle analysis of computing devices and on optimizations for scratch pad memory and GPUs.
http://www.cs.bris.ac.uk/Research/Micro/eaco-2.jsp

Tutorial: Embedded System Foundations of Cyber-Physical Systems
ARTIST Summer School in China 2011
Beijing, China – August 8-12, 2011

P. Marwedel started the summer school with a full-day tutorial on foundations of cyber-physical systems. He introduced the fundamentals of modeling, embedded system hardware,

evaluations of embedded systems and the mapping of applications to platforms. Also, he gave a brief introduction to compilation for explicit memory architectures. The tutorial was based on the second edition of the presenter's textbook on embedded systems. The tutorial made sure that the attendees were aware of the prerequisites of the remaining presentations of the summer school.
http://www.artist-embedded.org/artist/Overview,2239.html

Workshop: 1st MAPS User Group Workshop (MUG 2011)

Aachen, Germany – September 28-29, 2011

On Sep 28-29, 2011, ICE organized the 1st MAPS User Group Workshop (MUG 2011) in the UMIC research center in Aachen. MAPS is a programming tool suite for heterogeneous multicore architectures that has been developed in the context of the UMIC cluster. It uses both sequential C and a C language extension (CPN) for describing applications in the form of process networks, and it performs optimized temporal and spatial task-to-processor mapping for embedded MPSoC platforms. MUG 2011 attracted more than 20 participants from 15 international companies. The workshop covered an introduction to the MAPS programming model, task mapping and scheduling techniques, C code partitioning and various demonstrations. Moreover, the participants had lots of opportunities for hands-on work with the MAPS tools. MUG 2011 was very well received and provided many new contacts and valuable practical feedback to the MAPS team for its future roadmap.

http://www.ice.rwth-aachen.de/news/news-detail/browse/seite-2/angebote/1st-maps-user-group-workshop-mug-2011//185/

Workshop: 7th Workshop on Embedded Systems Education, 2011

Taipei, Taiwan – October 13th, 2011

Embedded system education is still a very young area and frequently restricted to teaching the details of microcontroller programming. A long-term objective of this workshop is to improve the visibility of work in the area and to stimulate the introduction of broader curricula. In 2011, P. Marwedel was again the main organizer of the workshop.

http://www.artist-embedded.org/artist/Topics-and-Focus,2305.htm

Workshop: 3rd Workshop on Software Synthesis, 2011

Taipei, Taiwan – October 14th, 2011

An increasing amount of software is not written manually any more. Rather, software is synthesized from abstract models of the required functionality. Software synthesis has been implemented in various disperse communities. The workshop aimed at bringing these communities together. Presenters at this workshop presented industrial as well as academic results. Top-level experts from different areas presented at the workshop. S. Bhattacharyya presented results of his work on synthesis from dataflow graphs. K. Ravindran (National Instruments) talked about the path from streaming models to software and hardware implementations. M. di Natale (SSSA, Pisa) described the deployment of real-time functions in automotive systems. R. Alur (University of Pennsylvania) demonstrated results in the area of software synthesis for control applications. N. Halbwachs (IMAG) gave an overview over code generation for synchronous languages. Experts expressed their strong interest in continuing this workshop in 2012. Also, Ted Baker (National Science Foundation, NSF) expressed the interest of his organization. We are planning to run the workshop also as part of ESWEEK 2012 in Tampere on Oct. 12th. The workshop was organized by P. Marwedel and A. Sangiovanni-Vincentelli and run by P. Marwedel.

http://www.artist-embedded.org/artist/Scope,2309.html

Tutorial: Energy modeling

Workshop of Collaborative research center SFB 876
Lüdenscheid, Germany, Oct. 20th, 2011
This tutorial by P. Marwedel demonstrated global trends on the energy consumption of computing and compared the advantages of measurement-based and model-based predictions of the energy consumption in computing. The potential of saving energy through an exploitation of the memory hierarchy was shown. The tutorial closed with an introduction to the life-cycle assessment (LCA) of the energy consumption of personal computers.
http://www.sfb876.tu-dortmund.de

Keynote: Parametric WCET Analysis
Nordic Workshop of Programming Theory
Västerås, Sweden– Oct 28, 2011
This keynote is described in the Timing Analysis activity report.

-- The above is new material, not present in the Y3 deliverable --

2.3 Operating Systems and Networks cluster

2.3.1 Meetings

Meeting: Cache-aware scheduling and timing analysis
City, Country: Aveiro, Portugal
Date: November 15, 2011
Objectives for the meeting: Understand how schedulability analysis and timing analysis tools can be integrated to properly select preemption points in the task code to reduce cache related overhead, stack usage and power consumption.
Organizer: Luis Almeida (University of Porto)
Other participants: Marko Bertogna (Pisa), Francesco Esposito (Pisa), Mauro Marinoni (Pisa), Christoph Cullmann (Absint), Martin Kaiser (Absint), Sebastian Altmeyer (USAAR), Claire Burguiere (USAAR), Jian-Jia Chen (ETHZ), Andreas Schranzhofer (ETHZ), Martino Ruggiero (University of Bologna), Paolo Burgio (University of Bologna).
Conclusions: A set of experiments were planned using the Erika kernel on the MPARM simulator to evaluate the effects of non-preemptive scheduling on cache behavior, stack usage and power consumption. A number of suggestions were identified to improve timing analysis to provide data cache and support and stack information for ARM7.

Meeting: Teaching how to do research to PhD students
City, Country: Pisa, Italy
Date: November 10-11, 2011
Objectives for the meeting: Understand how to teach PhD students how to approach research, write technical papers and make interesting presentations.
Organizer: Giorgio Buttazzo (Scuola Superiore Sant'Anna, Pisa), Gerhard Fohler (TUKL).
Conclusions: A program for a joint course to be given at both sites on 2012.

Meeting: Real-time support for multicore platforms
City, Country: Vienna*, Austria*
Date: December 1, 2011
Objectives for the meeting: Discuss how to extend advanced scheduling techniques and contract based virtualization to multicore platforms.
Organizer: Gerhard Fohler (TUKL).
Other participants: Giorgio Buttazzo (Pisa), Alan Burns (University of York), Luis Almeida (University of Porto), Eduardo Tovar (Polytechnic Institute of Porto).
Conclusions: Future research questions were identified to be worked on throughout the year, possibly leading to a joint project proposal.

Meeting: Workshop on Real-Time System Models for Schedulability Analysis
City, Country: Santander, Spain
Date: February 7-8, 2011
Objectives for the meeting: Present existing models of real-time systems, and propose extensions to fill the gaps that are required to cover state-of-the-art hardware platforms, operating systems, and scheduling techniques used in practice to develop real-time applications.

The cluster has also been quite active in disseminating the research results achieved in the context of the ArtistDesign network of excellence, as an overall strategy for reaching other research/academic/industrial communities with related interests.

2.3.2 Conferences and Workshops

Several scientific papers have been published and a number of workshops, and conferences have been organized by the cluster to spread the acquired knowledge in the scientific community. The conferences and workshops in which the cluster has been involved include:

1. RTAS 2011 - IEEE Real-Time and Embedded Technology and Applications Symposium, Chicago, Illinois, USA, April 12-14, 2011.
   URL: http://www.rtas.org/
2. RTSS 2011 - IEEE Real-Time Systems Symposium, Vienna (Austria), November 30th, - December 2nd 2011.
   URL: http://www.rtss.org/
3. ECRTS 2011 - Euromicro Conference on Real-Time Systems, Porto, Portugal, July 6-8, 2011.
   URL: http://ecrts11.ecrts.org
4. ETFA 2011 - IEEE International Conference on Emerging Technologies and Factory Automation, Toulouse, France, September 5-9, 2011.
   URL: http://www.etfa-2011.org/
5. RTCSA 2011 - IEEE International Conference on Embedded and Real-Time Computing Systems and Applications, Toyama, Japan, August 28-31, 2011.
   URL: http://www.jaist.ac.jp/rtcsa2011/
6. RTNS 2011 - International Conference on Real-Time and Network Systems, Nantes, France, September 29-30, 2011.
   URL: http://rtns2011.irccyn.ec-nantes.fr/
7. OSPERT 2011 – The 7th International Workshop on Operating Systems Platforms for Embedded Real-Time Applications, Porto, Portugal, July 5th, 2011.
   URL: http://www.seas.gwu.edu/~gparmer/ospert11/
8. WCET 2011 – The 11th International Workshop on Worst-Case Execution Time Analysis, Porto, Portugal, July 5th, 2011.
   URL: http://cs.furman.edu/~chealy/wcet2011/
9. RTN 2011 – The 10th International Workshop on Real-Time Networks, Porto, Portugal, July 5th, 2011.
   URL: http://www.rtn2011.org/
10. WATERS 2011 – 2nd International Workshop on Analysis Tools and Methodologies for Embedded and Real-time Systems, Porto, Portugal, July 5th, 2011.
    URL: http://retis.sssup.it/waters2011/
11. RTSOPS 2011: 2nd International Real-Time Scheduling Open Problems Seminar, Porto, Portugal, July 5th, 2011.
    URL: http://www.cs.wayne.edu/~fishern/Meetings/rtsops2011/
12. CPSWEEK 2011 – The 5th Cyber-Physical Systems Week, Chicago, Illinois, USA, April 12-14, 2011.
    URL: http://cpsweek2011.cs.illinois.edu/

13. APRES 2011: 3rd Workshop on Adaptive and Reconfigurable Embedded Systems, Chicago, Illinois, USA, April 11, 2011
    URL: http://apres2011.uwaterloo.ca/
14. ICCPS 2011: 2nd ACM/IEEE International Conference on Cyber-Physical Systems, Chicago, Illinois, USA, April 11, 2011.
    URL: http://precise.seas.upenn.edu/events/iccps11/
15. CRTS 2011 – 4th Workshop on Compositional Theory and Technology for Real-Time Embedded Systems, Vienna, Austria, November 29th, 2011.
    URL. http://www.rapitasystems.com/crts2011/
16. AVICPS 2011: 2nd International Workshop on Analytic Virtual Integration of Cyber-Physical Systems, Vienna, Austria, November 29th, 2011.
    URL: http://www.analyticintegration.org/
17. WCTT 2011: 1st International Workshop on Worst-case Traversal Time, Vienna, Austria, November 29th, 2011.
    URL: http://www.wctt.info/
18. SOMRES 2011: Workshop on Synthesis and Optimization Methods for Real-time Embedded Systems, Vienna, Austria, November 29th, 2011.
    URL: http://retis.sssup.it/synthesys/
19. RTSS@Work 2011: Real-Time SystemS at Work - Open Demo Session of Real-Time Techniques and Technologies, Vienna, Austria, November 29th, 2011.
    URL: http://webpages.cister.isep.ipp.pt/~smp/RTSS@Work/
20. DATE 2011 – Design, Automation & Test in Europe, Grenoble, France, March 14 – 18, 2011.
    URL: http://www.date-conference.com/
21. HSCC 2011: 14th ACM International Conference on Hybrid Systems: Computation and control, Chicago, Illinois, USA, April 12-14, 2011.
    URL: http://hscc2011.cs.sunysb.edu/
22. NeRES 2011: 2nd Workshop on Networks for Real-time Embedded Systems. Porto,Portugal, 10-11 November, 2011.
    URL: http://paginas.fe.up.pt/~ftt/neres2011/
23. MED 2011: The 19th Mediterranean Conference on Control and Automation, Corfu, Greece, June 20-23 2011.
    URL: http://www.med2011.org/
24. Special Track in INDIN 2011, IEEE 9th International Conference on Industrial Informatics, Caparica, Lisbon, Portugal, July 26-29, 2011.
    URL: http://www.uninova.pt/indin2011/home/home_i2011.php
25. Workshop on Real-Time System Models for Schedulability Analysis, University of Cantabria, Santander, Spain - February 7-8, 2011.
    URL: http://www.artist-embedded.org/artist/Introduction,2289.html
26. Ada Workshop (IRTAW-15), Liébana (Cantabria), Spain, September 2011.
    URL: http://www.artist-embedded.org/artist/IRTAW-15,2204.html

2.3.3 Courses and Seminars

- **Graduate Course on Combinatorial Optimization**
  Scuola Superiore Sant'Anna, Pisa, Italy – October-November 2011

  Objectives: The course covered several techniques of combinatorial optimization, namely complete methods such as Constraint Programming, Integer Linear Programming, Dynamic Programming and incomplete methods that go from simple local search to more sophisticated meta-heuristics. A final lecture on Hybrid Scheduling showed integrated methods for scheduling problems, in particular, allocation and scheduling of task graph applications on MPSoCs.

  Organizers: Giorgio Buttazzo (Scuola Superiore Sant'Anna), Michela Milano (Univ. of Bologna, Italy).

- **ARTIST Graduate Course on Real-Time Kernels for Microcontrollers**
  Scuola Superiore Sant'Anna, Pisa, Italy – June 13-17, 2011

  Objectives: The course was aimed at providing the fundamentals concepts of real-time computing systems, including scheduling, resource management and timing analysis; introducing the OSEK/VDX standards, taking as a reference implementation the Erika Enterprise kernel; showing how to apply such concepts in practice, with examples based on the Flex platform and the Microchip dsPIC DSC microcontrollers; teaching participants how to develop simple control applications using Erika Enterprise with code generation from functional models.

  Organizers: Giorgio Buttazzo (Scuola Superiore Sant'Anna), Pau Marti (Technical University of Catalonia, Barcelona, Spain), Ettore Ricciardi (ISTI-CNR, Pisa).

  URL: http://www.artist-embedded.org/artist/-ARTIST-Graduate-School-on-RT,1200-.html

- **Graduate Course on Android Framework**
  Scuola Superiore Sant'Anna, Pisa, Italy – November-December 2011

  Objectives: The course explained how to develop Android systems: from application bound entities, to the innovative (pseudo-)distributed IPC model, going through the key features of this framework; understanding how quality applications for Android should be developed. The framework analysis showed how an sample feature has been designed from the Java API down to the Android driver stub, enabling the student to extend the Android framework and to export its dedicated SDK.

  Organizers: Giorgio Buttazzo (Scuola Superiore Sant'Anna), Alberto Panizzo (Amarula Solutions, Italy).

- **Workshop on Real-Time System Models for Schedulability Analysis**
  University of Cantabria, Santander, Spain - February 7-8, 2011

  Objectives: Present existing models of real-time systems, and propose extensions to fill the gaps that are required to cover state-of-the-art hardware platforms, operating systems, and scheduling techniques used in practice to develop real-time applications.

  Organizers: Michael González Harbour (Universidad de Cantabria).

- **15th International Real-Time Ada Workshop (IRTAW-15)**
  Liébana (Cantabria), Spain, September 2011

  The 15th International Real-Time Ada Workshop (IRTAW-15) took place on September 14-16 of 2011 in Liébana (Cantabria), Spain. Since the late Eighties the International Real-Time Ada Workshop series has provided a forum for identifying issues with real-time system support in Ada and for exploring possible approaches and solutions, and has attracted participation from key members of the research, user, and implementer communities worldwide. Recent IRTAW meetings have significantly contributed to the Ada 2005 standard and to the proposals for Ada 2012, especially with respect to the tasking features, the real-time and high-integrity systems annexes, and the standardization of the Ravenscar profile. This particular meeting was organized by the University of Cantabria and received 22 participants from different countries in Europe and North America. The discussions were centred around multiprocessor real-time scheduling, multiprocessor resource control protocols, language profiles, application frameworks, and concurrency in Ada 2012. Some of the results of the workshop were submitted to the standardizaition bodies producing the Ada 2012 standard, and some others were captured in the proceedings to generate new work for future standardization phases.

  URL: http://www.artist-embedded.org/artist/IRTAW-15,2204.html

- **Participation in teaching activities in summer schools**
  - L. Almeida, Real-Time Communication for Embedded Systems, ArtistDesign Summer School in China 2011, Institute of Software – Chinese Academy of Sciences, Beijing, China, 6 hours lecture, 11-12 August 2011.
  - L. Almeida, Real-Time Systems Scheduling: Accessing Shared Resources / Message Scheduling on Networks / Challenges of Flexible Communication, Course at Universidad del Pays Vasco, Bilbao, Spain, 6h hours lectures, 3-4 May 2011.
  - L. Almeida, Real-Time Communication for Embedded Systems, Course at ENSIAS, Rabat, Morocco, 20 hours lectures, 19-21 December 2011.

2.3.4 Participation in Standards

Some cluster members are actively involved in the following standardization activities:

- UML Profile QoS and Fault Tolerance

  URL: http://www.artist-embedded.org/artist/UML-Profile-QoS-and-Fault.html
  Member: Miguel A. de Miguel, UP Madrid.

- Ada

  URL: http://www.artist-embedded.org/artist/UML-Profile-QoS-and-Fault.html
  Member: Alan Burns, Univ. of York.

- POSIX 1003

  In 2010, the POSIX.13 and POSIX.1d standards were reaffirmed. In addition, the process to revise these standards has been started. The scope of the revision is to align both standards with the current version of the POSIX.1 system services (2010 edition). Michael González is participating as a member of the working group, and is also the technical editor for both standards.

  URL: http://www.artist-embedded.org/artist/POSIX-IEEE-1003.html

Member: Michael Gonzalez Harbour, Univ. of Cantabria.

- MPEG Multimedia Middleware (M3W)

  URL: http://www.artist-embedded.org/artist/MPEG-Multimedia-Middleware-M3W.html

  Member: Alejandro Alonso, UP Madrid.

- TinyOS 15.4 and ZigBee Working Groups. Implementation of IEEE 802.15.4 and ZigBee on TinyOS

URL: http://www.open-ZB.net

URL: http://www.tinyos.net/

Participating group: CISTER-ISEP at Polytechnic Institute of Porto

- Lucia Lo Bello, from Univ. of Catania (affiliated to Pisa) is involved in standardization activities as Member of the International Electrotecnical Commission (IEC), Technical Committee SC65C, as member of Working Group 16, dealing with Wireless Industrial communication networks. Working Group 17, dealing with Coexistence in Wireless Industrial communication networks.
- Standardization effort was undertaken by the Scuola Superiore Sant'Anna of Pisa for including a new deadline-based reservation scheduler into the mainline Linux kernel. To achieve this goal, some core kernel developers, such as Thomas Gleixner (responsible for the i386 support) and Paul McKenney (responsible for the Read-Copy-Update synchronisation machinery into Linux), have been invited to fruitful technical meetings about the real-time support in the Linux kernel.

-- The above is new material, not present in the Y3 deliverable --

2.4 Hardware Platforms and MPSoC Design cluster

Meeting : MPSoC Cluster Meeting
Grenoble, France – March 2011
Objectives for the meeting: Status, plans and discussions for the cluster. The meeting was collocated with DATE 2011
Organizer: Jan Madsen (DTU)
Other participants: Most members of the cluster
Conclusions : Progress according to plans.

Meeting : 3-D NoC-based systems
EPFL and UNIBO had regular technical and update meetings along 2011, either via email or conference call in order to define short term actions and the future directions on the development of their synthesis tool for 3-D NoC-based systems.

-- The above is new material, not present in the Y3 deliverable --

2.5 Design for Adaptivity Transversal Activity

Meeting: TUKL
Kaiserslautern, May 10,11 2011
Continuation of the ACTORS resource management framework
Participants: ULUND, TUKL
Organizers, Gerhard Fohler, TUKL

Meeting: Ericsson
Kista, Sweden, Oct 6 2011
Discussions on joint project in adaptive resource management for telecommunication systems
Participants: ULUND, UIUC
Organizer: Johan Eker, Ericsson

Meeting: ULUND
Lund, Sweden, Nov 22. 2011
Continied discussions on joint project in adaptive resource management for telecommunication systems
Participants: Ericsson, UIUC
Organizer: Karl-Erik Årzén, ULUND

Workshop: APRES 2011, 3rd International Workshop on Adaptive and Recofigurable Embedded Systems. Within the CPSWEEK at Chicago, USA, 11 April, 2011.
The APRES series of workshops on adaptive and reconfigurable embedded systems with Luis Almeida (UPorto) amd Karl-Erik Årzén (ULUND) being members of the steering committee is one of the major events of this activity. The third workshop received 20 submissions including papers for oral presentations and abstracts for demos from which 9 papers were selected together with 4 demos. The workshop attracted 29 participants. The keynotes was given by Prof. John Knight of the University of Virginia, Charlottesville, USA.
URL: http://www.artist-embedded.org/artist/Overview,2331.html

Workshop: Joint LCCC and Artist Workshop on Control of Computing Systems, Lund, Sweden, Dec 5-7, 2011.
Objective: Performance and resource management in computing systems is increasingly important in everything from server systems in data centers to embedded systems. During recent years the use of feedback control techniques has attracted an increased attention both in academia and industry as a means for for realizing this. The objective of this workshop was to gather leading researchers in the field from both the control amd the computing communities and create an environment for cross-fertilization and new ideas.

Organizers:
- Karl-Erik Årzén, ULUND
- Tarek Abdelzaher, UIUC
- Anton Cervin, ULUND
- Anders Robertsson, ULUND
- Maria Kihl, ULUND

Participants: 55 participants including 27 invited speakers. In addition to the organizers several members of the cluster were represented and gave invited presentations incl, Luca Benini (UNIBO), Gerhard Fohler (TUKL), Enrico Bini (SSSA), Karl Henrik Johansson, Bo Wahlberg and Rolf Stadler (KTH), Johan Eker and Jimmie Håkansson (Ericsson). Industrial participation from IBM, Microsoft, Vm Ware, HP Labs, Advertising.com Group, in addition to Ericsson.

URL: http://www.lccc.lth.se/index.php?page=workshop-control-computing

Workshop: Reconfigurable and Communication-centric Systems-on-Chip (ReCoSoC), Montpellier, France, June 20-22, 2011
Leandro Soares Indrusiak, University of York was the program chair.

-- The above is new material, not present in the Y3 deliverable --

2.6 Integration Driven by Industrial Applications Transversal Activity

RECOMP Project

Within the RECOMP project, there are multiple joint technical meetings. The major ones were the General Assembly and Work Meetings in Helsinki (May 2011) and Porto (August 2011), where partners presented their achievements and discussed ongoing work on deliverables etc. The meetings are also used to foster collaborations between parnters.

Workshop: 4th Annual ICES Conference Stockholm,

Sweden, Sept. 1st , 2011

ICES 4th Annual Conference was entitled New Businesses based on Embedded Systems - How to Succeed!

80 people from industry and academia gathered together for this 1-day conference at Norra Latin, Stockholm, on 1st September 2011. The keynote of the conference was delivered by Charlotte Brogren head of VINNOVA – Sweden's Innovation Agency.

The conference opened with a look at different ways of entering the world of embedded systems, with speakers from Scania, ABB, Assa Abloy and InView sharing their experiences. Innovation and entrepreneurship are important aspects, all the way from education, as part of startups, but also, as in Sweden with many companies that have been around for a long time, inside such companies. The question is how to stimulate and promote innovation! This topic was discussed from different viewpoints and experiences were shared. Traditions/culture, education, legislation barriers and available funding are all important ingredients in creating an innovative climate.

For embedded systems, new business models play an important role.

Experiences and efforts in education at KTH that try to stimulate innovation and entrepreneurship were reported from the KTH ICTLabs (EIT KIC). T

The conference proved the value of the ICES network and the usefulness of bringing together entrepreneurs, companies, researchers and various supporting organizations was widely acknowledged. This year's Conference Exhbition also included examples of products and processes from ICES Member companies, ippi and KTH research groups, with demos and posters and a chance to talk.

Snapshots from ICES networking workshops during 2011

Stockholm, Sweden, April 12th, 2011

A number of workshops were organized by the Swedish embedded systems network ICES during 2011 (http://www.kth.se/itm/centra/ices/previous-events/). Each such workshop is organized by a team of academic researchers and industry representatives, and features thematic workshops with industrial and scientific presentations. The workshops serve several roles, including disseminating research results, making industrialist as well as researchers from different domains/disciplines meet, and provide a focal point for discussions which often results in the generation of new ideas.Example workshops during 2011 include the following:

- Lean Architecting - an ICES seminar with Scania – March 2011
- Power Management - an ICES-Enea seminar – April 2011

- Modelling & Design for Heterogeneous Embedded Systems – May 2011. This seminar presented results from the SysModel Artemis research project where KTH is a partner.
- ICES Enea Debugging Seminar – Multicore debugging – Nov. 2011

ICES also in 2011 arranged a couple of lab tours, at KTH for interested industrial stakeholders and for academic sharing, and also at industrial member companies (Ericsson hosted one such lab tour). These lab tours have been very popular among students, faculty as well as industry participants!

http://www.artist-embedded.org/artist/Overview,1937.html

Meeting: 2011 IWBDA: International Workshop on Bio-Design Automation at DAC

www.biodesignautomation.org/

Objectives/Description

The Third International Workshop on Bio-Design Automation (IWBDA) at DAC brought together researchers from the synthetic biology, systems biology, and design automation communities. The focus is on concepts, methodologies and software tools for the computational analysis of biological systems and the synthesis of novel biological systems.

Still in its early stages, the field of synthetic biology has been driven by experimental expertise; much of its success has been attributable to the skill of the researchers in specific domains of biology. There has been a concerted effort to assemble repositories of standardized components. However, creating and integrating synthetic components remains an ad hoc process. The field has now reached a stage where it calls for computer-aided design tools. The

electronic design automation (EDA) community has unique expertise to contribute to this endeavour. This workshop offered a forum for cross-disciplinary discussion, with the aim of seeding collaboration between the research communities.

Topics of interest included:

- Design methodologies for synthetic biology;
- Standardization of biological components;
- Automated assembly techniques;
- Computer-aided modeling and abstraction techniques;
- Engineering methods inspired by biology.

Meeting: Two Special Sessions on Compositional Techniques at DATE2011, **Organizers Alberto Sangiovanni Vincentelli and Joseph Sifakis**

Grenoble, *March 17th, 2011*

Participants: Trento, University of California at Berkeley, Verimag, ETH, INRIA, OFFIS, IST

Alberto Sangiovanni Vincentelli and Joseph SIfakis co-organized two special sessions of the Design and Test European Conference (DATE2011) on the achievements of our group. The allocation of two special sessions to the same group is an exceptional event due to the credibility of the team and the quality of the results.

Scope and Agenda

Special Session Type: Hot Topic

Special Session Title: Foundations of Component-based Design for Embedded Systems

Special Session Description
Component-based validation techniques for parallel and distributed embedded systems should be able to deal with heterogeneous components, interactions, and specification mechanisms. This special session describes a unified composition paradigm that allows the composition of subsystems with different execution and interaction semantics, combining computational and analytic models. This paradigm focuses on constructivity, which is reasoning about global system properties based on properties of its individual components.

Special Session Organizers:

Alberto Sangiovanni Vincentelli, University of California, Berkeley and University of Trento, USA and Italy, alberto@eecs.berkeley.edu: Joseph Sifakis, VERIMAG, France, sifakis@verimag.fr

Special Session Moderator

Joseph Sifakis, VERIMAG, France, sifakis@verimag.fr

Presentations (90 min total)

- **1st Presentation**
  - **Presentation Length 30 min:**
  - **Title:** Composing heterogeneous components for system-wide performance analysis
  - **Speaker** Lothar Thiele, ETHZ, Switzerland, thiele@ethz.ch**:**
  - **1st Author** Lothar Thiele, ETHZ, Switzerland**, thiele@ethz.ch:**
- **2nd Presentation:**

- **Presentation Length 30min**
- **Title:** Formal Methods for Composing Components
- **Speaker** Tom Henzinger, Institute of Science and Technology, Vienna, Austria, tah@ist.ac.at
- **1st Author** Tom Henzinger, President, Institute of Science and Technology, Vienna, Austria, tah@ist.ac.at

- **3rd Presentation:**
  - **Presentation Length 30min:**
  - **Title:** Requirement Engineering for Composition
  - **Speaker** Albert Benveniste, INRIA, Rennes, France, benveniste@inria.fr
  - **1st Author** Albert Benveniste, INRIA, Rennes, France, benveniste@inria.fr

Special Session Title: Flows, Applications and Future of Component-based Design for Embedded Systems

Special Session Description:
It is essential that theoretical results developed by the community of researchers in the domain of compositionality be integrated in coherent component-based design flows that must validated in comparison with existing industrial practices. Furthermore, compositionality results should be implemented in scalable supporting methods and tools. The special session presents a component-based design flow, its application to specific industrial domains and to diverse areas of design endeavors such as energy efficient buildings and synthetic biology.

Special Session Organizers:

Alberto Sangiovanni Vincentelli, University of California, Berkeley and University of Trento, USA and Italy, alberto@eecs.berkeley.edu: Joseph Sifakis, VERIMAG, France, sifakis@verimag.fr

Special Session Moderator

Alberto Sangiovanni Vincentelli, University of California, Berkeley and University of Trento, USA and Italy, alberto@eecs.berkeley.edu

Presentations

- **1st Presentation**
  - **Presentation Length 30 min:**
  - **Title:** Methods and Tools for Component-based Design
  - **Speaker** Joseph Sifakis, VERIMAG, France, sifakis@verimag.fr
  - **1st Author** Joseph Sifakis, VERIMAG, France, sifakis@verimag.fr **:**
- **2nd Presentation:**
  - **Presentation Length 30min**
  - **Title** Using contract-based component specifications for virtual integration testing and architecture design
  - **Speaker** Werner Damm, OFFIS, Germany, damm@offis.de
  - **1st Author** Werner Damm, OFFIS, Germany, damm@offis.de
  - **2nd Author** Eike Thaden, OFFIS, Germany
  - **3rd Author** Ingo Stierand, OFFIS, Germany
  - **4th Author** Thomas Peikenkamp, OFFIS, Germany
  - **5th Author** Hardi Hungar, OFFIS, Germany
- **3rd Presentation:**

- **Presentation Length 30min:**
- **Title:** Component-based Design for the Future
- **Speaker** Alberto Sangiovanni Vincentelli, University of California, Berkeley and University of Trento, USA and Italy, alberto@eecs.berkeley.edu
- **1st Author** Alberto Sangiovanni Vincentelli, University of California, Berkeley and University of Trento, USA and Italy, alberto@eecs.berkeley.edu

-- The above is new material, not present in the Y3 deliverable --

3. Staff Mobility and Exchanges

Staff Mobility and Exchanges between teams are essential for integration within and beyond the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams.

Mobility should be justified by and refer to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.

-- All new text: this entire chapter pertains only to activity in Year 4.--

3.1 Modelling and Validation cluster

During the 4th year the collaboration between partners has been intensified, with a high number of joint acitivities and publications involving exchange of staff: We highlight the following collaborative efforts referring to the more detailed description in the activity reports on *Modeling* and *Validation:*

- **Trento, KTH and UC Berkeley** collaboration on combining strengths of PtolemyII and Metropolis
- **Trento** and **UC Berkeley** collaboration on cyber-physical systems and contracts for circuits.
- **Several partners** collaborate on a white-paper on contracts.
- **IST Austria + VERIMAG** onrobust synthesis.
- **SPEEDS, CESAR, RECOMB, MBAT:** several partners participate and collaborate within other FP6 and ARTEMIST projects
- **INRIA**, **OFFIS**, **IST-Austria**, **TRENTO** and **Verimag** have collaborated intensively on contracts with plans for continuation.
- **Uppsala** is collaborating with **Absint**, **ETH** at Zurich, **TU Braunschweig**, and **Verimag** on Mixed Criticality Systems (MCS).
- **Uppsala** is collaborating with **ETH** at Zurich to combine analytic methods with model checking for efficient timing analysis.
- The work of **Saltzburg** on power isolation is part of a recent initiative in rigorous systems engineering (RiSE) with nine partners in Austria including **IST Austria**.
- **Uppsala** and **CISS** has continued collaboration on the distribution, maintainance and further dissemination of UPPAAL
- **CISS** and **INRIA** has collaborated on development compositional specification theories for probabilistic systems as well as the development of statistical model checking for networks of timed automata.
- **CISS** and **LSV** has collaborated intensely on the development of priced timed automata, energy automata, energy games and robustness for timed automata.
- **CISS**, **INRIA** and **RWTH** has collaborated on a specification theory based on abstract probabilistic automata.
- **CISS** and **INRIA** has collaborated on determinisation of timed automata using games, with the purpose of aid testing as well as statistical model checking

The activites involve more than 25 exchange vistist of more than 1 week duration.

3.2 SW Synthesis, Code Generation and Timing Analysis cluster

Visiting researcher: Prof. Reinhard Wilhelm (Saarland University)
Team visited: IRIT, Université Paul Sabatier Grenoble, November 2011,
Purpose: Habilitation of Christine Rochange

Visiting Researcher: Mihail Asavoaie is a PhD student at University Al. I. Cuza of Iași, working with prof. Dorel Lucanu
Team visited: Compiler Design Lab, Saarland University, November 2011
Mihail visited Reinhard Wilhelm's group and AbsInt to learn about the Saarland timing-analysis technology and in particular about the derivation of abstract processor models. Mihail cooperates on the K framework.

Visiting researcher: Vitor Rodrigues, University of Porto
Team visited: Compiler Design Lab, Saarland University
Vitor visited Reinhard Wilhelm's group to complete his functional-programming approach to timing analysis with a low-level analysis.

Visiting researcher: Jan Gustafsson, Mälardalen University
Team visited: Peter Puschner's real-time research group at TU Vienna, Austria
Vienna, Austria Oct. 4, 2011 to Oct. 7, 2011
Approximate cost for travel and lodging: 860 €

Reason for the visit: Discuss connections and cooperation between the flow-analysis research at Mälardalen University and Benedikt Huber's work with building an open timing analysis platform at TU Vienna. Jan Gustafsson also made a presentation of a current paper, published at RTNS 2011: "Automatic Generation of Timing Models for Timing Analysis of High-Level Code" for Peter Puschner's group and invited listeners.

Conclusions/objectives reached: Benedikt Huber's work on an open timing analysis platform was published at the WCET workshop in Porto 2011. His work includes using an open compiler framework (LLVM), flow analysis (using the SWEET tool from Mälardalen University), low-level analysis (using aiT from AbsInt) and a target platform (using LEON3). During the meetings during the visit, Mälardalen University and TU Vienna decided to intensify the cooperation to enhance our methods and tools. Especially, we will together enhance the development the C to ALF translator (developed at TU Vienna) and SWEET (developed at Mälardalen University, with the goal of a fully automatic WCET analysis of C programs. Areas that will be explored are handling of library functions and absolute addresses in C, and the different merging strategies that need to be used in SWEET. We also discussed cooperation in the area of automatic generation of timing models for timing analysis of high-level code, and timing measurement techniques.

Visiting student: Volker Seeker (Technical University of Berlin)
Team visited: Compiler and Architecture Design Group, Björn Franke (University of Edinburgh)
Edinburgh, United Kingdom – October 2010 to January 2011
Reason for the visit: Volker Seeker was a student of Computer Science at the Technical University of Berlin. He spent a couple of months at the University of Edinburgh to work on his master thesis. The topic of his thesis is "Design and Implementation of an Efficient Instruction Set Simulator for an Embedded Multi-Core Architecture". Volker's thesis has been jointly advised by Björn Franke (Edinburgh) and Sabine Glesner (Berlin). In September 2011, Volker Seeker's master thesis won the SET (Science, Engineering and Technology) award in the category "Best Information Technology Student" in London. Since November 2011, Volker Seeker has been a PhD student at the University of Edinburgh

-- The above is new material, not present in the Y3 deliverable --

3.3 Operating Systems and Networks cluster

Visiting researcher: PhD researcher, Daniele Alessandrelli (Scuola Superiore S.Anna, Pisa)
Team visited: University of Virginia at Charlottesville, USA (Prof. John Stankovic)
From January 2011 to July, 2011 *Approximate cost for travel and lodging: 5000 €*
Reason for the visit: Research collaboration on event management in wireless sensor networks for assisted living. Conclusions/objectives reached: Joint publication of research collaboration.

Visiting researcher: PhD researcher, Christian Nastasi (Scuola Superiore S.Anna, Pisa)
Team visited: Queen Mary Universit, London, UK (Prof. Andrea Cavallaro)
From August 2010 to February 2011 *Approximate cost for travel and lodging: 5000 €*
Reason for the visit: Research collaboration on wireless camera networks.
Conclusions/objectives reached: Joint publication of research collaboration.

Visiting researcher: PhD researcher, Gaetano Anastasi (Scuola Superiore S.Anna, Pisa)
Team visited: Distributed Real-Time Systems Lab - UC3M, Madrid, (Prof. Marisol García-Valls)
From October 2010 to April 2011 *Approximate cost for travel and lodging: 5000 €*
Reason for the visit: Research collaboration on QoS-based resource management.
Conclusions/objectives reached: Joint publication of research collaboration.

Visiting researcher: PhD Researcher, Antonio Romano (Scuola Superiore S.Anna, Pisa)
Team visited: United Technologies Research Center (UTRC), Cork, Ireland
From January 2011 to August 2011 *Approximate cost for travel and lodging: 5000 €*
Reason for the visit: Research on real-time operating systems and energy management in wireless sensor networks.
Conclusions/objectives reached: Joint thesis and research collaboration.

Visiting researcher: Associate Professor, Sverre Hendseth (Norwegian University of Science and Technology in Trondheim (NTNU).
Team visited: RETIS Lab., Scuola Superiore S. Anna, Pisa (Prof. Giorgio Buttazzo)
From August 2011 to July 2012 *Approximate cost for travel and lodging: 0 €*
Reason for the visit: Sabbatical on multiprocessor resource management.
Conclusions/objectives reached: Joint publication of research collaboration.

Visiting researcher: Post Doc, Moris Behnam, Malardalen University.
Team visited: Univeristy of Porto, Portugal (Prof. Luis Almeida)
From February 2011 to July of 2011 *Approximate cost for travel and lodging: 0 €*
Reason for the visit: Research on hierarchical scheduling in switched Ethernet.
Conclusions/objectives reached: Joint publication of research collaboration.

Visiting researcher: Post Doc, Manuel Barranco, University of the Balearic Islands, Spain.
Team visited: Univeristy of Porto, Portugal (Prof. Luis Almeida)
From October 2010 to February 2011 *Approximate cost for travel and lodging: 0 €*
Reason for the visit: Research on redundancy strategies and reliability analysis for a new generation of Ethernet switches with strong temporal protections for networked embedded systems. Conclusions/objectives reached: Joint thesis and research collaboration.

-- The above is new material, not present in the Y3 deliverable --

3.4 Hardware Platforms and MPSoC Design cluster

Visiting researcher : Prof. Paul Pop (DTU)
Team visited: Linköping, led by Petru Eles (Linköping University)
Several short visits during 2011
Reason for the visit: Common research on predictable fault tolerant systems.
Conclusions/objectives reached: Elaborated several approaches. One common publications for 2011.

Visiting researcher : Prof. Petru Eles (Linköping)
Team visited: DTU, led by Jan Madsen
One short visits during 2011
Reason for the visit: Common research on predictable fault tolerant systems.
Conclusions/objectives reached: Elaborated several approaches. One common publications for 2011.

Visiting researcher : Soheil Samii (Linköping University)
Team visited: Lund, led by Karl-Erik Årzén (Lund University)
Several short visits during 2011
Reason for the visit: Common research QoS modelling and optimisation of control applications.
Conclusions/objectives reached: Elaborated several approaches. One common publications for 2011.

Visiting researcher : Anton Cervin (Linköping University)
Team visited: Linköping, led by Petru Eles
Several short visits during 2011
Reason for the visit: Common research QoS modelling and optimisation of control applications.
Conclusions/objectives reached: Elaborated several approaches. One common publications for 2011.

Visiting researcher : Vana Jelicic (Faculty of Electrical Engineering and Computing, University of Zagreb, Croatia)
Team visited: UNIBO (Micrel Lab), led by Luca Benini
Bologna,Italy – September, 2011 to December, 2011
Approximate cost for travel and lodging: 7000 €
Reason for the visit: Investigation of power aware policies for multimodal wireless sensor networks and energy consuming sensors (e.g. gas sensors). Conclusions/objectives reached: The scientific work achived good results and a publication submitted to the IEEE Transaction on Sensors.

Visiting student : Christian Pinto (University of Bologna UNIBO)
Team visited: STMicroelectronics
Milan,Italy – May, 2011 to December, 2011
Approximate cost for travel and lodging: 7000 €
Reason for the visit: Integration of the existing P2012 simulation infrastructure with a full Linux environment, with the final goal of the integration with Google's Android. In deep, each P2012 SDK release comes with a simulation infrastructure modeling an ARM host processor, provided by Arm Fast Model tools, and a P2012 device (Gepop, single or multi cluster). The scientific work was aimed at obtaining a linux support for software developers in testing P2012 accelerated applications with a full Arm-Linux development environment.

Visiting researcher : Francesco Paterna (University of Bologna UNIBO)
Team visited: Brown University (USA), research group led by Prof. Sherief Reda

Rhode Island USA,Italy – June, 2011 to September, 2011
Reason for the visit: Investigation Adaptive Thermoelectrical Cooling Techniques to improve Reliability and Performance in multicore processors.

Visiting student: Daniele Bortolotti (University of Bologna UNIBO)
Team visited:EPFL
Lausanne,Swithzerland – June, 2011 to September, 2011
Approximate cost for travel and lodging: 7000 €
Reason for the visit: Developing of a SystemC simulation environment for ultra-low power MPSoCs. The goal in this design is to synergistically exploit near threashold computation in conjunction with multi-core architecture design to enable ultra-low-power wearable health monitoring systems.

Visiting student: Vladimir Petrovic (University of Belgrade)
Team visited: Micrel Lab (UNIBO)
Bologna, Italy Nov 30, 2011 - March 31 2012
Approximate cost for travel and lodging: 1780€
Reason for the visit: Design and implementation of a multi-port multi-banked data caches for ultra low power and many core architectures. Data caches are widely used in modern System on Chips (SoC) to bridge the increasing gap between processor speed and memory access time (also know as memory wall).

Visiting student: Masoud Dehyadegari (University of Tehran)
Team visited: Micrel Lab (UNIBO)
Bologna, Italy: from September 2011 - to March 2012
Approximate cost for travel and lodging: 4500€
Reason for the visit: Design and implementation, through an high level synthesis flow, of Hardware accellerators for Many core platform.

Visiting student: Mikkel K. Jakobsen (DTU)
Team visited: Axel Jantsch (KTH)
Several short visits during 2011
Reason for the visit: Extensions of the ForSyDe modelling framework and development of SystemC templates.

Visiting student: Junhe Gan (DTU)
Team visited: Axel Jantsch (KTH)
8 months visit during 2011
Reason for the visit: Development of a design space exploration strategy to address risk management in the early stages of the design process.

-- The above is new material, not present in the Y3 deliverable --

3.5 Design for Adaptivity Transversal Activity

Visiting researcher: Tarek Abdelzaher (UIUC)
Team visited: ULUND led by Karl-Erik Årzén
Lund, Sweden, August – December 2011
Approximate cost for travel and lodging: 5.000 €
Reason for the visit: Sabbatical visit to work on adaptive resource management and control of server systems with the researchers at ULUND

-- The above is new material, not present in the Y3 deliverable --

3.6 Design for Predictability Transversal Activity

Visiting researcher : Prof. Petru Eles (Linköping)
Team visited: DTU, led by Jan Madsen (DTU)
June 2011
Reason for the visit: Common research on predictable fault tolerant systems.
Conclusions/objectives reached: Elaborated several approaches. Written one common publication for 2011.

Visiting researcher: Prof. Reinhard Wilhelm (Saarland University)
Team visited: IRIT, Université Paul Sabatier Grenoble, November 2011,
Purpose: Habilitation of Christine Rochange

Visiting Researcher: Mihail Asavoaie is a PhD student at University Al. I. Cuza of Iași, working with prof. Dorel Lucanu
Team visited: Compiler Design Lab, Saarland University, November 2011
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Visiting researcher: *Vitor Rodrigues*, University of Porto
Team visited: Compiler Design Lab, Saarland University
Vitor visited Reinhard Wilhelm's group to complete his functional-programming approach to timing analysis with a low-level analysis.

Visiting researcher: Jan Gustafsson, Mälardalen University
Team visited: Peter Puschner's real-time research group at TU Vienna, Austria
Vienna, Austria Oct. 4, 2011 to Oct. 7, 2011
Approximate cost for travel and lodging: 860 €

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Conclusions/objectives reached: Benedikt Huber's work on an open timing analysis platform was published at the WCET workshop in Porto 2011. His work includes using an open compiler framework (LLVM), flow analysis (using the SWEET tool from Mälardalen University), low-level analysis (using aiT from AbsInt) and a target platform (using LEON3). During the meetings during the visit, we (Mälardalen University and TU Vienna) decided to intensify the cooperation to enhance our methods and tools. Especially, we will together enhance the development the C to ALF translator (developed at TU Vienna) and SWEET (developed at Mälardalen University,

with the goal of a fully automatic WCET analysis of C programs. Areas that will be explored are handling of library functions and absolute addresses in C, and the different merging strategies that need to be used in SWEET. We also discussed cooperation in the area of automatic generation of timing models for timing analysis of high-level code, and timing measurement techniques.

-- The above is new material, not present in the Y3 deliverable --

3.7 Integration Driven by Industrial Applications Transversal Activity

Visiting researcher: PhD, Lei Feng(Volvo)
Team visited: KTH led by Martin Törngren (KTH)
Approximate cost for travel and lodging: 1000 €
Reason for the visit: Continued collaboration between Volvo and KTH through the ATESST2, MAENAD and CESAR projects. Lei has since 2010 been employed by Volvo by worked part time at KTH. This has proven a fruitful cooperation.

Visiting researcher: Prof Martin Törngren
Team visited: UC Berkeley, group led by Professor Edward Lee.
September 1st – December 20th, 2011,
Approximate cost: 30 k€
Reason for the visit: Martin Törngren was invited to UC Berkeley as a visiting scholar to promote collaboration with Berkeley as well as with Trento through Alberto Sangiovanni-Vincentelli. The autumn was fruitful and several collaborations have been initiated including a study on real-time control systems based design approaches and Martin has also participated in ongoing work in combining the strengths of the Ptolemy II and MetroII approaches and environments. The promising collaboration has resulted in the fact that Martin Törngren will prolong his study and stay also during the spring at UC Berkeley.

Visiting researcher: Lic tec. Matthias Biehl
Team visited: MCGill CAMPaM workshop hosted by Prof. Hans Vangheluwe.
April 15-22, 2011
Approximate cost: 1000 €
Reason for the visit: Martin Törngren and Matthias Biehl were invited to the CAMPaM workshop and Matthias could make it and represented KTH. The 2011 workshop had the goal further the state-of-the-art in Computer Automated Multi-Paradigm Modelling (http://msdl.cs.mcgill.ca/conferences/CAMPaM/2011).

The main outcome from the point of view of KTH was the paper cited previously [DC11].

-- The above is new material, not present in the Y3 deliverable --

4. Tools and Platforms

A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.

ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

-- All new text: this entire chapter pertains only to activity in Year 4.--

4.1 Modelling and Validation cluster

Here we list some of the stable, downloadable tools and platforms of the cluster. The cluster partners are working on several other tools and platforms. For more and detailed information we refer to the reports of the activities *Modeling* and *Validation*.

- **AMT**
  - AMT (Analog Monitoring Tool) is a tool for checking the correctness of analogue and mixed-signal simulation traces with respect to a formal specification expressed as an assertion. The specification language supported by the tool is STL/PSL, an extension of the temporal logic inspired by the PSL language, which allows expressing properties of real-valued continuous-time behaviors.
  - http://www-verimag.imag.fr/~nickovic/index.php?id=nickovic&page=amt

- **IF TOOLBOX**
  - IF is a language for the structured representation of concurrent real-time systems and a set of tools allowing the analysis and verification of requirements on such systems. The tool evolved from the CADP toolset. Its development was motivated by the need for a structured representation of systems, allowing the application of simplifications for avoiding state explosion before its translation into a global (symbolic) transition relation. In particular, IF has frontends allowing the verification and analysis of models of real-time systems represented in SDL and UML.
  - http://www-if.imag.fr./

- **MARTE**
  - MARTE consists in defining foundations for model-based description of real time and embedded systems. These core concepts are then refined for both modeling and analyzing concerns. Modeling parts provides support required from specification to detailed design of real-time and embedded characteristics of systems. MARTE concerns also model-based analysis. In this sense, the intent is not to define new techniques for analyzing real-time and embedded systems, but to support them. Hence, it provides facilities to annotate models with information required to perform specific analysis. Especially, MARTE focuses on performance and schedulability analysis. But, it defines also a general framework for quantitative analysis which intends to refine/specialize any other kind of analysis.
  - http://www.omgmarte.org/

- **METROPOLIS**

The aim of this tool environment is

  - Establishing formal design methodologies is imperative to effectively
  - Managing complex design tasks required in modern-date system designs. It involves defining levels of abstraction to formally represent systems being designed, as well as formulating problems to be addressed at and across the abstraction levels. This calls for a design environment in which systems can be unambiguously represented throughout the abstraction levels, the design problems can be mathematically formulated, and tools can be incorporated to solve some of the problems automatically. Developing such an environment is precisely the goal of Metropolis.

    Metropolis consists of an infrastructure, a tool set, and design methodologies for various application domains. The infrastructure provides a mechanism such that heterogeneous components of a system can be represented uniformly and tools for formal methods can be applied naturally.
  - http://embedded.eecs.berkeley.edu/metropolis/index.html

- **PHAVER**
  - PHAVer is a tool for verifying safety properties of hybrid systems. It stands out from other tools with the following features:
    - exact and robust arithmetic with unlimited precision,
    - on-the-fly over-approximation of piecewise affine dynamics
    - improved algorithms and termination heuristics
    - support for compositional and assume-guarantee reasoning.
  - http://www-verimag.imag.fr/~frehse/phaver_web/index.html

- **UPPAAL**
  - Uppaal is an integrated tool environment for modeling, validation and verification of real-time systems modeled as networks of timed automata, extended with data types (bounded integers, arrays, etc.).

    The tool is developed in collaboration between the Department of Information Technology at Uppsala University, Sweden and the Department of Computer Science at Aalborg University in Denmark.

- www.uppaal.com

- **UPPAAL TIGA**
  - UPPAAL TIGA (Fig. 1) is an extension of UPPAAL [BDL04] and it implements the first efficient on-the-fly algorithm for solving games based on timed game automata with respect to reachability and safety properties. Though timed games for long have been known to be decidable there has until now been a lack of efficient and truly on-the-fly algorithms for their analysis.
  - http://www.cs.aau.dk/~adavid/tiga/

- **UPPAAL TRON**
  - Uppaal TRON is a testing tool, based on Uppaal engine, suited for black-box conformance testing of timed systems, mainly targeted for embedded software commonly found in various controllers. By online we mean that tests are derived, executed and checked simultaneously while maintaining the connection to the system in real-time.
  - http://www.cs.aau.dk/~marius/tron/

- **UPPAAL SMC**
  - UPPAAL SMC provides a new scalable, simulation-based engine for UPPAAL allowing for so-called statistical model checking of performance properties of networks of timed automata (NTA). The engine is based on a *natural* stochastic semantics of NTAs based on delay-distributions between outputs for each component with the semantics of networks given in terms of races. The tool supports the estimation and hypothesis testing of probabilistic properties applying for the latter efficient sequential algorithms leading to order-of-magnitude reduction in the number of runs required for a given level of confidence.
  - The tool has been applied to a number of cases, demonstrating significantly improved performance compared with other existing statistical model checking engines (YMER and PRISM). Also, a distributed implementation of the SMC engine has been made – with improved methods for avoiding bias, and with experimentally shown linear speed-up.
  - http://people.cs.aau.dk/~adavid/smc/

- **SARTS**
  - SARTS is a model based schedulability analysis tool used for hard real-time systems. SARTS is used to translate hard real-time systems, implemented in Java, to a finite state machine in the modeling tool Uppaal.

    The system being analyzed must be implemented in SCJ2, a safety critical profile for Java developed in this project, based on SCJ. The target hardware is the time predictable Java processor JOP, developed specifically for hard real-time systems.

    Several experiments have been conducted to illustrate the accuracy of SARTS compared to existing tools. It is shown how the model based approach can result in a more accurate analysis, than possible with traditional analyses.

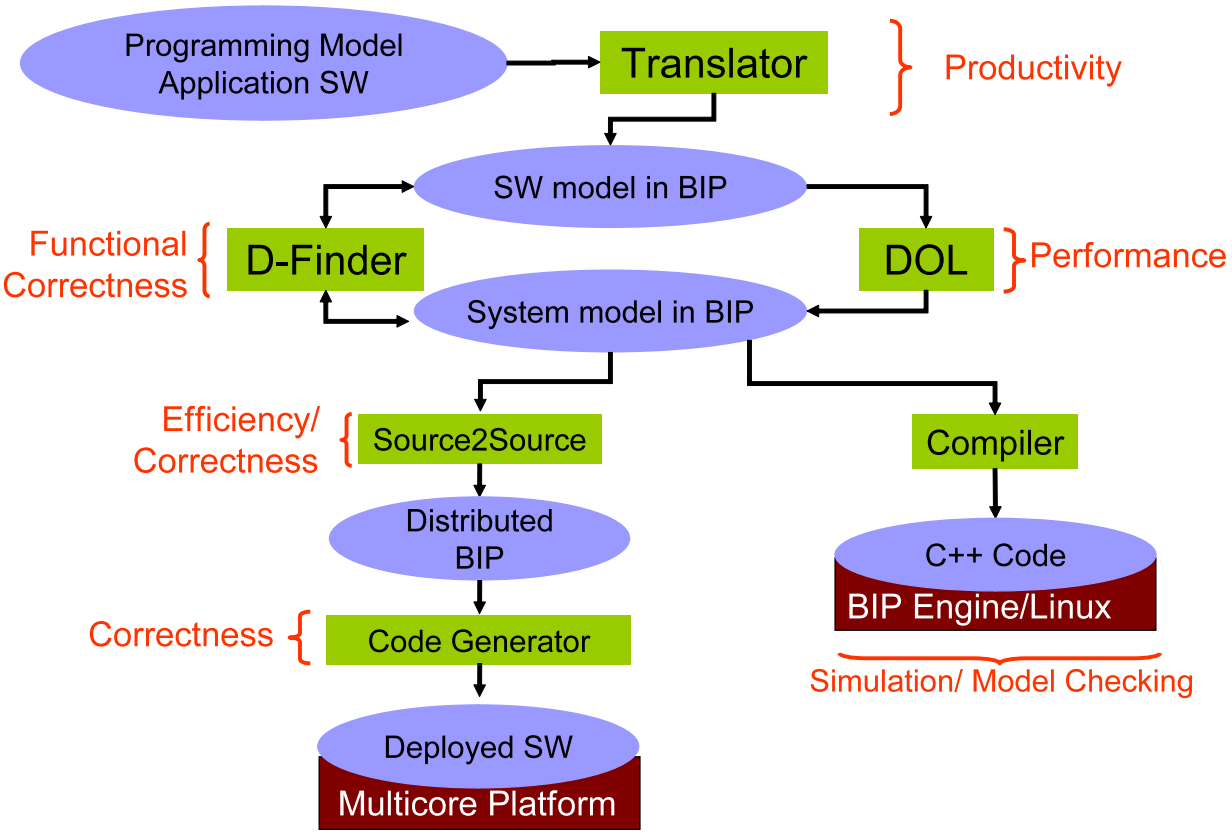
- http://sarts.boegholm.dk/

- **STG**
  - STG (Symbolic Test Generator) generates conformance tests, based on this framework:
    - Implementation: black-box, only input/output behavior is observable.
    - Specification: IOSTS(input/output behavior + internal structure)
    - Test Purpose: IOSTS, tells which part of the specification is to be tested
    - Test Case: IOSTS generated by STG from a specification and a test purpose
      - Test Cases are symbolic, and possibly parameterized by constants
      - They take into account possible non-determinism of the Spec;
      - They include a verdict (no manual interpretation needed)
  - http://www.irisa.fr/prive/ployette/stg-doc/stg-web.html

- **TIMES**
  - TIMES is a **T**ool for **M**odeling and **I**mplementation of **E**mbedded **S**ystems. It is a tool set for modelling, schedulability analysis, synthesis of (optimal) schedules and executable code. It is appropriate for systems that can be described as a set of tasks which are triggered periodically or sporadically by time or external events.
  - http://www.timestool.com/

- **BIP Design and Validation platform**
  - **objectives**: The vision is to use BIP as a unifying semantic model used along a complete and rigorous (model-based) system design flow. We have already implemented a significant part of this vision such as encompassing heterogeneous programming paradigms and scalable constructive verification techniques. The focus for the long term is to complete ongoing work on correct-by-construction transformations allowing to get from an application software model its implementation on some target platform, in particular multicore platforms.
  - **Main results**: The BIP toolset supports a design flow for the development of heterogeneous real-time systems and their correct implementation. It starts from application software written in domain-specific languages, e.g. synchronous, data flow, event driven languages. Different translators generate a unique BIP model of the application This BIP model can be analyzed by checking deadlock-freedom with **D-Finder**.
  - The transformation of the BIP model into an application is achieved by progressively enriching the model with information about the resources of the target platform. The process of modification of the model in order to take into account physical resource is still under study. It is driven by architectural constraints provided by the **DOL** tool (ETHZ) used for performance analysis. DOL provides a partitioning of the BIP model as well as a mapping of high level primitives into their implementation. To the BIP model, are then applied source-to-source transformations to obtain a functionally equivalent distributed BIP model. The latter differs from the initial model in that multiparty interaction, strong synchronization in particular, is expressed by using protocols based on asynchronous message passing. The distributed BIP model is obtained by application of a set of syntactic transformations that are shown to be correct. http://www-verimag.imag.fr/~async/bip.php

- The most recent developments take into account platform constraints. We have developed code generators generating from BIP models code for distributed platforms where we try to minimize the number of synchronizations by taking into account static and dynamic knowledge. We have also developed a code generator for time extended BIP specification which specifies timing requirements on one hand and estimations on worst case execution times of basic actions.



4.2 SW Synthesis, Code Generation and Timing Analysis cluster

4.2.1 Tool or Platform: WCC

Objectives

WCC is the leading tool for exploring the integration of worst-case execution time-aware analysis into compilers. WCC accepts Standard C code (conforming to C-99) with gcc extensions. WCC is used in combination with gcc for ARM. WCC supports the generation of TriCore and ARM binary code. Therefore, interoperability with other tools used in industry is provided.

Main Results

In a previous project, aiT was integrated with an experimental worst-case execution time aware compiler called WCC. During the last year, this integrated tool set was continued to be used for exploring the optimization potential for compiler optimizations using WCETs as the objective function. Work on multi-objective optimization was continued.

Current work

The current work explores the optimization potential of WCC further.

Participating partners:

- TU Dortmund
  TU Dortmund designs WCC and explores the optimization potential.
- AbsInt, Saarbrücken
  AbsInt provides aiT.

Web
http://ls12-www.cs.tu-dortmund.de/research/activities/wcc/

Related Publications

Heiko Falk and Helena Kotthaus. WCET-driven Cache-aware Code Positioning. *In Proceedings of the International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, pages 145-154, Taipei, Taiwan, October 2011.

Sascha Plazar, Jan C. Kleinsorge, Heiko Falk and Peter Marwedel. WCET-driven Branch Prediction aware Code Positioning. *In Proceedings of the International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, pages 165-174, Taipei, Taiwan, October 2011.

Jan C. Kleinsorge, Heiko Falk and Peter Marwedel. A Synergetic Approach to Accurate Analysis of Cache-Related Preemption Delay. *In Proceedings of the International Conference on Embedded Software (EMSOFT)*, pages 329-338, Taipei, Taiwan, October 2011.

Samarjit Chakraborty, Marco Di Natale, Heiko Falk, Martin Lukasiewyzc and Frank Slomka. Timing and Schedulability Analysis for Distributed Automotive Control Applications. *In Tutorial at the International Conference on Embedded Software (EMSOFT)*, pages 349-350, Taipei, Taiwan, October 2011.

Heiko Falk, Norman Schmitz and Florian Schmoll. WCET-aware Register Allocation based on Integer-Linear Programming. *In Proceedings of the 23rd Euromicro Conference on Real-Time Systems (ECRTS)*, pages 13-22, Porto / Portugal, July 2011.

Paul Lokuciejewski, Sascha Plazar, Heiko Falk, Peter Marwedel and Lothar Thiele. Approximating Pareto optimal compiler optimization sequences---a trade-off between WCET, ACET and code size. *Software: Practice and Experience*, May 2011. DOI 10.1002/spe.1079

-- Changes wrt Y3 deliverable --

The potential of using WCET as a cost function has been explored further.

4.2.2 MAPS

Objectives

MAPS (MPSoC Application Programming Studio) is proposed and developed in ICE, RWTH Aachen to tackle the challenge of programming future heterogeneous MPSoC platforms. It targets efficient code generation for multiple applications at a time and predefined heterogeneous MPSoC platforms. MAPS accepts both standard sequential C code and a light-weight C extension which models parallel process networks as inputs. It does C to C translation and produces C code as output for different target programming environments such as TI's OMAP. It can be used as a multicore compiler in those environments, which currently is done manually. In this way, interoperability with existing environments is achieved.

Main Results

In 2011, MAPS has been extended on many fronts of multicore programming. Firstly, MAPS has been extended to use calibrated MPSoC models for the SW mapping exploration. Efficient software mapping exploration of streaming applications, representing typical embedded applications targeted at MPSoC hardware, is becoming more and more important to cope with the increasing demand of multiple applications running simultaneously. As state of the art simulators usually have the accuracy versus speed tradeoff, a tool flow to automatically generate and calibrate abstract MPSoC models of streaming applications has been proposed. The methodology and tool flow have been applied to a real life dual ARM/DSP SoC, TI's heterogeneous OMAP3530 and the results are promising. This work has been presented initially in the MAP2MPSOC workshop (June 2011) as an extended abstract and the full paper appeared in the SoC conference (Nov. 2011). Other topics such as mapping and scheduling and application of MAPS in the SDR design have been also worked on. A number of conference and journal publications have been achieved this year. MAPS, as a complete solution enabling programming for real-life complex MPSoCs, has been presented for the first time to industrial partners in the 1st MAPS User Group Workshop (MUG 2011) held in Aachen in September. More than 20 industrial participants joined the interactive workshop and had hands-on with the tools. The MAPS tools were well received with a lot of feedback for future enhancements.

Current work

MAPS is under continuous development in many aspects to enhance its capabilities, such as multi-application RT scenario, retargeting to more multicore back-ends, etc. MAPS is part of RWTH Aachen's Ultra high speed Mobile Information and Communication (UMIC) research cluster. RWTH Aachen has been actively discussing MAPS with ArtistDesign partners at the annual Rheinfels workshop of MAP2MPSOC.

Participating partners:

- RWTH Aachen
  RWTH Aachen is designing and developing the MAPS tools.
- ACE
  ACE provides the CoSy compiler framework for use in the MAPS tools.
- Compaan
  Compaan provides the HotSpot Parallelizer to couple with the MAPS tools.

Web

http://www.ice.rwth-aachen.de/research/tools-projects/entry/detail/maps-mpsoc-application-programming-studio-sss/

Related Publications

Castrillon, J., Shah, A., Murillo, L., Leupers, R., and Ascheid, G. Backend for Virtual Platforms with Hardware Scheduler in the MAPS Framework. *In Proceedings of the 2nd IEEE Latin American Symposium on Circuits and Systems LASCAS'11.* Feb. 2011

Maximilian Odendahl, Weihua Sheng, Stefan Schürmans, Anastasia Stulova, Jeronimo Castrillon, Rainer Leupers. MPSoC Mapping Exploration by using Calibrated Models. *In MAP2MPSOC workshop*. June 2011

Castrillon, J., Sheng, W., and Leupers, R. Trends in Embedded Software Synthesis. *In International Conference On Embedded Computer Systems: Architecture, Modeling, and Simulation (SAMOS'11) (Carro, L. and Pimentel, A. D., eds.) pp. 347–354*. July 2011

Weiss, M., Castrillon, J., and Leupers, R. Novel Architecture and Programming Support for High-speed, Low Power and Flexible Next Generation Communication ICs. *In Proceedings of the Semiconductor Conference Dresden 2011 (SCD'11) pp. 1–4*. Sept. 2011

Castrillon, J., Schürmans, S., Stulova, A., Sheng, W., Kempf, T., Leupers, R., Ascheid, G., and Meyr, H. Component-Based Waveform Development: The Nucleus Tool Flow for Efficient and Portable Software Defined Radio. *In Analog Integrated Circuits and Signal Processing, vol. 69, no. 2, pp. 173–190*. Oct. 2011.

Sheng, W., Schürmans, S., Odendahl, M., Leupers, R., and Ascheid, G. Automatic Calibration of Streaming Applications for Software Mapping Exploration. *In Proceedings of the International Symposium on System-on-Chip (SoC)*. November 2011.

Castrillon, J., Leupers, R., and Ascheid, G. MAPS: Mapping Concurrent Dataflow Applications to Heterogeneous MPSoCs. *In IEEE Transactions on Industrial Informatics*. Nov. 2011.

Sheng, W., Castrillon, J., Stulova, A., Odendahl, M., Leupers, R., and Ascheid, G. Programming Heterogeneous MPSoCs using MAPS. *First International Software Technology Exchange Workshop 2011.* Nov. 2011.

-- Changes wrt Y3 deliverable –

The MAPS toolset has been extended in cooperation with other partners.

4.2.3 CoSy

Objectives

CoSy is a mature commercial development compiler platform.

Main Results

RWTH integrated additional optimizations into CoSy. TU Berlin used CoSy for its research on compiler verification. IMEC used CoSy as a platform for generating compilers. RWTH Aachen used CoSy for its MAPS tools.

CoSy is already used by many industrial costumers of ACE.

Current work

Work on additional optimizations continues at RWTH Aachen and so does the work at TU Berlin and IMEC. There is the trend toward using MPSoCs as the target platform.

Participating partners

- RWTH Aachen
- TU Berlin
- IMEC vzw

Web
http://www.ace.nl/compiler/cosy.html

Related Publications

See 4.3.2.

4.2.4 ICD-C

Objectives

ICD-C is a development platform with special support for source-to-source transformations. Source-to-source transformations can be implemented without loosing any information about the original C program. It can also be used in cases where full control over the libraries is required. ICD-C accepts Standard C code (conforming to C-99) with gcc extensions. ICD-C supports the generation of standard binary formats like ELF. Therefore, interoperability with other tools used in industry is provided.

Main Results

ICD-C was used for the integration of compilers with timing analysis and the impact of optimizing the WCET was studied in a number of cases. Also, it was used for memory-architecture aware pre-pass compilation tools. For their mode analysis on C code, Saarland University uses the ICD-C compiler infrastructure developed at ICD / TU Dortmund. This semi-automatic mode derivation from C code tries to superimpose a mode structure on code which may be generated from automata, from other control models or may be handwritten.

Current work

Current work is extending the support for caches and aims at reducing the number of calls of the WCET estimator in order to speed-up optimization. Machine-learning techniques are being tried as a promising approach. Mnemee partners are using ICD-C. For their mode analysis on C code, Saarland University uses the ICD-C compiler infrastructure developed at Dortmund.

Participating partners:

- TU Dortmund
- Saarland University (via the PREDATOR project)

- U. Passau
- ICD Dortmund (via the Mnemee project)
- TU Eindhoven (via the Mnemee project)
- IMEC (via the Mnemee project)
- ICCS (via the Mnemee project)

Web

http://www.icd.de/es/index.html

Related Publications

See also 4.3.1 and 4.3.5

-- Changes wrt Y3 deliverable --

None.

4.2.5 MH – parallelization assistant and MH static memory allocation for MPSoC and the Mnemee tool flow

Objectives

The main objectives of the framework is to offer an automatic source code parallelization and memory hierarchy management in order to map efficiently embedded software application on MPSoC platforms. This tool suite is also used in the Platform and MPSoC Design cluster.

Main Results

IMEC's MH tool is integrated into the Mnemee tool flow. Both are currently a stable tools and in regular use. We observed that resource-aware automatic parallelization is very successfully complementing traditional, resource-unaware parallelization. Work on parallelization has therefore been extended.

The input of the Mnemee tool flow is the sequential source code of the application written in C.

External impacts

The Mnemee tool flow, where the MH tool is integrated, can be used to automate the already existing tool chains of embedded design industries, by replacing traditional manual techniques.Two industrial cases have been used to demonstrate the applicability of the Mnemee approach in their design flow, emphasizing the automation achieved:

- In the communication domain, the IEEE 802.16e system for broadband wireless communications was the target of Intracom Telecom.
- In the multimedia domain, the application was a state of the art low bit rate speech coder based on the enhanced Mixed Excitation Linear Predictive (MELPe) algorithm.

Current work

Work performed on parallelization in the context of the Mnemee FP 7 project has been transferred from ICD to TU Dortmund. At TU Dortmund, this work is being extended. The work

at TU Dortmund is using MH for implementing the parallelism detected by its own tool. The commercial simulator COMET has been integrated with the Mnemee tools and the support of operating systems has also been extended.

Participating partners

- NTUA/ICCS
  This partner is integrating the dynamic data type and dynamic memory management tools and design flows with the IMEC MPSoC mapping tool flows.
- TU Dortmund/ICD
  This partner is extending automatic parallelization.

Web
http://www.mnemee.org/

Related Publications

Daniel Cordes and Peter Marwedel. Multi-Objective Aware Extraction of Task-Level Parallelism Using Genetic Algorithms. *In Proceedings of Design, Automation and Test in Europe (DATE 2012)*, Dresden, Germany, March 2012, (written in 2011)

Daniel Cordes, Andreas Heinig, Peter Marwedel and Arindam Mallik. Automatic Extraction of Pipeline Parallelism for Embedded Software Using Linear Programming. *In Proceedings of the Seventeenth IEEE International Conference on Parallel and Distributed Systems (ICPADS 2011)*, Tainan, Taiwan, December 2011.

A. Mallik, S. Mamagkakis, C. Baloukas, L. Papadopoulos, D. Soudris, S. Stuijk, O. Jovanovic, F. Schmoll, D. Cordes, R. Pyka, P. Marwedel, F. Capman, S. Collet, N. Mitas and D. Kritharidis: MNEMEE – An automated toolflow for parallelization and memory management in MPSoC platforms, *DAC, 2011, (presentation at the user's forum)*

-- Changes wrt Y3 deliverable --

The listings of MH and Mnemee have been integrated. Both are in regular use.

4.2.6 aiT

Objectives

aiT is the leading tool for computing worst case execution times (WCETs).). aiT is a tool which is already used in industry, for example by Airbus. It is the interest of AbsInt to design aiT such that it can be used in combination with other industrial tools and aiT has been accordingly designed.

Main Results

A prototype implementation of the UCB computation as developed by Saarland University has been integrated by AbsInt into the aiT Timing Analyzer. The analysis is implemented for the ARM7 and has been tested on smaller benchmark programs. In Year 4, the implementation has been optimized greatly (much higher performance and reduced memory consumption), and the analysis has been extended to other target processors including MPC55xx, MPC603e, and Leon2.

Current work

Current work is concerned with optimizing the performance of the analysis and exploring its potential on larger examples, and its practical usage in an overall system analysis. Implementations for further processors are also underway.

Related publications:

Daniel Grund, Jan Reineke, Reinhard Wilhelm: A Template for Predictability Definitions with Supporting Evidence. PPES 2011: 22-31

Daniel Grund, Jan Reineke, Gernot Gebhard: Branch target buffers: WCET analysis framework and timing predictability. Journal of Systems Architecture - Embedded Systems Design 57(6): 625-637 (2011)

Pascal Montag, Sebastian Altmeyer: Precise WCET calculation in highly variant real-time systems. DATE 2011: 920-925

Ernst Althaus, Sebastian Altmeyer, Rouven Naujoks: Symbolic Worst Case Execution Times. ICTAC 2011: 25-44

Ernst Althaus, Sebastian Altmeyer, Rouven Naujoks: Precise and efficient parametric path analysis. LCTES 2011: 141-150

Sebastian Altmeyer, Claire Maiza: Cache-related preemption delay via useful cache blocks: Survey and redefinition. Journal of Systems Architecture - Embedded Systems Design 57(7): 707-719 (2011)

Christoph Cullmann: Cache persistence analysis: a novel approachtheory and practice. LCTES 2011: 121-130

Gernot Gebhard, Christoph Cullmann, Reinhold Heckmann: Software Structure and WCET Predictability. PPES 2011: 1-10

Sebastian Altmeyer, Robert Davis and Claire Maiza: Cache-Related Pre-Emption Delay Aware Response Time Analysis For Fixed Priority Pre-Emptive Systems, IEEE RTSS, Vienna 2011

Participating partners:

- AbsInt, Saarbrücken
  AbsInt provides aiT and support for aiT.
- Saarland University
  Fundamental research results on timing analysis are provided by this partner
- TU Dortmund
  TU Dortmund uses aiT.

Web
http://www.absint.com

-- Changes wrt Y3 deliverable --

The text has been updated from the text of Y3.

4.2.7 Bound-T

Objectives

Bound-T is a tool for computing worst case execution time bounds (WCETs) by static analysis of machine code.

Current work and main results

Work on Bound-T in this period focused on two issues. Firstly, work continued on extending the model of the computations in the program under analysis to include the finite size (number of bits) of storage elements and the bit-precise semantics of integer arithmetic and other operations on binary words. This work is now supported by the new project APARTS, a Marie Curie IAPP collaboration between Mälardalen and Tidorum. Initial results on an improved polyhedral analysis of finite-size computations were published. However, this analysis was implemented in the SWEET tool from Mälardalen, not yet in Bound-T. Secondly, Bound-T was extended to allow the program under analysis to be exported in ALF form, for further analysis by SWEET. This means that Bound-T can be used as a front-end for SWEET, to analyze machine-code programs for any processor that Bound-T supports. Moreover, Bound-T will be able to use SWEET's powerful value-analysis and flow-analysis as a sub-step in its own analyses.

Participating partners:

- Tidorum, Helsinki
  Tidorum provides Bound-T and support for Bound-T.
- Mälardalen
  Mälardalen University develops the SWEET tool for flow analysis and WCET analysis and defines the ALF language for modeling computations and control flow, which is the input language for SWEET.

Web
http://www.bound-t.com

-- Changes wrt Y3 deliverable --

The text has been updated from the text of Y3.

4.2.8 SWEET

Objectives

SWEET (SWEdish Execution time analysis Tool) is a prototype WCET analysis tool developed at MDH. In particular, SWEET serves as an environment for the development and evaluation of advanced methods for automatic program flow analysis. This makes the program flow analysis component of SWEET an interesting candidate to use as plug-in with other WCET analysis tools, since it can reduce the need for manual annotations.

Main Results

SWEET has been equipped with different interfaces for its program flow analysis, including the ALF code format for representing code on different levels, a novel "Flow Fact" format for

expressing precise program flow constraints, and alternative backends producing program flow constraints in the AIS annotation format for aiT, and for the commercial tool RapiTime from Rapita Systems, respectively.

The interfaces have allowed SWEET to be integrated with other tools. Besides the integration with aiT and RapiTime, enabled by the backends mentioned above, it has been equipped with a C front-end through the SATIrE tool from TU Vienna. This allows SWEET to perform program flow analysis on source code level. SWEET has been extended to perform parametric WCET analysis. An alternative C frontend, using the open LLVM compiler framework, also exists in prototype form.

This frontend allows SWEET to analyze any language that LLVM can parse, including C99. SWEET also has a frontend, which uses aiT's binary reader, that allows SWEET to analyze PowerPC binaries.

Current work

We now work on making SWEET available to a larger audience. This includes a release of SWEET as freeware, as well as making SWEET available for running on a server through a web interface.

Partners

- Mälardalen University
- AbsInt
- TU Vienna

Related Publications

Andreas Ermedahl, Jan Gustafsson, and Björn Lisper. *Deriving WCET Bounds by Abstract Execution*. Chris Healy (ed) Proc. 11th International Workshop on Worst-Case Execution Time Analysis (WCET 2011), Austrian Computer Society (OCG), Porto, Portugal, July, 2011

-- Changes wrt Y3 deliverable --

SWEET is publicly available.

4.2.9 LooPo

Objectives

LooPo is a tool suite for the automatic parallelization of loop programs in the polyhedron model, developed at the University of Passau. LooPo offers a number of dependence analysis tools, schedulers and allocators, and it does code generation for shared-memory and distributed-memory machines. The LooPo project has been going on since 1994 and has been funded repeatedly by the DFG.

LooPo accepts loop nests in C or Fortran notation or a polyhedral specification as input. Polly is implemented as an optimization pass in the LLVM tool chain; therefore, it can be applied to all codes that can be compiled by LLVM, e.g., programs conforming to the C99 and C++98 standards. Therefore, LooPo can be used in combination with other tools used in industry.

Main results

Passau's focus has been on extending the applicability of the polyhedron model. Over the years, features like WHILE loops, conditionals, tiling and non-affinity of the loop bounds and array index expressions have been included. Substatement parallelization has been made possible and LooPo has been adapted to Grid computing. At TU Dortmund, LooPo was compared with PLUTO, a parallelization tool developed by Uday Bondhugula at the Ohio State University. The results are available as a Bachelor thesis written by Richard Hellwig. Except for one application, LooPo outperformed PLUTO with respect to minimizing energy consumption and run-time.

Current work

Current activities in the project are to optimize loop nests for the programming of GPGPUs, in particular, with scratchpad memories and to make extend the polyhedron with dynamic methods of program analysis and code generation. On the latter subject, a new LooPo component, named Polly, has been developed by Tobias Grosser in a Diploma thesis at the University of Passau. Polly recognizes polyhedral structures in the intermediate representation IR of the compiler tool suite LLVM. This liberates polyhedral analysis methods from a specific source language like FORTRAN or C. Many different languages, also languages from different programming paradigms, can be compiled to LLVM-IR. The future goal is to exploit also run-time information in a polyhedral analysis at the level of LLVM-IR. Program structures that violate the requirements of the polyhedron model at compile time can turn into trivial structures with the additional knowledge given at run time. This can widen the applicability of the polyhedron model for loop parallelization dramatically.

Andreas Simbürger (doctoral student in Passau) is using Polly to evaluate the potential for dynamic loop optimizations in real-world applications from different domains, with encouraging preliminary results. Polly is also the subject of a master thesis (in Passau) in which it is being combined with a domain-specific compiler for image processing on GPUs developed in Erlangen. The goal is to detect and extract image processing codes automatically from programs written in general-purpose programming languages and running them on GPU hardware after optimization by LooPo and the DSL compiler.

Partners

- University of Passau
- TU Dortmund
- U. Erlangen

Web

http://www.infosun.fim.uni-passau.de/cl/loopo/

Related Publications

Tobias Grosser, Hongbin Zheng, Ragesh Aloor, Andreas Simbürger, Armin Größlinger, and Louis-Noël Pouchet. Polly – Polyhedral Optimization in LLVM. In Christophe Alias and Cédric Bastoul, editors, *Proceedings of the First International Workshop on Polyhedral Compilation Techniques (IMPACT)*, 6pp. INRIA Grenoble Rhône-Alpes, April 2011.

Tobias Grosser. Enabling Polyhedral Optimizations in LLVM, *Master Thesis, Department of Informatics and Mathematics, University of Passau*, April 2011.

-- The above is new material, not present in the Y3 deliverable --

4.2.10 CHRONOS for Multi-cores: Tool Flow

Objectives

With the rapid deployment of multi-core architectures, worst case execution time (WCET) analysis of real time systems has become an increasingly difficult problem. Multi-core architectures extensively employ shared resources. Two such meaningful examples of shared resources are shared cache and shared bus. Shared resources introduce unpredictability in execution time due to the presence of inter-core conflicts. Moreover, the interaction of inter-core conflicts with different other micro-architectural features (e.g. pipeline, branch prediction) makes the overall WCET analysis a very difficult problem.

The multi-core CHRONOS tool builds on top of the existing open-source single core WCET analyzer CHRONOS available from http://www.comp.nus.edu.sg/~rpembed/chronos which was developed at the National University of Singapore and was first released in 2006-07.

The purpose of the multi-core CHRONOS tool (developed in the course of this project) is to provide a unified WCET analysis framework that includes most of the basic components in a multi-core processor (e.g. pipeline, private cache, shared cache, branch prediction, shared bus). CHRONOS addresses the challenging issue of multi-core timing analysis by providing a compositional WCET analysis framework, and thereby avoiding the enumeration of thread interleaving.

Main Results

The implementation of the first prototype version has been finished. Multi-core CHRONOS has been built on top of its single-core counterpart. The multi-core prototype retains all the features of the single core CHRONOS version (I.e. advanced micro-architectural features like superscalar and out-of-order processors, history based branch predictors and speculative execution). Additionally, we implement the analysis of shared instruction cache and shared bus with round-robin arbitration policy. The integration of shared cache and shared bus has been performed in such a fashion that we can give a safe timing estimate even in the presence of timing anomalies.

To validate the analysis result of the tool, the partners also provide a simulator implementing the same micro-architectural features. The simulator is based on the simplescalar infrastructure and has been extended / modified to verify the result of multi-core CHRONOS.

The prototype version of the tool is running for an extensive set of benchmarks in Malardalen benchmark suite. We have tested the prototype for many different micro-architectural configurations. Initial results are promising - we can obtain tight WCET estimates (overestimation within 50% for most of the cases) very quickly. Details of the tool and the results are available at http://www.comp.nus.edu.sg/~rpembed/chronos-multi-core.html

The tool can be used to pin-point the sources of WCET overestimation in a multi-core setting. Therefore, it can be very useful for worst-case performance oriented compiler optimizations in multi-cores.

Current Work

Current work includes the integration of data cache analysis in the multi-core CHRONOS and extensive testing of the tool for some real world benchmarks.

Partners

- National University of Singapore
- TU Dortmund

Web

http://www.comp.nus.edu.sg/~rpembed/chronos-multi-core.html

Related Publications

Timon Kelter, Heiko Falk, Peter Marwedel, Sudipta Chattopadhyay and Abhik Roychoudhury. Bus-Aware Multicore WCET Analysis through TDMA Offset Bounds. *In Proceedings of the 23rd Euromicro Conference on Real-Time Systems (ECRTS)*, pages 3-12, Porto / Portugal, July 2011.

Timon Kelter, Heiko Falk, Peter Marwedel, Sudipta Chattopadhyay and Abhik Roychoudhury. Bus-Aware Multicore WCET Analysis through TDMA Offset Bounds. Technical Report #837, TU Dortmund, Faculty of Computer Science 12, January 2011

Sudipta Chattopadhyay, Chong Lee Kee, Abhik Roychoudhury, Timon Kelter, Peter Marwedel and Heiko Falk, A Unified WCET Analysis Framework for Multi-core Platforms, In *Proceedings of 18th IEEE Real-time and Embedded Technology and Applications Symposium (RTAS) 2012*, (written in 2011).

-- Changes wrt Y3 deliverable --

The cooperation with the University of Singapore has become much stronger in Y4.

4.3 Operating Systems and Networks cluster

4.3.1 A simulation environment for Multimedia Sensor Networks

Objectives

Investigation of distributed target tracking algorithms for Wireless Multimedia Sensor Networks.

Main Results

A simulation environment has been developed to model the communication layers, the sensing and distributed application logic of a Wireless Multimedia Sensor Networks (WMSN). This Wireless Simulation Environment for Multimedia Networks (WiSE-MNet) is based on Castalia/OMNet++ and is available as open source to the research community. The environment is designed to be flexible and extensible, and has a simple camera model that enables the simulation of distributed computer-vision algorithms at a high level of abstraction. The effectiveness of WiSE-MNet has been demonstrated with a distributed tracking application.

Current Work

We are currently studying more realistic tracking scenarios, addressing problem such as the full vision processing pipeline, synchronization issues and integration with heterogeneous sensors. Another important problem to be addressed for large scale networks is the presence of multiple objects (in general many objects). In this context, target tracking becomes much more complex, because approaches for multiple hypothesis tracking are necessary to accounts for interaction between targets, data association, false positive/negative detections and so on.

Participating Partners

- Scuola Superiore Sant'Anna, Pisa
- Queen Mary University of London

Web

http://rtn.sssup.it/index.php/research-activities/distributed-processing-with-wireless-multimedia-sensor-networks/distributed-target-tracking

http://rtn.sssup.it/index.php/research-activities/distributed-processing-with-wireless-multimedia-sensor-networks/realistic-simulations

http://rtn.sssup.it/index.php/software/2-uncategorised/45

Related publications

1. C. Nastasi, A. Cavallaro, “Distributed target tracking under realistic network conditions” In Proc. of Sensor Signal Processing for Defence (SSPD), London, UK, 28-29 September, 2011
2. C. Nastasi, A. Cavallaro, “WiSE-MNet: an experimental environment for Wireless Multimedia Sensor Networks” Proc. of Sensor Signal Processing for Defence (SSPD), London, UK, 28-29 September, 2011

4.3.2 PartiCore – A Partitioning Tool for Multi-core Reservations

Objectives

Develop a tool for partitioning parallel real-time applications on a set of multiprocessor reservations with the objective of minimizing the required computational resources.

Main Results

The tool consists of a C++ library and a GUI-based tool. A real-time application is modeled as a set of tasks with given precedence constraints, specified as a Directed Acyclic Graph (DAG). The application is sporadic, meaning that it is cyclically activated with a minimum inter-arrival time T and must complete within a given relative deadline D, which can be less than or equal to T. Using PartiCore, the application is partitioned into flows, each allocated on a virtual processor that is an abstraction of a sequential machine achieved through a resource reservation mechanism. Allocation optimizes resource usage taking timing constraints into account.

Current work

The analysis and the allocation is being extended to take resource constraints into account.

Participating partners:

- Scuola Superiore Sant'Anna of Pisa (analysis and tool implementation)
- University of Kaiserslautern (support for resource management)
- University of Lund (support for application model)
- EPFL Lausanne (support for the specification of realistic multimedia applications).

Web
http://particore.sssup.it/

Related Publications

1. Giorgio Buttazzo, Enrico Bini, and Yifan Wu, "Partitioning Parallel Applications on Multiprocessor Reservations", IEEE Transactions on Industrial Informatics, Vol. 7, No. 2, pp. 302-315, May 2011.
2. Yifan Wu, Giorgio Buttazzo, Enrico Bini, Anton Cervin, "Parameter Selection for Real-time Controllers in Resource-Constrained Systems", IEEE Transactions on Industrial Informatics, Vol. 6, No. 4, pp. 610-620, November 2010.
3. Giorgio Buttazzo, Enrico Bini, and Yifan Wu, "Partitioning Parallel Applications on Multiprocessor Reservations", Proceedings of the 22nd Euromicro Conference on Real-Time Systems (ECRTS 10), Brussels, Belgium, July 6-9, 2010.
4. Giorgio Buttazzo, Enrico Bini, and Yifan Wu, "Heuristics for Partitioning Parallel Applications on Virtual Multiprocessors", Proceedings of the First International Workshop on Adaptive Resource Management (WARM 2010), Stockholm, Sweden, April 12, 2010.
5. Enrico Bini, Giorgio Buttazzo and Yifan Wu, "Selecting the Minimum Consumed Bandwidth of an EDF Task Set", Proceedings of the 2nd Workshop on Compositional Theory and Technology for Real-Time Embedded Systems (CRTS 2009), Washington, D.C., USA, December 1, 2009.
6. Yifan Wu, Enrico Bini, and Giorgio Buttazzo, "A Framework for Designing Embedded Real-Time Controllers", Proceedings of the 14th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2008), Kaohsiung, Taiwan, August 25-27, 2008.

4.3.3 YaoSim: Yet Another Operating system SIMulator

Objectives

Develop an operating systems simulator for scheduling real-time tasks under limited preemptive scheduling.

Main Results

YaoSim has been developed at Retis Lab of the Scuola Superiore Sant'Anna as an internal project. This software package simulates different scheduling policies on randomly generated task sets in which preemption can be fully enabled, fully disabled, or partially enabled through specific algorithms. It is written in C language and compiled with GCC 4.3.4 and above. The program is released as open source, to allow other researchers to extend the software with other algorithms and test their novel scheduling algorithms using a common framework.

Current work

The tool is being used to test the schedulability level of several limited preemptive approaches.

Participating partners:

- Scuola Superiore Sant'Anna of Pisa (analysis and tool implementation)
- University of Illinois at Urbana Champaign (schedulability analysis)
- University of Modena and Reggio Emilia (schedulability tests)

Web
http://yaosim.sssup.it/

Related Publications

7. Yifan Wu, Enrico Bini, and Giorgio Buttazzo, "A Framework for Designing Embedded Real-Time Controllers", Proceedings of the 14th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2008), Kaohsiung, Taiwan, August 25-27, 2008.

4.3.4 Marte OS

Objectives

Efficient operating systems for embedded applications.

Main Results
MarTE OS is a Hard Real-Time Operating System for embedded applications that follows the Minimal Real-Time POSIX.13 subset. It provides an easy to use and controlled environment to develop Multi-Thread Real-Time applications. It supports mixed language applications in Ada, C and C++ and is available under the GNU General Public License 2.

Participating partners:

- University of Cantabria

Web
http://marte.unican.es

4.3.5 HaRTES Ethernet switch

Objectives

Build a predictable and reconfigurable Ethernet switch for hard real-time communications.

Main Results

HaRTES Ethernet switch is a novel Ethernet switch for hard real-time communications that is fully online reconfigurable and supports both isochronous and asynchronous traffic. It has also been extended to support multi-level hierarchical server-based scheduling and thus providing composable virtual channels with strong temporal protection. The switch has been demonstrated at APRES 2011 (CPSWEEK) and RTSS 2011, as well as at CMU, Pittsburgh and GM, Detroit.

Current work

Definition of a scalable resource reservation protocol for networks of such switches.

Participating partners:

- University fo Aveiro,
- University of Porto,
- University of the Balearic Islands,
- Mälardalen University

Web

http://www.ieeta.pt/lse/hartes/

Related Publications

1. Rui Santos, Paulo Pedreiras, Moris Behnam, Thomas Nolte, Luis Almeida. Multi-level Hierarchical Scheduling in Ethernet Switches. EMSOFT 2011, International Conference on Embedded Software. Taipei, Taiwan, 9-14 October, 2011..
2. Rui Santos, Ricardo Marau, Arnaldo Oliveira, Paulo Pedreiras, Luis Almeida. Designing a Costumized Ethernet Switch for Safe Hard Real-Time Communication. WFCS 2008 – 7th IEEE Workshop on Factory Communication Systems. Dresden, Germany. 21-23 May 2008.

4.3.6 Flexible Time-Triggered framework

Objectives

Bringing flexibility to the Time-Triggered paradigm.

Main Results

The Flexible Time-Triggered framework is a network methodology for bringing flexibility to the Time-Triggered paradigm by making use of online traffic scheduling. The first protocol implemented according to this paradigm was FTT-CAN and the most recent is FTT-SE that operates over switched Ethernet. Notably, the FTT protocols support any kind of traffic scheduling, which makes them ideal for leveraging hierarchical scheduling frameworks on

networks providing composable virtual channels through temporal partitions. FTT-CAN has been successfully deployed in mobile robots and other industrial machinery. FTT-SE has been deployed in an adaptive industrial video surveillance system, in a health-care system and in numerous feedback control testbeds. It was also proposed for avionics of military airplanes.

Current work

Definition of a scalable architecture, with end-to-end resource reservation.

Participating partners:

- University of Porto
- University of Aveiro
- Technical University of Valencia (Engineering School of Alcoy)
- Carnegie Mellon University
- Malardalen University

Toulouse University **Web**
http://www.fe.up.pt/ftt

Related Publications

1. Javier Silvestre, Ricardo Marau, Paulo Pedreiras, Luis Almeida. On-line QoS Management for Multimedia Real-Time Transmission in Industrial Networks, IEEE Transactions on Industrial Electronics, 58(3):1061-1071. DOI: 10.1109/TIE.2010.2049711, March 2011
2. Moris Behnam, Zahid Iqbal, Pedro Silva, Ricardo Marau, Luís Almeida, Paulo Portugal. Engineering and Analyzing Multi-Switch Networks with Single Point of Control. WCTT 2011 - Int. Workshop on Worst-Case Traversal-Time, a satellite event of RTSS 2011, Vienna, Austria, November 29, 2011.
3. Ricardo Marau, Karthik Lakshmanan, Paulo Pedreiras, Luis Almeida, Raj Rajkumar, Luis Almeida. Efficient Elastic Resource Management for Dynamic Embedded Systems. ICESS 2011, The 8th IEEE International Conference on Embedded Software and Systems, Changsha, China, November 16-18, 2011.
4. L. Almeida, R. Marau, K. Lakshmanan and R. Rajkumar. On the schedulability analysis for dynamic QoS management in distributed embedded systems. SEUS 2010, 8th IFIP Workshop on Software Technologies for Future Embedded & Ubiquitous Systems, Waidhofen/Ybbs, Austria, Oct. 13-15, 2010.
5. R. Marau, L. Almeida, K. Lakshmanan, R. Rajkumar, P. Pedreiras. Utilization-based Schedulability Analysis for Switched Ethernet aiming Dynamic QoS Management. ETFA 2010, 15th IEEE Conference on Emerging Technologies and Factory Automation. Bilbao, Spain, 13-16 September 2010.
6. Ricardo Marau, Luis Almeida, Mario Sousa, Paulo Pedreiras. A middleware to support dynamic reconfiguration of real-time networks. ETFA 2010, 15th IEEE Conference on Emerging Technologies and Factory Automation. Bilbao, Spain, 13-16 September 2010.
7. A. Mifdaoui, F. Frances, and C. Fraboul. Performance analysis of a master/slave switched ethernet for military embedded applications. Industrial Informatics, IEEE Transactions on, 6(4):534 –547, nov. 2010

4.3.7 iLAND

Objectives

A middleware architecture for supporting timely reconfiguration is distributed soft real-time systems

Main Results

The tool consists of a C library for offering communication support, and reconfiguration of distributed real-time systems. Also, profiling tools are offered for tuning the QoS parameters of distributed applications. They are based on services modelled as a set of services (tasks) with specified as a directed acyclic graph. Services can be deployed across a network of nodes and different versions of the iLAND architecture can be used (satellite, planet, or star) depending on the computational power of the devices and the role of the different nodes in the iLAND network. A laboratory prototype based on the FTT-SE protocol has been demonstrated at the ARTEMIS Summit 2011 and at RTSS 2011.

Current work

A virtual machine is being finalized that contains the two upper layers of the architecture for soft real-time. Real-time support implementation is not sufficient nor implemented in full, but it is expected for the future.

Participating partners:

- Universidad Carlos III de Madrid (architecture design, reconfiguration protocol, and implementation)
- University of Porto (contributor to real-time support)

Web
http://www.iland-artemis.org
http://www.it.uc3m.es/drequiem

Related Publications

1. Marisol García-Valls, Alejandro Alonso, Juan Antonio de la Puente. A dual-band priority assignment algorithm for QoS resource management. Future Generation Computer Systems, Elsevier. DOI: 10.1016/j.future.2011.10.005. December 2011.
2. M. García-Valls, P. Basanta-Val, I. Estévez-Ayres. Real-time reconfiguration in multimedia embedded systems. IEEE Transactions on Consumer Electronics, 57(3):1280-1287, August 2011
3. Marisol García-Valls, Iago Rodríguez-López, Laura Fernández Villar, Iria Estévez-Ayres and Pablo Basanta-Val. Towards a middleware architecture for deterministic reconfiguration of service-based networked applications ETFA 2010. Bilbao, Spain. September 2010.
4. Marisol García-Valls, F. Gómez Molinero. Real-Time Reconfiguration: A Vision and its Reality . IEEE International Conference on Industrial Informatics (IEEE INDIN 2011). IEEE Computer Society Press. Caparica, Portugal. July 26 - 29, 2011.
5. M. García-Valls, P. Basanta-Val , I. Estevez-Ayres. Supporting service composition and real-time execution through characterization of QoS properties. In 6th International

Symposium on Software Engineering for Adaptive and Self-Managing Systems Sponsored by ACM SIGSOFT, IEEE TCSE May 2011.

6. I. Rodríguez-López, M. García-Valls, Marisol. Architecting a Common Bridge Abstraction over Different Middleware Paradigms. 16th International Conference on Reliable Software Technologies - Ada Europe 2011. Edinburgh, UK. June, 2011.
7. Iria Estévez-Ayres, Marisol García-Valls, Pablo Basanta-Val, Jorge Díez-Sánchez: A hybrid approach for selecting service-based real-time composition algorithms in heterogeneous environments. Concurrency and Computation: Practice and Experience 23(15): 1816-1851 (2011)
8. P. Basanta-Val, M. García-Valls, I. Estévez-Ayres. A dual programing model for distributed real-time Java. IEEE Transactions on Industrial Informatics, Nov. 2011.
9. P. Basanta-Val, M. García-Valls, I. Estévez-Ayres. Non-Functional Information Transmission Patterns for Distributed Real-Time Java. Software Practice and Experience. 41(12): 1409–1435 (2011)
10. Pablo Basanta-Val, Marisol García-Valls and Iria Estévez-Ayres. Fine tuning of the multiplexing facilities of Java's Remote Method Invocation. Concurrency and Computation Practice and Experience. 23(11): 236-1260, August 2011.
11. Pablo Basanta-Val, Marisol García-Valls and Iria Estévez-Ayres. Extending the Concurrency Model of the Real-Time Specification for Java. Concurrency and Computation: Practice and Experience, 23(14): 1623-1645 (2011)

4.3.8 Interoperability between tools, Use Cases and Scenarios

Interoperability

The cluster on Operating Systems and Networks continued to work across academia and industry in the integration of appropriate tool-flows and towards tool integration and interoperability in a manner that is usable for both industry and continued academic research.

One example of this is the work within the FP7 project JEOPARD, concentrating upon Java based tool flows for multicore heterogeneous real-time systems; this included Java Virtual Machine tool vendors, real-time operating system tool vendors, and academic research that influenced Java language standards.

Another example is the FP7 project MADES which concentrates upon tool-flows for model-driven real-time systems; this includes UML tool vendors, the community Eclipse effort (providing overall integration), and an open source model transformation toolset vendor.

Another tools has been developed within the FP7 project ACTORS, which helps the designer in the analysis and partitioning real-time parallel applications on top of multicore platforms.

Use Cases and Scenarios

Use-cases for real-time embedded systems have been published and/or are being developed from a number of past and ongoing EU FP7 projects (JEOPARD, MADES, T-CREST, Touchmore).

These provide real examples of design flows and tool chains that are being developed for current and future real-time embedded systems.

-- The above is new material, not present in the Y3 deliverable --

4.4 Hardware Platforms and MPSoC Design cluster

4.4.1 Tool: SymTA/S

Objectives

SymTA/S is a tool for the development and verification of embedded multiprocessor real-time systems. The existing technology is mainly suitable for event or time-driven systems with message passing as the main task interaction. The tool shall be extended to cover the timing implications of multicore processors, or multiprocessor-systems-on-chip.

Main Results

In several previous projects (funded by german DFG, “Sureal”, funded by german BMBF, ARTIST2, and others), the compositional analysis approach has been transferred into a tool framework which is now also commercially available. The available modelling options capture typical problems in todays automotive systems (CAN bus utilization, end-to-end deadlines,…). This addresses a growing need for formal methods in the industry. The topics currently under research (see below) address future problems which can be expected to become of increasing industrial interest in the future.

Current work

The research version of the tool framework is currently being developed into several new directions: Modeling of shared resources for multiprocessor-system-on-chips (see ArtistDesign Activity 6.2: Platform and MpSoC Analysis), the modelling of hierarchical event models (in the scope of the COMBEST project), and the demonstrator platform for adaptive systems (see ArtistDesign 7.1: Design for Adaptivity). Besides the extension of the applicability into new domains, a major focus within ArtistDesign is the synergetic coupling of tools, as well as the correspoinding development of models.

Interoperability

Analysis methods developed during the last four years have been prototypically implemented in the tool SymTA/S and used in collaboration with industrial partners for the analysis of realistic use cases (e.g. in the automotive domain). The GUI of the tool was extended with new elements which allow the modelling of new components (e.g. shared resources in multi-core setup), the input of the systems’ parameters and the visualization of the obtained results. The current tool implementation does not meet the requirements of a commercial tool, but it can already serve as a prototype for demonstration or as a proof of concept even for industrial customers. Collaboration with industrial partners showed that the developed formal analysis methods provide tight analysis results for realistic use cases. This has increased the acceptance of formal analysis methods and triggered the integration of the research solutions in the commercially available version of the tool SymTA/S. Also, the total tool box provided by Symtavision was extended and now includes a tracing tool.

Integration of MPA and SymTA/S continued

During the last four years ETHZ and TU Braunschweig continuously worked on coupling the tools SymTA/S and MPA. The interface developed for tool coupling now allows combining the strengths of the two tools. The interface has been implemented as a plug-in for the research

version of the tool SymTA/S and as an extension to the RTC Toolbox. Since the RTC Toolbox is not commercially supported, there are no plans to make the developed tool coupling commercially available. However, a research partner would be able to run the RTC toolbox with the SymTA/S research version.

Use Cases and Scenarios

Multiple use cases have been addressed by TU Braunschweig in collaboration with industrial partners. TU Braunschweig and GM focused on adapting research solutions to possible future automotive setups. In this scope Ethernet based solutions for in-vehicle networking and multi-core setups were examined. The applicability and the performance (i.e. how useful are the obtainable results) of timing analysis methods to current and future automotive E/E architectures was investigated by TU Braunschweig in collaboration with Daimler AG. First analysis results were often overestimated by such a large amount that were deemed unusable by Daimler. As a consequence new analysis solutions have been developed. These give much tighter results than the formal techniques previously available. R&D work was also conducted between TU Braunschweig, Toyota Information Technology Center (T-ITC), and Symtavision GmbH. The goal of the projects was to develop efficient methods for calculating the reliability of automotive communication systems with respect to real-time requirements. Feasibility of reliability analysis for real-world systems could be demonstrated based on different CAN bus examples provided by Toyota-ITC. All these R&D activities were focused on realistic use cases and resulted in a better understanding of the industry's problems and requirements by the research community and of the research outcome by the industrial partners.

Participating partners:

- TU Braunschweig.

  TU Braunschweig investigates synergies in the coupling of methods and implements prototypical implementations of the research results.

- Symtavision GmbH.

  Symtavision is the commercial co-developer of the tool framework. A focus within ArtistDesign is the coupling of with other industrially available tools (such as aiT).

- ETHZ.

  Collaboration on the coupling of MPA and SymTA/S with respect to modelling of hierarchical event models.

- Absint GmbH.

  The aiT tool supplies task timing models, which are required for system level analysis.

Web
http://www.symtavision.com/
http://www.ida.ing.tu-bs.de/index.php?id=symtas
http://www.ida.ing.tu-bs.de/en/research/projects/accord/

Related Publications

1. Simon Schliecker and Arne Hamann and Razvan Racu and Rolf Ernst. "Formal Methods for System Level Performance Analysis and Optimization." In *Proc. of the Design Verification Conference (DVCon)*, San José, CA, February 2008.

2. Jonas Rox and Rolf Ernst. "Modeling Event Stream Hierarchies with Hierarchical Event Models." In Proc. Design, Automation and Test in Europe (DATE 2008), March 2008.
3. Mircea Negrean, Simon Schliecker and Rolf Ernst, **"Response-Time Analysis of Arbitrarily Activated Tasks in Multiprocessor Systems with Shared Resources,"** in Proc. of Design, Automation, and Test in Europe (DATE), (Nice, France), April 2009
4. Simon Schliecker, Mircea Negrean and Rolf Ernst, **"Bounding the Shared Resource Load for the Performance Analysis of Multiprocessor Systems,"** in *Proc. of Design, Automation, and Test in Europe (DATE)*, (Dresden, Germany), March 2010
5. Mircea Negrean, Simon Schliecker and Rolf Ernst, "**Timing Implications of Sharing Resources in Multicore Real-Time Automotive Systems**," in *SAE World Congress*, vol. System Level Architecture Design Tools and Methods (AE318), (Detroit, MI, USA), April 2010 *(this paper was selected for SAE Journals – see next publication)*
6. Mircea Negrean, Simon Schliecker, and Rolf Ernst, **"Timing Implications of Sharing Resources in Multicore Real-Time Automotive Systems,"** *SAE International Journal of Passenger Cars - Electronic and Electrical Systems*, vol. 3, No. 1, pp. 27-40, August 2010 *(previous publication was selected for SAE Journals)*

-- Changes wrt Y3 deliverable --

No changes with respect to Year 3.

4.4.2 Tool: Analysis and optimisation framework for fault tolerant distributed embedded systems

Objectives

Linköping University and DTU are working on an environment and tool-set for the analysis and design optimisation of safety critical, fault tolerant real-time embedded applications. The emphasis is on the issue of transient faults and the goal is to develop tools for scheduling, mapping, and system optimisation.

Main results

A strategy for the synthesis of fault tolerant schedules has been developed. It can handle both hard and soft real-time tasks. The goal is to guarantee the deadlines for the hard processes even in the case of faults, while maximizing the overall utility. Time/utility functions are used to capture the utility of soft processes. Process re-execution is employed to recover from multiple faults. A single static schedule computed off-line is not fault tolerant and is pessimistic in terms of utility, while a purely online approach, which computes a new schedule every time a process fails or completes, incurs an unacceptable overhead. Thus, a quasi-static scheduling strategy is used, where a set of schedules is synthesized off-line and, at run time, the scheduler will select the right schedule based on the occurrence of faults and the actual execution times of processes. An optimisation technique for the generation of schedule tables supporting such a quasi-static scheduling approach has been developed and implemented.

Current work

Ongoing work is towards development of cost-optimisation techniques by considering processors with various hardening levels and the associated tradeoffs.

During the second **year DTU** and **Linköping** have continued their cooperation related to the design and optimisation of fault tolerant mixed hard/soft real-time systems. During the second

year the emphasis of the work has been on the analysis and optimisation of fault-tolerant hard real-time embedded systems, based on an approach in which hardware and software fault tolerance techniques are combined. The basic trade-off is between processor hardening in hardware and process re-execution in software which, together, have to provide the required levels of fault tolerance against transient faults with the lowest-possible system costs.

The goal for the third year is the development of new optimisation approaches for implementation of error detection techniques.

Participating partners

Linköping: Scheduling techniques, fault tolerant systems, design optimisation.

DTU: System level optimisation techniques

Publications

1. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Synthesis of Flexible Fault-Tolerant Schedules with Preemption for Mixed Soft and Hard Real-Time Systems”, 11th EUROMICRO CONFERENCE on DIGITAL SYSTEM DESIGN (DSD 2008), Parma, Italy, September 3-5, 2008, pp. 71-80.
2. Petru Eles, Viacheslav Izosimov, Paul Pop, Zebo Peng, “Synthesis of Fault-Tolerant Embedded Systems”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, pp. 1117-1122.
3. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Scheduling of Fault-Tolerant Embedded Systems with Soft and Hard Timing Constraints”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, 915-920.
4. P. Pop, V. Izosimov, P. Eles, and Z. Peng. Design Optimization of Time- and Cost-Constrained Fault-Tolerant Embedded Systems with Checkpointing and Replication. IEEE Transactions on Very Large Scale Integrated (VLSI) Systems, 17(3):389-402. 2009.
5. V. Izosimov, I. Polian, P. Pop, P. Eles, and Z. Peng. Analysis and Optimization of Fault-Tolerant Embedded Systems with Hardened Processors. Proceedings of DATE: Design Automation and Test in Europe, IEEE, 2009, pp. 682 – 687.Tool or Platform :

-- Changes wrt Y3 deliverable --

No changes with respect to Year 3.

4.4.3 Tool: MPMH – an integration of MPA parallelization assistant and MH static memory allocation for MPSoC

Objectives

The main objectives of the framework is to offer an automatic source code parallelization (MPA tool) and memory hierarchy management (MH tool) in order to map efficiently embedded software application on MPSoC platforms. In order to tackle MPSoC programming issues in a MPSoC platform in an efficient way, a single tool performing optimized memory allocation (MH) and parallelizing sequential code (MPA) is an ideal solution. This tool suite is also used in the Platform and MPSoC Design cluster.

Main Results

The following challenges appear when integrating MPA and MH:
• information flow between MPA and MH
• interference between analyses and transformations of both tools

• MPA is not platform-aware and as a result may ruin the benefits obtained by MH
• profiling information (sequential) is hard to match with the parallelized code
• no optimization interactions between MPA and MH possible with the present implementation.

The integrated MPMH tool addresses these challenges and performs common data analyses from both tools, dependent on the Atomium Analysis framework, only once.

Current work
Currently, the affiliated partners of IMEC (ie, DUTH/ICCS and TU/e) and core partners (TUDortmund/ICD and KTH) are trying to integrate their tool and design flows with the IMEC MPA + MH MPSoC mapping framework in the memory and interconnect specific context of the MNEMEE and MOSART FP7 projects, respectively.

Participating partners:

- DUTH/ICCS This partner is integrating the dynamic data type and dynamic memory management tools and design flows with the IMEC MPSoC mapping tool flows.
- TUDortmund/ICD This partner is integrating its pre-compiler and compiler framework to the static MH tool of IMEC.
- TU/e This partner is integrating its SDF3 framework in the context of system scenarios with the IMEC MPSoC mapping tool flows.
- KTH This partner is integrating its NoC simulation and exploration framework with the MPA tool of IMEC.

Web
http://www.mnemee.org/
http://www.mosart-project.org/

Related Publications
Daniel Cordes, Peter Marwedel, and Arindam Mallik. Automatic Parallelization of Embedded Software Using Hierarchical Task Graphs and Integer Linear Programming. In *Proceedings of CODES+ISSS, 2010)*, Scottsdale / US, October 2010. (Also reported in the SSCGTA Cluster deliverable)

-- Changes wrt Y3 deliverable --

No changes with respect to Year 3.

4.4.4 Tool: MoVES - Modelling and Verification of Embedded Systems

Objectives
The MoVES framework is being developed to assist in the early phases of embedded systems design. The framework can be used to conduct schedulability analysis and has the potential to reason about different types of resource usage such as memory usage and power consumption.

Main Results
In several projects (MoDES, DaNES, ARTIST2, ArtistDesign) a model-based approach to analysis of embedded systems has been analyzed. This has resultet in the MoVES framework, which is now available online. The framework consists of a model- and a trace generator. From a system specification MoVES builds a model suitable for verification using an external verification back-end. In the case of e.g. verified non-schedulability, the trace generator provides the user with an understandable trace that leads to a missed deadline of the system.

Current work
The current version of the framework is based on a simple specification language where a system is modelled as an application running on an execution platform. The application is modelled through the individual tasks, and the execution platform is modelled through the processing elements, including the operating systems, and their interconnections. The tasks and processing elements are characterized by their real-time properties. Currently, verification can be conducted using two different verification back-ends, a) the original Uppaal model-checker for timed-automata models and b) a developmental Uppaal model-checker for stop-watch automata.

Participating partners:

- DTU: Provides the MoVES development environment.
- AAU: Provides the UPPAAL verification engine

Web
http://www.imm.dtu.dk/moves

Related Publications

1. Aske Brekling, Michael R. Hansen, Jan Madsen, MoVES - A Framework for Modelling and Verifying Embedded Systems, The 21st International Conference on Microelectronics, Marrakech, Morocco, 2009
2. Jan Madsen, Michael R. Hansen, Aske W. Brekling, A Modelling and Analysis Framework for Embedded Systems, Model-Based Design of Heterogeneous Embedded Systems, CRC Press, 2009
3. Aske Brekling, Michael R. Hansen, Jan Madsen, Analysis of Quantitative Properties of Hardware Specifications, The 21st Nordic Workshop on Programming Theory, Technical University of Denmark, 2009

-- Changes wrt Y3 deliverable --

No changes with respect to Year 3.

4.4.5 Tool: MPA (Modular Performance Analysis)

Objectives
The tool MPA (modular performance analysis) is based on an extension of network calculus that is termed real-time calculus (RTC). The purpose of the tool is to perform an end-to-end real-time analysis of complex distributed embedded systems. The implementation is based on a Java mathematical library for max-+ algebra with an associated Matlab interface.

Main Results
Within ARTISTDesign, the MPA tool box has been (a) extended towards the new results together with University Braunschweig (TUBS) related to hierarchical event streams and (b) it has been linked to the Symta/S tool suite as described above. In addition, the toolbox has been used in the context of various application studies from avionic and automotive domain.

Current work
We are currently working towards linking the toolbox to other performance analysis frameworks, e.g. UPPAAL from Uppsala University (Wang Yi, Bengt Jonsson). Some first promising results are available already. In addition, we are intending to use the method to investigate the interaction between memory access and computations in MPSoC platforms. This will be continued together with University Saarland (Reinhard Wilhelm).

Participating partners
- ETHZ: Provides and maintains the MPA toolbox
- TUBS: Link to the Symta/S tool suite, development of algorithms and methods for hierarchical event stream analysis.

Web
http://www.mpa.ethz.ch/

Related Publications
ETHZ: Kai Lampka, Simon Perathoner, Lothar Thiele: Analytic Real-Time Analysis and Timed Automata: A Hybrid Method for Analyzing Embedded Real-Time Systems. 8th ACM & IEEE International conference on Embedded software, EMSOFT 2009, CD edition, ACM, Grenoble, France, pages 107-116, October, 2009.

ETHZ: Lothar Thiele, Nikolay Stoimenov: Modular Performance Analysis of Cyclic Dataflow Graphs. EMSOFT 09: Proceedings of the 9th ACM international conference on Embedded software, Grenoble, France, pages 127-136, October, 2009.

ETHZ & TUBS: Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: Influence of Different Abstractions on the Performance Analysis of Distributed Hard Real-Time Systems Design Automation for Embedded Systems, Springer Science+Business Media, LLC, Vol. 13, No. 1, pages 27-49, June, 2009.

ETHZ & TUBS: Simon Perathoner, Tobias Rein, Lothar Thiele, Kai Lampka and Jonas Rox: Modeling Structured Event Streams in System Level Performance Analysis, submitted to Conference on Languages, Compilers, and Tools for Embedded Systems LCTES, Stockholm, Sweden, April 2010

-- Changes wrt Y3 deliverable --

No changes with respect to Year 3.

4.4.6 Tool: DOL (Distributed Operation Layer)

Objectives

The DOL environment is a complete high-level compilation environment for MPSoC platforms. It consists of a graphical input specification interface for (a) application and (b) platform, a link to analytic performance analysis based on MPA, a simulation environment based on MPARM (Univeristy Bologna, Luca Benini) and a multi-objective optimization environment based on PISA (http://www.tik.ethz.ch/~sop/pisa/) for mapping (binding of application components to computation resources and communication links to paths on the platform). The environment has been successfully used to map complex applications to various platforms such as IBM Cell, MPARM (UNIBO) and ATMEL Diopsys.

Main Results

In the framework of ARTISTDesign, the DOL environment has been successfully linked and coupled to the MPARM simulation and design environment from University Bologna. This way, DOL could be used for ARM-based MPSoC architectures and extended with a state-of-the-art simulation environment. Main results are the comparison of analytic performance analysis with simulation-based performance numbers.

Current work

In the future, the coupling between MPARM and DOL will be used in order to investigate new concepts for predictable and efficient communication fabrics, including intelligent DMA controllers, scratchpad memories and flexible TDMA scheduling policies.

Participating Partners

ETH: Provides the DOL software development environment.

UNIBO: Provides the MPARM environment, including simulation capabilities and new concepts for predictable communication fabrics.

Web

http://www.tik.ee.ethz.ch/~shapes/dol.html

Related Publications

W. Haid, K. Huang, I. Bacivarov, and L. Thiele. Multiprocessor SoC Software Design Flows. IEEE Signal Processing Magazine, vol. 26, no. 6, pp. 64—71, Nov. 2009.

W. Haid, L. Schor, K. Huang, I. Bacivarov, and L. Thiele. Efficient Execution of Kahn Process Networks on Multi-Processor Systems Using Protothreads and Windowed FIFOs. In Proc. IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia), pages 35—44, Grenoble, France, Oct. 2009.

W. Haid, M. Keller, K. Huang, I. Bacivarov, and L. Thiele. Generation and Calibration of Compositional Performance Analysis Models for Multi-Processor Systems. In Proc. Int'l Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), pages 92—99, Samos, Greece, July 2009. Awarded the Stamatis Vassiliadis Best Paper Award.

K. Huang, I. Bacivarov, J. Liu, and W. Haid. A Modular Fast Simulation Framework for Stream-Oriented MPSoC. In IEEE Symposium on Industrial Embedded Systems (SIES), pages 74—81, Lausanne, Switzerland, July 2009.

-- Changes wrt Y3 deliverable --

No changes with respect to Year 3.

4.4.7 Platform: Multicore Network on Chip Platform (McNoC)

Objectives

KTH is developing a comlete multi-core platform based on an NoC with a distributed and shared/private memory system.

Main results

A communication network with adaptive routing has been developed. Also, a programmable controller for memory and data management, called Data Management Engine (DME), has been developed and implemented. The DME, together with the Leon3 processor is part of every node. It manages the local memory and provides access to remote and off-chip memory. Furthermore, a dynamically configurable globally ratio-chronous-locally synchrounous clocking has been integrated. Finally a hierarchical power management scheme is part of the platform. The platform is modeld in Verilog/VHDL.

On the DME (as DME microcode) a cache coherency schem, several memory consistency models, a virtual address space support, and a dynamic memory allocation library has been implemented.

Current work

Ongoing work focuses on scalable and distributed cache coherency algorithms, that can by used for heterogeneous SoCs. Of particular interest are coherence mechanisms that can integrate different local cache controllers and policies in the different nodes.

Participating partners:

KTH working on the overall platform development

NTUA in Athens on dynamic memory allocation;

partners outside the NoE: NUDT, China on DME hardware.

Publications:

1. Xiaowen Chen, Zhonghai Lu, Axel Jantsch, and Shuming Chen, "Supporting Distributed Shared Memory on Multi-core Network-on-Chips Using a Dual Microcoded Controller", Proceedings of the confernece for Design Automation and Test in Europe, Dresden, Germany, March 2010.
2. Xiaowen Chen, Zhonghai Lu, Axel Jantsch, and Shuming Chen, "Supporting Efficient Synchronization in Multi-core NoCs Using Dynamic Buffer Allocation Technique", Proceedings of the IEEE Annual Symposium on VLSI, Kefalonia, Greece, July 2010.
3. Xiaowen Chen, Zhonghai Lu, Axel Jantsch, and Shuming Chen, "Handling Shared Variable Synchronization in Multi-core Network-on-Chip with Distributed Memory", International SOC Conference, Las Vegas, Nevada, September 2010.
4. Xiaowen Chen, Shuming Chen, Zhonghai Lu, and Axel Jantsch, "Area and Performance Optimization of Barrier Synchronization on Multi-core Network-on-Chips", 3rd IEEE International Conference on Computer and Electrical Engineering (ICCEE), Chengdu, China, November 2010.
5. Xiaowen Chen, Zhonghai Lu, Shuming Chen, and Axel Jantsch, "Run-time Partitioning of Hybrid Distributed Shared Memory on Multi-core Network-on-Chips", The 3rd IEEE

International Symposium on Parallel Architectures, Algorithms and Programming (PAAP 2010), Dalian, China, December 2010.

6. Xiaowen Chen, Shuming Chen, Zhonghai Lu, and Axel Jantsch, "Multi-FPGA Implementation of a Network-on-Chip Based Many-core Architecture with Fast Barrier Synchronization Mechanism", Proceedings of the IEEE Norchip Conference, Tampere, Finland, November 2010.
7. Bernard Candaele, Sylvain Aguirre, Michel Sarlotte, Iraklis Anagnostopoulos, Sotirios Xydis, Alexandros Bartzas, Dimitris Bekiaris, Dimitrios Soudris, Zhonghai Lu, Xiaowen Chen, Jean-Michel Chabloz, Ahmed Hemani, Axel Jantsch, Geert Vanmeerbeeck, Jari Kreku, Kari Tiensyrja, Fragkiskos Ieromnimon, Dimitrios Kritharidis, Andreas Wiefrink, Bart Vanthournout, and Philippe Martin, "Mapping Optimisation for Scalable multi-core ARchiTecture: The MOSART approach", Proceedings of the IEEE Annual Symposium on VLSI, Kefalonia, Greece, July 2010.
8. Abdul Naeem, Xiaowen Chen, Zhonghai Lu, and Axel Jantsch, "Scalability of Weak Consistency in NoC based Multicore Architectures", Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Paris, France, June 2010.
9. Chaochao Feng, Jinwen Li, Zhonghai Lu, Axel Jantsch, and Minxuan Zhang. Evaluation of deflection routing on various NoC topologies. In *Proceedings of the IEEE International Conference on ASIC (ASICON)*, Xiamen, China, October 2011.
10. Wenmin Hu, Zhonghai Lu, Axel Jantsch, Hengzhu Liu, Botao Zhang, and Dongpei Liu. Network-on-chip multicasting with low latency path setup. In *Proceedings of the VLSI-SoC Conference*, October 2011.
11. Fahimeh Jafari, Axel Jantsch, and Zhonghai Lu. Output process of variable bit-rate flows in on-chip networks based on aggregate scheduling. In *Proceedings of the International Conference on Computer Design*, Amherst, Massachusetts, USA, October 2011.
12. Abdul Naeem, Axel Jantsch, Xiaowen Chen, and Zhonghai Lu. Realization and scalability of release and protected release considtency models in noc based systems. In *Proceedings of the Euromicro Conference on Digital Systems Design (DSD)*, Oulu, Finland, September 2011.
13. Chaochao Feng, Zhonghai Lu, Axel Jantsch, Minxuan Zhang, Jinwen Li, and Jiang Jiang. A low-overhead fault-aware deflection routing algorithm for 3D network-on-chip. In *Proceedings of the IEEE Annual Symposium on VLSI (ISVLSI)*, Chennai, India, July 2011.
14. Matt Grange, Roshan Weerasekera, Dinesh Pamunuwa, Axel Jantsch, and Awet Yemane Waldezione. Optimal network architectures for minimizing average distance in k-ary n-dimensional mesh networks. In *Proceedings of the Networks on Chip Symposium (NoCS)*, Pittsburgh, Pennsylvania, USA, May 2011.
15. Xiaowen Chen, Zhonghai Lu, Axel Jantsch, Shuming Chen, and Hai Liu. Cooperative communication based barrier synchronization in on-chip mesh architectures. *IEICE Electronics Express*, 8(22):1856-1862, 2011.
16. Iraklis Anagnostopoulos, Sotirios Xydis, Alexandros Bartzas, Zhonghai Lu, Dimitrios Soudris, and Axel Jantsch. Custom microcoded dynamic memory management for distributed on-chip memory organizations. *IEEE Embedded Systems Letters*, 2011.
17. Bernard Candaele, Sylvain Aguirre, Michel Sarlotte, Iraklis Anagnostopoulos, Sotirios Xydis, Alexandros Bartzas, Dimitris Bekiaris, Dimitrios Soudris, Zhonghai Lu, Xiaowen Chen, Jean-Michel Chabloz, Ahmed Hemani, Axel Jantsch, Geert Vanmeerbeeck, Jari Kreku, Kari Tiensyrja, Fragkiskos Ieromnimon, Dimitrios Kritharidis, Andreas Wiefrink,

Bart Vanthournout, and Philippe Martin. The MOSART mapping optimization for multi-core architectures. In *Designing Very Large Scale Integration Systems: Emerging Trends and Challenges*. Springer, 2011.

18. Wenmin Hu, Zhonghai Lu, Axel Jantsch, and Hengzhu Liu. Power-efficient tree-based multicast support for networks-on-chip. In *Proceedings of the Asian Pacific Design Automation Conference (ASPDAC)*, Tokyo, Japan, January 2011.
19. Axel Jantsch, Xiaowen Chen, Abdul Naeem, Yuang Zhang, Sandro Penolazzi, and Zhonghai Lu. Memory architecture and management in an NoC platform. In Axel Jantsch and Dimitrios Soudris, editors, *Scalable Multi-core Architectures: Design Methodologies and Tools*. Springer, 2011.
20. Abdul Naeem, Xiaowen Chen, Zhonghai Lu, and Axel Jantsch. Realization and performance comparison of sequential and weak memory consistency models in network-on-chip based multi-core systems. In *Proceedings of the 16th Asian Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Japan, January 2011.
21. Axel Jantsch and Dimitrios Soudris, editors. *Scalable Multi-core Architectures: Design, Methodologies, and Tools*. Springer, 2011.

-- Changes wrt Y2 deliverable --

Publications list updated.

4.4.8 Tool: Formal System Design (ForSyDe)

Objective
A modelling framework for heterogeneous SoC that allows to model HW and SW at different timing abstractions from continuous time to untimed. The semantic is formally defined and is the basis for formal design transformations, analysis, and synthesis.

Main results
The modelling framework has been defined and experimental implementation has been implemented in Haskell. It support continuous timed, discrete timed, synchronous and untimed Models of Computation. A VHDL back-end supports synthesis of synchronous models into HW. Several design transformations have been formulated and realized.

Current work
Ongoing work focuses on reformulating the discrete timed MoC for more efficient modelling, Also, the framework is being implemented in SystemC as a set of templates and modelling rules.

Participating partners:
- KTH: works on the SystemC implementation
- DTU: focuses on the discrete timed MoC

Publications:

1. Jun Zhu, Ingo Sander, and Axel Jantsch, "Performance analysis of reconfigurations in adaptive real-time streaming applications", ACM Transactions in Embedded Computing Systems -- Special issue on Embedded Systems for Real-time Multimedia, 2010.
2. Jun Zhu, Ingo Sander, and Axel Jantsch, "Pareto Efficient Design for Reconfigurable Streaming Applications on CPU/FPGAs", Proceedings of Design Automation and Test in Europe (DATE '10), Dresden, Germany, March 2010.
3. Jun Zhu, Ingo Sander, and Axel Jantsch, "Constrained Global Scheduling of Streaming Applications on MPSoCs", Proceedings of the conference on Asia South Pacific Design Automation (ASP-DAC '10), Taipei, Republic of China, January 2010.
4. Jun Zhu, Ingo Sander, and Axel Jantsch, "HetMoC: Heterogeneous Modeling in SystemC", Proceedings of the Forum on Design Langauges (FDL), Southhampton, UK, September 2010.
5. Seyed Hosein Attarzadeh Niaki and Ingo Sander. Semi-formal refinement of heterogeneous embedded systems by foreign model integration. In *2011 Forum on Specification and Design Languages (FDL)*, pages 1-8. IEEE, September 2011.
6. Seyed Hosein Attarzadeh Niaki and Ingo Sander. Co-simulation of embedded systems in a heterogeneous MoC-based modeling framework. In *2011 6th IEEE International Symposium on Industrial Embedded Systems (SIES)*, pages 238-247. IEEE, June 2011.
7. M. K. Jakobsen, J. Madsen, S. H. A. Niaki, I. Sander, J. Hansen, “System level modeling with open source tools”, to appear in proceedings of Embedded World 2012.

-- Changes wrt Y3 deliverable --

Publications list updated.

4.5 Design for Adaptivity Transversal Activity

4.5.1 SWEET (SWEdish Execution Time tool)

Objectives

SWEET is a WCET analysis tool. It is an academic prototype: the main objective is to use it as a test bench for methods in WCET analysis, and then mainly flow analysis to produce program flow constraints (upper bounds on # of loop iterations, information about infeasible paths, etc.).

Main Results

SWEET has been used to develop and test various methods for constraining program flow. It has also been used in industrial case studies. The results indicate that the developed methods do improve on the number of automatically detected program flow constraints, as well as on the precision of the resulting WCET bound. Recently, SWEET has been reengineered to use the "ALF" format for its flow analysis, and it has been provided with backends to generate program flow constraints for the commercial WCET analysis tools aiT and RapiTime from AbsInt GmbH and Rapita Systems Ltd, respectively. Translators to ALF from C, and the PPC and NECV850 binary formats, have been implemented as well.

Current work

A version of SWEET that performs parametric WCET analysis has been implemented. This version handles arithmetic wraparounds correctly. An alternative C-to-ALF translator, which uses the LLVM compiler framework, has also been implemented.

Participating partners:

- Mälardalen University

  Maintains and develops SWEET, develops methods for parametric WCET analysis.
- Technical University of Vienna

  LLVM to ALF translator, use of SWEET.

Web

http://www.mrtc.mdh.se/projects/wcet/sweet.html

4.5.2 Hardware setup to demonstrate self-protection and adaptability of embedded Real-Time Systems

Objectives

A demonstrator for self-protection and adaptability in real-time systems is being developed. It demonstrates the feasibility and cost of run-time adaptation and protection with respect to performance metrics such as end-to-end latencies. Furthermore, the demonstrator acts as a platform to evaluate performance of the proposed methodologies.

Main Results

The demonstrator consisting of a timing sensitive control application as well as a second disturbing application (audio streaming) has been completed and is used to show self-

protection (audio streaming is denied access to the system) as well as self-configuration using the optimization techniques developed last year (audio streaming is allowed at low priority).

The demonstrator has been extended by a memory protection scheme using the available MMU of the PPC603e core, which efficiently isolates the runtime environment from user applications as well as user applications from each other.

Participating partners:

- TU Braunschweig
- Symtavision GmbH
- Universität Erlangen

Related Publications

Moritz Neukirchner, Steffen Stein, Harald Schrom, Johannes Schlatow, Rolf Ernst. Contract-Based Dynamic Task Management for Mixed-Criticality Systems, 6th IEEE International Symposium on Industrial Embedded Systems (SIES), 2011

Moritz Neukirchner, Steffen Stein, Rolf Ernst. The EPOC Architecture – Enabling Evolution under Hard Constraints. In Organic Computing – A Paradigm Shift for Complex Systems, Birkhäuser Science, 2011

4.5.3 TrueTime

Objectives

To provide a flexible simulation platform for networked embedded real-time systems with a particular focus on control applications. TrueTime implements simulation models for a multi-tasking real-time kernel and data link layer network protocols that execute embedded in the Matlab/Simulink environment. Using TrueTime it is possible to experiment with adaptive resource management and network protocols and investigate how this influence application performance.

Current work

- Support for simulation of WirelessHART networks is being added in collaboration with ABB Corporate Research (Alf Isaksson)

- Work on porting the entire TrueTime toolbox from Simulink to Modelica has been initiatied in collaboration with Vanderbilt University (Janos Sztipanovits) as a part of the DARPA META-2/FANG programme. The goal is to port the TrueTime S-function blocks into the FMI/FMU format supported by Modelica, and in particular the two open-source versions of Modelica: JModelica and OpenModelica. The main part of this work will start in February 2012.

Interoperability

The TrueTime simulator from ULUND will be part of the META integrated tool chain for model-based development of cyber-physical systems, currently being developed by Vanderbilt University within the DARPA project AVM (Adaptive Vehicle Make).

Adaptivity is a cross-cutting property that affects all the stages of embedded system development. The tools and platforms listed in the Adaptivity deliverable all address quite separate parts of embedded system design, so separate that tool interoperability is not a realistic issue.

Participating partners:

- ULUND
  Toolbox development.
- SSSA, TUKL, Aveiro, KTH ...
  Users of the toolbox

Web

http://www3.control.lth.se/truetime/

4.5.4 Other Tools and Platforms

Fault Tolerant Nostrum (KTH)

The KTH Network-on-Chip has been developed into a complete fault tolerant platform, based on adaptive routing, that can tolerate transient, intermittent, and permanent faults with a

combination of techniques at the link, the network and the transport layer. The cost-performance-robustness trade-off is appealing. With added area cost of around 10% a significant number of faults can be tolerated with low performance and power penalty.

Web site: http://www.ict.kth.se/nostrum

SPARTS: Comparing Schedulers and Power Management Strategies (IPPorto)

SPARTS aims at providing a solid framework to simulate scheduling mechanisms and power management strategies of a generic real-time device. This does not provide an ISA, but rather captures behaviour via abstract parameters, like execution time of a particular job, concrete inter arrival time of a job. Great care was taken to model overheads in the system when it comes to power management and context switches and such. Additionally a focus was set on the difference between worst-case task parameters and concrete parameters of a specific job of that task.

http://www.cister.isep.ipp.pt/projects/sparts/

4.5.5 Multimedia Use Case

Within the ACTORS project on “Adaptivity and Resource Management in Embedded Systems”, resource management for multimedia applications executing on smart phones has been used as the main use case. For this use case a tool chain involving dataflow modelling, design space exploration, model transformation, automatic code generation, and dynamic resource management has been developed.

-- Changes wrt Y3 deliverable --

The text above only contains the tools / platforms for which something significant has changed with respect to previous years. Tools such as SHARK, ERIKA or ForSyDe mentioned in the earleri deliverables are still of relevance to this activity.

4.6 Design for Predictability Transversal Activity

4.6.1 Tool or Platform: aiT

Objectives

aiT is the leading tool for computing worst case execution times (WCETs).

Main Results

A prototype implementation of the UCB computation as developed by Saarland University has been integrated by AbsInt into the aiT Timing Analyzer. The analysis is implemented for the ARM7 and has been tested on smaller benchmark programs.

Current work

Current work is concerned with optimising the performance of the analysis and exploring its potential on larger examples. Implementations for other processors are also underway.

Web
http://www.absint.com/

Related publications:

Daniel Grund, Jan Reineke, Reinhard Wilhelm: A Template for Predictability Definitions with Supporting Evidence. PPES 2011: 22-31

Daniel Grund, Jan Reineke, Gernot Gebhard: Branch target buffers: WCET analysis framework and timing predictability. Journal of Systems Architecture - Embedded Systems Design 57(6): 625-637 (2011)

Pascal Montag, Sebastian Altmeyer: Precise WCET calculation in highly variant real-time systems. DATE 2011: 920-925

Ernst Althaus, Sebastian Altmeyer, Rouven Naujoks: Symbolic Worst Case Execution Times. ICTAC 2011: 25-44

Ernst Althaus, Sebastian Altmeyer, Rouven Naujoks: Precise and efficient parametric path analysis. LCTES 2011: 141-150

Sebastian Altmeyer, Claire Maiza: Cache-related preemption delay via useful cache blocks: Survey and redefinition. Journal of Systems Architecture - Embedded Systems Design 57(7): 707-719 (2011)

Christoph Cullmann: Cache persistence analysis: a novel approachtheory and practice. LCTES 2011: 121-130

Gernot Gebhard, Christoph Cullmann, Reinhold Heckmann: Software Structure and WCET Predictability. PPES 2011: 1-10

Sebastian Altmeyer, Robert Davis and Claire Maiza: Cache-Related Pre-Emption Delay Aware Response Time Analysis For Fixed Priority Pre-Emptive Systems, IEEE RTSS, Vienna 2011

4.6.2 Tool or Platform: WCC

Objectives

WCC is the leading WCET-aware compiler. The WCET analyzer aiT has been tightly integrated into the compiler.

Main Results

In the course of ArtistDesign, WCC has matured and is currently evaluated in an industrial context. WCC's single-task WCET-aware optimizations developed during ArtistDesign are able to outperform well-established compilers like e.g. the GCC. First steps towards WCET-aware compilation for multi-task systems are made, more work in this area and towards support of multi-core systems will be done in the near future.

Current work

The current work explores the optimization potential of WCC and extends it towards multi-task and multi-core systems.

Participating partners:

- TU Dortmund
  TU Dortmund integrates aiT into WCC and explores the optimization potential.
- AbsInt, Saarbrücken
  AbsInt provides aiT.

Web
http://ls12-www.cs.tu-dortmund.de/research/activities/wcc/

Related Publications

Heiko Falk and Helena Kotthaus. WCET-driven Cache-aware Code Positioning. *In Proceedings of the International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, pages 145-154, Taipei, Taiwan, October 2011 (best paper candidate)

Sascha Plazar, Jan C. Kleinsorge, Heiko Falk and Peter Marwedel. WCET-driven Branch Prediction aware Code Positioning. *In Proceedings of the International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, pages 165-174, Taipei, Taiwan, October 2011.

Jan C. Kleinsorge, Heiko Falk and Peter Marwedel. A Synergetic Approach To Accurate Analysis Of Cache-Related Preemption Delay. *In Proceedings of the International Conference on Embedded Software (EMSOFT)*, pages 329-338, Taipei, Taiwan, October 2011.

Samarjit Chakraborty, Marco Di Natale, Heiko Falk, Martin Lukasiewyzc and Frank Slomka. Timing and Schedulability Analysis for Distributed Automotive Control Applications. *In Tutorial at the International Conference on Embedded Software (EMSOFT)*, pages 349-350, Taipei, Taiwan, October 2011.
Heiko Falk, Norman Schmitz and Florian Schmoll. WCET-aware Register Allocation based on Integer-Linear Programming. *In Proceedings of the 23rd Euromicro Conference on Real-Time Systems (ECRTS)*, pages 13-22, Porto / Portugal, July 2011.

Paul Lokuciejewski, Sascha Plazar, Heiko Falk, Peter Marwedel and Lothar Thiele. Approximating Pareto optimal compiler optimization sequences---a trade-off between WCET, ACET and code size. *Software: Practice and Experience*, May 2011. DOI 10.1002/spe.1079

4.6.3 Tool or Platform : MAST

Objectives

The main objective of MAST is to provide a model to describe the timing behaviour of real-time applications, in such a way that automatic schedulability analysis can be performed to assess the ability of the application to meet all of its timing requirements. Also an objective is that this real-time model can be obtained from a more detailed design model described, for instance, in MARTE, the UML profile for real-time embedded systems.

Main Results

MAST defines a model to describe the timing behaviour of real-time systems designed to be analysable via schedulability analysis techniques. MAST also provides an open-source set of tools to perform schedulability analysis or other timing analysis, with the goal of assessing whether the system will be able to meet its timing requirements, and, via sensitivity analysis, how far or close is the system from meeting its timing requirements. Tools are also provided to help the designer in the assignment of scheduling parameters. By having an explicit model of the system and automatic analysis tools it is also possible to perform design space exploration. A discrete event simulator is also provided to obtain statistical performance information of the modelled system.

Current work

The original MAST model is now being enhanced to accommodate new modelling capabilities, partition-based scheduling as one of the base policies to use in the hierarchical scheduling modelling capabilities, support for clock synchronization, and support for resource reservation techniques. The new model is called MAST-2. The discrete event simulator has been redesign to accommodate the new MAST-2 model, and the schedulability analysis tools are being updated.

Participating partners:

- University of Cantabria

Web

http://mast.unican.es/

4.6.4 Tool or Platform : MPA (Modular Performance Analysis)

Objectives

The tool MPA (modular performance analysis) is based on an extension of network calculus that is termed real-time calculus (RTC). The purpose of the tool is to perform an end-to-end real-time analysis of complex distributed embedded systems. The implementation is based on a Java mathematical library for max-+ algebra with an associated Matlab interface.

Main Results

Within ARTISTDesign, the MPA tool box has been (a) extended towards the new results together with University Braunschweig (TUBS) related to hierarchical event streams and (b) it has been linked to the Symta/S tool suite as described above. In addition, the toolbox has been used in the context of various application studies from avionic and automotive domain.

In the 4th year of ARTISTDesign, the toolbox has been linked to other performance analysis frameworks, in partciular UPPAAL from Uppsala University (Wang Yi, Bengt Jonsson). Some first promising results are available already. Especially, we have been investigating the interaction of memory accesses on the bus- and memory system of multi-core platforms. To this end, we developed a block-based representation of applications (super-block- model) and analysed the worst-case response time of corresponding tasks.

In addition, we used the method to investigate the interaction between memory access and computations in MPSoC platforms. This work has been undertaken together with University Saarland (Reinhard Wilhelm). In particular, the WCET analysis results have been used to calibrate the higher level performance analysis, i.e. to determine (a) worst case cycle counts for processing and (b) worst-case memory accesses.

All the corresponding interfaces and analysis methods have been implemented in the toolbox in the 4th year of ARTISTDesign and are now openly available.

Future work

The MPA toolbox has reached a certain level of maturity. It is in use for education and has been central to several international projects like SHAPES and COMBEST. It will be extended on demand with new functions, especially for the analysis of mixed criticality systems.

Participating partners

ETHZ: Provides and maintains the MPA toolbox

TUBS: Link to the Symta/S tool suite, development of algorithms and methods for hierarchical event stream analysis.

Web

http://www.mpa.ethz.ch/

Related Publications

ETHZ: Kai Lampka, Simon Perathoner, Lothar Thiele: Analytic Real-Time Analysis and Timed Automata: A Hybrid Method for Analyzing Embedded Real-Time Systems. 8th ACM & IEEE International conference on Embedded software, EMSOFT 2009, CD edition, ACM, Grenoble, France, pages 107-116, October, 2009.

ETHZ: Lothar Thiele, Nikolay Stoimenov: Modular Performance Analysis of Cyclic Dataflow Graphs. EMSOFT 09: Proceedings of the 9th ACM international conference on Embedded software, Grenoble, France, pages 127-136, October, 2009.

ETHZ & TUBS: Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: Influence of Different Abstractions on the Performance Analysis of Distributed Hard Real-Time Systems Design Automation for Embedded Systems, Springer Science+Business Media, LLC, Vol. 13, No. 1, pages 27-49, June, 2009.

ETHZ & TUBS: Simon Perathoner, Tobias Rein, Lothar Thiele, Kai Lampka and Jonas Rox: Modeling Structured Event Streams in System Level Performance Analysis, submitted to Conference on Languages, Compilers, and Tools for Embedded Systems LCTES, Stockholm, Sweden, April 2010

4.6.5 Tool or Platform : MPARM

MPARM is a virtual SoC platform based on the SystemC simulation kernel, which could be used to model both HW and SW of complex systems. It has been developed by UNIBO for the past 7 years and has been shared with more than 20 research partners, who have substantially contributed to its evolution.

The classical system architecture simulated by the default MPARM distribution was represented so far by a homogeneous multicore system based on shared bus communication.

During the last year, MPARM has been enhanced with several HW parametric and customizable models, namely a new ARM11 ISS fully Harvard-architecure (i.e. with separated ports for data and instruction paths), a logarithmic interconnect crossbar, an accurate NoC model, a multi-ported L1 scratchpad memory, a DRAM controller (based on DRASIM2).

MPARM is now capable of simulating cluster-based manycore platforms, i.e. composed by several computation tiles (or clusters) connected via a mesh NoC. The computation tiles are supposed to be homogeneous and consist of a variable number of ARM11 cores, L1 instruction caches, a L1 multiport scratchpad memory for data, a DRAM memory controller, a network interface, a logarithmic crossbar, a set of devices for efficient intra-tile synchronization and a variable number of core tiles.

4.7 Integration Driven by Industrial Applications Transversal Activity

4.7.1 Tool or Platform: SymTA/S

Objectives

SymTA/S is a tool for the development and verification of embedded multiprocessor real-time systems. The existing technology is mainly suitable for event or time-driven systems with message passing as the main task interaction. The tool shall be extended to cover the timing implications of multicore processors, or multiprocessor-systems-on-chip.

Main Results

In several previous projects (funded by german DFG, “Sureal”, funded by german BMBF, ARTIST2, and others), the compositional analysis approach has been transferred into a tool framework which is now also commercially available. The available modelling options capture typical problems in todays automotive systems (CAN bus utilization, end-to-end deadlines,…). This addresses a growing need for formal methods in the industry. The topics currently under research (see below) address future problems which can be expected to become of increasing industrial interest in the future.

Current work

The research version of the tool framework is currently being developed into several new directions: Modeling of shared resources for multiprocessor-system-on-chips (see ArtistDesign Activity 6.2: Platform and MpSoC Analysis), the modelling of hierarchical event models (in the scope of the COMBEST project), the demonstrator platform for adaptive systems (see ArtistDesign 7.1: Design for Adaptivity), and the reliability analysis (as presented in Section 3.1 Technical Achievements of the Industry-driven integrtation activity 7.3). Besides the extension of the applicability into new domains driven by industrial applications, a major focus within ArtistDesign is the synergetic coupling of tools, as well as the corresponding development of models.

Participating partners:

- TU Braunschweig.

  TU Braunschweig investigates synergies in the coupling of methods and implements prototypical implementations of the research results.

- Symtavision GmbH.

  Symtavision is the commercial co-developer of the tool framework. A focus within ArtistDesign is the coupling of with other industrially available tools (such as aiT).

- ETHZ.

  Collaboration on the coupling of MPA and SymTA/S with respect to modelling of hierarchical event models.

- Absint GmbH.

  The aiT tool supplies task timing models, which are required for system level analysis.

Web

http://www.ida.ing.tu-bs.de/forschung/projekte/symtas/

http://www.symtavision.com/

Related Publications

- Simon Schliecker, Jonas Rox, Mircea Negrean, Kai Richter, Marek Jersak and Rolf Ernst, **"System Level Performance Analysis for Real-Time Automotive Multi-Core and Network Architectures,"***Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 28, No. 7, pp. 979-992, July 2009.
- Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst and Michael González Harbour, **"Influence of different abstractions on the performance analysis of distributed hard real-time systems,"** *Journal Design Automation for Embedded Systems*, vol. 13, No. 1, pp. 27-49, June 2009
- Mircea Negrean, Simon Schliecker and Rolf Ernst, **"Response-Time Analysis of Arbitrarily Activated Tasks in Multiprocessor Systems with Shared Resources,"** in *Proc. of Design, Automation, and Test in Europe (DATE)*, (Nice, France), April 2009
-

4.7.2 COSI

Objectives

COSI (Communication Synthesis Infrastructure) is a software framework for interconnect infrastructure analysis and synthesis

Main Results

The framework allows developing specialized flows and tools for communication synthesis as exemplified by the release of COSI-NOC (Communication Synthesis Infrastructure for Network-on-Chips), a software toolkit for the automatic synthesis of synchronous networks-on-chip based on the platform-based design paradigm, and by COSI-BAD, for building automation design.

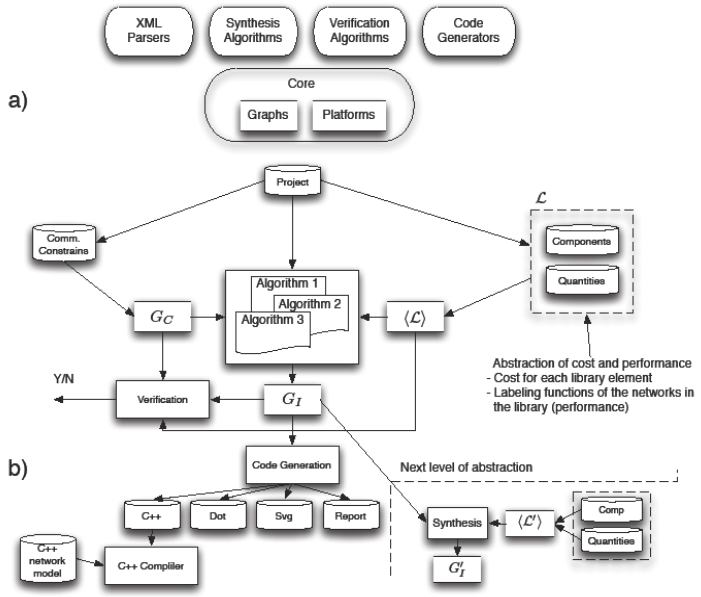


Figure 1. The COSI Platform-Based Design-like structure

	Quantities	CommStructs	Library	Models	Rules	Platforms	Environment	I/O	Algorithms
Core	Ports Bandwidth Flows...	Graphs							ShortestPath Tsp SpanningTree FacilityLocation Kmedian
On-Chip Communication	Interface IpGeometry NodeParam	Specification PitInstance Implementation	Router Link Bus	Ho-Area Ho-Power Orion	Critical length Deadlock	RouterLink BusNoc	Rectangle	Parsers SvgGen Parquet interface SyscGen	DegreeConstrained LatencyConstrained Hierarchical
Building Automation	Interface NodeParam Threads	Specification PitInstance Implementation	Sensor Actuator Controller TwistedPair	TokenRing 802.15.4	WiringRule NodePosition	DaisyChain TreeWireless	Walls CableLadder	BuildingParser SvgGen Desyre interface	DaisyChainPartition WirelessTree

Figure 2. How the COSI framework has been used to generate specific synthesis tools.

Current work

We continue to work towards expanding COSI capabilities, including better models for router delays, bus models, and support for the generation of synthesizable RTL description of the synthesized on-chip interconnection network. In this domain, we are integrating Metro with COSI. Meanwhile, we also plan to continue our work on the extension of the communication synthesis approach to the design of large-scale network for distributed embedded systems such as those that can be found in smart buildings and to airplane power distribution.

Participating partners:

- **Trento**
  Setting the directions of the framework. Methodology and theory. Integrating COSI with Metro.
- **UC Berkeley**
  Tool development and application to Network on Chip and intelligent buildings
- **Columbia**
  Participation in the development of the methodology.
- **UTC**

  Application to intelligent buildings and avionics.

Web
http://embedded.eecs.berkeley.edu/cosi/

Related Publications

[PCSV08] A. Pinto, L. Carloni and A. Sangiovanni Vincentelli, COSI: A Framework for the Design of Interconnection Networks, IEEE Design and Test of Computers, vol. 25, n. 5, Sept-Oct. 2008, pp. 402-415.

[PCVS09] A. Pinto, L.P. Carloni, and A. Sangiovanni-Vincentelli. "A Methodology for Constraint-Driven Synthesis of On-Chip Communications," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 28, No. 3, March 2009.

-- Changes wrt Y3 deliverable --

No change.

4.7.3 Metropolis and Metro II

Objectives

System-Level Design (SLD) means many different things to many different people. In our view, system-level design is about the design of a whole that consists of several components where specifications are given in terms of functionality with additional:

- constraints on the properties the design has to satisfy and on the components that are available for implementation and
- objective functions that express the desirable features of the design when completed.

This definition is general since it relates to many different application domains, from semiconductors to systems such as cars and airplanes, buildings, telecommunication and biological systems. To deal with system-level problems, our view is that the issue to address is not developing new tools, albeit they are essential to advance the state of the art in design, rather it is the understanding of the principles of system design, the necessary change to design methodologies and the dynamics of the supply chain. Developing this understanding is necessary to define a sound approach to the needs of the system and component industry as they try to serve their customers better, to develop their products faster and with higher quality.

Main Results

This contribution was about principles and how a unified methodology together with a supporting software framework, as challenging as it may seem, can be developed to bring the embedded electronics industry to a new level of efficiency. To demonstrate this view, we developed over the years Metropolis, a software framework supporting the methodology and Metro II, a second generation framework built to alleviate the problems we encountered when applying Metropolis to industrial test cases.

Current work

We are integrating this framework with the COSI framework to provide a full communication requirement capture, synthesis, verification and implementation. In parallel, we are interfacing Ptolemy to Metro II to offer a new way of entering designs using the graphical UI of Ptolemy II. In addition, TRENTO in collaboration with VERIMAG has worked on the integration of BIP functional models into the MetroII environment, in order to study the performance of the system when mapped onto different architecture platforms. The tool integration enriches the capabilities of the two tools and preserves the structure and the semantics of the original model. The method has been tested on a distributed sorting algorithm case study.

Participating partners:

- **Trento**

  Tool development, application of the framework to a UMTS case study.

- **UC Berkeley**

  Tool development, interface with Ptolemy II

- **Verimag**

  Integration with BIP

- **Sun Microsystems**

  Application to multi-core development
- **UTC**

  Interface with COSI and application to smart buildings and avionics.
- **National Instruments**

  Industrial development of the ideas put forth by the frameworks
- **Intel**

  Application to SoC design and development of architectural models

Web

http://chess.eecs.berkeley.edu/chess/forum/17.html

Related Publications

[DSDP09] D. Densmore, A. Simalatsar, A. Davare, R. Passerone, and A. Sangiovanni-Vincentelli. “UMTS MPSoC design evaluation using a system level design framework”. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE09)*, Nice, France, April 20-24, 2009.

[BDDD09] F. Balarin, A. Davare, M. D'Angelo, D. Densmore, T. Meyerowitz, R. Passerone, A. Pinto, A. Sangiovanni-Vincentelli, A. Simalatsar, Y. Watanabe, G. Yang and Q. Zhu. “Platform-Based Design and Frameworks: Metropolis and Metro II”. In *Model-Based Design for Embedded Systems,* chapter 10, page 259. CRC Press, Taylor and Francis Group, Boca Raton, London, New York, November 2009.

-- Changes wrt Y3 deliverable --

Reported on integration between BIP and MetroII

4.7.4 Parametric Schedulability Analysis

Objectives

Parametric Schedulability Analysis (PSA) performs parametric analysis on a real time system model. A real time system consists of tasks with deadlines. Each task can have different activation patterns (periodic, aperiodic) and different design parameters such as computation time and the offset in the task activation pattern.

In the design phase of real time systems, every design variable must be assigned a value that would ensure the correct function of the system, achieved when none of the tasks misses its deadline. The classical real-time scheduling theory and available tools so far only provide designers with analysis of the system for a specific choice of the parameters. And most of the time it does not offer flexibility in the choice of the activation patterns for each tasks.

In contrast to the state of the art, this tool enables users to specify their models with full parametric views of the design variables. The tool then performs parametric schedulability analysis of the system and provides the user with information of the region of the parameter values that will guarantee the system to be schedulable. This information can then be used as a guide in deciding the optimum design variable values.

Main Results

- Automatic parameter constraints derivation for periodic tasks with offsets using symbolic model checking

For a system with all periodic tasks with offsets and fixed priority with preemptive scheduling policy, the modelling of the system has been taken care of. The admitted design variables are computation time, periods, offsets, and deadlines. Given the system specification below:

- the number of tasks,
- which design variable(s) would be set as parameters,
- the upper bound and lower bound for the parameter values, and
- the valuation for other fixed design variables,

the tool performs parameter analysis on the system and provides the region of feasible values for the parameters in the form of constraints.

Partial analysis of the system, i.e., only checking the feasibility of some higher priority tasks, is also allowed. This feature is the implementation for the work in [RTSS08].

- UPPAAL trace sampling

The tool utilizes a parameter space sampling technique to obtain regions in shorter time. Users can set the granularity of the sampling by specifying the number of datapoints to be searched in each parameter space. The tool performs sensitivity analysis on the datasample points and collects the resulting region. This approach is suitable for larger systems or cases with many parameters where full symbolic exploration of the parameter space is expensive. This approach could be done independently or in combination with the full symbolic analysis of the parametric system.

Current work

TRENTO and ETHZ have worked on the parametric analysis and validation of embedded systems specified in real-time calculus. For this, the partners have developed an integration flow between Modular Performance Analysis (MPA) developed at ETHZ and the Parametric Schedulability Analysis (PSA) developed at TRENTO. The tool allows the feasibility of a system to be studied in a range of parameters. The method has been tested on simple cases, and on a more advanced system that uses state based components which are difficult to model in MPA.

Participating partners:

- **Trento**
  Tool development, case studies
- **ETHZ**
  Integration with MPA

Related Publications

[RTSS08] Alessandro Cimatti, Luigi Palopoli, Yusi Ramadian, Symbolic Computation of Schedulability Regions Using Parametric Timed Automata, In Proceedings of IEEE Real-Time Systems Symposium'2008. pp.80~89

[SRPL11] Alena Simalatsar, Yusi Ramadian, Roberto Passerone, Kai Lampka, Simon Perathoner and Lothar Thiele. Enabling Parametric Feasibility Analysis in Real-time Calculus Driven Performance Evaluation. In Proceedings of the International Conference on Compilers,

Architectures and Synthesis of Embedded Systems (CASES11), Taipei, Taiwan, October 9-14, 2011.

-- Changes wrt Y3 deliverable --

This is new material, not reported in the Y3 deliverable

5. Assessment of the Workpackage at the end of Y4

The ArtistDesign Network of Excellence is a significant evolutionary step for integrating the leading embedded systems design research teams in Europe.

The overall assessment for the WP at the end of ArtistDesign of the NoE (Jan 2008–Mar 2012) is very positive - both in terms of impact on the overall structuring and lasting integration within the consortium and more generally within the area in Europe.

- The ArtistDesign clusters have been actively pursuing operational integration through joint meetings, staff mobility, and shared platforms and tools.
- The level of activity shows that the Cluster / Activity structure and research topics defined for ArtistDesign make sense, and are viable vehicles for integrating the area. In operational terms, they generate sufficient interest for the partners and individual researchers to participate actively in the joint meetings, to exchange personnel, and to orient the tools and platforms developed to make sense within this structure.
- There is clearly a growing level of maturity for tools and platforms – and the partner teams are actively pursuing a policy of implementing tools, demontrators, and in many cases their accompanying methodologies.
- Nonetheless, it is important to remember that these are tools and platforms for research. The aim is not necessarily always for these to lead to commercially viable tools and start-up companies. In general, they are the concrete realisation of the state-of-the-research, allowing to explore possibilities for future research and later tools (some of which may in turn lead to commercially viable products).

In particular, in Y4 we have had 52 joint technical meetings (public and private), covering a broad spectrum of topics and bringing together a wide audience.

The NoE has facilitated the mobility of 58 researchers in Year 4. This is widely considered to be the best way to integrated research teams, through the phyical transfer of persons and competencies. They lead to lasting collaboration and synergy.

The level of effort has been maintained. We currently have 50 tools and platforms developed in collaboration with ArtistDesign, covering the technical domains of the NoE.

-- Changes wrt Y3 deliverable –

Updated to take into account the Year 4 results.