



IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Activity Progress Report for Year 3

Software Synthesis and Code Generation

Cluster:

SW Synthesis, Code Generation and Timing Analysis

Activity Leader:

Prof. Dr. Peter Marwedel (TU Dortmund)

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Policy Objective (abstract)

The objective of this activity is to provide software synthesis and code generation tools which are required for modern embedded architectures. Due to the constraints of such architectures, the tools have to generate very efficient code. A particular focus is on the mapping of applications to multi-processor systems on a chip (MPSoCs). The parallelism found in such architectures poses a particular challenge. In addition, other selected tools (linking, for example, timing analysis and compilation) are also considered.

Versions

number	comment	date
1.0	First version delivered to the reviewers	February 4 th 2010

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1. Overview of the Activity

1.1 ArtistDesign participants and their role within the Activity

Prof. Dr. Peter Marwedel – TU Dortmund, Dortmund (Germany)

Prof. Marwedel's role is to lead this activity. His team works on resource aware compilation, worst-case execution time (WCET) aware compilation and provides results on compilation for MPSoCs.

Prof. Dr. Maja D'Hondt – IMEC, Leuven (Belgium)

The team led by Prof. D'Hondt will introduce novel source code parallelization and source-to-source optimizations for MPSoC platforms aiming at an exploitation of the memory hierarchy.

Prof. Dr. Christian Lengauer – U. Passau, Passau (Germany)

Prof. Lengauer's team has advanced knowledge in program analysis techniques. This knowledge was initially generated in the context of high-performance computing and shall now be used for compilation to MPSoCs.

Prof. Dr. Rainer Leupers – RWTH Aachen, Aachen (Germany)

The team led by Prof. Leupers works on compiler platforms, adaptive compilation, and MPSoC compilation. The group's MAPS project provides a reference for tools mapping algorithms to MPSoCs.

-- Changes wrt Y2 deliverable --

The contact person at IMEC has changed. No other changes with respect to Year 2.

1.2 Affiliated participants and their role within the Activity

Joseph van Vlijmen – ACE, Amsterdam (Netherlands)

ACE (including van team member van Vlijmen) is a key player in the compiler domain in Europe and the world. This partner provides a view on industrial requirements and practices.

Dr. Björn Franke – University of Edinburgh, Edinburgh (UK)

Dr. Franke's team has advanced knowledge in program analysis techniques. This knowledge was initially generated in the context of high-performance computing and shall now be used, for example, for compilation to MPSoCs.

Prof. Dr. Sabine Glesner – TU Berlin, Berlin (Germany)

The team led by Prof. Glesner provides its expertise on program verification and compiler optimization to the network. This expertise will help verifying transformations as well as developing optimizing compiler transformations of single programs and applications.

Prof. Dr. Paul Kelly – Imperial College, London (UK)

Prof. Kelly's team has advanced knowledge in program analysis techniques. This knowledge was initially generated in the context of high-performance computing and shall now be used, for example, for compilation to MPSoCs.

Prof. Dr. Alain Darté – ENS, Lyon (France)

Prof. Darté's team has advanced knowledge in program analysis techniques. This

knowledge was initially generated in the context of high-performance computing and shall now be used, for example, for compilation to MPSoCs.

Dr. Marco Bekooji, Ruben van Royen – NXP, Eindhoven (Netherlands)

The team led by Dr. Bekooji has advanced knowledge in software synthesis from non-imperative models of computation. Within its area of expertise, the team has already designed tools mapping applications to multi-processors.

Dr. Bart Kienhuis – Compaan Design B.V., Leiden (Netherlands)

This partner's team has advanced knowledge in software synthesis from non-imperative models of computation. Within its area of expertise, the team has already designed tools mapping applications to multi-processors.

Prof. Dr. Ed Deprettere – Leiden Embedded Research Center, Leiden Institute of Advanced Computer Science, Leiden University (Netherlands)

This team is making its expertise on the Daedalus framework available in the network. Team members have been actively participating in the Rheinfels workshops on mapping of applications to MPSoCs and will continue to do so.

Prof. Dr. Soonhoi Ha – Seoul National University (South Korea)

The group of Soonhoi Ha has a strong history of working on the HOPES framework for mapping applications to MPSoCs. Due to being an affiliated member of the network, the expertise resulting from the design of HOPES is available in the network.

Prof. Dr.-Ing. Jürgen Teich – University of Erlangen-Nuremberg (Germany)

This partner's team has been working on the SystemCoDesigner framework for mapping applications to MPSoCs. Due to being an affiliated member of the network, the expertise resulting from the design of SystemCoDesigner is available in the network.

-- Changes wrt Y2 deliverable --

In Year 3, Ed Deprettere, Soonhoi Ha and Jürgen Teich have been added as affiliates.

1.3 Starting Date, and Expected Ending Date

This activity started with day 1 of the network. This activity includes the difficult problem of mapping applications to MPSoCs. We cannot expect that this problem will be completely solved at the end of the funding period. Therefore, work on this problem will be required for a number of years, even though the activity will formally be finished at the end of the funding period.

-- Changes wrt Y2 deliverable --

No changes with respect to Year 2.

1.4 Policy Objective

Software synthesis, code generation, and timing analysis tools provide the necessary link between embedded execution platforms and applications. The recent trend toward multi-processor systems has amplified the need for research in this area.

In order to achieve the required critical mass without increasing the number of partners beyond a manageable number, affiliated partners are added. These affiliated partners complement the work done by the core partners. For the same reason, external partners from outside the project have been integrated into the work of the network. At some time, some external partners might become affiliated partners.

-- Changes wrt Y2 deliverable --

No changes with respect to Year 2.

1.5 Background

Software synthesis and code generation tools are indispensable tools for developing embedded systems. They are frequently assumed to be available. New architectural features are introduced all the time, assuming that “somebody” will provide the expected tools. However, the design of such tools poses many very difficult challenges. There is always the risk of major losses of investments if the expected tools cannot be designed in the available time.

Existing compilers represent very valuable software components which cannot be easily replaced by new methods. Many companies hesitate to replace their existing proven compilers by less well-debugged research results. Therefore, this cluster is extensively considering software synthesis and pre-pass source-to-source optimization tools, which can be used with several standard compilers. Pre-pass optimizers decouple the process of code generation and that of particular optimizations for certain architectural features.

The following is an enumeration of the background in the various areas of this activity:

1. Parallelism as available in MPSoCs is a particularly challenging new architectural feature. Significant effort on automatic parallelization has been spent in the context of high performance computing. Due to this effort, automatic parallelization has become feasible provided certain assumptions about the applications are met. The same results are not yet available for embedded systems. For embedded systems, the situation is different in various respects. MPSoCs, for example, are characterized by communication speeds which are comparable to the speeds of larger on-chip memories. As a result, communication based on the message-passing interface (MPI) is completely ill-designed, since it uses memory buffers extensively. Due to its limitations, special variants of MPI exist. Also, embedded system applications are different from general purpose or high performance computing. They are typically more “well-behaved” in that features like recursion, dynamic loop bounds, dynamic memory allocation, pointers, dynamic class loading etc. are much less frequent, simplifying the analysis. However, heterogeneity of processing elements, real-time constraints, streaming data, limited communication resources and energy awareness impose additional restrictions.
2. Most embedded systems are integrated into a physical environment. In such an environment, time is frequently the most critical resource. It has been found that the lack of timing in the core abstraction of computer science is a serious flaw (see, for example, Edward A. Lee: <http://ptolemy.eecs.berkeley.edu/publications/papers/05/APOT/APOT.pdf> . Reconciling code generation and timing models should therefore receive more attention.
3. Efficiency of embedded systems is a main concern. Therefore, optimized architectures are required and resource allocation has to be handled with care. There are many

proposals for optimizing architectures. For example, customized instruction sets, exploitation of attached FPGAs and multimedia instructions have been suggested. Most of these features require special consideration in compilers and code generation. Resource allocation includes the allocation of execution time, energy, memory space, bandwidth etc. Traditionally, these resources have been allocated independently. Integrated resource allocation is still not generally available. Memory allocation can be considered as a special case of resource allocation. Access times and energy consumption increase with the size of the memory. There is a growing gap between the speed of processors and the speeds of memories, even for larger on-chip memories of MPSoCs. Memory hierarchies are introduced to ease the problems resulting from this gap. Memory hierarchies are extremely important. Currently available memory hierarchies are typically designed to provide a good average-case performance. However, methods for increasing the average-case performance often deteriorate the worst-case performance and the timing predictability. Hence, timing predictability is becoming a key bottleneck for high-performance embedded systems and the memory system is a key source of unpredictability. Furthermore, memory hierarchies have not been designed for an efficient use of the available energy. In general, the link between memory architectures and compilation techniques is rather weak.

4. Software generation has evolved to a level where compilers are key components, but not the only components that are useful for generating executable code. New models of computations such as data-flow based models aim at avoiding the well-known disadvantages of imperative programming styles. Software synthesizers generate imperative code from abstract specifications such as Matlab, or Kahn process networks. It can also be expected that the link between software engineering and embedded systems will become stronger. Hence, trends like the use of UML-based system models do have to be respected as well. For the above models, code is synthesized from specifications in non-imperative languages.
5. Many applications in the embedded systems domain are not only resource-restricted but also safety-critical. This in turn requires compilers for embedded processors to be both efficient and correct. One crucial phase in the compiler is the code generation. Due to its complexity, further increased by reason of parallel processing which needs substantial support, it is highly error prone. Hence, verification of code generation is necessary to ensure that transformations preserve the semantics during compilation.
6. Work on this activity is also linked to the ArtistDesign transversal clusters.

-- Changes wrt Y2 deliverable --

No changes with respect to Year 2.

1.6 Technical Description: Joint Research

In order to make the results available to as many designers as possible, tools will be based on pre-pass source-to-source optimization tools whenever feasible. This way, the mapping of applications to MPSoCs can be added to many existing, proven tool flows. Investments into compilers can be protected, the development effort can be reduced and the focus on new optimization techniques can be increased. The key advantage of pre-pass optimizers is their applicability in a large number of tool chains. Such tool chains do not require new compilers to be written. They may be using a compiler from a family of compilers (such as gcc) or specially designed compilers. Pre-pass optimizers can easily support a family of compilers without any modification and different compilers with only few modifications. Pre-pass optimizers do

already exist for memory-architecture aware compilation and program parallelization. IMEC and partners at the Universities of Dortmund, Passau, and Edinburgh have significant experience with the design of pre-pass optimizers. They reflect the fact that the resources of a network of excellence are limited.

The following joint work with a focus on integration has been or will be performed in this activity:

1. *Compilation techniques for MPSoCs* cannot be developed from scratch since the problems to be solved are very challenging. The current project will certainly not provide enough resources to develop completely new techniques. Fortunately, we can build upon compilation techniques for high-performance computing. Using the limited resources, we established a link between the high-performance computing and the embedded system domain. Integration activities will comprise an in-depth analysis of the applicability of techniques designed in one domain to the other domain. For this purpose, it is very essential that the proposed project includes enough expertise in different areas of applications. Knowledge about hardware architectures would not be sufficient to really check the applicability of the techniques. The University of Passau is a link to the high-performance community. Cooperation with core partners and selected affiliates is used to check which of the existing techniques can be employed in embedded systems and which extensions are needed. Twelve months after the start of the network, a plan for integration of tools and for closing gaps was expected. After 24 months, the design of the integration work should be complete. Later, available automatic parallelization techniques will be integrated to close identified gaps in the tool support. After 36 months, the implementation of the integrated tools should be complete. After 48 months, an evaluation of the integration should be available. This area has not been tackled in the Artist2 network of excellence.
2. Reconciliation of compilers and timing analysis bridges the two activities of this cluster. The work in this area builds on top of the integration work performed in the Artist2 network of excellence. The existing integration of timing analysis and compilers will be used to explore the potential of this approach further. Additional information can be passed between compilers and timing analysis. The impact of optimizing for WCET has to be studied further. Additional hardware components have to be studied. The influence of context switches has to be analysed. Techniques for reducing the number of calls of timing analysers would be of interest. A detailed list of papers is included in sections 2.2. and 2.4.
3. The efficiency of designs is dealt with in ArtistDesign. It can be achieved with many different means. Research on specialized instructions and new optimizations can be expected. If feasible, such optimizations will be implemented as pre-pass optimizations so that they can be used with various compilers. Memory architectures will be considered in-depth, due to their potential for contributing toward an overall efficiency. Memory architectures are very important for the mapping to networked processors. Indeed, the mapping of applications to processing elements may be significantly affected by the connectivity of the memories. Hence, optimized mappings to memories are considered as well. Such techniques should provide optimization techniques taking several objectives into account. Work in this area builds on top of previous work in the Artist2 network.
4. Software synthesis has not been considered in the compiler cluster of Artist2. It is considered as well in ArtistDesign. The activity includes affiliate partners specializing on software synthesis and cooperating experts from other clusters. The second workshop in this area (WSS), held during ESWEEK, had top-level presenters. A. Sangiovanni-Vincentelli, P. Marwedel and S. Ha served as associate editors for a special issue of *IEEE Transactions on Industrial Informatics*, covering the scope of our workshops

SCOPES, MAP2MPSoCs and the Workshop on Software Synthesis. Unfortunately, many of the submitted papers were not resulting from our workshops and only few of the papers met our standards for quality.

5. In addition to topics 1 to 4, members of this activity will also extend the areas for which the correctness of compilers has been shown via formal verification, focussing on the crucial code generation phase during compilation. The work in this area builds on top of the work performed in the Artist2 network of excellence.
6. The members of this activity will also contribute to the thematic activities of the Transversal Integration work package, focussing on predictability and adaptivity issues. This area has not been tackled in the Artist2 network.

-- Changes wrt Y2 deliverable --

Software synthesis has been given even more attention, as requested by the reviewers. No other changes.

1.7 Work achieved in Year 1 (Jan-Dec 2008)

The following work was performed for the different areas of the activity:

1. It was important to set up the required interaction of the partners regarding compilation for MPSoCs. The partners started with an intensive workshop in June, 2008. The workshop was held from June 16 to June 17, 2008 at Rheinfels Castle, St. Goar, Germany. Due to the complexity of the problem and the limited manpower of the network, we invited a number of European groups known to be working in relevant areas to the workshop, including members of the HIPEAC network of excellence and the ACOSTES project. This way, we tried to reach out far beyond the limited set of ArtistDesign partners, using these partners as the seed for a larger network of cooperating partners. A more detailed report is available in the Y1 deliverables as well as on the workshop web pages (see <http://www.artist-embedded.org/artist/Mapping-of-Applications-to-MPSoCs.html>). A summary from the workshop was presented at the CASA workshop held as part of the Embedded Systems Week in Atlanta on Oct. 19th, 2008.

In addition, several smaller meetings took place. This work was performed in cooperation with the execution platforms cluster and involved teams outside the ArtistDesign network.

2. Regarding the reconciliation of compilers and timing analysis, significant work was performed as well. The key questions to be solved were: how much would a compiler benefit from a tight integration with timing analysis? How much different are the code generation results for an optimization of the average case and of the worst case? Will the average run time increase if we optimize for the worst case?
3. Regarding the work on design efficiency, the problem tackled concerned the integration of various tools from various partners (not just limited to this activity).
4. For software synthesis, the question was how to find a link to the work on mapping of applications to MPSoCs.
5. Concerning the support for verification of code generation, TU Berlin has continued its work on formalizing important parts of the semantics of the intermediate representation, of assembler and machine code and examples of transformation rules that describe the compilation between intermediate forms. In particular, we investigated the different kinds of number representations and the rules describing their compilation. Using the Isabelle/HOL theorem prover, we formalized various kinds of integer data types in assemblers. In one of

the code generation rules of a compiler developed at TU Berlin (using the CoSy tool from ACE, Amsterdam), we found a mistake arising from a copy&paste bug when deriving one rule from a very similar, already existing rule.

Besides the research on compiler verification, TU Berlin was also involved in research on compiler optimization. The work on compiler optimizations for parallel architectures has been continued. A demonstrator has been completed together with research on VLIW optimizations based on machine learning. Furthermore, current work deals with optimizations for MPSoCs.

6. For transversal integration, getting requirements from industry was a key goal

Resources of the network were used to support the cooperation. Research work was paid through other resources.

-- No changes wrt Y2 deliverable --

This section was already presented in the Y2 deliverable, in section 1.7.

1.8 Work achieved in Year 2 (Jan-Dec 2009)

1. Work on the mapping of applications to MPSoCs has been continued. First of all, the second workshop on mapping of applications to MPSoCs was held at Rheinfels Castle in June 2009. We managed to reach out far beyond the ArtistDesign partners by inviting prominent European, Asian and American researchers in the field. The road toward new integrated tools has been followed. The work on MAPS at Aachen continued in cooperation with other partners. TU Dortmund and ETH Zürich worked on an extension of the mapping and optimization framework DOL which was developed at Zürich. As a result DOL was extended by the integration of memory hierarchies in the mapping decision and design space exploration of the tool. Work on the integration of energy optimization is still ongoing.
2. Regarding the reconciliation of compilers and timing analysis: The impact of WCET minimization has been analyzed for additional optimizations, including optimizations for registers and scratch pad memories.

Machine learning has shown its capabilities for an automatic generation of heuristics used by compiler optimizations. In Y2, supervised learning approaches are studied for the first time in the context of an automatic minimization of the WCET. Using a reconciling of a WCET-aware compiler and a machine learning tool, heuristics for a WCET-aware function inlining and loop invariant code motion have been developed. The model selection problem, i.e., selecting learning algorithms and their respective parameters, has been tackled by an evolutionary algorithm that automatically finds good solutions within the large search space.

3. Regarding the work on design efficiency; The MPARM simulator has been used by a number of partners. In addition, TU Dortmund has ported IMEC's RTLlib, thus allowing us to use MPARM together with IMEC's MPA tools.

MPA parallelization assistant tool and MH static memory assignment tool by IMEC have been integrated more tightly. The main problems tackled were in respect with cleaning sequential source code in order to parallelize it more efficiently, parallelization exploration, FIFOs sizing and FIFOs access management.

The MH static memory assignment tools by IMEC have been integrated tighter with the DMM dynamic memory assignment tools by NTUA. The main problem tackled was in respect with data interdependencies and sharing physical memory resources.

4. Going beyond the plan, software synthesis was not integrated into the second Rheinfels workshop. Rather, we organized a separate workshop on this issue during the Embedded Systems Week at Grenoble. This approach required a bit more work, but turned out to be more useful, since we could maintain a clear focus for both workshops.
5. Concerning the support for verification of code generation, TU Berlin continued its cooperation and its work on formalizing important parts of the semantics of the intermediate representation.
6. Members of the cluster also contributed to work on predictability and industrial applications.

Also, the educational workshop WESE was organized by the leader of this activity. The workshop attracted top researchers. For example, the keynote was given by Edward A. Lee (UC Berkeley). In order to improve the visibility of the results, WESE papers are now included in the ACM digital library.

Another problem perpendicular to the cluster structure was tackled by the leader of the cluster: in order to extend the accessibility of results, the activity leader became editor for a special series of books on embedded systems published by Springer (see <http://www.springer.com/series/8563>).

Several months of work was spent on improving available educational material: the bulk of the work on the next (extended) edition of the textbook "Embedded System Design" by P. Marwedel was completed. It is being tested in a course held during the winter of 2009/2010. The second edition is scheduled to be published during the first quarter of 2010.

Technical achievements include the following

1. A high-level virtual platform for early MPSoC software development (RWTH Aachen, ACE)
<http://www.iss.rwth-aachen.de>
2. Integration RTLib and MPARM (TU Dortmund, IMEC)
<http://ls12-www.cs.tu-dortmund.de/staff/heinig/research/projects/r2g/>
3. CleanC, MPA parallelization assistant and MH static memory allocation for MPSoC (IMEC vzw)
<http://www.imec.be/cleanc>
4. Scheduling and data management using system scenarios (IMEC vzw, NTUA, TU/e)
5. Mapping of applications to HW/SW-platforms comprising FPGAs (University of Passau)
6. Making the LooPo loop optimizer available in the embedded world (University of Passau, TU Dortmund)
<https://www.infosun.fim.uni-passau.de/trac/LooPo/>
7. Extending the polyhedron model for automatic loop parallelization to include non-linearities (University of Passau)

Details on the achievements can be found in the Y2 deliverable.

-- No changes wrt Y2 deliverable --

This section was already presented in the Y2 deliverable, in sections 1.8 and 2.1. Publication of the mentioned textbook was delayed until the last quarter of 2010.

1.9 Problems Tackled in Year 3 (Jan-Dec 2010)

1. In order to improve the cooperation on solving the problem of mapping applications to MPSoCs, we continued to run the Rheinfels series of workshops. The third workshop was held on June 28-29, 2010 (see <http://www.artist-embedded.org/artist/-map2mpsoc-2011-.html>). The SCOPES workshop was held back-to-back at Rheinfels Castle. It was held on June 27-28, 2010 (see <http://www.artist-embedded.org/artist/-SCOPES-2010-.html>). Also, work on actual mapping tools was continued. The MAPS tool was extended in cooperation with other partners. Cooperation between ETH Zürich and TU Dortmund was continued.
2. Work on code optimizations taking the WCET into account was extended toward multi-objective optimization, multi-cores and links with operating systems. More information on this work linking the two activities of this cluster can be found in the deliverable on timing analysis.
3. Work on memory-architecture-aware compilation tools was continued. The focus was on pre-pass compilation tools and on the support of multi-processor systems.
4. Work on compiler verification was continued. Semantics of intermediate and assembler/machine code were formalized such that it can also be executed. Also the transformation between intermediate and assembler/machine code was given such that the compiler can be generated using the code generator of the Isabelle/HOL theorem prover.
5. We continued to contribute to the state of the art in Embedded Systems Education. The 2nd edition of the text book "Embedded System Design" by P. Marwedel was published. The book is one of the components of a comprehensive solution for an initial embedded systems course, since slides, simulation software and (new by the end of 2010) recorded lectures are also provided on the web (see <http://ls12-www.cs.tu-dortmund.de/en/staff/marwedel/es-book/slides10/> for the most recent information). Translations into various languages are either available or being scheduled. Furthermore, P. Marwedel continued to work on the publication of a series of books on Embedded Systems to be published by Springer (see <http://www.springer.com/series/8563>). Also, the network was involved in the organization of the WESE workshop in 2010.
6. We organized the second workshop on software synthesis during the Embedded Systems Week (<http://www.artist-embedded.org/artist/Scope,2121.htm> l). Top-level experts (e.g. from UC Berkeley) presented at the workshop. Also, we organized a call for a special edition of the journal *IEEE Transactions on Industrial Informatics*. This topic does now receive increased attention.
7. The partners contributed to other activities, such as the transversal activities
8. TU Dortmund has continued to port IMEC's RTLib. In addition the RTEMS operating system was ported to the commercial CoMET simulator from Synopsis (see <http://www.synopsys.com/Community/Interoperability/SystemLevelCatalyst/Pages/MVaST.aspx>). Due to high simulation speed of CoMET, big benchmark applications can be executed now.

-- The above is new material, not present in the Y2 deliverable --

2. Summary of Activity Progress in Year 3 *(Jan-Dec 2010)*

2.1 *Technical Achievements*

MPMH – an integration of MPA parallelization assistant and MH static memory allocation for MPSoC (IMEC vzw, NTUA)

In order to tackle MPSoC programming issues in a MPSoC platform in an efficient way, a single tool performing optimized memory allocation (MH) and parallelizing sequential code (MPA) is an ideal solution. The following challenges appear when integrating MPA and MH:

- information flow between MPA and MH
- interference between analyses and transformations of both tools
- MPA is not platform-aware and as a result may ruin the benefits obtained by MH
- profiling information (sequential) is hard to match with the parallelized code
- no optimization interactions between MPA and MH possible with the present implementation.

The integrated MPMH tool addresses these challenges and performs common data analyses for both tools only once. MPMH is integrated into the Atomium Analysis framework.

Regarding memory optimizations the work in loop transformation methodologies has continued. Furthermore, the MPA tool is applied in the context of a heterogeneous multicore platform for Software-Defined Radio.

CPN: A C Language Extension for Compiling Process Network Applications for MPSoCs (RWTH Aachen)

RWTH Aachen has proposed C for Process Networks (CPN) as an extension of C that allows to write programs based on KPN (Kahn Process Network) and SDF (Synchronous Dataflow) and to transform existing C applications to those MoCs (Models of Computation). The CPN extension is kept minimum, yet provides special features to allow C programmers to write or port parallel applications easily without having to learn a new language or to use target-specific APIs. Researchers at RWTH Aachen have implemented an extensible compiler for CPN-enhanced applications to automatically generate C source code for both shared memory and message passing targets to be fed into the C toolchains provided by MPSoC vendors. In the MAP2MPSOC workshop (June 2010), researchers from RWTH Aachen presented how CPN is used to support dataflow programming in the MAPS (MPSoC Application Programming Studio) methodology.

<http://www.iss.rwth-aachen.de>

Mapping Streaming Applications onto OMAP (RWTH Aachen, Compaan/ACE)

RWTH Aachen (Germany) and Compaan/ACE (Netherlands) have worked together to couple Compaan's technology (HotSpot Parallelizer) which transforms sequential C code into parallel process networks with the MAPS compiler towards real-life heterogeneous MPSoC backends. A joint demo has been established in this year's DAC (June 2010) to exhibit mapping multiple streaming applications to a commercial multi-processor SoC, the Texas Instruments OMAP 3530. The MAPS (MPSoC Application Programming Studio) project is a research effort to tackle the challenge of programming heterogeneous MPSoCs, ranging over multi-application modelling, efficient scheduling/mapping and code generation. This joint work enables a complete mapping and compilation flow of streaming Kahn Process Networks (KPN) applications for the OMAP architecture. The demo showed practical scenarios such as quick mapping exploration, parallelizing sequential part and dynamic mapping, using both tools and was well received in the DAC exhibition.

<http://www.iss.rwth-aachen.de>

Accelerator Programming (Passau, TU Dortmund, Erlangen)

Dortmund and Passau are cooperating on code optimizations of for loop codes for embedded many core systems, especially for GPUs. In Dortmund, low-cost and low-power GPUs are

used for real-time processing of images obtained from optical biosensors. So far, GPU codes have been written by hand and require manual fine-tuning for high performance. The loop parallelizer LooPo (developed in Passau) is being extended to generate optimized image processing code for GPUs from given sequential code. At TU Dortmund, LooPo was compared with PLUTO, a parallelization tool developed by Uday Bondhugula at the Ohio State University. The results are available as a Bachelor thesis written by Richard Hellwig. Except for one application, LooPo outperformed PLUTO with respect to minimizing energy consumption and run-time.

Christian Lengauer is external examiner of the dissertation by Hritam Dutta, advised by Jürgen Teich in Erlangen and entitled "Synthesis and Exploration of Loop Accelerators for Systems-on-a-Chip". Hritam Dutta applies polyhedral methods in the hardware-software codesign of domain-specific accelerators. The thesis will be submitted early in 2011.

Encyclopedia of Parallel Computing (Passau)

Prof. David Padua and Springer-Verlag are putting together an encyclopedia of parallel computing. Prof. Lengauer is co-editor and contributor of four entries on modelling and verification (see the citation list).

<http://www.springer.com/computer/swe/book/978-0-387-09765-7>

Dependable Embedded Real-Time Systems (TU Dortmund)

TU Dortmund is working on dependability issues which will occur in future embedded systems. Due to smaller structure sizes as well as reduced operating voltages, future embedded systems will be exposed to non-negligible rates of transient errors in memory as well as in logic components. The FEHLER research project intends to find flexible, software-based methods to handle errors in real-time critical systems. Two initial publications analyze the vulnerability of a real-time critical multimedia application to transient memory errors. Using a novel classification approach, error handling can take place while adhering to real-time constraints. The FEHLER project is funded for two years in the context of the German Research Foundation (DFG) priority program SPP1500.

Lifecycle assessment of the ecological impact of IT devices (TU Dortmund)

Reducing the energy consumption of systems is a prevalent research topics not only in embedded systems, but increasingly in different areas of IT due to the effect of energy consumption on CO₂ production and global warming. However, in many cases, analyses of the ecological impact of IT equipment are restricted to the use of devices. In this analysis, TU Dortmund provides a holistic view of the lifecycle of typical IT devices, including production, transportation, use, and recycling. The results show that more than 50% of the overall CO₂ production of an IT device like a PC or notebook computer is actually caused by the production processes. Thus, while the reduction of energy consumption at run-time is still an important goal, manufacturers should also take a close look at the production processes.

Optimizing Execution Runtimes of R Programs (TU Dortmund)

The GNU R language is very popular in the domain of statistics. Its functional character supports the rapid development of biostatistical analyses and algorithms. Due to a time consuming evaluation and processing by a runtime interpreter, such R programs require immense computing power and waste a lot of performance compared to imperative languages.

In this activity, TU Dortmund evaluated the possible effect of a sophisticated compiler tool chain for GNU R which automatically should translate R programs to efficient machine code. In case studies, standard optimization techniques were manually applied to R programs. R programs were also translated to imperative C code with subsequent compilation to machine code. An evaluation showed that the resulting machine code could outperform the GNU R interpreter by a factor of more than 50.

-- The above is new material, not present in the Y2 deliverable --

2.2 Individual Publications Resulting from these Achievements

RWTH Aachen

Leupers, R. and J. Castrillon. "MPSoC Programming using the MAPS Compiler". In *Proceedings of the 15th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages pp. 897-902, Taipei, Taiwan, Jan 2010.

Castrillon, J., Velasquez, R., Stulova, A., Sheng, W., Ceng, J., Leupers, R., Ascheid, G., and H. Meyr. "Trace-based KPN Composability Analysis for Mapping Simultaneous Applications to MPSoC Platforms". In *Proceedings of the Design, Automation and Test in Europe Conference and Exhibition (DATE 2010)*, Dresden, Germany, Mar 2010.

Leupers, R., Thiele, L., Nie, X., Kienhuis, B., Weiss, M. and T. Isshiki. "Cool MPSoC Programming". In *Proceedings of the Design, Automation and Test in Europe Conference (DATE 2010)*, Dresden, Germany, March 2010.

S. Schürmans, W. Sheng, A. Stulova, J. Castrillon, R. Leupers, "C for Process Networks", In MAP2MPSOC (Mapping Applications to MPSoCs), St. Goar, Germany, June 2010

Rainer Leupers, Weihua Sheng, Jeronimo Castrillon, Chapter "Software Compilation Techniques for MPSoCs" in the book "Handbook of Signal Processing Systems", Springer, Bhattacharyya, S.S.; Deprettere, E.F.; Leupers, R.; Takala, J. (Eds.) <http://www.springer.com/engineering/signals/book/978-1-4419-6344-4>

Castrillon, J., Schuermans, S., Stulova, A., Sheng, W., Kempf, T., Ishaque, A., Leupers, R., Ascheid, G. and H. Meyr. "Component-based Waveform Development: the Nucleus Tool Flow for Efficient and Portable SDR". In *2010 Wireless Innovation Conference and Product Exposition (SDR'10)*. Washington D.C., USA, Dec 2010.

TU Dortmund

Frank Weichert, Marcel Gaspar, Constantin Timm, Alexander Zybin, Evgeny Gurevich, Michael Engel, Heinrich Müller, and Peter Marwedel. Signal analysis and classification for plasmon assisted microscopy of nanoobjects. Technical Report 830, TU Dortmund, Faculty of Computer Science 12, 2010.

Constantin Timm, Andrej Gelenberg, Frank Weichert, and Peter Marwedel. Reducing the Energy Consumption of Embedded Systems by Integrating General Purpose GPUs. Technical Report 829, TU Dortmund, Faculty of Computer Science 12, 2010.

Paul Lokuciejewski, Marco Stolpe, Katharina Morik, and Peter Marwedel. Automatic Selection of Machine Learning Models for WCET-aware Compiler Heuristic Generation. In *Proceedings of the 4th Workshop on Statistical and Machine Learning Approaches to Architectures and Compilation (SMART)*, pages 3-17, Pisa / Italy, January 2010.

Frank Weichert, Marcel Gaspar, Constantin Timm, Alexander Zybin, Evgeny Gurevich, Michael Engel, Heinrich Müller, and Peter Marwedel. Signal Analysis and Classification for Surface Plasmon Assisted Microscopy of Nanoobjects. *Sensors and Actuators B: Chemical, Elsevier*, 151:281-290, 2010.

Peter Marwedel and Michael Engel. Plea for a Holistic Analysis of the Relationship between Information Technology and Carbon-Dioxide Emissions. In *Workshop on Energy-aware Systems and Methods (GI-ITG)*, Hannover / Germany, February 2010.

Frank Weichert, Marcel Gaspar, Alexander Zybin, Evgeny Gurevich, Alexander Görtz, Constantin Timm, Heinrich Müller, and Peter Marwedel. Plasmonen-unterstützte Mikroskopie zur Detektion von Viren. In *Bildverarbeitung für die Medizin, Aachen / Germany, March 2010*.

Robert Pyka, Felipe Klein, Peter Marwedel, and Stylianos Mamagkakis. Versatile system-level memory-aware platform description approach for embedded MPSoCs. In Proceedings of the ACM SIGPLAN/SIGBED 2010 conference on Languages, compilers, and tools for embedded systems (LCTES '10). 9-16, April 2010

Sascha Plazar, Paul Lokuciejewski, and Peter Marwedel. WCET-driven Cache-aware Memory Content Selection. In *Proceedings of the 13th IEEE International Symposium on Object/Component/Service-oriented Real-time Distributed Computing (ISORC)*, pages 107-114, Carmona / Spain, May 2010.

Paul Lokuciejewski, Sascha Plazar, Heiko Falk, Peter Marwedel, and Lothar Thiele. Multi-Objective Exploration of Compiler Optimizations for Real-Time Systems. In *Proceedings of the 13th International Symposium on Object/Component/Service-oriented Real-time Distributed Computing (ISORC)*, pages 115-122, Carmona / Spain, May 2010.

Paul Lokuciejewski, Timon Kelter, and Peter Marwedel. Superblock-Based Source Code Optimizations for WCET Reduction. In *Proceedings of the 7th International Conference on Embedded Software and Systems (ICESS)*, pages 1918-1925, Bradford / UK, June 2010.

Sascha Plazar, Peter Marwedel, and Jörg Rahnenführer. Optimizing Execution Runtimes of R Programs. In *Book of Abstracts of International Symposium on Business and Industrial Statistics (ISBIS)*, pages 81-82, Portoroz (Portorose) / Slovenia, July 2010.

Heiko Falk and Paul Lokuciejewski. A compiler framework for the reduction of worst-case execution times. *Journal on Real-Time Systems*, 46(2):251-300, October 2010. DOI 10.1007/s11241-010-9101-x.

Andreas Heinig, Michael Engel, Florian Schmoll, and Peter Marwedel. Using Application Knowledge to Improve Embedded Systems Dependability. In *Proceedings of the Workshop on Hot Topics in System Dependability (HotDep 2010)*, Vancouver, Canada, October 2010. USENIX Association.

Andreas Heinig, Michael Engel, Florian Schmoll, and Peter Marwedel. Improving Transient Memory Fault Resilience of an H.264 Decoder. In *Proceedings of the Workshop on Embedded Systems for Real-time Multimedia (ESTIMedia 2010)*, Scottsdale, AZ, USA, October 2010. IEEE Computer Society Press.

Paul Lokuciejewski and Peter Marwedel. *Worst-Case Execution Time Aware Compilation Techniques for Real-Time Systems*. Springer, November 2010.

Peter Marwedel and Michael Engel. Ein Plädoyer für eine holistische Analyse der Zusammenhänge zwischen Informationstechnologie und Kohlendioxid-Emissionen. In *Proceedings of the VDE-Kongress E-Mobility*. Leipzig, Germany, November 2010

Constantin Timm, Andrej Gelenberg, Peter Marwedel, and Frank Weichert. Energy Considerations within the Integration of General Purpose GPUs in Embedded Systems. In Proceedings of the International Conference on Advances in *Distributed and Parallel Computing*. *Global Science & Technology Forum*, November 2010.

Andreas Heinig. R²G: Supporting POSIX like semantics in a distributed RTEMS system. Technical Report 836, TU Dortmund, Faculty of Computer Science 12, December 2010.

Peter Marwedel, *Embedded System Design*, Macedonian translation of the 1st English edition, 2009 (official publication date, actually available in 2010), ISBN 978-60865029-3-5

Peter Marwedel. Embedded System Design – Embedded System Foundations of Cyber-Physical Systems, 2nd edition, Springer, 2011 (official publication date, actually available in 2010), ISBN 978-94-007-0256-1

Peter Marwedel. Embedded and Cyber-Physical Systems in a Nutshell, DAC Knowledge Center, 2010, http://www.dac.com/front_end+topics.aspx?article=58&topic=1

Richard Hellwig. Nutzbarkeitsanalyse von Schleifenparallelisierern für GPGPU-Anwendungen in Eingebetteten Systemen (Usability Analysis of Loop Parallelizers for GPGPU-Applications in Embedded Systems), Bachelor thesis, TU Dortmund, 2010

IMEC

Sven Verdoolaege, Martin Palkovic, Marcel Bruynooghe, Gerda Janssens and Francky Catthoor. Experience with widening based equivalence checking in realistic multimedia systems. In Journal of Electronic Testing, Volume 26, Number 2, pages 279-292, 2010.

Martin Palkovic, Praveen Raghavan, Li Min, Antoine Dejonghe, Liesbet Van der Perre and Francky Catthoor. Future Software-Defined Radio Platforms and Mapping Flows. In IEEE Signal Processing Magazine, vol.27, no.2, pp.22-33, March 2010.

University of Passau

Armin Größlinger: "The Challenges of Non-linear Parameters and Variables in Automatic Loop Parallelization", Doctoral Dissertation, Department of Informatics and Mathematics, University of Passau, December 2009; recipient of the Dissertation Prize 2010 of the CommuniGate Communication Service GmbH

Soufiane Baghdadi, Armin Größlinger and Albert Cohen: "Putting Automatic Polyhedral Compilation for GPGPUs to Work", In *Proceedings 15th Workshop on Compilers for Parallel Computing*, July 2010

Paul Feautrier and Christian Lengauer: "The Polyhedron Model", Encyclopedia for Parallel Computing, David Padua et al. (eds.), Springer-Verlag, accepted and to appear in 2011

Christian Lengauer: "Owicki-Gries Method of Axiomatic Verification of Parallel, Shared-Memory Programs", Encyclopedia for Parallel Computing, David Padua et al. (eds.), Springer-Verlag, accepted and to appear in 2011

Christian Lengauer: "Axiomatic Verification of Monitors", Encyclopedia for Parallel Computing, David Padua et al. (eds.), Springer-Verlag, accepted and to appear in 2011

Martin Fränzle and Christian Lengauer: "Semantic Independence", Encyclopedia for Parallel Computing, David Padua et al. (eds.), Springer-Verlag, accepted and to appear in 2011

TU Berlin

Thomas Göthel and Sabine Glesner. Towards the Semi-Automatic Verification of Parameterized Real-Time Systems using Network Invariants. In *Proceedings of the 8th IEEE International Conference on Software Engineering and Formal Methods*, 2010.

Sabine Glesner, Björn Bartels, Thomas Göthel and Moritz Kleine. The VATES-Diamond as a Verifier's Best Friend. In: Verification, Induction, Termination Analysis - Festschrift for Christoph Walther on the Occasion of His 60th Birthday, Springer Verlag, Lecture Notes in Computer Science, 2010.

Björn Bartels and Sabine Glesner. Formal Modeling and Verification of Low-Level Software Programs. 10th International Conference on Quality Software (QSIC 2010), IEEE Computer Society, 2010.

Dirk Tetzlaff and Sabine Glesner. Intelligent Task Mapping using Machine Learning. In *Proceedings of the 2010 International Conference on Computational Intelligence and Software Engineering (CiSE 2010)*, IEEE Computer Society, 2010.

University of Erlangen-Nuremberg

Joachim Falk, Christian Zebelein, Christian Haubelt and Jürgen Teich. A Rule-Based Static Dataflow Clustering Algorithm for Efficient Embedded Software Synthesis. To appear in *Proceedings of Design, Automation and Test in Europe (DATE'11)*, 2011.

Joachim Falk, Christian Zebelein, Joachim Keinert, Christian Haubelt, Jürgen Teich and Shuvra S. Bhattacharyya. Analysis of SystemC Actor Networks for Efficient Synthesis. To appear in *ACM Transactions on Embedded Computing Systems*, 2010.

Felix Reimann, Michael Glaß, Christian Haubelt, Michael Eberl and Jürgen Teich. Improving Platform-Based System Synthesis by Satisfiability Modulo Theories Solving. In *Proceedings of the Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, pp. 135—144, 2010.

Jens Gladigau, Andreas Gerstlauer, Martin Streubühr, Christian Haubelt and Jürgen Teich. A System-Level Synthesis Approach from Formal Application Models to Generic Bus-Based MPSoCs. In *Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS)*, pp. 118-125, 2010.

Martin Lukasiewicz, Michael Glaß and Jürgen Teich. Robust Design of Embedded Systems. In *Proceedings of Design, Automation and Test in Europe (DATE 2010)*, pp. 1578-1583, 2010.

Christian Zebelein, Joachim Falk, Christian Haubelt, Jürgen Teich and Rainer Dorsch. Efficient High-Level Modeling in the Networking Domain. In *Proceedings of Design, Automation and Test in Europe (DATE 2010)*, pp. 1189-1194, 2010.

Joachim Falk, Christian Zebelein, Christian Haubelt, Jürgen Teich and Rainer Dorsch. Integrating Hardware/Firmware Verification Efforts Using SystemC High-Level Models. In *Proceedings of the Workshop für Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen*, pp. 137-146, 2010.

-- The above are new references, not present in the Y2 deliverable --

2.3 Interaction and Building Excellence between Partners

Main interaction between the partners was through the 3rd workshop on the mapping of applications to MPSoCs on June 29-30, 2010.

TU Dortmund is cooperating with ETH Zürich on exploring the idea of extending the design space exploration from ETZ Zürich with memory-aware techniques.

The partners from Dortmund (at ICD), Leuven (at IMEC) and Eindhoven (at TU Eindhoven, member in another ArtistDesign cluster) are jointly working on the MNEMEE project funded through the 7th framework (see <http://www.mnemee.org>). TU Eindhoven is actively using the compiler development framework ICD-C (see <http://www.icd.de/es/index.html>) into some of its tools. Members of the team at TU Dortmund contribute to updates of the MPARM simulator from U. Bologna with IMEC's RTLlib, thus allowing us to use MPARM together with IMEC's MPA tools.

Dortmund and Passau pursued the idea of using the ICD-C compiler from Dortmund as a frontend and/or backend for the loop parallelizer LooPo from Passau.

The partners from IMEC, DUTH and KTH are jointly working on the MOSART project funded through the 7th framework (see <http://www.mosart-project.org>).

The partners from RWTH Aachen and TU Dortmund are jointly teaching a course in retargetable compilation (including memory-architecture aware compilation) at the Advanced Learning and Research Institute (ALARI) in Lugano, Switzerland (see <http://www.alari.ch>).

The partners from Dortmund and members of other ArtistDesign activities (Bologna, Pisa, Saarbrücken, Zürich) are jointly working on the PREDATOR project funded through the 7th framework (see <http://www.predator-project.eu>).

RWTH Aachen is also a member of the HIPEAC Network of Excellence where they lead the research cluster on Design Methodology and Tools. Within this NoE and carrying the ARTIST banner they have interacted with the top level academic and industrial partners.

RWTH Aachen is participating in a large scale project funded by the German government, the excellence cluster “Ultra high-speed Mobile Information and Communication” (UMIC) where they lead the sub-area “RF Subsystems and SoC Design”. In the “Nucleus” project of UMIC, Aachen has been looking into the research topics on designing and mapping SDR (software-defined radio) applications onto heterogeneous MPSoC platforms.

RWTH Aachen and Compaan are co-operating on mapping Kahn Process Networks applications onto a real-life TI OMAP platform through a master thesis work. The results have been demonstrated in the Compaan Booth in this year’s DAC event.

RWTH Aachen and ACE are co-operating on a technique to generate C-code from a high-level intermediate representation of C compiler during a master thesis work. The results have been integrated into commercial ACE CoSy tool offerings.

TU Berlin and ACE extended their cooperation concerning the development of optimizing compiler transformations as well as verifying transformations.

TU Dortmund and TU Eindhoven are cooperating to develop a novel solution for mapping applications cost-efficiently to the memory hierarchy of any MP-SoC platform. Both groups have continued to work on this.

Christos Baloukas of the Institute of Communication and Computer Systems (ICCS, associated to the National Technical University of Athens) visited TU Dortmund.

-- Changes wrt Y2 deliverable --

Further integration of tools was achieved for all partners.

2.4 Joint Publications Resulting from these Achievements

Paul Lokuciejewski, Sascha Plazar, Heiko Falk, Peter Marwedel, and Lothar Thiele. Multi-Objective Exploration of Compiler Optimizations for Real-Time Systems. In *Proceedings of the 13th International Symposium on Object/Component/Service-oriented Real-time Distributed Computing (ISORC)*, pages 115-122, Carmona / Spain, May 2010.

Daniel Cordes, Peter Marwedel, and Arindam Mallik. Automatic Parallelization of Embedded Software Using Hierarchical Task Graphs and Integer Linear Programming. In *Proceedings of CODES+ISSS, 2010*, Scottsdale / US, October 2010.

Yiannis Iosifidis, Arindam Mallik, Stylianos Mamagkakis, Eddy De Greef, Alexandros Bartzas, Dimitrios Soudris, and Francky Catthoor. A framework for automatic parallelization, static and dynamic memory optimization in MPSoC platforms. In *Proceedings of the 47th ACM/IEEE Design Automation Conference – DAC*, pages 549-554, Anaheim (California) / USA, June 2010. Also listed in Scheduling & Resource mgt deliverable and in Integration driven by Industrial Applications deliverable.

Christos Baloukas, Lazaros Papadopoulos, Dimitrios Soudris, Sander Stuijk, Olivera Jovanovic, Florian Schmoll, Daniel Cordes, Robert Pyka, Arindam Mallik, Stylianos Mamagkakis, François Capman, Séverin Collet, Nikolaos Mitas, and Dimitrios Kritharidis. Mapping embedded applications on MPSoCs: the MNEMEE approach. In *Proceedings of the Annual Symposium on VLSI, ISVLSI 2010*, 5-7 July 2010, Lixouri, Kefalonia, Greece. Also listed in Scheduling & Resource mgt deliverable and in Integration driven by Industrial Applications deliverable.

Christos Baloukas, Lazaros Papadopoulos, Robert Pyka, Dimitrios Soudris, and Peter Marwedel. An Automatic Framework for Dynamic Data Structures Optimization in C. In *Proceedings of the 18th international conference on Very Large Scale Integration (VLSI), System-on-Chip (SoC), VLSI-SOC 2010*, 27-29 September 2010, Madrid, Spain

Christos Baloukas, Marijn Temmerman, Anne Keller, Stylianos Mamagkakis, Francky Catthoor, Dimitrios Soudris and Serge Demeyer. Abstract and concrete data type optimizations at the UML and C/C++ level for dynamic embedded software. Book chapter in *Behavioral Modeling for Embedded Systems and Technologies: Applications for Design and Implementation*. Pages 55-84, IGI Global, 2010.

Rainer Leupers, Weihua Sheng, Jeronimo Castrillon, Chapter "Software Compilation Techniques for MPSoCs" in the book "Handbook of Signal Processing Systems", Springer, Bhattacharyya, S.S.; Deprettere, E.F.; Leupers, R.; Takala, J. (Eds.) <http://www.springer.com/engineering/signals/book/978-1-4419-6344-4>

Leupers, R., Thiele, L., Nie, X., Kienhuis, B., Weiss, M. and T. Isshiki. "Cool MPSoC Programming". In Proc. of the Design, Automation and Test in Europe Conference (DATE 2010), Dresden, Germany, March 2010.

-- The above are new references, not present in the Y2 deliverable --

2.5 Keynotes, Workshops, Tutorials

Course: Retargetable Compilation

Lugano, Switzerland, Feb. 16-19 & Feb 23-25, 2010

Objectives: Spreading excellence in memory-architecture aware compilation and processor retargetability beyond ArtistDesign partners.

Presenters: Peter Marwedel (TU Dortmund), Rainer Leupers (RWTH Aachen)

Other participants: about 20 students

Conclusion: The new, extended format turned out to be very useful.

<http://www.alari.ch>

ICT 4 Energy Efficiency

Brussels, Belgium – Feb. 23rd, 2010

IMEC representatives and P. Marwedel participated at a forum on energy efficiency organized by the Commission of the European Communities. The goal was to provide a contribution in the area of energy efficiency for embedded systems.

IFIP WG 2.11 (Program Generation)

St. Andrews, Scotland, March 1-3rd, 2010

C. Lengauer presented the proposal for a priority research programme "Manycore"

<http://resource-aware.org/do/view/WG211/M8Schedule>

D-CON

Bamberg, Germany, March 4-5th, 2010

C. Lengauer gave the keynote on polyhedral loop parallelization at the concurrency workshop.

<http://concurrency-theory.service.tu-berlin.de/joomla/d-con/d-con-2010>

Cebit

Hannover, Germany – March 9th, 2010

P. Marwedel participated at a panel at the Cebit fair. The purpose was to contribute an embedded systems view on energy efficiency issues of ICT.

Winter school course: Rainer Leupers, Cool MPSoC Design

ASCI Winter School 2010, Soesterberg, The Netherlands – Mar 16-18, 2010

Wireless multimedia terminals are among the key drivers for MPSoC platform evolution. R. Leupers gave a lecture on Cool MPSoC Design in ASCI winter school on embedded system. Wireless multimedia terminals are among the key drivers for MPSoC platform evolution. Heterogeneous multi-processor architectures achieve high performance and can lead to a significant reduction in energy consumption for this class of applications. However, just designing energy efficient hardware is not enough. Programming models and tools for efficient MPSoC programming are equally important to ensure optimum platform utilization. Unfortunately, this discipline is still in its infancy, which endangers the return on investment for MPSoC architecture designs. RWTH Aachen has analyzed the programming methodology requirements for heterogeneous MPSoC platforms and R. Leupers has outlined the approaches taken in MAPS compiler project at RWTH Aachen.

http://www.asci.tudelft.nl/pages/events.php?event_id=1

Special Session: Rainer Leupers (organizer), Cool MPSoC Design

DATE 2010, Dresden – March 11th, 2010

The problems of programming MPSoCs (as already described for the ASCI Winter School above), were also discussed at a special session at DATE. On one hand there is a need of maintaining and gradually porting a large amount of legacy code to MPSoCs. On the other hand, special C language extensions for parallel programming as well as adapted process network programming models provide a great opportunity to completely rethink the traditional sequential programming paradigm for sake of higher efficiency and productivity. MPSoC programming is more than just code parallelisation, though. Besides energy efficiency, limited and specialized processing resources, and real-time constraints also growing software complexity and mapping of simultaneous applications need to be taken into account. The purpose of this session was to analyze the programming methodology requirements for heterogeneous MPSoC platforms and to outline new approaches. With emphasis on wireless applications, this special session has provided a blend of academia/industry presentations, including contributions from innovative startup companies in that domain. This way, it has aimed at consolidation of real life requirements and novel solutions, and stressed the need for intensified and cooperative research activities in MPSoC programming.

<http://www.date-conference.com/>

Meeting: Brief meeting at DATE

DATE 2010, Dresden – March 11th, 2010-12-10

Participants of the cluster, including members from RWTH Aachen, TU Berlin, TU Dortmund, and IMEC meet at DATE on March 11th. They discussed the state of cooperation, in particular preparations for the MAP2MPSoC flagship workshop at Rheinfels castle in June.

Poster session at DATE 2010

Dresden, Germany – March 12th, 2010

The presentation during the Friday poster session at DATE was focused on the automatic parallelization step developed in the MNEMEE project. Furthermore, the embedding of this technique into the integrated toolflow has been presented to the audience.

Industrial Workshop

Stockholm, Sweden – April 12th, 2010

L. Thiele, P. Marwedel, AbsInt and other members of the PREDATOR project organized an industrial workshop during the Cyber-physical systems week.

Seminar 10191 on Program Composition and Optimization: Autotuning, Scheduling, Metaprogramming and Beyond

Schloss Dagstuhl, May 9-12, 2010

C. Lengauer participated in this seminar on new paradigms for parallel programming. Its purpose was to bring together researchers from the two communities of software composition and program optimization. Domain-specific approaches for embedded systems were also discussed.

<http://www.dagstuhl.de/de/programm/kalender/semhp/?semnr=10191>

Joint demo at ACE/Compaan Booth at DAC 2010 (Anaheim), "Mapping Streaming Applications onto OMAP"

Anaheim, US - June 13-18, 2010

RWTH Aachen (Germany) and Compaan/ACE (Netherlands) have worked together to couple Compaan's technology (HotSpot Parallelizer) which transforms sequential C code into parallel process networks with the MAPS compiler towards real-life heterogeneous MPSoC backends. A joint demo has been established in this year's DAC (June 2010) to exhibit mapping multiple streaming applications to a commercial multi-processor SoC, the Texas Instruments OMAP 3530. The MAPS (MPSoC Application Programming Studio) project is a research effort to tackle the challenge of programming heterogeneous MPSoCs, ranging over multi-application modelling, efficient scheduling/mapping and code generation. This joint work enables a complete mapping and compilation flow of streaming Kahn Process Networks (KPN) applications for the OMAP architecture. The demo showed practical scenarios such as quick mapping exploration, parallelizing sequential part and dynamic mapping, using both tools and was well received in the DAC exhibition.

<http://www.dac.com>

Tutorial: SystemC for Holistic System Design

Anaheim, CA – June 18th, 2010

At this year Design Automation Conference (DAC), Jürgen Teich organized a Friday tutorial covering the topic "SystemC for Holistic System Design with Digital Hardware, Analog Hardware, and Software".

Workshop: Software & Compilers for Embedded Systems (SCOPES) 2010

St. Goar, Germany – June 28-29, 2010

SCOPES focuses on the software generation process for modern embedded systems. Topics of interest include all aspects of the compilation process, starting with suitable modelling and specification techniques and programming languages for embedded systems. The emphasis of the workshop lies on code generation techniques for embedded processors. The exploitation of specialized instruction set characteristics is as important as the development of new

optimizations for embedded application domains. Cost criteria for the entire code generation and optimization process include run time, timing predictability, energy dissipation, code size and others. Since today's embedded devices frequently consist of a multi-processor system-on-chip, the scope of this workshop is not limited to single-processor systems but particularly covers compilation techniques for MPSoC architectures.

In addition, this workshop puts a spotlight on the interactions between compilers and other components in the embedded system design process. This includes compiler support for e.g. architecture exploration during HW/SW codesign or interactions between operating systems and compilation techniques. Finally, techniques for compiler aided profiling, measurement, debugging and validation of embedded software were also covered by this workshop, because stability of embedded software is mandatory.

SCOPES 2010 was the 13th workshop in a series of workshops initially called "International Workshop on Code Generation for Embedded Processors". The name SCOPES has been used since the 4th workshop. The scope of the workshop remains software for embedded systems with emphasis on code generation (compilers) for embedded processors.

SCOPES 2010 was organized by Ed Deprettere Leiden University and was held back-to-back with the MAP2MPSoCs workshop.

<http://www.scopesconf.org/scopes-10>

Keynote: Rainer Leupers, System Level MPSoC Design: A Bright Future for Compiler Technology?

SCOPES 2010, St. Goar, Germany – June 29th, 2010-12-02

R. Leupers delivered a keynote speech regarding system level MPSoC design in the SCOPES 2010. Looking back at the SCOPES history, compiler research for embedded processors started out in the 1990s with two major ambitions: (1) more architecture aware code optimizations to better support specialized target machines such as DSPs, and (2) higher flexibility to enable compiler retargeting over a wide range of machines. These research efforts have led to numerous results, many of which are part of industrial products today. So, what is left to do in embedded compilers and who -in a world with "free" tools like GCC and LLVM- will pay for them? Naturally, the evolution of embedded processor architectures demands for a never-ending stream of code optimization innovations. However, he argued that the current trend towards ESL design of embedded MPSoC platforms opens up the most promising new opportunities for compiler research, going far beyond the obvious problem of sequential code partitioning. Increasingly complex software stacks, consolidation of the MPSoC platform market, and higher design abstraction levels induce many interesting novel compiler technology use cases, some of which have been highlighted in the keynote.

<http://www.scopesconf.org/scopes-10/>

Meeting: 3rd Workshop on Mapping Applications to MPSoCs, 2010

St. Goar, Germany – June 29-30, 2010

This is the flagship workshop of this cluster. For the second edition, it was possible to attract researchers from all over the world as presenters. New participants included researchers from the Universities of l'Aquila, Munich, Leuven and Karlsruhe as well as industrial representatives, for example from Lantiq. This way, we managed to establish links to key researchers outside the network and potential new affiliate members. The workshop is now a key forum for discussions in this area. Attendees expressed their strong interest to continue this series of informal workshops as a platform for discussions.

<http://www.artist-embedded.org/artist/-map2mpsoc-2010-.html>

Tutorial: Rheinfels MNEMEE tutorial

St. Goar, Germany – June 30th, 2010

The MNEMEE toolflow was demonstrated for the second time in a MNEMEE workshop collocated with 3rd Workshop on Mapping of Applications to MPSoCs and the SCOPES Workshop. The placement of these workshops facilitated the attendance of the industrial and academic workshop participants. Besides an introductory part where an overview of the whole toolflow has been presented, interactive presentations of the MNEMEE tools have been shown by each partner.

Workshop: Application-specific Systems, Architectures and Processors

Rennes, France, – July 7-9, 2010

The conference covers the theory and practice of application-specific systems, architectures and processors. It builds upon traditional strengths in areas such as arithmetic, cryptography, compression, signal and image processing, application-specific instruction processors, etc. ASAP 2010 was co-organized by Jürgen Teich.

Tutorial: Model-Based Embedded Systems Design

Rabat, Morocco – July 12th, 2010

P. Marwedel presented a full-day tutorial on model-based design of embedded systems at the first African ArtistDesign Summer School.

<http://www.artist-embedded.org/artist/Overview,1958.html>

ARTIST Summer School in Europe 2010

Grenoble, September 5-10, 2010

Armin Größlinger from Passau participated.

Tutorial: Invasive Computing - Basic Concepts and Foreseen Benefits

Autrans, France, September 7th, 2010

Jürgen Teich presented a novel paradigm for organizing the computations of large scale MPSoCs of the future at the ARTIST Summer School Europe 2010. The main idea of Invasive Computing relies on the vision that applications will organize themselves and spread their computational load at run-time on processors, communication and memory resources in phases called invasion, and, depending on available degree of parallelism, dynamically changing user objectives or in dependence of the state of the underlying hardware such as temperature profile, load, permissions, or faultiness, again retreat from these.

<http://www.artist-embedded.org/artist/Overview,2064.html>

Tutorial: Scottsdale MNEMEE tutorial

Scottsdale, US – October 24th, 2010

Members of the teams from Dortmund, TU Eindhoven and IMEC presented results of the MNEMEE workshop at ESWEEK. A tool flow for memory optimizations was demonstrated as a Sunday-Tutorial related to this series of Conferences. The format of a half-a-day tutorial provided in-depth presentations of the tools and techniques developed in MNEMEE.

Workshop: 6th Workshop on Embedded Systems Education, 2010

Scottsdale, US, – October 28th, 2010

Embedded system education is still a very young area and frequently restricted to teaching the details of microcontroller programming. A long-term objective of this workshop is to improve the visibility of work in the area and to stimulate the introduction of broader curricula. In 2010, P. Marwedel was again the main organizer of the workshop. Visibility was improved by the

inclusion of the proceedings in the ACM digital library. Presenters included top researchers from the US and Asia. The workshop was run by Kenneth Ricks (University of Alabama) and Bruno Bouyssounouse (IMAG).

<http://www.artist-embedded.org/artist/-WESE-10-.html>

Workshop: Compiler-Assisted System-On-Chip Assembly, 2010

Scottsdale, US, – October 28th, 2010

The Workshop on Compiler-Assisted System-On-Chip Assembly gives researchers working on compilation and synthesis of systems-on-chip a venue to learn about the work of their peers and discuss ongoing research in detail. CASA 2010 puts a special emphasis on compilation techniques for designing Multi-Processor SoCs (MPSoCs). The workshop has been organized and run by Christian Haubelt (University of Erlangen-Nuremberg) and Andreas Gerstlauer (University of Texas, Austin).

Workshop: 2nd Workshop on Software Synthesis, 2010

Scottsdale, US, France, – October 29th, 2010

An increasing amount of software is not written manually any more. Rather, software is synthesized from abstract models of the required functionality. Software synthesis has been implemented in various disperse communities. The workshop aimed at bringing these communities together. Presenters at this workshop presented industrial as well as academic results. The workshop was organized by P. Marwedel and A. Sangiovanni-Vincentelli and run by A. Sangiovanni-Vincentelli.

<http://www.artist-embedded.org/artist/-WSS-10-.html>

-- The above is new material, not present in the Y2 deliverable --

3. Milestones, and Future Evolution

3.1 *Problems to be Tackled in Year 4* (Jan 2011 – Dec 2011)

1. In order to improve the cooperation on solving the problem of mapping applications to MPSoCs, we will continue to run the Rheinfels series of workshops. The fourth workshop is scheduled to take place on June 28-29, 2011 (see <http://www.artist-embedded.org/artist/-map2mpsoc-2011-.html>). The SCOPES workshop will be held at Rheinfels Castle as well. It will be held on June 27-28, 2011 (see <http://www.artist-embedded.org/artist/-SCOPES-2011-.html>). Also, work on actual mapping tools will continue. The MAPS tool will be extended in cooperation with other partners. Cooperation between ETH Zürich and TU Dortmund will be continuing.
2. Work on code optimizations taking the WCET into account will be further extended toward multi-objective optimization, multi-cores and links with operating systems.
3. Work on memory-architecture-aware compilation tools will be continued. The focus will be on pre-pass compilation tools and on the support of multi-processor systems. Reliability will be added as an additional objective.
4. Work on compiler verification will be continued. It is planned to investigate if semantics of intermediate and assembler/machine code can be formalized such that it can also be executed. Also the transformation between intermediate and assembler/machine code shall be given such that the compiler can be generated using the code generator of the Isabelle/HOL theorem prover.
5. We will be continuing to contribution to the state of the art in Embedded Systems Education. The second edition of the text book “Embedded System Design” will be translated into additional languages. Video material and simulation tools will be made available. P. Marwedel will also continue to work on the publication of a series of books on Embedded Systems to be published by Springer (see <http://www.springer.com/series/8563>). Also, the network will be involved in the organization of the next WESE workshop, scheduled for 2011.
6. We are planning to organize a third workshop on software synthesis during the Embedded Systems Week in 2011.
7. The partners will also contribute to other activities, such as the transversal activities

-- Changes wrt Y2 deliverable --

Work performed in the first three years will be extended.

3.2 *Current and Future Milestones*

The following list of current and future milestones used the same enumeration which was used in sections 1.5 to 1.7.

1. Mapping of applications to MPSoCs

- The identification of the needs and possible approaches was the focus of the first year. The goal was to come up with ideas for the design of mapping tools and to see how existing tools could be integrated into a flow meeting the requirements. *This goal has been achieved. The results from the Rheinfels*

workshops ((see <http://www.artist-embedded.org/artist/Mapping-of-Applications-to-MPSoCs.html>) *provide sufficient input.*

- The design of an integrated tool flow will be the goal for the second year. This design will comprise the key decisions regarding interfaces and implementations. It will not include a full implementation. *Work on mapping tools is actually ahead of schedule. A prototype of the MAPS tool suite is available. A first demo of the Mnemee tools was performed in June at Rheinfels castle*
- The completion of mapping tools will be the goal for the third year. This implementation will be based on the design to be available at the end of the second year. *The state of the art is improving as can be seen from the progress for the MAPS tool as well as from the results of the Mnemee project. The corresponding tools can now be used. Added affiliate partners demonstrate alternate approaches.*
- **The evaluation of an integrated tool flow will be the goal for the fourth year.**

2. Reconciliation of timing analysis and compilers

- The impact of WCET-aware compilation on the resulting code should be analyzed. *This goal has been achieved. Several WCET-aware optimizations have been designed and their impact on the code quality has been published.*
- The analysis of the impact of WCET-aware compilation on the resulting code should be continued in the second year, since many of the standard optimizations have not been considered yet. *Several additional optimizations have been considered, as can be seen from the list of publications.*
- For year 3, we plan extending the work toward multi-objective optimization, integration with the operating system and beyond the current focus one target architecture. *This goal has been achieved. For example, see the paper by Lokuciejewski et al. listed in section 2.4.*
- **A critical evaluation of advantages and limitations of WCET-aware compilation should be performed.**

3. Resource-aware compilation

- Support for predicated execution should be available. Support for extended modelling of memory architectures in the MPARM simulator should be available. An interface for driving simulators and optimizers from the same architectural description should be designed. *These goals have been achieved. A paper on exploiting predicated execution has been published by RWTH Aachen. The extended version of MPARM has been submitted to Bologna by TU Dortmund. The MACC framework for architecture-aware compilation has been designed.*
- MPARM should be used as a key simulation tool by an extended set of partners. *The link to IMEC's MPA tools has been created, even though this was not among the initial targets.* Additional support for special features of embedded processors should be available. *Support for scratchpad memories has been extended. Areas 2 and 3 should be linked by exploiting memory hierarchies in WCET-aware compilers. This work should be performed in year 2 of the network. WCET-aware scratchpad allocation was published at DAC.*
- Results from the integration in year 2 should be available in year 3. *This goal has been achieved. For example, see the paper by Cordes et al. at CODES/ISSS 2010 (see section 2.4).*

- **At least one source-to-source transformation tool exploiting memory hierarchies should be made publicly available in year 4.**

4. Software synthesis

- The impact of software synthesis should be analysed. *NXP and Compaan presented their results at the Rheinfels workshop. Nevertheless, this goal has been only partially achieved in year 1. Attention has been increased in Y2 and Y3.*
- Due to the increasing importance of non-standard models of computation, software synthesis will be continued as a sidetrack (in Y2). *A special workshop on software synthesis (WSS) was held during the embedded systems week 2009.*
- The new workshop will be held during the embedded systems week 2010 (Y3) as well. *The workshop was held as scheduled. There were presentations by top researchers from UC Berkeley, CMU and IMAG. In addition, A. Sangiovanni-Vincentelli and P. Marwedel were working as editors of a Special edition of IEEE Transactions on Industrial Informatics with a special focus on software synthesis. Unfortunately, only few of the submitted papers were of the expected quality.*
- **WSS will be held again in 2011 (Y4).**

5. Development and Verification of compiler transformations

- The goal here is to facilitate compilers to generate efficient and correct code. *This goal has been achieved in Y1. Papers on verifying code transformation during compilation and on interprocedural speculative optimization techniques have been published by TU Berlin.*
- Improving the support of compilers towards efficient and correct code generation will be the goal for the second year. Additional transformations will be considered in the verification effort. *This goal has been achieved in Y2.*
- Verification of compiler transformations will remain a goal for the third year. To achieve also more efficient quality assurance methods, TU Berlin is complementing the verification methods with test methods. The goal is to automatically generate tests for the correctness of optimizing compilers given the specification (e.g. the code generation specification as used by ACE as input for the CoSy tool suite) of the compilers. *This goal has been achieved in Y3.*
- **Verification of compiler transformations will continue in Y4.**

6. Transversal cluster

- The activity maintains a link to the transversal cluster. *This goal has been achieved. The activity leader participated in the meeting at Rome on Nov. 12th and 13th 2008.*
- *Contributions in the area of timing predictability have been made in years 2 and 3. The workshop on software synthesis provided a strong interface to industrial applications and was jointly organized in cooperation with the corresponding transversal cluster. Also, partners worked on a special issue of IEEE Transactions on Industrial Informatics in this area.*
- **The activity will maintain a link to the transversal cluster in Y4. Cooperation will be on a partner by partner basis.**

3.3 Main Funding

The ArtistDesign NoE funds integration and building excellence with the partners, and with the European research landscape as a whole. Beyond this “glue” for integration and excellence, during Year 3 this activity has benefited from direct funding from:

- **RWTH Aachen**

The ISS institute at RWTH Aachen University also receives funds from

- Deutsche Forschungsgemeinschaft (DFG), e.g. via the new Excellence Cluster UMIC (Ultra High Speed Mobile Information and Communication), a large scale next-generation mobile internet research program.
- EU FP7 projects like EURETILE HiPEAC, DSPACE and NEWCOM.
- Industrial partners like Siemens, Nokia, Synopsys, ACE, Huawei and Ericsson

- **TU Dortmund**

The group works on several projects, including

- the PREDATOR project targeting predictable designs
<http://www.predator-project.eu>
- the FEHLER project addressing the conflict between reliability and meeting real-time constraints
<http://ls12-www.cs.tu-dortmund.de/research/activities/fehler/index.html>,
- the MNEMEE project, which is performed at Dortmund’s technology transfer center ICD. MNEMEE focuses on the exploitation of the memory hierarchy
<http://www.mnemee.org>,
- the MADNESS project, which aims at the definition of innovative system-level design methodologies for embedded systems, able to drive the optimal composition of an heterogeneous MPSoC architecture
<http://www.madnessproject.org>,
- a coordinated research action (SFB 876) of 18 professors (with P. Marwedel as the co-chair) and their teams on providing information by resource-constrained data analysis, which generated first results in 2010 and includes funding by Deutsche Forschungsgemeinschaft (DFG) for 12 projects from 2011 onwards
[http://www-ai.cs.uni-dortmund.de/auto?self=\\$fz10eqynthe](http://www-ai.cs.uni-dortmund.de/auto?self=$fz10eqynthe)
- public funding (at TU Dortmund) and industrial contracts (at ICD).

- **IMEC, Leuven**

IMEC works on many projects, including:

- MOSART IST-215244 Project:
Mapping Optimization for Scalable multi-core ARchiTecture. ArtistDesign partners involved: Interuniversitair Micro-Elektronica Centrum (IMEC) vzw., Democritus Uni. Thrace (DUTH) and Kungliga Tekniska Hagskolan (KTH)
<http://www.mosart-project.org/>
- MNEMEE IST-216224 Project:
Memory maNagEMEnt technology for adaptive and efficient design of Embedded systems. ArtistDesign partners involved: Interuniversitair Micro-Elektronica Centrum (IMEC) vzw., Democritus Uni. Thrace (DUTH) and Technische Universiteit Eindhoven (TU/e)
<http://www.mnemee.org/>
- **IMEC Apollo research program:**
Disruptive technologies needed to realize nomadic embedded systems for 2012

and beyond. These are technology aware architectures, multiprocessor system-on-chip technology, and reliable design methodologies for sub-45nm unreliable components. For the Apollo research, IMEC cooperates with industrial partners, such as integrated device manufacturers, fabless and fablite IC solution providers, and system integrators.

http://www2.imec.be/imec_sites/objects/80acd42f851591023f893a7d96fd96bf/annualreport.pdf (page 36)

- **University of Passau**

The group works on several projects, including

- the CompSpread project supported by the Deutsche Forschungsgemeinschaft (DFG) (terminated in September 2010)
- the FeatureFoundation project supported by the Deutsche Forschungsgemeinschaft (DFG). This project related to aspect- and feature-oriented programming is expected to find applications for embedded system programming (renewal pending).
- University funds

- **TU Berlin**

- The group for Software Engineering for Embedded Systems at TU Berlin currently also receives funding from the Deutsche Forschungsgemeinschaft (DFG) for four projects:
 - DFG project VATES (Verification and Transformation of Embedded Systems).
 - DFG project “Optimization and Verification during the Compilation of Higher Programming Languages”, funded within the Emmy Noether excellence program of the DFG.
 - DFG project “Correct Model Transformations (KorMoran)”
 - Funding within the DFG Research Training Group (Graduiertenkolleg) SOAMED
- Funding for the project “Methods for Model Quality (MeMo)” by the Investitionsbank Berlin
- University funding

-- Changes wrt Y2 deliverable --

The partners have been able to secure new funding in a highly competitive environment. New projects include the FEHLER project and Collaborative Research Center SFB 876 at TU Dortmund (both supported by Deutsche Forschungsgemeinschaft (DFG) as well as MADNESS (supported by the EC and involving partners from Dortmund, Eindhoven and Leuven).

4. Internal Reviewers for this Deliverable

- Prof. C. Lengauer (U. Passau)
- Prof. Dr. Olaf Spinczyk (TU Dortmund, Informatik 12)