PROJECT FINAL REPORT

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Name of the scientific representative of the project's co-ordinator[1], Title and Organisation:

Joseph SIFAKIS, – UJF VERIMAG (partner n°2)

Tel: +33 4 56 52 03 51

Fax: +33 4 56 52 03 50

E-mail: Joseph.Sifakis@imag.fr,

Project website[7] address: http://www.artist-embedded.org/

[1] Usually the contact person of the coordinator as specified in Art. 8.1. of the Grant Agreement.

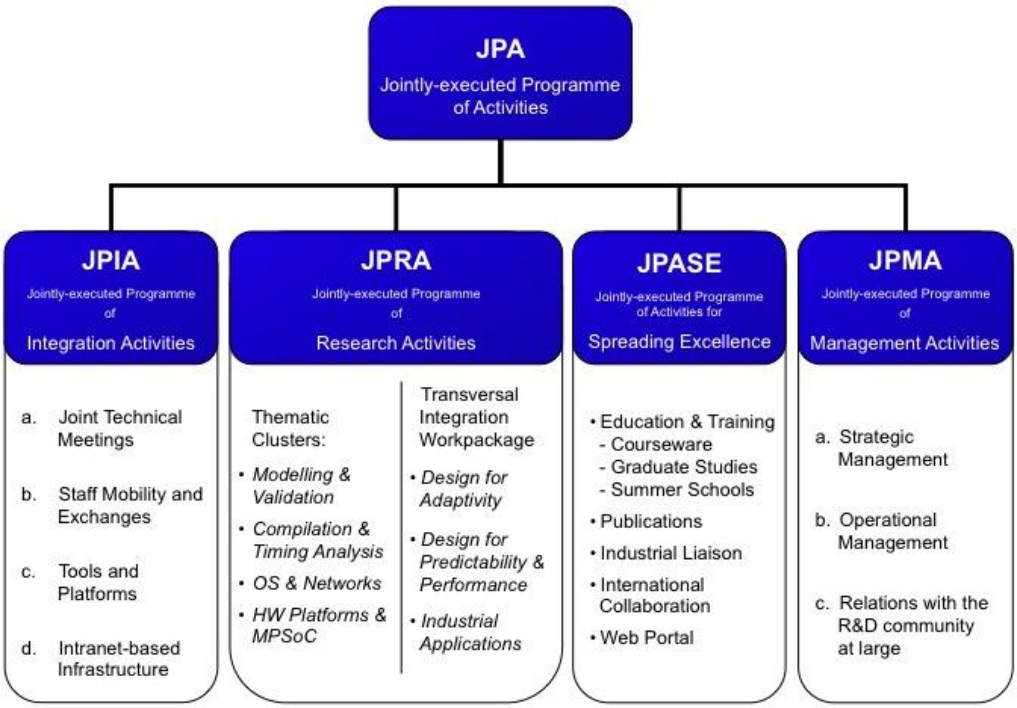
1. Final publishable summary report

- Executive summary

ArtistDesign has been a driving force for federating the European research community in Embedded Systems Design. It brought together 31 of the best research teams as core partners, 15 Industrial and SME affiliated Industrial partners, 25 affiliated Academic partners, and 5 affiliated International Collaboration partners who participate actively in the technical meetings and events.

The central objective for the ArtistDesign European Network of Excellence on Embedded Systems Design was to build on existing structures and links forged in the FP6 Artist2 NoE, to become a virtual Center of Excellence in Embedded Systems Design. This was mainly achieved through tight integration between the central players of the European research community. These teams have already established a long-term vision for embedded systems in Europe, which advances the emergence of Embedded Systems as a mature discipline.

The research effort integrates topics, teams, and competencies, grouped into 4 Thematic Clusters: "Modelling and Validation", "Software Synthesis, Code Generation, and Timing Analysis", "Operating Systems and Networks", "Platforms and MPSoC". "Transversal Integration" covering both industrial applications and design issues aims for integration between clusters.



The NoE had a very dynamic International Collaboration programme, interacting at top levels with the best research centers and industrial partners in the USA: (NSF, NASA, SRI, Boeing, Honeywell, Windriver, Carnegie Mellon, Vanderbilt, Berkeley, UPenn, UNC Chapel Hill, UIUC, etc) and in Asia (Tsinghua University, Chinese Academy of Sciences, Seoul National University, East China Normal University, etc).

ArtistDesign also had a very strong tradition of Summer Schools and Graduate Schools (http://www.artist-embedded.org/artist/-Schools-.html), and major workshops (http://www.artist-embedded.org/artist/-Workshops-and-Seminars,29-.html).

ArtistDesign builds on existing international visibility and recognition, to play a leading role in structuring the area.

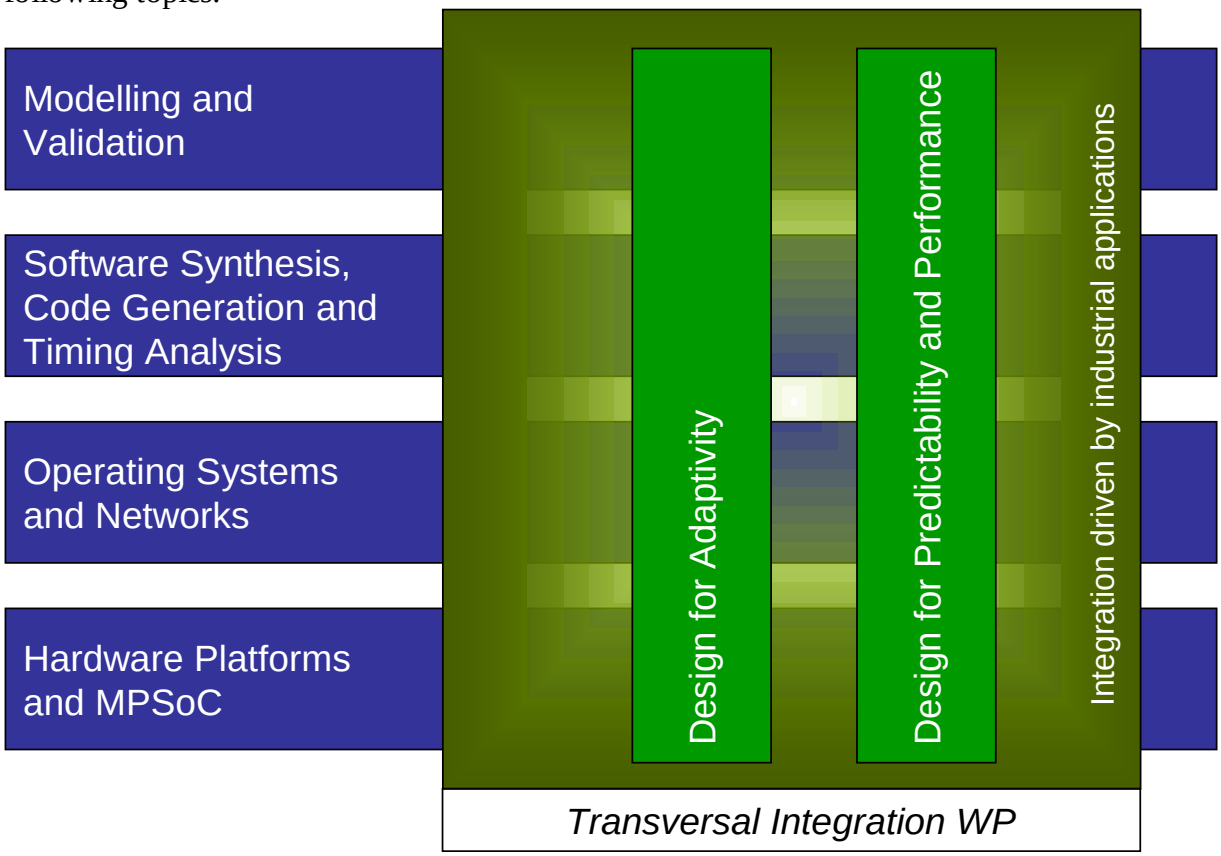
- Summary description of project context and objectives.

The NoE was composed of intra and inter-cluster research activities on cutting-edge topics in embedded systems design. While the main bulk of financing for these activities was taken up by outside programmes (Integrated Projects, National Programmes, Industrial Contracts, etc), the ArtistDesign NoE financed the extra effort derived from integrating these into a single coherent research programme.

Thus, the essential ingredient within ArtistDesign was the JPRA, which motivated the participating research teams far more than the actual financing, was tiny in comparison with the overall research aims. It was completed by the Joint Programme of Integrating Activities (JPIA), and the Joint Programme of Activities for Spreading Excellence (JPASE), and overseen by the Joint Programme of Management Activities (JPMA).

The structure of the research activities reflects the following decomposition of the embedded systems design flow.

This design flow was composed of the following cooperating activities, starting with component-based modelling and leading to implementation. These activities must be well coordinated, and supported by tools and methods to ensure satisfactory levels of productivity and quality. Accordingly, we have structured the area of embedded systems design into the following topics.



Modelling and Validation. Unlike other computer systems, embedded systems are strongly connected with a physical environment. A scientific foundation for embedded systems must therefore deal simultaneously with software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based. The overall objective of this activity was to develop model and component-based theories, methods, and tools that establish a coherent family of design flows spanning the areas of computer science, control, and hardware. The activity brings together the most important teams in the area of model and component based design in Europe.

SW Synthesis, Code Generation and Timing Analysis. There was a continuing demand for higher performance of information processing, which stimulates using a growing amount of parallelism (including using multiple processors). This trend affects the design of embedded systems. We address issues related to multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces. Such processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors. Timing analysis was also affected by the trend toward the new platforms. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Also, timing analysis beyond the single processor was required. Hence, timing analysis will also consider the timing of communication. The overall objective was to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors.

Operating Systems and Networks. We investigate how current real-time operating systems have to be extended or modified to support emerging real-time embedded systems characterized by a high degree of complexity, highly variable resource requirements and parallel processing such as multicores. Most embedded systems are often characterized by scarce resources in terms of processing power, memory, space, weight, energy, and cost. Hence, another objective was to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, whilst guaranteeing isolation properties. Also, to support dynamic applications with variable resource requirements or to cope with unpredictable resource availability, feedback control techniques for resource management at the operating system and application level are also investigated.

Hardware Platforms and MPSoC Design. While hardware platforms for embedded applications will continue to be multi-core, with increasing degrees of parallelism, the evolution trajectory on programming models, design-time and run-time application environments was much less clear. The consequence was fragmentation: while many research teams are working on one or more of these domains, there was little communication and integration, this leads to duplication of results and overall slow progress. The teams involved in this activity have a wide-ranging research experience, which covers all the key areas in MPSoC application specification mapping. The integration activity supported by ArtistDesign will help the participants to the cluster in strengthening the coherency of their approaches and focus on addressing complementary issues in a synergistic fashion.

Design for Adaptivity. An embedded hardware-software system was adaptive, if it can modify its behaviour and/or architecture to changing requirements. Adaptivity was increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity was a cross-cutting system characteristic that affects both hardware and software. At the software-level adaptivity was mainly concerned with flexible and adaptive resource scheduling, e.g., CPU time scheduling. At the hardware-level adaptivity includes both adaptation of operation modes, e.g., supply voltage and clock frequency, processor instruction sets, and dynamic management of hardware resources, e.g., processing elements and memory.

Design for Predictability and Performance. Many applications have strict requirements on timing, and limited resources (memory, processing power, power consumption, etc.). All systems also have increasing demands on (average) performance, which has motivated the introduction of features such as caching, pipelining, and (now becoming very prominent) multiprocessor platforms. Almost all such efficiency-increasing features drastically increase variability and decrease analyzability of response-times, etc. and thus have a detrimental effect on predictability. Since the introduction of new architectural features was inevitable, it was important to: a) develop technology and design techniques for achieving predictability of systems built on modern platforms, and b) investigate the trade-offs between performance and predictability.

Integration Driven by Industrial Applications. To have a strong impact on industry and society at large, the results of the Thematic Clusters need to be harmonized in an overall design flow that can sustain the embedded design chain from conception of the product to its implementation. The design chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g., Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI, Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics). Today, there was stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There was a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company.

Spreading Excellence. ArtistDesign leverages on the worldwide visibility of its activities. It is progressively creating a European embedded systems design community and spreading the "Artist culture" in all major research institutions.

To ensure that the next generation of researchers will continue in this direction we, as a consortium, have devoted a great deal of effort to Spreading Excellence, in both academic and industrial circles. Furthermore, through our links with both core and affiliated partners, we actively set up permanent links between industry and public research, based on existing partner collaborations with major industrial players in the area.

The JPASE activities spread excellence and structure the community at large. They are planned by the Strategic Management Board, and are implemented by ArtistDesign core and affiliated partners.

The NoE leverages on its members and teams, who play a main role in the organisation of world-class scientific events, to disseminate results in the area. We expect that the NoE's structured and authoritative dissemination will have a strong effect on the community as a whole, for orienting and creating synergy for research.

- A description of the main S&T results/foregrounds

Work progress and achievements during the period

i. Modelling Activity and the Validation Activity

Both research activities with the cluster – the Modelling Activity and the Validation Activity – have progressed substantially within the fourth year, and with significant synergy between proposed modelling formalisms and methods and validation techniques they support:
The work on Component Modeling and Compositional Validation involved several partners that produced significant results on compositional modelling and verification:

Results on modelling can be summarized as follows:

- Composition frameworks for behaviour and properties of heterogeneous systems such as assume/guarantee reasoning, interface automata, modal transition systems as well composition frameworks for tool integration based on meta-models and model-transformations have been consolidated and applied to case studies.
- Resource modelling techniques applied to design space exploration, multi-core scheduling, performance evaluation and derivation of distributed implementations from global specifications.
- Quantitative modelling techniques for weighted automata, priced timed automata and quantitative communication models.

Results on validation can be summarized as follows:

- Quantitative Validation covering a wide range of techniques for WCET analysis, schedulability analysis, frequency analysis of timed automata, analysis of parametric quantitative models, and analysis of resource consumption using energy- and price-extensions of timed automata. These techniques use new notions of metrics and robustness.
- Cross-Layer Validation focusing on model-based testing techniques such conformance testing of real-time systems using time- and data abstractions, asynchronous testing and test-case generation for embedded Simulink, incremental testing of composite systems as well as runtime monitoring.

In addition to these results, the Cluster has endeavoured a considerable integration effort for connecting tools, joint meetings, open workshops and joint publications.

ii. Software Synthesis, Code Generation and Timing Analysis

In year 4, we have seen a further proliferation of the basic techniques studied by this cluster. The importance of using multi-processor systems has been continuing to grow. Any session on programming multi-cores and multi-processor systems was filled with people. Fortunately, ArtistDesign was active in this area.
The work on software synthesis and code generation focused on the development of tools and resource-aware compilation. We developed two tools for mapping applications to multi-core or multi-processor platforms (RWTH Aachen, IMEC). Our work on resource-aware compilation has continued with new results on energy efficiency and thermal behavior control as well as with fundamental machine-learning techniques for optimized code generation.

In program flow analysis, MDH and Tidorum have made advances towards increased soundness by developing an advanced relational value analysis that takes possible overflows and wraparounds into account. This was important for small embedded systems, where wraparounds are common

Additional activities include the organization of an international workshop on Software Synthesis (http://www.artist-embedded.org/artist/-WSS-11-.html) and development of new educational material on software synthesis, compilers and timing analysis in the second edition of the textbook on embedded systems by P. Marwedel.

The work on timing analysis and timing predictability has progressed significantly in two directions. The first focuses on enforcing predictability through determinism. It produced new and industrially relevant results on cache analysis and ache-aware memory allocation that have been taken up by commercial tools such as aiT from Absint. The second takes a probabilistic approach and relies on randomization to make timings on micro-level independent. Very promising initial results has been obtained.
Advances in hybrid WCET analysis methods, which include elements of measurements and testing, have been made (MDH, York, TU Vienna). Such timing models can be used to provide worst-case timing estimates early as well as small but appropriate sets of test vectors for tasks with very large input sets, and evaluation of coverage metrics for test-data generation.

Finally, the Cluster has achieved increased integration of timing analysis tools and compilation tools (TU Dortmund, TU Vienna).

iii. Operating Systems and Networks

The work developed by the cluster involved several partners that produced significant results summarized as follows:

The work on operating systems and middleware focuses on resource reservation and predictability. We developed an implementation of a real-time scheduler in the Linux kernel, with a support for resource reservation. We also developed a programming framework to support resource reservation of concurrent real-time applications on multi-core platforms, considered by Ericsson for software development in next generation cell phones. Finally, we proposed a comprehensive taxonomy for the resources currently used in embedded real-time systems.
Our work on predictability includes cache-aware analysis and scheduling for safety-critical applications, in collaboration with the Cluster on Compilers and Timing analysis.
The Cluster also developed a middleware and communication protocol for teams of mobile robots that are self-reconfigurable and provide efficient support to intensive interactions and which have been adopted by several teams in the RoboCup Middle Size League.
The work on networks includes two toolsets. One for the design, analysis, configuration and deployment of dense WSNs, the other was the MAST (Modelling and Analysis Suite for Real-Time Applications), which was enhanced with more networking components and analysis, namely for switched networks such as AFDX. Also a number of communication protocols and tools, developed for improving predictability and adaptivity in (industrial) networked embedded systems.

The cluster teams have been involved in many European projects, had strong interaction with industry and disseminated their work through active participation in world class conferences, workshops and schools.

iv. Hardware Platform and MPSoC Design

The Cluster has continued its efforts to establish an integrated modelling and design methodology that can take into account predictability and resource-awareness with focus on efficiency. This work has benefited from fruitful collaboration with the Cluster on Modelling

and Validation and Timing Analysis as well as from the transversal activities on design from adaptivity and predictability.
Main results can be summarized as follows:

- Fault tolerant distributed embedded systems: We have developed results for handling both processor and communication faults in distributed real-time systems for automotive applications, based on CAN or FlexRay communication.
- Performance analysis methods: TU Braunschweig and ETH Zurich have developed very original and relevant results. They have collaborated to establish a method for coupling the tools SymTA/S and MPA. Relying on different analysis techniques each of the two tools can be individually used to evaluate the performance of embedded real-time systems. The interface developed for tool coupling now allows combining the strengths of the two tools. Evaluations have been jointly performed and the work resulted in joint publications.
- MPSoC design: Major activities on MPSoC design have focused on application parallelization, platform mapping, memory hierarchy management, application scenario exploitation, and run-time resource management, including reconfigurable systems. The outcome of these 4 years was the development of related tools, tool integration in tool chains in collaboration with several ArtistDesign partners, and highly referenced publications.
- Energy harvesting: We have developed new node level scheduling techniques (UNIBO and ETHZ) as well as network level routing algorithms (DTU), and have demonstrated that these techniques can lead to considerable extensions of the lifetime of the network. One specific outcome was the founding of the company WISPES srl (Wireless Self-Powered Electronic Systems) that aims at providing technologies and devices able to add wireless communication and local computation to the customer's monitoring and sensing activities.
- Temperature and energy aware optimization: EPFL has developed a novel online thermal management policy based on dynamic voltage and frequency scaling for high-performance 3-D systems with liquid cooling. The approach was able to gain up to 50% as compared to current state-of-the-art thermal control techniques.

Finally, the Cluster has an impressive record of joint publications, invited talks, analysis and design tools and industrial collaborations.

On the widespread use of multi/core and many core processor architectures

a. The Need for Multiprocessing

Embedded devices perform an increasingly wide variety of high and low-level tasks. With the growing availability of high speed mobile and Wi-Fi networks, embedded devices will increasingly be used for performance-intensive tasks that were previously handled by traditional non-embedded computers. For example, the next generation of smartphones (called “Super phones”) and tablets will be used for a wide variety of tasks such as playback of high definition 1080p videos, Adobe® Flash®-based online gaming, Flash-based streaming high definition videos, visually rich gaming, video editing, simultaneous HD video downloads, encode and uploads, and real-time HD video conferencing.

Even for high-end devices, the current generation of embedded processors is not designed to deal with this tidal wave of high performance use cases. The quality of performance for devices based on single core CPUs rapidly degrades when users run several applications concurrently, or run performance intensive applications. To improve CPU performance, engineers employ several techniques, such as using faster and smaller semiconductor processes, increasing core operating frequency and voltage, using larger cores, and using larger on-die caches.

Increasing the size of the CPU core or cache delivers performance increases only up to a certain level, beyond which thermal and heat dissipation issues make any further increase in core and cache size impractical. From basic semiconductor physics we know that increasing operating frequency and voltage can exponentially increase power consumption of semiconductor devices. Even though engineers may be able to squeeze out higher performance by increasing frequency and voltage, the performance increase would drastically reduce battery life. In addition, processors that consume higher power would require larger cooling solutions resulting in an undesired expansion in device size. Therefore, increasing the operating frequency of the processor to meet the ever-increasing performance requirements of mobile applications is not a viable solution for the long run.

b. Trends

For several decades processors were primarily single core architectures and CPU makers increased performance by increasing operating frequencies, core sizes, and using smaller manufacturing processes allowing more transistors in the same chip area. However, CPU manufacturers realized that the continual increase in frequency and core sizes caused exponential increases in power consumption and excessive heat dissipation. Therefore, CPU makers developed multi-core CPU architectures to continue delivering higher performance processors, while limiting the power consumption of these processors. Most desktop and notebook systems today use either a dual or quad core processor and consume significantly lower power than their single core predecessors. But mobile devices like smartphones and tablets benefit even more from multi-core architectures because the battery life benefits are so substantial. Dual-core processors and quad-core are now the standard.

Embedded application processors are facing the same performance and power challenges that desktop and notebook CPUs faced a few years ago. Applications are already stretching the capabilities of current single core mobile processors. To further increase the performance and stay within embedded power budgets, it is likely that most embedded processors will eventually have multi-core processors. Mobile operating systems such as Android, Windows®CE, and Symbian are capable of operating in a multi-core environment, and have the features required to efficiently harness the multiple processing cores of the underlying hardware.

v. Design for Adaptivity

Research Trends and Vision on "Design for Complex Adaptive Systems"

Real-time systems constitute a notable share of today's embedded computers that needs special attention. The design of robust and fault-tolerant real-time systems is a highly active research area that has produced numerous approaches for evaluating and increasing system robustness against selected fault scenarios. These methodologies can be applied throughout the design process of an embedded system and yield systems that are highly robust against a selected set of disturbances in the field. Future embedded systems, however, will undergo an evolution in both hard- and software configuration during their lifetime. In the automotive industry, it is already common to update or add software components during the lifetime of a product, producing a variety of software configurations in the field. To ensure functional and temporal correctness of all possible configurations, OEMs have to maintain a complex versioning database and perform exhaustive testing to cover the whole configuration landscape. This already constitutes a problem today, which will grow into a major challenge in the future.

Designing embedded systems to be robust and fault-tolerant will not ultimately solve this problem, as the evolution an embedded system goes through during its lifetime cannot be foreseen at design time. Hence, embedded systems need to be adaptive to changing conditions, in the sense that they need to be able to meet given requirements including safety, security, and performance,

in the presence of uncertainty in its external environment or internal execution platform. Adaptivity can be seen as a means for enforcing predictability in the presence of uncertainty.

The uncertainty can be viewed as the difference between the average and the worst-case behavior of a system and its environment. The trend in embedded system is towards drastically increasing uncertainty due to, e.g., execution platforms with increasingly sophisticated HW/SW architectures (layering, caches, multiple cores, speculative execution etc), increased connectivity with complex and non-deterministic external environments, increased amount of difficult-to analyze software, and increased variability with respect to use cases.

One technique for achieving adaptivity in particular in software-based systems is feedback. In many embedded systems worst-case designs are unfeasible for several reasons. One of these is the over-provisioning of resources that this typically implies. Other reasons are uncertainties associated with worst-case resource utilization estimates and on-line changes in objectives, external conditions and use cases. In a feedback-based resource management system, the allocation of resources is based on a comparison of the actual resource utilization by, e.g., a set of activities or tasks, with the desired resource utilization. The difference is then used for deciding how the resources should be allocated to the different activities. The decision mechanism constitutes the feedback controller in the scheduling scheme. Feedback control makes it possible to deal with uncertainties and variations in a controlled way.

Feedback scheduling is primarily suited for soft real-time applications and adaptive real-time applications, where missing one or more deadlines does not jeopardize correct system behavior, but only causes performance degradation. For this type of systems, the goal is typically to meet some Quality of Service requirement. The adaptive class of real-time systems is a suitable description for a many practical applications. This includes different types of multimedia applications, but also many control and signal processing applications. An important research trend here is how to best model embedded computing system from a control perspective. Different model formalisms can be considered, from pure discrete event based models to fluid continuous-time approximative models.

The research trends related to adaptivity in embedded systems are numerous since adaptivity is crosscutting. In hardware-based oriented embedded systems there are work performed on modeling and hardware generation for adaptive processes and applications. Emerging architectures such as partially reconfigurable, either fine-grained or coarse-grained, FPGAs provide a huge potential for adaptivity in the area of embedded systems. Since many system functions are only executed at particular points of time they can share an adaptive component with other system functions, which can significantly reduce the design costs. However, adaptivity adds another dimension of complexity into system design since the system behavior changes during the course of adaptation. This imposes additional requirements on the design process, in particular system verification.

In the software-oriented part of embedded systems there is also a considerable work on computational models that allow for adaptivity, how adaptivity can be provided in component-based architectures, adaptive task models for scheduling, program language constructs supporting adaptivity, and run-time support for adaptive resource management from operating systems, middleware, and communication networks. The resources in the latter case typically include clock cycles, memory, communication bandwidth, and energy, but could in general also include other resources which are allocated dynamically.

The cyber-physical system (CPS) trend has also strong relations to the work within this activity. One example of this is holistic design approaches that integrate physical aspects such as power and heat, with cyber aspects.

The work done within ARTIST on Adaptive Systems includes numerous highlights:

- Scheduling analysis: Efficient and effective scheduling analysis for fixed priority systems has been developed that takes into account tasks arriving and leaving the system. Furthermore, a new method for allocation and scheduling of parallel tasks in soft-real time systems (multimedia decoding) in the presence of post-silicon, process and ageing induced variability in a nominally homogeneous target multi-core platform has been developed.

- Memory: Dynamically adaptable memory architectures for supporting dynamic real-time process loads have been developed.

- Collaboration frameworks: An adaptable cooperation-based framework for networked embedded systems with heterogeneous nodes has been developed, allowing constrained devices to cooperate with more powerful (or less congested) neighbours, to meet allocation requests and handle stringent constraints, opportunistically taking advantage of global resources and processing power.

- Service adaptation: Techniques have been developed for adapting the service request handling behaviour to the specific requirements of the services in Service Oriented Architectures (SOA). CPU contracts are used to ensure sufficient computation time for dealing with services with special requirements.

- Run-time resource management: An adaptive resource manager for distributed embedded systems aimed at multimedia applications, e.g., broadcast management systems, was developed. Considerable savings in power consumption, hardware cost and system size were reported in an industrial case study. Parallel to this a QoS based adaptive resource management system for homogeneous multicore platforms was developed.

- Run-time analysis: A distributed approach for in-system run-time performance analysis of embedded systems, complemented by a framework enabling access control and runtime-optimization through the use of distributed algorithms.

- Sensor networks: New approaches to adaptive energy management of energy harvesting system using solar cells have been developed. Based on a prediction of the future available energy, the application parameters are adapted in order to maximize the utility in a long-term perspective.

- Control techniques: A new method for optimizing the timing parameters of real-time control tasks in resource-constrained embedded systems has been derived. Also, new feedback scheduling techniques and new event-driven sampling mechanisms have been proposed.

- Adaptivity in networks: Here various ways of adapting a communication channel to varying application requirements or environmental conditions to enhance the efficiency of medium utilization have been proposed. For controlled access networks with isolated virtual channels the guaranteed bandwidth and latency can be adapted online using the Flexible Time-Triggered (FTT) paradigm on switched Ethernet, either with COTS switches (FTT-SE protocol) or enhanced ones (FTT-enabled switch).

- Programmable hardware: A new type of ultra-fault-tolerant FPGA named the eDNA architecture has been conceived all the way from development of the concept, to the implementation of a prototype, to test in a space related case study NASA JPL.

- WCET analysis: Parametric WCET bounds, where the WCET bound depends on the values of certain inputs, can be used in adaptive real-time systems where the scheduling of tasks adapts to external factors such as varying data sizes affecting the running times of tasks. A general method for parametric WCET analysis, which combines a number of advanced

symbolic techniques including relational abstract interpretation, counting of integer points in polyhedra, and parametric integer programming has been developed and implemented in the WCET analysis tool SWEET.

- Reference architectures: A reference architecture for automotive embedded systems that addresses the needs for flexible and automatic run-time reconfiguration has been proposed. The research focus was the development of technical support in terms of middleware services for a closed adaptation of distributed embedded systems. In addition to the reference architecture an information model of the control parameters that represent the target system configuration alternatives, environmental parameters, and internal conditions has been defined and a functional design has been performed.

vi. Design for Predictability and Performance

Research Trends and Vision on "Design for Predictability and Performance"

Predictability can be regarded as an effect of choosing suitable hardware and software architectures (in a wide sense) that lead to systems whose worst-case behaviour is easy to predict, and of utilizing analysis techniques that are able to provide these guarantees for the chosen system architecture. Important architectural considerations occur on many levels in a system hierarchy. As a general rule, static allocation of resources leads to predictable systems, whereas dynamic allocation makes predictability difficult. Challenges addressed by this activity appear at all levels of abstraction in the design process:

- **Modeling and Validation of systems and of components**: Principles and structures for system and component modeling that are conducive to achieving predictability are being investigated. A natual approach is to enable *a priori* predictability analysis and to support mappings to platform architectures that preserve predictability. Investigations of how modeling and analysis techniques extend to non-traditional system structures, including parallel, distributed and networked architectures, for which predictability is more difficult to achieve is currently a very active research area. A more fundamental research direction is to develop precise definitions and characterizations of central concepts, including *predictability and robustness.* Another overarching research theme is to explore trade-offs between predictability, resource consumption, and performance.
- **Compiler Techniques and Program Analysis**: Timing analysis, i.e., predicting the worst-case execution time (WCET) of a piece of code, is a hard problem, but significant breakthroughs have been obtained in recent years for many types of processors. Commercial tools, all from Europe, are available. Research in timing analysis is closely dependent on research on system-design concepts that increase predictability. The issues stretch from the processor architecture across all layers to the application and is caused by the variability of execution times. The goal is to increase the predictability of system behaviour. An important issue is also timing analysis for compilation, especially in the light of multiple processors and other architectural features. An important goal is to marry timing analysis with compilation, in order to make timing properties immediately visible to the embedded systems developer.

- **OS/MW/Networks**: On the operating system level, scheduling and reservation of resources is a widely researched topic, with a vast literature. Operating system mechanisms, such as scheduling, mutual exclusion, interrupt handling and communication, can heavily affect task execution behaviour and hence the timing predictability of a system. For example, preemptive scheduling reduces program locality in the cache, increasing the worst-case execution time of tasks compared with non-preemptive execution. The object-oriented programming style, although attractive as a software development methodology, introduces dynamics into the execution time by the dynamic binding of methods to calls. Techniques that improve predictability include schemes that a priori reserve resources in a wide sense. This can be in the form of reserving time slots for execution of tasks, reserving time slots for communication between tasks (e.g., in the time-triggered architecture and in the synchronous programming paradigm). In future research, it is important to explore the tradeoff between performance and predictability in scheduling. Also important is to investigate of software architectures for time-predictable real-time operating systems, with the goal to avoid that the execution of OS code adversely affects the time-predictability of application tasks and vice versa, thus making the computation-time needs of both operating system activities and application tasks easily predictable.
- **System and Processor Architecture:** Simple processor architectures lead to more predictable systems than complicated ones. Current architectures include many features that decrease predictability, such as implicit concurrency, e.g., pipelining, super-scalarity, out-of-order execution, and dynamically scheduled multi-threading. The restricted processor-memory channel-bandwidth and the growing speed gap between processor and memory has led to the introduction of deep memory hierarchies and several types of speculation. Dynamic power management technology, which is critical for reducing the power consumption of hardware, also has a significant impact on predictability. Research on predictability has considered, e.g., to replace dynamic memory management by static and predictable ones, such as scratchpads, to characterize and develop more predictable replacement policies in dynamic caches,

  The current introduction of multicore processors provides new challenges to predictability. They introduce new opportunities for parallelism and communication, in order to enable higher performance. At the same time they pose new significant challenges for the building of predictable systems. One major problem is that multiprocessor techniques typically introduce new forms of interference, even between activities that are logically unrelated. For instance, execution on one processor may interfere with the timing of an unrelated activity on another processor through a shared L2 or L3 cache. The timing of memory accesses can be affected by unrelated memory accesses of other processors through interference on a shared bus, and so on. It is not yet clear how to build predictable and performant systems on multicore platforms.

The work done within ARTIST on Predictability and Performance includes numerous highlights:

The Predator project has made strong progress in its attempt to reconcile Predictability with Performance. The integration of the AbsInt timing-analysis tool aiT with the WCET-aware compiler of TUDortmund was described separately. Another recent achievement of the project concerns the determination of context-switch costs, which provides support for schedulability analysis for preemptive scheduling strategies. Insights into the predictability properties of architectural features have found their way into the embedded-systems industry, e.g., as a result of collaboration in European projects. These insights, however, are still at odds with trends at the processor manufacturers' side. Suppliers of time-critical embedded systems cannot find platforms with the required predictability properties on the market.

The trends to multi-core platforms presents a significant challenge to the building of predictable and performant systems, and there was still significant hesitation to migrating embedded systems to multi-cores. Significant advances on isolation and analysis techniques have been made (to a large extent by ARTIST-Design partners): progress was made, e.g., in the area of deterministic access protocols and controllers for shared resources such as buses or memory. However, the worst-case delay used in safe approximations was still often too high to be acceptable.

A good collection of insights was gathered at the PPES workshop, organized by ARTIST-Design, jointly with Predator and Merasa, as a satellite event of DATE 2011 in Grenoble. Overviews about architecture and software issues were given, e.g. including a survey on predictability and performance requirements in avionics systems, and a template for, partly analytically, partly intuitively; estimating the predictability of hardware features was presented.

During year 4, development of support for the MARTE standard (initiated during ARTIST2), led by U. Cantabria, has provided increased support for scheduling and code generation. The work on integration between timing analysis tools has matured: several of the leading timing analysis tools have been integrated by efforts in the All-Times project (described in the report on Timing analysis).
A notable trend during Year 4 has been the work on reconciling predictability with performance, developing techniques for optimizing performance along several dimensions (e.g., combing WCET with average-case timing). Work in this direction (by Bologna, ETHZ, Linköping, Trento) has considered different forms of multi-objective optimization of embedded software; such possibilities also exist in the WCC compiler. Another increasingly important topic has been to make scheduling and timing analysis robust to inaccuracies in assumptions about, e.g., execution times, interferences, etc.
Work on the integration of timing analysis and compilation, in the context of the WCC compiler, aimed at removing some of the earlier restrictions. The work started at TU Dortmund considering WCET-aware basic block reordering has been finished. Unconditional branches are avoided and the prediction of conditional branches was supported by the developed techniques. A genetic approach applies evolutionary algorithms considering the WCET of the program to optimize as fitness value with the costs of high optimization times. Thus, an integer-linear programming-based approach has been developed which determines the optimal order of basic blocks and also takes the branch prediction into account [PKFM11]. Furthermore, WCET-aware cache locking and code positioning has been improved. The integration and enhancement of a framework for the static analysis of software and hardware as announced in last year's report has been advanced. The extension of WCC's native analysis capabilities allows for novel approaches especially in the domain of multitask- and multicore-aware compilation. A much higher degree of control over system states directly affected by optimization decisions can thus be achieved. The primary effort was made in the direction of tightening timing estimations and the evaluation and improvement of cache analysis techniques with a focus on improving compiler optimizations [KFM11].
http://ls12-www.cs.tu-dortmund.de/research/activities/wcc

vii. Industrial Integration

Each of the ArtistDesign Thematic Clusters (WP3-WP6) is important per se for advancing the state-of-the-art in embedded system design. However, if we wish to have a strong impact on industry and society at large, the results of the thematic clusters have to be harmonized in an overall design flow that can sustain the industrial embedded design chain from conception of the product to its implementation.

The chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g., Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI, Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics).

Today, there is stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, the system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There is a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company. The benefits of these flows and methods are obvious as they provide shorter time to market and better quality designs but require a will of the industrial segment to work together towards this goal. In the automotive domain, Autosar is an excellent step in that direction. Other industrial segments are less cohesive in searching for a unified approach to design. In addition, society concerns such as energy, health and environment conservation, are offering new business opportunities for emerging technologies such as wireless sensor networks. The difficulty in these new opportunities resides in lack of standards and of experience with new communication concepts and, last but not least, in security.

We believe that all the thematic clusters bring something important to all industrial segments, but we need to pay attention to the way the results obtained by the clusters are formulated. Integration is a matter of modelling and providing interfaces that guarantee that the properties of the components are maintained after integration. Integration takes two forms: an horizontal one where different IPs coming from different companies or from different design groups in the same company have to be assembled; a vertical one, where the requirements are clearly and possibly formally communicated from a higher level player to a lower level one and where the information about the capabilities and limitations of the IPs are unambiguously communicated from the lower level to the higher level. The ultimate goal of this activity is to provide the “meta rules” according to which the design transformations are carried out and interfaces are built and hence to provide strong guidance to the clusters to make their results more relevant and applicable. Understanding the roles and dynamics of an existing, well-established, vertical industrial segment is a complex task. We could only imagine the complexity of industrial segments that are coming together in these years. While we do target some industrial domain to be the driver for this activity, we understand that our research is going to be more relevant and better quality if we can distil some common traits of these domains and work with those to choose at a later date which particular chains to address.

The transversal activity hence has two prongs:

- to dive into particular vertical industrial segments and package design methods out of the thematic cluster results for the segments;
- to identify some important common features among verticals and work towards developing methods to address these topics.

We note that the two concerns that are also part of the Transversal JPRAs (predictability and adaptability) are common to almost all industrial concerns: For this reason, they provide a

framework to start the work on integration driven by industrial applications. Predictability has been a goal since the beginning of the modern industry: predicting the capabilities of existing components allows companies to come to market faster with new products and prevents taking dead ends; predicting the effort needed to develop parts of the design and their correct integration prevents early recalls and associated costs. The faster is the dynamics of the industry, the more important is to have predictability in design.

Adaptability is the property of a design to be adapted to changing environments and working conditions. Reconfigurability, programmability, dynamic restructuring are all facets of adaptability. Novel approaches to communication could benefit greatly from adaptability. In fact, much research is being carried out to design devices that could sense available bandwidth and adapt the communication protocol to the most convenient band at the time.

We believe that it will be eventually easier to compose the vertical design industrial flows once these two sub-flows have been examined and results obtained. In addition, being generic concerns they do not require effort from the academic partners to understand the modus operandi of entire industrial segments and offer a shorter time to results.

The vertical industrial segment motivated prong will begin by bringing up-to-speed the largest possible number of participants to the logic of the design chain by organizing workshops for discussion with the participants to the chain.

We proposed at the onset of the activity to target Automotive, Nomadic and Health Applications as potential vertical segments where we have a range of maturity from well-established (automotive) to emerging (health). At the 2008 meeting in Rome of the ArtistDesign partners, the three vertical markets of interest were identified as:

1. Automotive/avionics since we noted a strong similarity in the overarching issues faced by these two industrial segments that are driven by safety concerns and have to consider distributed implementations;
2. Health applications with particular emphasis on equipment design and manufacturing and a new thrust in the use of emebedded system design methodologies to synthetic biology;
3. Energy efficient buildings, a novel field of great interest to the European Community as well as to the rest of the world as 30% of energy consumption is considered to be in commercial buildings.

These applications address an established area of excellence of European Industry where international competition is fierce, an area of growth where again European Industry has a strong position but where the dynamics are fast and new applications are envisioned in strategic areas such as elderly care, and a new area with great potential where energy conservation concerns are going to place a great political emphasis. In addition, we believe that synthetic biology is going to have a fundamental role for the foreseeable future in the definition of new organisms to foster the creation of new drugs as well as new materials. Given the nature of this work, the main participants in the cluster are the groups that have industrial vocation such as ESI, OFFIS, and IMEC.

viii. Spreading Excellence

On the potential impact (including the socio-economic impact and the wider societal implications of the project so far) and the main dissemination activities and exploitation of results

Our actions for Spreading Excellence were at 2 levels:

- *Targeted towards affiliated partners*
  Affiliated partners are not core members in the consortium, but receive support for travelling to ArtistDesign meetings, and actively contribute to the implementation of the Joint Programme of Activities (JPA). These affiliated partners include industrial, SME, academic, and international collaboration affiliates.
- *Targeted towards the scientific and technical community in the large*
  This is achieved mainly bottom-up through the organisation of scientific events, publications, distribution of tools and components, industrial partnerships (not funded by ArtistDesign), education; and through the ArtistDesign web pages.
- *Targeted towards students*
  A particular focus has been placed on the ARTIST Summer Schools this year – with a truly outstanding programme of lecturers, and the innovation of providing the lectures in video form on the Artist website.

Regarding Scientific events, we distinguish between conferences and workshops, schools, and high-level events mainly for International Collaboration.

High Level Events for International Collaboration

High-level Events are intended to gather together the very best world-leading experts from academia and industry, to discuss progress on the state of the art, relevant work directions.

Three ArtistDesign members are on the steering board for the ARTEMIS European Technology Platform. In this capacity, they participate in working groups for defining the overall European long term strategy in the area.

Publications

The ArtistDesign community has pusrsued a very active publishing policy, with a strong presence in scientific journals and conferences, as attested by the extensive list of publications provided in this document. Publication of research is a bottom-up process, which may seem chaotic – but this is intrinsic to research.

Tools and Components

The ArtistDesign community plays a leading role in the distribution of software tools and components, on verification/validation tools. Some tools are distributed free of charge, such as UPAAL, IF. Others are commercialised, such as AbsInt, SymTA/S. For many other tools used in the platforms, and shared between the Artist partners, a common dissemination policy has not yet been defined.

Industrial Liaison

ArtistDesign has a wide array of affiliated industrial and SME partners (see the Thematic and Transversal Activity deliverables). Most of these partners have participated in some way in the ArtistDesign technical meetings and the overall effort. There is strong, high-level industry participation through the various Spreading Excellence events organised by ArtistDesign. Our active involvement in the European Technology Platform ARTEMIS also could have a significant and long-term impact.

We believe that the strong involvement of four main ArtistDesign partners in the SPEEDS Integrated Project has a very positive impact on progress in the state of the art, in component-based embedded systems engineering.

Affiliated partners

Affiliated partners are not core members in the consortium, but receive support for travelling to ArtistDesign meetings, and actively contribute to the implementation of the Jointly-executed Programme of Activities (JPA). These affiliated partners include industrial, SME, academic, and international affiliates.

Scientific and Technical Community in the Large

Interaction with these other scientific communities is achieved mainly bottom-up through the organisation of scientific events, publications, distribution of tools and components, industrial partnerships (not funded by ArtistDesign), education; and through the ArtistDesign web pages.

Our sponsoring policy aims specifically at enforcing integration of existing scientific events in the area. This is sought in particular through the Embedded Systems Week (http://www.esweek.org/), in which we play a crucial role.

Another concrete example is our action within the DATE conference (http://www.date-conference.com/), in which we are working to shift the emphasis towards becoming the central European conference on embedded systems design, in collaboration with the ARTEMIS European Technology Platform.

Regarding Scientific events, we distinguish between conferences and workshops, schools, and high-level events mainly for International Collaboration.

The ARTIST community now clearly leads the initiatives for organizing the most significant conferences in the area. In Europe, it has a very strong presence in the DATE conference, which is becoming the main conference on embedded systems within Europe. Over the past 10 years, 9 general chairs of DATE have been leading ARTIST members.

Artist partners are also active members of the ACM's SIGBED, and the IEEE's upcoming Special Interest Group on Embedded Systems currently being set up. Artist members actively work for structuring international events on embedded systems.

International Collaboration

International Collaboration has been one of the central activities pursued within ARTIST since 2003, and is described in detail in this document.

All of the recurring ARTIST International Collaboration events have continued and been expanded within ArtistDesign in 2011. Further details about the schools are available in the section "Organisation of Schools".

Publications

The ArtistDesign community is extremely active in publishing in scientific journals and conferences, as attested by the list of joint publications provided in this document.

Joint publications seem to be a reliable measure of integration and building excellence between the partners.

Industrial Liaison

ArtistDesign has a wide array of affiliated industrial and SME partners, as described in the deliverables' "Affiliated Partners" sections. Most of these partners participate in some way in the ArtistDesign technical meetings and the overall effort. There is strong, high-level industry participation through the various Spreading Excellence events organised by ArtistDesign.

Our active involvement in the European Technology Platform ARTEMIS also could have a significant and long-term impact. Several ArtistDesign partners, including VERIMAG, BOLOGNA, OFFIS and TU Vienna, are actively involved in the ARTEMIS ETP. The ArtistDesign Strategic Management Board was actively consulted for finalizing the 2011 release of the ARTEMIS Strategic Research Agenda.

In addition, each ArtistDesign partner has an outstanding track record for interaction with industry. Globally, the ArtistDesign consortium has a very strong impact on European R&D in embedded systems. This impact is visible via the achievements in Integrated Projects and STREPs (see below).

Links with ARTEMISIA

ArtistDesign has strong links to ARTEMIS, through:

- Representation on the **ARTEMIS Industry Association Steering Board**:
  - Joseph Sifakis is the CNRS representative
  - Luca Beninni is the University of Bologna representative
- Partner membership in **ARTEMIS "B"** (Research Organisations & Universities) http://www.artemisia-association.org/member_status
  - Arne Skou is the Aalborg University representative
  - Denis Platter is the CEA representative
  - Joseph Sifakis is the CNRS-Verimag representative
  - Boudewijn Haverkort is the Embedded Systems Institute representative
  - Rudy Lauwereins is the IMEC representative
  - Jean-Pierre Banâtre is the INRIA representative
  - Eduardo Tovar is the Instituto Superior de Engenharia do Porto representative (Instituto Politécnico do Porto in ArtistDesign)
  - Gunnar Landgren is the KTH representative
  - Bernhard Josko is the OFFIS representative
  - Jan Madsen is the TU Denmark representative
  - José Carlos Gómez Sal is the University of Cantabria representative
  - Luca Benini is the University of Bologna representative
  - Farid Ouabdesselam is the Université Joseph Fourier representative

- Strong *informal* links. For example, the ArtistDesign Strategic Management Board was asked to review and comment on the latest edition of the Strategic Research Agenda, published in 2011.
- Strong representation by ArtistDesign partners in ARTEMIS projects,

Sustainable Integration from ARTIST (EMSIG Special Interest Group)

The integration achieved within ARTIST will continue well beyond the end of the NoE, most notably through some of the more important initiatives within the Spreading Excellence effort.

For example, the newly-created EMSIG (Embedded systems Special Interest Group: http://emsig.embedded-systems-portal.org/ chair is Peter Marwedel, TU Dortmund), created within EDAA (http://www.edaa.com/) the permanent structure that handles the DATE conference, aims to:

- leverage on the ArtistDesign NoE results
- help to structure the Embedded Systems Design community
- identify areas of future research and development
- interact on a high level with industry, funding agencies, and other world-class structures (eg ARTEMIS)
- support the advancement of state of the art embedded systems design approaches
- facilitate the exchange of ideas and knowledge in embedded systems design
- provide visibility and dissemination (eg: web hosting for events), projects
- support the creation of project consortia
- spread knowledge in embedded systems design
- support the application of embedded systems technology

The ARTIST Summer School is also continuing beyond ARTIST, with support from Nano-Tera (EPFL): http://emsig.embedded-systems-portal.org/links/summer-schools#1027

Long-term Dissemination Channels

These include :

- The DATE conference (http://www.date-conference.com/), which has drawn a very large proportion of its General Chairs from the ARTIST NoE's prominent members.
- The CPSWeek conference (http://www.cpsweek.org/), which has always had very tight links with the ARTIST NoE
- Prof. Peter Marwedel's authoritative book "Embedded Systems Design" (http://www.springer.com/engineering/circuits+%26+systems/book/978-94-007-0256-1) This is part of a larger book series at Springer on Embedded Systems: http://www.springer.com/series/8563?detailsPage=titles

ArtistDesign Web Portal

Objectives and Background Information

The ArtistDesign Web Portal was a major tool for Spreading Excellence within the Embedded Systems Community. Its aim was rather ambitious: to be the focal point of reference for events and announcements of interest to the embedded systems community.

The web portal disseminates information about contacts (ArtistDesign core and affiliated partners), the ArtistDesign JPA activities, as well a fairly thorough set of links to sites of interest to the embedded systems community.

As can be seen, a great deal of effort has been put into the web site, both for ergonomics / graphical quality, as for the contents.

The web site includes several features that help keep it coherent and up to date:

Authorised users (principally, the ArtistDesign partners) can access the back end of the site to modify and update information directly. The changes are immediately visible on the site, which greatly streamlines the updating process.

It's possible to track changes and go back to previous versions of individual web pages.

Events are automatically sorted by date, and transferred to 'Past Events'. When appropriate.

Structural information (hierarchy of pages) was maintained automatically.

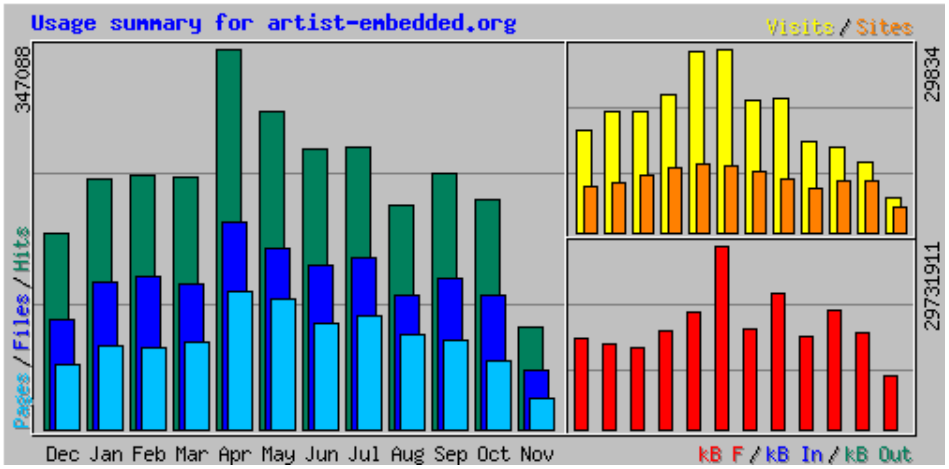
Ergnomics are set for the entire site. The "look and feel" of the site was always homogeneous thoughout the site. It's possible to change these ergonomics, and these changes are applied homogeneously throughout the site, via automated machanisms.

Structure

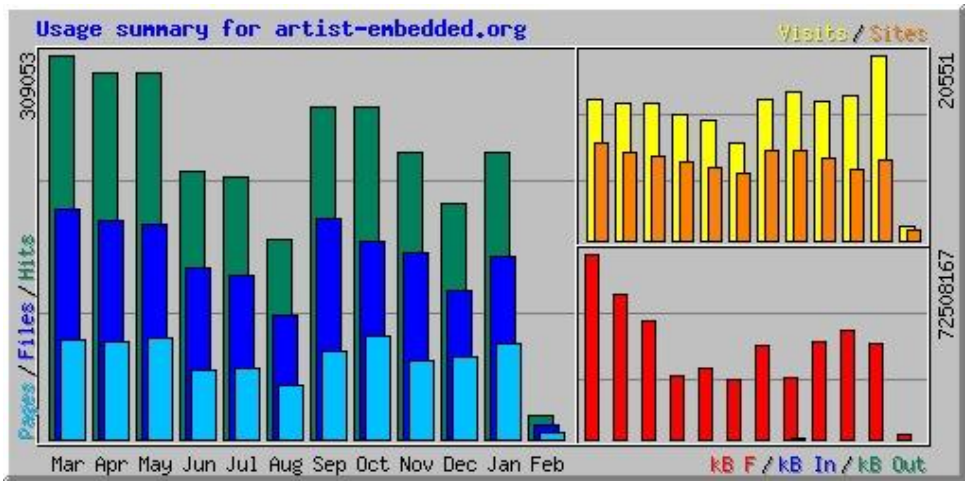
The structure of the ArtistDesign web site was visible on the Site Map: http://www.artist-embedded.org/artist/spip.php?page=plan). Analysis of Visits to the Portal

Number of Visits Overall

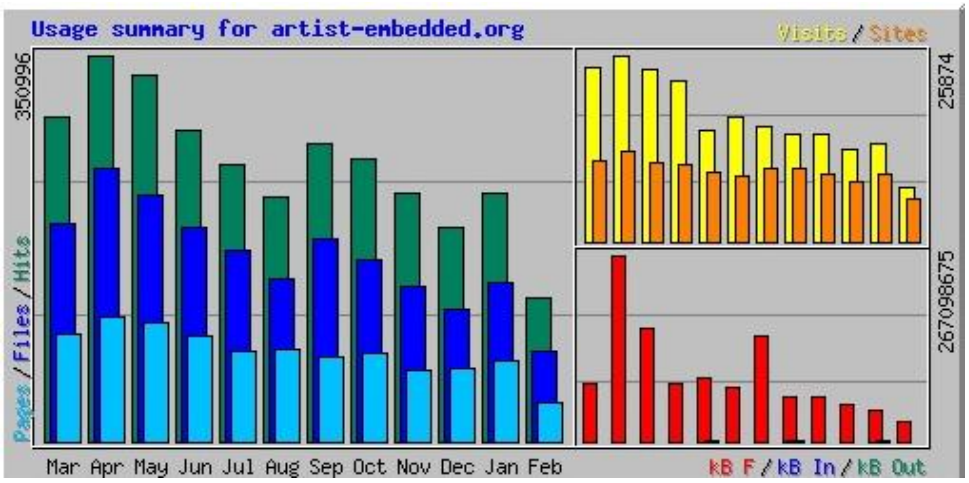
Year 1

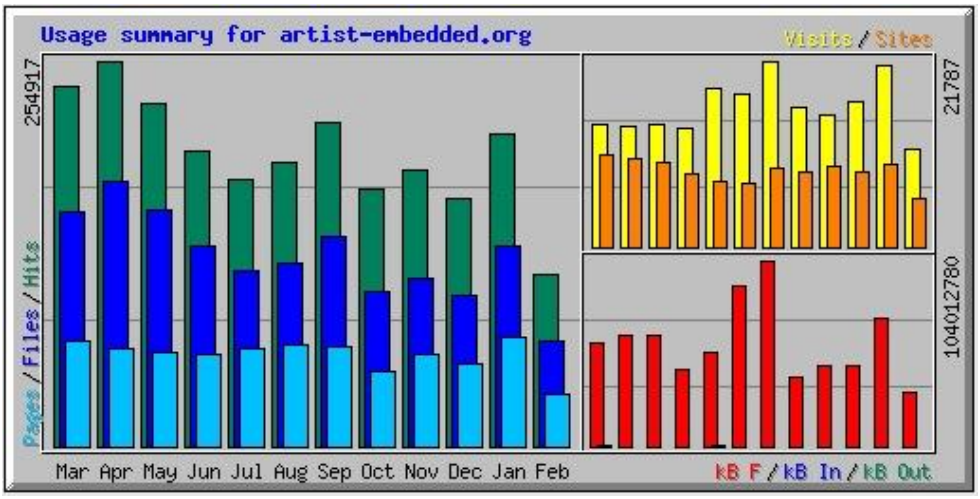


Year 2



Year 3





The main conclusion from this analysis was that visits to the site are largely driven by the ARTIST events organised (workshops, conferences, schools), and that this drives visits to the other sections: “Embedded Systems Links”, and “Research and Integration”.

Yearly variations do not necessarily imply that the portal has had less impact. For example, if key information (eg: the program or registration or venue) was missing from a workshop page, then it can logically be expected that visitors will return often, generating *more* traffic for what was, finally, *lower* impact and usability.

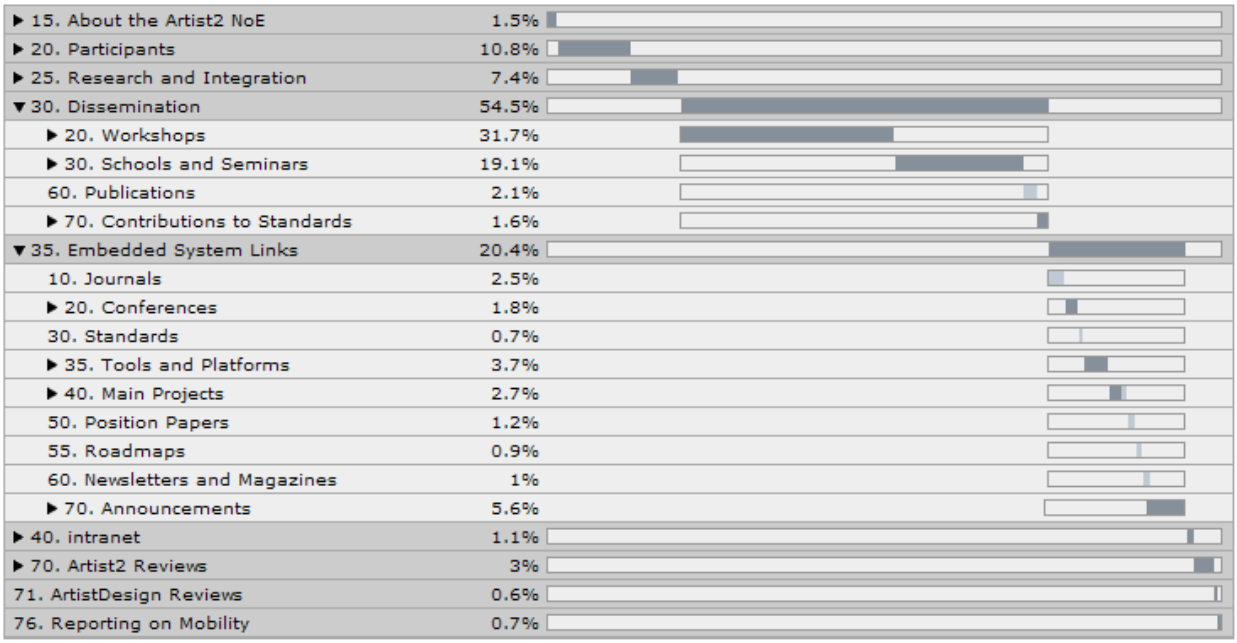
It was important to note that a deep analysis of the pertinence and effectivity of the web portal would need to go beyond the numerical analysis provided here. The real impact of a website was

in whether or not the members of the community find the information relevant, and how it helps them in their daily tasks.

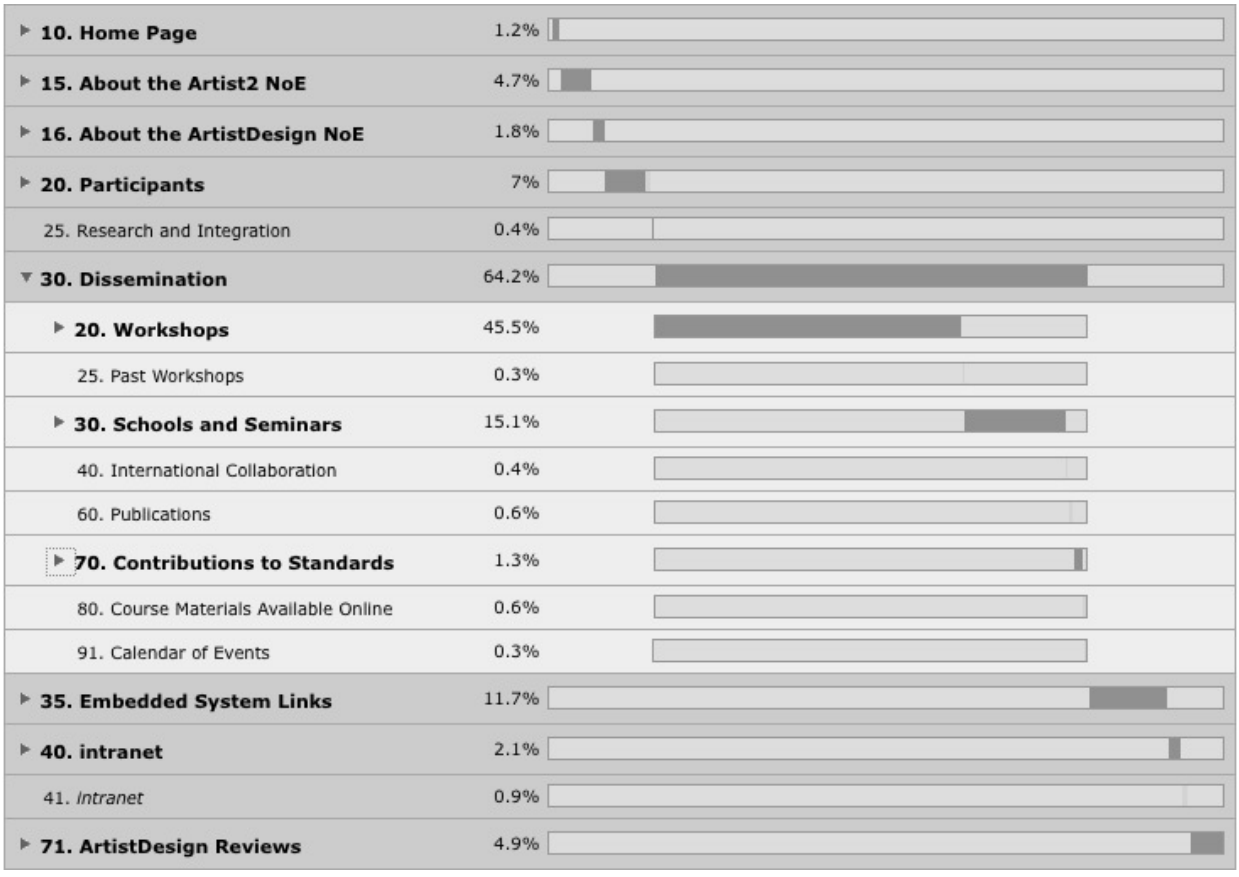
Visits Distribution within the site

The tables below show the distribution of visits to the various parts of the portal.

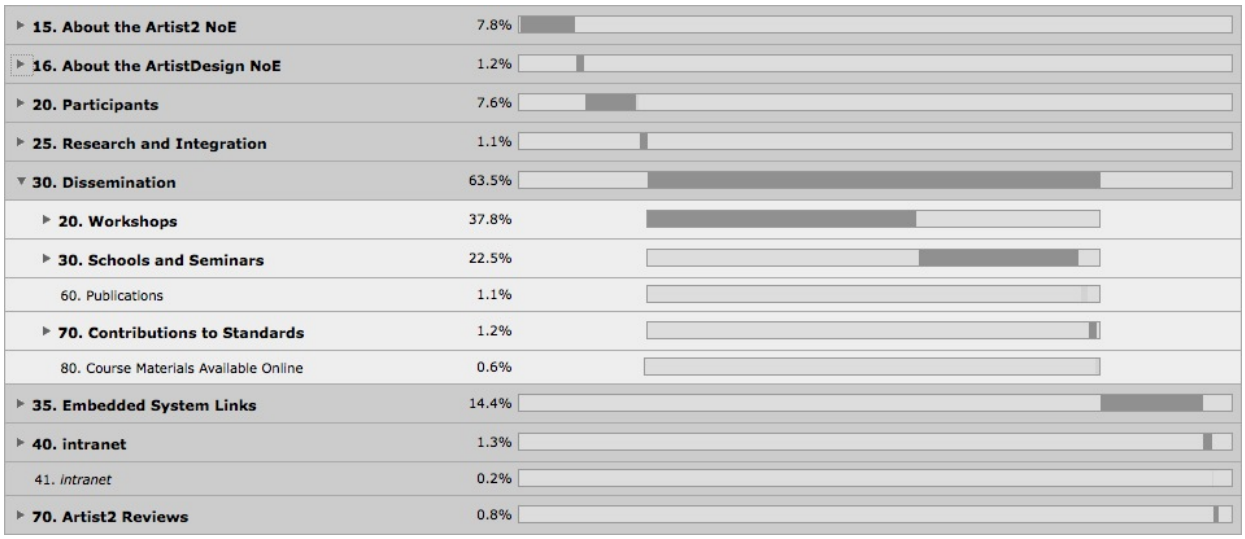
Year 1



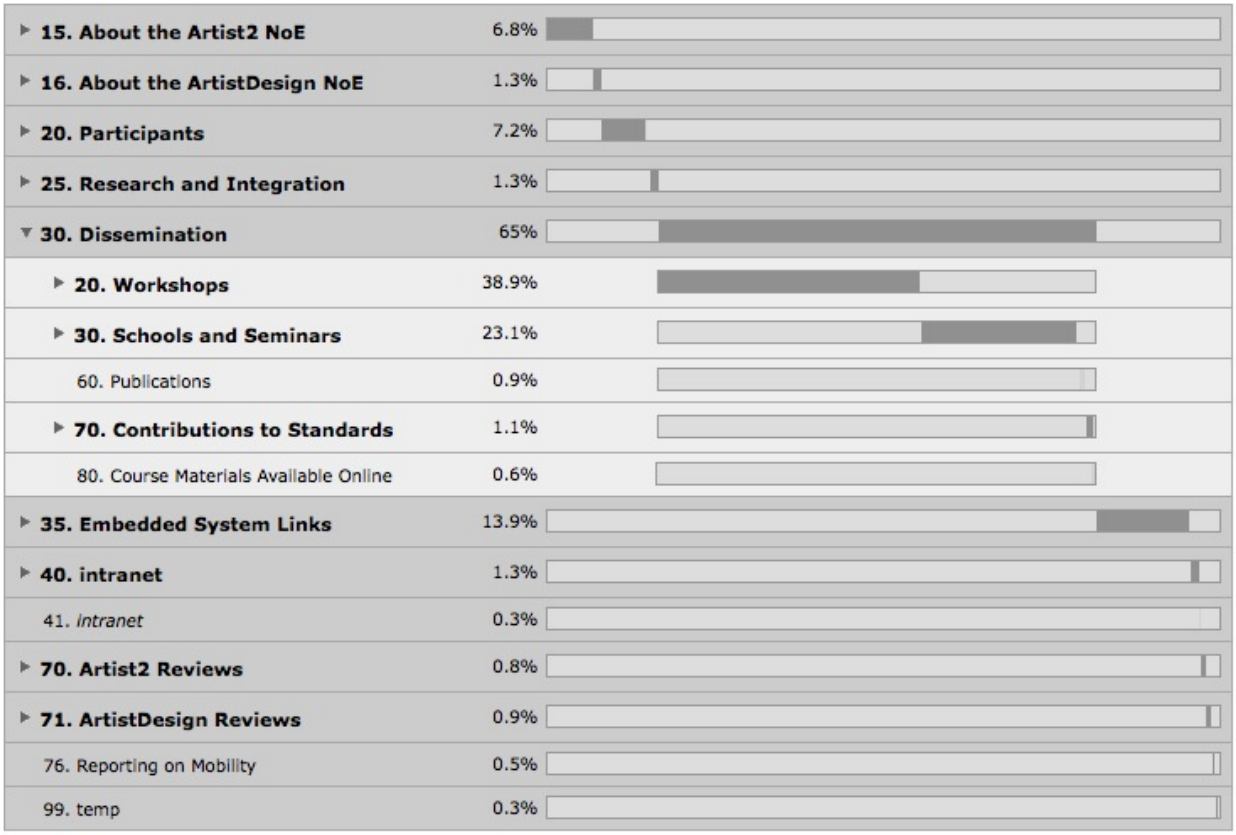
Year 2



Year 3


15. About the Artist2 NoE 7.8%
16. About the ArtistDesign NoE 1.2%
20. Participants 7.6%
25. Research and Integration 1.1%
30. Dissemination 63.5%
20. Workshops 37.8%
30. Schools and Seminars 22.5%
60. Publications 1.1%
70. Contributions to Standards 1.2%
80. Course Materials Available Online 0.6%
35. Embedded System Links 14.4%
40. intranet 1.3%
41. intranet 0.2%
70. Artist2 Reviews 0.8%

Year 4


15. About the Artist2 NoE 6.8%
16. About the ArtistDesign NoE 1.3%
20. Participants 7.2%
25. Research and Integration 1.3%
30. Dissemination 65%
20. Workshops 38.9%
30. Schools and Seminars 23.1%
60. Publications 0.9%
70. Contributions to Standards 1.1%
80. Course Materials Available Online 0.6%
35. Embedded System Links 13.9%
40. intranet 1.3%
41. intranet 0.3%
70. Artist2 Reviews 0.8%
71. ArtistDesign Reviews 0.9%
76. Reporting on Mobility 0.5%
99. temp 0.3%

2. Use and dissemination of foreground

The main instruments for using and disseminating knowledge are:

- Workshops and Schools organised.
  The list was quite impressive, and was provided in the deliverable on "Spreading Excellence".
- ArtistDesign Web Portal http://www.artist-embedded.org/
  Here also, the quantity of information made available to the greater embedded systems community was quite impressive, and continuously growing. This was possible through the efforts of the entire consortium, which now have direct access for updating the contents.
- Course Materials.
  There was a growing body of course materials made available via the ARTIST web portal.
- Publications.
  The ArtistDesign consortium was very prolific in publishing research articles, surveys, textbooks, roadmaps, and position papers.

The plan should consist of:

- Section A

This section should describe the dissemination measures, including any scientific publications relating to foreground. **Its content will be made available in the public domain** thus demonstrating the added-value and positive impact of the project on the European Union.

- Section B

This section should specify the exploitable foreground and provide the plans for exploitation. All these data can be public or confidential; the report must clearly mark non-publishable (confidential) parts that will be treated as such by the Commission. Information under Section B that was not marked as confidential **will be made available in the public domain** thus demonstrating the added-value and positive impact of the project on the European Union.

Section A (public)

List of articles for the 4th year of the project.

#	Title of the article	Journal Name	Volume	Issues	Pages		Month	Year	Author_1		Author_2		Author_3		Author_4		Author_5	
					from	to			Initials	Surname	Initials	Surname	Initials	Surname	Initials	Surname	Initials	Surname
1	Timed parity games: Complexity and robu	Logical Methods in Computer Science						2010	K	Chatterjee	T	Henzinge	S	Vinayak				
2	Separate Compilation of Hierarchical Real-Time Programs into Linear-bounded Embedded Machine Code	Science of Computer Programming						2010	A	Ghosal	D	Iercan	C	Kirsch	T	Henzinge	A	Sangiovanni-Vincentelli
3	Chapter "Software Compilation Techniques for MPSoCs"	in the book "Handbook of Signal Processing Systems"						2010	R	Leupers	W	Sheng	J	Castrillon	S	Bhattacha	EF	Deprettere
4	"Visual Sensor Networks for infomobility"	Pattern Recognition and Image Analysis: Advances in Mathematical Theory and Applications"						2011	M	Magrini	D	Moroni	C	Nastasi	P	Pagano	M	Petracca
5	Synthesis of Multi-task Implementations of Simulink Models with Minimum IEEE Transactions	on Industrial Informatics (TII)	6	4	637	651	NOV	2010	M	Di Natale	L	Guo	H	Zeng	A	Sangiovanni	Vincentelli	
6	Optimization of Task Allocation and Priority Assignment in Hard Real-time Distributed Systems	ACM Transactions in Embedded Computing Systems (TECS)						2010	Q	Zhu	H	Zeng	W	Zheng	M	Di Natale	A	Sangiovanni Vincentelli
7	Optimal Synthesis of Communication Procedures in Real-Time Synchronous Reactive Models	Delays IEEE Transactions on Industrial Informatics (TII)	6	4	729	743	NOV	2010	G	Wang	M	Di Natale	A	Sangiovanni	Vincentelli			
8	Separate compilation of hierarchical real-time programs into linear-bounded embedded machine code	Science of Computer Programming						2010	A	Ghosal	D	Iercan	C	Kirsch	T	Henzinge	A	Sangiovanni Vincentelli
9	"Optimizing the Software Architecture for Extensibility in Hard Real-time Distributed Systems"	Delays IEEE Transactions on Industrial Informatics (TII)	6	3				2010	Q	Zhu	Y	Yang	M	Di Natale	E	Scholte	A	Sangiovanni Vincentelli
10	"Comparative Analysis of NoCs for Two-Dimensional Versus Three-Dimensional SoCs Supporting Multiple Voltage and Frequency Islands	" IEEE Transactions on Circuits and Systems II: Express Briefs	57	5	364	368	MAY	2010	C	Seiculescu	S	Murali	L	Benini	G	De Micheli		

List of papers over the 4th year of the project:

#	Title of the article	Name of event	Author_1 Initials	Author_1 Surname	Author_2 Initials	Author_2 Surname	Author_3 Initials	Author_3 Surname	Author_4 Initials	Author_4 Surname	Author_5 Initials	Author_5 Surname
1	Robustness in the Presence of Liveness	CAV 2010: 410-424	R	Bloem	K	Chatterjee	K	Greimel	T	Henzinger	B	Jobstmann
2	Timed automata with observers under energy constraints	In Proceedings of the 13th ACM International Conference on Hybrid Systems: Computation and Control HSCC2010	P	Bouyer	U	Fahrenberg	KG	Larsen	N	Markey		
3	Generalized mean-payoff and energy games	Proceedings of the 30th Annual Conference on Foundations of Software Technology and Theoretical Computer Science (FSTTCS)	K	Chatterjee	L	Doyen	T	Henzinger	JF	Raskin		
4	Timed i/o automata: a complete specification theory for real-time systems	In Proceedings of the 13th ACM International Conference on Hybrid Systems: Computation and Control HSCC2010	A	David	KG	Larsen	A	Legay	U	Nyman	A	Wasowski
5	Model-Implemented Fault Injection for Hardware Fault Simulation	Models Workshop on Model-Driven Engineering	R	Svennings	H	Eriksson	J	Vinter	M	Törngren		
6	Timed I/O automata: a complete specification theory for real-time systems	In International Conference on Hybrid Systems: Computation and Control (HSCC'10)	A	David	KG	Larsen	A	Legay	U	Nyman	A	Wasowski
7	Statistical Model Checking: An Overview	International Conference on Runtime Verification RV'10	A	Legay	B	Delahaye	S	Bensalem				
8	Statistical Abstraction and Model-Checking of Large Heterogeneous Systems	IFIP International Conference on Formal Techniques for Distributed Systems FMOODS/FORTE'10	A	Basu	S	Bensalem	M	Bozga	B	Caillaud	B	Delahaye
9	On zone-based analysis of duration probabilistic automata	In Proceedings of INFINITY International Workshop on Verification of Infinite-State Systems	O	Maler	KG	Larsen	B	Krogh				
10	An Automatic Framework for Dynamic Data Structures Optimization in C	In Proceedings of the 18th international conference on Very Large Scale Integration (VLSI)	C	Baloukas	L	Papadopoul	R	Pyka	D	Soudris	P	Marwedel
11	Predictability Considerations in the Design of Multi-Core Embedded Systems	Proceedings of Embedded Real Time Software and Systems (ERTSS)	C	Cullmann	C	Ferdinand	G	Gebhard	D	Grund	C	Maiza
12	"Optimum Allocation of Distributed Service Workflows with Probabilistic Real-Time Guarantees	Springer Service Oriented Computing and Applications (SOCA); 2010;	K	Konstantel	T	Cucinotta	T	Varvarigou				
13	"A Real-time Service Oriented Infrastructure	" to appear in Proceedings of the Annual International Conference on Real-Time and Embedded Systems (RTES 2010)	D	Kyriazis	A	Menychtas	G	Kousiouris	K	Oberle	T	Voith
14	"Timing Analysis and Optimization of FlexRay Dynamic Segment"	ICESS Conference	H	Zeng	A	Ghosal	M	Di Natale				

15	“Modeling Languages for Real-time and Embedded Systems: Requirements and Standards-Based Solutions”	Model-Based Engineering of Embedded Real-Time Systems (MBEERTS)	S	Gérard	H	Espinoza	F	Terrier	F	Tufo	G	Gentile
16	Dynamic Scheduling and Control-Quality Optimization of Self-Triggered Control Applications	In Proc	S	Samii	P	Eles	Z	Peng	P	Tabuada	A	Cervin
17	Parameter Selection for Real-Time Controllers in Resource-Constrained Systems	IEEE Transactions on Industrial Informatics	Y	Wu	G	Buttazzo	E	Bini	A	Cervin		
18	Improving the efficiency of Ethernet switches for real-time communication	WARM 2010 - Workshop on Adaptive Resource Management (within the Cyber-Physical Systems Week)	R	Santos	A	Vieira	R	Marau	P	Pedreiras	A	Oliveira
19	Reconfigurable Real-Time Service-Oriented Middleware with FTT-CORBA	ETFA 2010	I	Calvo	L	Almeida	F	Pérez	A	Noguero	M	Marcos
20	INDEXYS a Logical Step beyond GENESYS	SAFECOMP 10	A	Eckel	P	Milbredt	Z	Zaid Al-Ars	S	Schneele	B	Vermeulen
21	Model-Based Power Estimation of NoC-Based MPSoCs	25th South Symposium on Microelectronics (SIM)	L	Ost	G	Guindani	L	Indrusiak	F	Moraes		
22	Factory Automation	Chapter 9	L	Lo Bello	E	Toscano	S	Vittorio				
23	“Real-Time Communications over Cluster-Tree Wireless Sensor Networks”	PhD Thesis in Electrical Engineering and Information Technology	P	Jurcik								
24	“Scalable instruction set simulator for thousand-core architectures running on GPGPUs”	High Performance Computing and Simulation (HPCS)	S	Raghav	M	Ruggiero	D	Atienza	C	Pinto	A	Marongiu
25	``Networks on Chips: from Research to Products	'' in Proceedings of the 47th Design Automation Conference (DAC 2010)	G	De Micheli	C	Seiculescu	S	Murali	L	Benini	F	Angiolini
26	Adaptive Power Management for Environmentally Powered Systems (2010)	in: Computers	C	Moser	L	Thiele	D	Brunelli	L	Benini		

27	"Cool MPSoC programming	Design; Automation & Test in Europe Conference & Exhibition (DATE); 2010 ; vol;; no;; pp;1488-1493; 8-12 March 2010;	R	Leupers	L	Thiele	X	Nie	B	Kienhuis	M	Weiss
28	"Multi-objective Exploration of Compiler Optimizations for Real-Time Systems	Object-Oriented Real-Time Distributed Computing; IEEE International Symposium on; pp; 115-122; 2010 13th IEEE International Symposium on Object/Component/Service-Oriented Real-Time Distributed Computing; 2010;	P	Lokuciejew	S	Plazar	H	Falk	P	Marwedel	L	Thiele
29	: Adaptive Power Management for Environmentally Powered Systems	IEEE Transactions on Computers (59:4)	C	Moser	L	Thiele	D	Brunelli	L	Benini		
30	Synchronous Reactive Task Management for Fine Grain Parallelism in Manycores Architectures	Submitted to Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures 2010	M	Ojail	K	Ben Chehida	Y	Lhuillier	R	David	L	Benini
31	Dynamic Scheduling and Control-Quality Optimization of Self-Triggered Control Applications	Proceedings of 31st IEEE Real-Time Systems Symposium (RTSS10)	S	Samii	P	Eles	Z	Peng	P	Tabuada	A	Cervin
32	“Adaptive Resource Management Framework for Mobile Terminals - the ACTORS Approach”	In Proc of the First International Workshop on Adaptive Reesource Management (WARM 2010)	V	Romero Se	KE	Årzén	S	Schorr	R	Guerra	G	Fohler
33	“A framework for automatic parallelization static and dynamic memory optimization in MPSoC platforms”	In Proceedings of the 47th ACM/IEEE Design Automation Conference – DAC	Y	Iosifidis	A	Mallik	S	Mamagkakis	E	De Greef	A	Bartzas
34	“Adaptive Power Management for Real-Time Event Streams”	15th IEEE Conf on Asia and South Pacific Design Automation Conference (ASP-DAC)	K	Huang	L	Santinelli	JJ	Chen	L	Thiele	GC	Buttazzo
35	“Adaptive Power Management for Environmentally Powered Systems”	IEEE Transactions on Computers (59:4)	C	Moser	L	Thiele	D	Brunelli	L	Benini		
36	Approximating Pareto Optimal Compiler Optimization Sequences - a Trade-Off between WCET	ACET and Code Size	P	Lokuciejew	S	Plazar	H	Falk	P	Marwedel	L	Thiele
37	Moving from Federated to Integrated Architectures in Automotive: The Role of Standards Methods and Tools	Proceedings of the IEEE	M	Di Natale	A	Sangiovanni Vincentelli						
38	Model-based Safety Engineering of Interdependent Functions in Automotive Vehicles Using EAST-ADL2	29th International Conference on Computer Safety Reliability and Security (SAFECOMP)	A	Sandberg	D	Chen	H	Lönn	R	Johansson	L	Feng
39	Abstract and concrete data type optimizations at the UML and C/C++ level for dynamic embedded software	Book chapter in Behavioral Modeling for Embedded Systems and Technologies: Applications for Design and Implementation (2010)	C	Baloukas	M	Temmerma	A	Keller	S	Mamagkak	F	Catthoor

Section B (Confidential[2] or public: confidential information to be marked clearly)
Part B1

None

Part B2
Please complete the table hereafter:

NONE

In addition to the table, please provide a text to explain the exploitable foreground, in particular:

- Its purpose
- How the foreground might be exploited, when and by whom
- IPR exploitable measures taken or intended
- Further research necessary, if any
- Potential/expected impact (quantify where possible)

[2] Note to be confused with the "EU CONFIDENTIAL" classification for some security research projects.

3. Report on societal implications

Replies to the following questions will assist the Commission to obtain statistics and indicators on societal and socio-economic issues addressed by projects. The questions are arranged in a number of key themes. As well as producing certain statistics, the replies will also help identify those projects that have shown a real engagement with wider societal issues, and thereby identify interesting approaches to these issues and best practices. The replies for individual projects will not be made public.

A General Information *(completed automatically when **Grant Agreement number** is entered.*	
Grant Agreement Number:	**214373**
Title of Project:	**ArtistDesign – Design for Embedded Systems**
Name and Title of Coordinator:	Joseph SIFAKIS (scientific coordinator)

B Ethics	
1. Did your project undergo an Ethics Review (and/or Screening)? • If Yes: have you described the progress of compliance with the relevant Ethics Review/Screening Requirements in the frame of the periodic/final project reports? Special Reminder: the progress of compliance with the Ethics Review/Screening Requirements should be described in the Period/Final Project Reports under the Section 3.2.2 *'Work Progress and Achievements'*	***~~0Yes~~ 0No***
2. Please indicate whether your project involved any of the following issues (tick box) :	
RESEARCH ON HUMANS	
• Did the project involve children?	***0No***
• Did the project involve patients?	***0No***
• Did the project involve persons not able to give consent?	***0No***
• Did the project involve adult healthy volunteers?	***0No***
• Did the project involve Human genetic material?	***0No***
• Did the project involve Human biological samples?	***0No***
• Did the project involve Human data collection?	***0No***
RESEARCH ON HUMAN EMBRYO/FOETUS	
• Did the project involve Human Embryos?	***0No***
• Did the project involve Human Foetal Tissue / Cells?	***0No***
• Did the project involve Human Embryonic Stem Cells (hESCs)?	***0No***
• Did the project on human Embryonic Stem Cells involve cells in culture?	***0No***
• Did the project on human Embryonic Stem Cells involve the derivation of cells from Embryos?	***0No***
PRIVACY	
• Did the project involve processing of genetic information or personal data (eg. health, sexual lifestyle, ethnicity, political opinion, religious or philosophical conviction)?	***0No***
• Did the project involve tracking the location or observation of people?	***0No***
RESEARCH ON ANIMALS	
• Did the project involve research on animals?	***0No***
• Were those animals transgenic small laboratory animals?	***0No***
• Were those animals transgenic farm animals?	***0No***

• Were those animals cloned farm animals?	***0No***
• Were those animals non-human primates?	***0No***
RESEARCH INVOLVING DEVELOPING COUNTRIES	
• Did the project involve the use of local resources (genetic, animal, plant etc)?	***0No***
• Was the project of benefit to local community (capacity building, access to healthcare, education etc)?	***0No***
DUAL USE	
• Research having direct military use	~~0 Yes~~ 0 No
• Research having the potential for terrorist abuse	***0No***

C Workforce Statistics

3. Workforce statistics for the project: Please indicate in the table below the number of people who worked on the project (on a headcount basis).

Type of Position	Number of Women	Number of Men
Scientific Coordinator	0	1
Work package leaders	2	5
Experienced researchers (i.e. PhD holders)	15	35
PhD Students	8	10
Other	2	2

4. How many additional researchers (in companies and universities) were recruited specifically for this project?	
Of which, indicate the number of men:	15

D Gender Aspects

5. Did you carry out specific Gender Equality Actions under the project?

○ Yes
x No

6. Which of the following actions did you carry out and how effective were they?

		Not at all effective				Very effective
❑	Design and implement an equal opportunity policy	x	○	○	○	○
❑	Set targets to achieve a gender balance in the workforce	x	○	○	○	○
❑	Organise conferences and workshops on gender	x	○	○	○	○
❑	Actions to improve work-life balance	x	○	○	○	○

○ Other:

7. Was there a gender dimension associated with the research content – i.e. wherever people were the focus of the research as, for example, consumers, users, patients or in trials, was the issue of gender considered and addressed?

○ Yes- please specify

x No

E Synergies with Science Education

8. Did your project involve working with students and/or school pupils (e.g. open days, participation in science festivals and events, prizes/competitions or joint projects)?

x Yes- please specify: Conferences & courses

○ No

9. Did the project generate any science education material (e.g. kits, websites, explanatory booklets, DVDs)?

X Yes- please specify: DVD on content of summer schools

○ No

F Interdisciplinarity

10. Which disciplines (see list below) are involved in your project?

x Main discipline[3]:

○ Associated discipline[3]:

○ Associated discipline[3]:

G Engaging with Civil society and policy makers

11a Did your project engage with societal actors beyond the research community? *(if 'No', go to Question 14)*

○ Yes
x No

11b If yes, did you engage with citizens (citizens' panels / juries) or organised civil society (NGOs, patients' groups etc.)?

○ No
○ Yes- in determining what research should be performed
○ Yes - in implementing the research
○ Yes, in communicating /disseminating / using the results of the project

[3] Insert number from list below (Frascati Manual).

11c In doing so, did your project involve actors whose role is mainly to organise the dialogue with citizens and organised civil society (e.g. professional mediator; communication company, science museums)?	○ ○	Yes No

12. Did you engage with government / public bodies or policy makers (including international organisations)

- ○ No
- ○ Yes- in framing the research agenda
- ○ Yes - in implementing the research agenda
- ○ Yes, in communicating /disseminating / using the results of the project

13a Will the project generate outputs (expertise or scientific advice) which could be used by policy makers?

- ○ Yes – as a **primary** objective (please indicate areas below- multiple answers possible)
- ○ Yes – as a **secondary** objective (please indicate areas below - multiple answer possible)
- ○ No

13b If Yes, in which fields?

Agriculture		Energy		Human rights	
Audiovisual and Media		Enlargement		Information Society	
Budget		Enterprise		Institutional affairs	
Competition		Environment		Internal Market	
Consumers		External Relations		Justice, freedom and security	
Culture		External Trade		Public Health	
Customs		Fisheries and Maritime Affairs		Regional Policy	
Development Economic and Monetary Affairs		Food Safety		Research and Innovation	
		Foreign and Security Policy		Space	
Education, Training, Youth		Fraud		Taxation	
Employment and Social Affairs		Humanitarian aid		Transport	

13c If Yes, at which level?

- ○ Local / regional levels
- ○ National level
- ○ European level
- ○ International level

H Use and dissemination

14. How many Articles were published/accepted for publication in peer-reviewed journals?	**More than 250**
To how many of these is open access[4] provided?	
How many of these are published in open access journals?	
How many of these are published in open repositories?	
To how many of these is open access not provided?	
Please check all applicable reasons for not providing open access:	
❑ publisher's licensing agreement would not permit publishing in a repository ❑ no suitable repository available ❑ no suitable open access journal available ❑ no funds available to publish in an open access journal X lack of time and resources ❑ lack of information on open access ❑ other[5]: ……	

15. How many new patent applications ('priority filings') have been made? *("Technologically unique": multiple applications for the same invention in different jurisdictions should be counted as just one application of grant).*		**0**
16. Indicate how many of the following Intellectual Property Rights were applied for (give number in each box).	Trademark	**0**
	Registered design	**0**
	Other	**0**
17. How many spin-off companies were created / are planned as a direct result of the project?		**0**
Indicate the approximate number of additional jobs in these companies:		**0**

18. Please indicate whether your project has a potential impact on employment, in comparison with the situation before your project:

❑	Increase in employment, or	❑	In small & medium-sized enterprises
❑	Safeguard employment, or	❑	In large companies
❑	Decrease in employment,	❑	None of the above / not relevant to the project
X	Difficult to estimate / not possible to quantify		

19. For your project partnership please estimate the employment effect resulting directly from your participation in Full Time Equivalent (*FTE = one person working fulltime for a year*) jobs:	*Indicate figure:*

[4] Open Access is defined as free of charge access for anyone via Internet.
[5] For instance: classification for security project.

Difficult to estimate / not possible to quantify	x

I Media and Communication to the general public

20. As part of the project, were any of the beneficiaries professionals in communication or media relations?

x Yes ○ No

21. As part of the project, have any beneficiaries received professional media / communication training / advice to improve communication with the general public?

○ Yes x No

22 Which of the following have been used to communicate information about your project to the general public, or have resulted from your project?

x	Press Release	x	Coverage in specialist press
❑	Media briefing	❑	Coverage in general (non-specialist) press
❑	TV coverage / report	❑	Coverage in national press
❑	Radio coverage / report	❑	Coverage in international press
x	Brochures /posters / flyers	x	Website for the general public / internet
x	DVD /Film /Multimedia	x	Event targeting general public (festival, conference, exhibition, science café)

23 In which languages are the information products for the general public produced?

❑	Language of the coordinator	x	English
❑	Other language(s)		

***Question F-10*:** Classification of Scientific Disciplines according to the Frascati Manual 2002 (Proposed Standard Practice for Surveys on Research and Experimental Development, OECD 2002):

FIELDS OF SCIENCE AND TECHNOLOGY

1. NATURAL SCIENCES

1.1 Mathematics and computer sciences [mathematics and other allied fields: computer sciences and other allied subjects (software development only; hardware development should be classified in the engineering fields)]

1.2 Physical sciences (astronomy and space sciences, physics and other allied subjects)

1.3 Chemical sciences (chemistry, other allied subjects)

1.4 Earth and related environmental sciences (geology, geophysics, mineralogy, physical geography and other geosciences, meteorology and other atmospheric sciences including climatic research, oceanography, vulcanology, palaeoecology, other allied sciences)

1.5 Biological sciences (biology, botany, bacteriology, microbiology, zoology, entomology, genetics, biochemistry, biophysics, other allied sciences, excluding clinical and veterinary sciences)

2 ENGINEERING AND TECHNOLOGY

2.1 Civil engineering (architecture engineering, building science and engineering, construction engineering, municipal and structural engineering and other allied subjects)

2.2 Electrical engineering, electronics [electrical engineering, electronics, communication engineering and systems, computer engineering (hardware only) and other allied subjects]

2.3. Other engineering sciences (such as chemical, aeronautical and space, mechanical, metallurgical and materials engineering, and their specialised subdivisions; forest products; applied sciences such as

geodesy, industrial chemistry, etc.; the science and technology of food production; specialised technologies of interdisciplinary fields, e.g. systems analysis, metallurgy, mining, textile technology and other applied subjects)

3. MEDICAL SCIENCES

3.1 Basic medicine (anatomy, cytology, physiology, genetics, pharmacy, pharmacology, toxicology, immunology and immunohaematology, clinical chemistry, clinical microbiology, pathology)

3.2 Clinical medicine (anaesthesiology, paediatrics, obstetrics and gynaecology, internal medicine, surgery, dentistry, neurology, psychiatry, radiology, therapeutics, otorhinolaryngology, ophthalmology)

3.3 Health sciences (public health services, social medicine, hygiene, nursing, epidemiology)

4. AGRICULTURAL SCIENCES

4.1 Agriculture, forestry, fisheries and allied sciences (agronomy, animal husbandry, fisheries, forestry, horticulture, other allied subjects)

4.2 Veterinary medicine

5. SOCIAL SCIENCES

5.1 Psychology

5.2 Economics

5.3 Educational sciences (education and training and other allied subjects)

5.4 Other social sciences [anthropology (social and cultural) and ethnology, demography, geography (human, economic and social), town and country planning, management, law, linguistics, political sciences, sociology, organisation and methods, miscellaneous social sciences and interdisciplinary , methodological and historical S1T activities relating to subjects in this group. Physical anthropology, physical geography and psychophysiology should normally be classified with the natural sciences].

6. HUMANITIES

6.1 History (history, prehistory and history, together with auxiliary historical disciplines such as archaeology, numismatics, palaeography, genealogy, etc.)

6.2 Languages and literature (ancient and modern)

6.3 Other humanities [philosophy (including the history of science and technology) arts, history of art, art criticism, painting, sculpture, musicology, dramatic art excluding artistic "research" of any kind, religion, theology, other fields and subjects pertaining to the humanities, methodological, historical and other S1T activities relating to the subjects in this group]