INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

Grant Agreement nº 216373

D2.6 First report on Sponsoring of Events program

Due date of deliverable: 28-02-2010
Actual submission date: 28-02-2010

Start date of project: 01-01-2008 Duration: 39 months

Project coordinator: Prof. Francisco Gámiz, UGR
Project coordinator organisation: University of Granada, Spain Rev.1

Project co-funded by the European Commission within the Seventh Framework Programme (FP7)		
Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

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1. Introduction

Other of the goals of EUROSOI+ project is to increase knowledge and expertise about SOI technology in Europe by enhancing interaction and synergy between academic groups and industry. To do so, we will sponsor SOI related events all over the world, in particular, conferences, training courses, and scientific publications (other than the ones organized by EUROSOI+).

EUROSOI+ will support additional activities in Europe that contribute to the development of its objectives, such as conferences, training courses, scientific publications, etc. Applicants should send the coordinator a short proposal (max. 4 pages) including a short CV and describing the purpose of the event (conference, course, etc.), duration, detailed budget, support requested, etc. Partial support (e.g. grants for travelling and subsistence, organization) will be given on a competitive basis to events satisfying a priori the following conditions:

1. the field covered by the event should fall within at least one of the strategic research domains defined by EUROSOI+.
2. At least one EUROSOI+ partner should be involved in the organizing committee of the event.

The beneficiary of this grant for the support of such events will have to provide the coordinator with a written report explaining the nature of the event and how the event contributes to the development of EUROSOI+ objectives. At the end of the project, the coordinator will elaborate a report summarizing the activity (Deliverables D2.6&D2.7

2.- Sponsoring of events.

Since the starting of the project in 2008 the following tasks have been performed in this line of actuation:

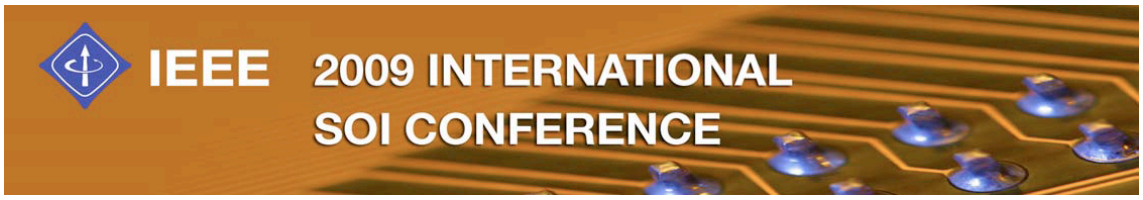
A. IEEE International Conference on Silicon-on-Insulator.

In October, 2008 and October, 2009, Noel Rodriguez (UGR) attended the IEEE International SOI Conference in USA to promote the activities of EUROSOI in the United States (http://www.soiconference.org).

A1.- IEEE International SOI conference, 2008

The 34th IEEE International Silicon on Insulator (SOI) Conference, provided a comprehensive review of the current state of the technology. The Conference comprised a Technical Program, the principal activity; a Short Course; a Fundamentals Class; and an evening Panel Discussion. That year's Short Course was "Extreme SOI – Technology, Applications, Test" delivered by six specialists covering a comprehensive overview of the following advanced SOI topics: ultra low power technology and application, soft errors in advanced technologies, high temperature electronics, Built In Self Test, SOI photonic circuits and optical interconnects, as well as future prospects for extreme ultra low power. The Short Course was organized by Dr. Vyshnavi Suntharalingam of MIT Lincoln Laboratory. The Technical Program Committee, chaired by Dr. Mario Pelella of AMD, selected an exceptional set of technical papers that substantially advance the field. The new information broadened the perspectives of active SOI specialists as well as provided the necessary background for newcomers to this exciting technology. The Plenary Session, which kicked off the Technical Program featured three invited speakers discussing various key topics related to SOI technologies. An optional "SOI Devices and Circuits Fundamentals Class", provided conference attendees with an enhanced overall experience and an improved understanding of SOI device physics and SOI circuit design. This educational class, organized by Dr. Jurczak Malgorzata of IMEC, was instructed by two pioneers of the SOI community. The topic of the Panel Discussion was "Will SOI Enter the Foundry Market?" Organized by Dr. Jean Luc Pelloie of ARM, the panel comprised distinguished experts discussing their views on this important topic. Dr. Robert H. Dennard of IBM, inventor of the DRAM memory cell and author of the MOS "scaling theory", also gave a nice talk. Dr. Dennard's talk was entitled "Reflections on the Evolution of MOS/CMOS Scaling and Possible Future Directions". It presented a personal history of MOS scaling from the early years, covering the different phases of scaling, how it has evolved and where we are today. The challenges for the future were discussed along with thoughts about how SOI technology may help.

A2.- IEEE International SOI conference, 2009



The 2009 IEEE International Silicon on Insulator (SOI) Conference provided a comprehensive review of the current state of the technology. It comprised a Technical Program; a Short Course; a Fundamentals Class; and an evening Panel Discussion. The theme of this year's Short Course was "Ultra-thin SOI Devices: The Way to the Future." Five renowned experts in the field provided a comprehensive overview of the operation and technology of these advanced fully depleted SOI device architectures. The topics covered included: process, process integration, electrical operation, device physics, modeling, and circuit design, including memory applications. The Short Course was organized by Dr. Jean-Luc Pelloie of ARM. The Technical Program Committee, chaired by Dr. Carlos Mazure of Soitec, selected a truly exceptional set of papers that substantially advance the field. The new information will broaden the perspectives of active specialists as well as provide the necessary background for newcomers to SOI technology. The Plenary Session, which kicks off the Technical Program on Tuesday, October 6th, will feature three invited speakers discussing various timely topics of keen interest to the SOI Community. Also a SOI Device and Circuit Fundamentals class was offered that provided attendees an opportunity to improve their skills and understanding of SOI device operation and SOI circuit design. The two classes covered the basic physics, performance comparison, and scaling limits of SOI devices and various aspects of SOI Analog circuit design including noise, ESD, passive components, and low power design. This educational class was organized by Dr. Samuel Fung of TSMC.

The topic of the Evening Panel Discussion was "Issues and Opportunities in Circuit Design: Bulk vs. PDSOI vs. FDSOI." The panel, organized by Dr. Bruce Doris of IBM, was comprised of distinguished industry experts conveying and supporting their views on this important topic. We look forward to a lively debate as the audience will be encouraged to challenge panel members with alternate opinions.

B. **Korean International Summer School on Nanoelectronics (nano KISS 2010)**

SOI Technology: Materials, Devices and Applications
7th-10th April 2010
Pyeongsan Academy, Daegu, KOREA
http://nano-kiss.knu.ac.kr

Nano-KISS, an international school for promoting high-level scientific and technical information, announced the final program of its first annual meeting, this year dedicated to silicon-on-insulator (SOI) materials, devices, and circuits. Key to nano-KISS success will be the strong synergy between fundamental science, applied physics, technology, and SOI application-oriented developments. Nano-KISS was inspired by the European Summer School MIGAS, supported by SINANO and EUROSOI programs. World-leading experts will give extended lectures and will entertain topical discussions with the participants. Professor J.P.Colinge (Tyndall, Ireland) will explain the benefits of SOI technology for the microelectronics market while introducing a variety of SOI devices and circuits. Dr. S. W. Chung (Hynix) and Prof. S. H. Kong (KNU, Korea) will focus on the development of floating-body SOI DRAMs and MEMS/NEMS, respectively. Dr C. Mazure (Soitec, France) will describe advanced technologies for SOI wafers. Dr. T. Ernst (LETI, France) and Prof. A. Zaslavsky (Brown Univ, USA) will present the operating mechanisms of single-gate, multiple-gate and tunneling transistors. Advanced reliability and characterization issues will be addressed by Profs. R. Schrimpf (Vanderbilt Univ, USA) and S. Cristoloveanu (Grenoble Univ, France). Finally, the secrets of CMOS technology and circuit design will be unveiled by Drs. D-W. Kim (Samsung) and R. Ferrant (France), respectively. “SOI is entering an exciting period of developments. Originally used for high-performance microprocessors, SOI is now moving to other markets dedicated to low-power and mobile applications, memory and power devices,” notes the School chair Sorin Cristoloveanu.

Korean International Summer School on Nanoelectronics (nano-KISS 2010)

SOI Technology : Materials, Devices, and Applications

7th - 10th APRIL 2010, Pyeongsan Academy, Daegu, KOREA

NANO KISS

KOREAN INTERNATIONAL SUMMER SCHOOL ON NANOELECTRONICS

The Korean International Summer School on Nanoelectronics is a new annual event, starting in 2010. Nano-KISS will offer every year a panel of detailed lectures on emerging fields in nano-micro-electronics, given by world-class experts. The first edition in 2010 is dedicated to advanced SOI concepts and technologies. It is a unique opportunity for senior and junior researchers to update their knowledge in the rapidly growing field of SOI components. Nano-KISS will bring together scientists from all over the world universities, R&D centers and companies. Nano-KISS is based on the successful model of MIGAS, the International Summer School on Microelectronics, organized for many years in Grenoble area. Nano-KISS is organized by Kyungpook National University (KNU) and Grenoble Institute of Technology (INPG) via World-Class University and Brain Korea 21 projects. Pyeongsan academy, located in the famous Palgong provincial park, is a very attractive place for combining top level lectures with scientific interactions and recreational activities.

Nano-KISS is especially designed for the benefit of PhD students, engineers and researchers from academic laboratories and semiconductor industry.

2010 Scientific Program

- **Introduction to SOI devices and applications**
  - Why SOI? – Prof. J-P. Colinge (Tyndall, Ireland)
  - Benefit for processors, low-power CMOS, RF, power, and high temperature applications – Prof. J-P. Colinge (Tyndall, Ireland)
  - SOI Device Zoo – Prof. J-P. Colinge (Tyndall, Ireland)
  - Technology Modules for SOI – Dr. D. W. Kim (Samsung, Korea)
- **SOI Materials**
  - Standard Smart-Cut and beyond (ETSOI, GeOI, alter BOX, etc) – Dr. Carlos Mazure(CTO SOITEC)
- **Physics of SOI transistors**
  - Mechanisms in partially depleted, fully depleted, and multiple-gate MOSFETs – Dr. T. Ernst (LETI, France)
  - Advanced modeling and simulation – Dr. T. Ernst (LETI, France)
- **Electrical characterization and reliability**
  - Characterization techniques for SOI materials and transistors – Prof. Sorin Cristoloveanu (INPG & KNU)
  - Reliability and variability issues – Prof. R. Schrimpf (Vanderbilt Univ, USA)
- **Designing SOI circuits**
  - Circuit design for SOI – Dr. R. Ferrant (France)
- **From Micro to Nano**
  - Ultimate CMOS scaling and More-than-Moore devices – Prof. Alex Zaslavsky (Brown Univ, USA)
- **Applications**
  - MEMS, NEMS, sensors – Prof. S. H. Kong (KNU, Korea)
  - SOI floating-body memories – Dr. S. W. Chung (Hynix, Korea)

Organizing Committee

- Prof. Sorin Cristoloveanu (INPG & KNU), chair
- Prof. Jung-Hee Lee (KNU), co-chair
- Prof. Jong-Hyun Lee (KNU)
- Prof. Jong-Ho Lee (SNU)
- Prof. Sung-Ho Kong (KNU)
- Prof. Young-Ho Bae (Uiduk Univ.)
- Prof. Laurent Montes (INPG)
- Dr. Kyoung-Il Na (INPG)
- Mr. Ki-Sik Im (KNU)

Registration date & fee

- **On-line** : January 1th – March 31th, 2010
  http://nano-kiss.knu.ac.kr
- **On-Site** : April 6th – 7th
- **Registration fee**
  - Industry : 400,000 wons
  - Students : 200,000 wons

Contact

- **Ki-Sik IM (KNU)** : ksim@ee.knu.ac.kr
- **Kyoung-IL NA (INPG)** : nak@minatec.inpg.fr

Korean International Summer School on Nanoelectronics (Nano-KISS 2010)
SOI Technology: Materials, Devices, and Applications

Time	Wednesday 07-04-2010	Thursday 08-04-2010	Friday 09-04-2010	Saturday 10-04-2010
7:00	Registration	Breakfast	Breakfast	Breakfast
8:00				
8:30				
9:00		Mechanisms in partially depleted, fully depleted, and multiple-gate MOSFETs Dr. T. Ernst (LETI, FRANCE)	Circuit design for SOI Dr. R. Ferrant (FRANCE)	MEMS, NEMS, sensors Prof. S. H. Kong (KNU, KOREA)
9:30	Why SOI? Prof. J. P. Colinge (Tyndall, IRELAND)			
10:00				
10:30		coffee break	coffee break	coffee break
11:00	coffee break	Ultimate CMOS scaling and More-than-Moore devices Prof. Alex Zaslavsky (Brown Univ, USA)	Advanced modeling and simulation Dr. T. Ernst (LETI, FRANCE)	SOI floating-body memories Dr. S. W. Chung (Hynix, KOREA)
11:30	SOI zoo Prof. J. P. Colinge (Tyndall, IRELAND)			
12:00				
12:30	Lunch & interactions	Lunch & interactions	Lunch & interactions	Lunch & interactions
13:00				
13:30				
14:00				
14:30				
15:00				
15:30	Technolo for • TOP Dr. D. … …. (Samsung, KOREA)	Characterization techniques for SOI materials and transistors Prof. Sorin Cristoloveanu (IMEP & KNU, FRANCE)	Social program	
16:00				
16:30	coffee break	coffee break		
17:00	Standard Smart-Cut and beyond (ETSOI, GEOL, alter BOX, etc) Dr. Carlos Mazurë (CTO SOITEC)	Reliability issues Prof. R. Schrimpf (Vanderbilt Univ, USA)		
17:30				
18:00			Rump session	
18:30		Dinner		
19:00	Welcome reception		Conference Dinner	
19:30				
20:00				
20:30				

C. **International SemOI Workshop "Nanoscaled Semiconductor-on-Insulator Materials, Sensors and Devices"** 26-30 April, 2010, Kyiv, Ukraine

The goal of this workshop is to debate about the recent developments in nanometer down scaled Semiconductor-on-Insulator (SemOI) systems which are basis blocks for modern high-sensitive sensors in a wide range of applications such as telecommunications, radiation control, biomedical instrumentation, chemical analysis, etc. SemOI is foreseen as a key technology for the integration of high quality and resistant nanoscaled devices and integrated circuits that must operate in harsh environment.

The topics to be covered include:

- Semiconductor-on-Insulator material technology
- Nanoscale CMOS devices and circuits
- New SemOI materials and nanoscaled devices on its basis
- SemOI sensors and new SemOI systems
- Diagnostic techniques for nanoscale SemOI materials and devices
- Technology and economics

Keynote speakers:

V.P.Bondarenko (BSUIR, Belarus); M.Bawedin (Univ. of Cambridge, UK); C.Colinge (California State Univ., USA); J.P.Colinge (Tyndall NI, Ireland); D.Flandre (UCL, Belgium); G.Gamble (Queen's Univ., Belfast, UK), F.Gamiz (Granada Univ., Spain); N. Horiguchi (IMEC, Leuven, Belgium); S. Ingebrandt (Univ. Appl. Sci. Kaizerslautern, Germany); D. Leadley (Univ. of Warwick, UK), N.Lukyanchykova (ISP NASU, Ukraine), J.Martino (Univ. of Sao Paulo, Brazil), B.B.Majkusiak (WUT, Warsaw, Poland), A.A.Orlikovsky (IPT RAS, Russia), V.Popov (ISP RAS, Novosibirsk, Russia); J.P.Raskin (UCL, LLN, Belgium), S.Roy (Univ. of Glasgow, UK), U.Schwalke (TU Darmstadt, Germany)

PROGRAMME

of the 6st SemOI WORKSHOP & 1st Ukrainian-French SOI Seminar

1st day (Monday, April 26)
a.m.

9^{00} Opening ceremony

Ukrainian-French Seminar

9^{30} **(Invited) Silicon-based devices and materials for nanoscale FETs**

Francis Balestra

MINATEC, SINANO, France

10^{00} **(Invited) Selected SOI puzzles and tentative answers**

K-I. Na,[1] W. Van Den Daele,[1] L. Pham-Nguyen,[1] M. Bawedin,[1] K-H. Park,[1] J. Wan,[1] K. Tachi,[1,2] S-J. Chang,[1] I. Ionica,[1] Y-H. Bae,[1,3] J.A. Chroboczek,[1] C. Fenouillet-Beranger,[2,4]T. Ernst,[2] E. Augendre,[2] C. Le Royer,[2] A. Zaslavsky,[1,5] H. Iwai,[6] **S. Cristoloveanu**[1]

[1]*IMEP-LAHC, Grenoble INP Minatec, France*
[2]*CEA-LETI, Minatec, France*
[3]*Uiduk University, Gangdong, Gyeogju, Korea*
[4]*STMicroelectronics, Crolles Cedex, France*
[5]*Division of Engineering, Brown University, Providence, USA*
[6]*Frontier Research Center, Tokyo Institute of Technology, Yokohama, Japan*

10^{30} **(Invited) From ultra thin silicon SOI to FDSOI devices**

Carlos Mazuré, Bich-Yen Nguyen, Walter Schwarzenbach, Daniel Delpra, Konstantin Bourdelle

SOITEC, Bernin, France

11^{00} Coffee break

Ukrainian-French Seminar

11^{30} **(Invited) Ultrathin body SOI transistors for 22 nm technology node and beyond**
T. Poiroux, F. Andrieu, O. Weber, C. Fenouillet-Béranger, C. Buj-Dufournet, P. Perreau, L. Tosti, L. Brevard and O. Faynot
CEA-LETI, MINATEC, France

12^{00} **(Invited) Special Features of the Back-Gate Effects in UTB SOI MOSFETs**

T.E.Rudenko[1]**,** V. Kilchytska[2], J.-P. Raskin[2], F. Andrieu[3], O. Faynot[3],Y. Le Tiec[3], K. Landry[4], A. Nazarov[1], and D. Flandre[2]
[1] *Institute of Semiconductor Physics, NAS of Ukraine, Kyiv, Ukraine*
[2] *Université catholique de Louvain, Louvain-la-Neuve, Belgium*
[3] *CEA-LETI MINATEC, Grenoble, France*
[4] *SOITEC, Bernin, France*

12^{30} **(Invited) Amorphous silicon-carbon alloy films on SOI as a functional material for MEMS technologies**
A.V. Vasin[1], A. V. Rusavsky[1], V. S. Lysenko[1], A. N. Nazarov[1], Yu. Ishikawa[2], Sh. Muto[3], T. Kimura[3], N. André[4] and J.-P.Raskin[4]
[1]*Institute of Semiconductor Physics, NAS of Ukraine, Kyiv, Ukraine*
[2]*Japan Fine Ceramics Center, Nagoya, Japan*
[3]*Department of Materials, Physics and Energy Engineering, Nagoya University, Japan*

13^{00} Lunch

p.m.
SemOI WORKSHOP
SOI Material and Devices Technologies

14^{30} **(Invited) High Resistivity SOI wafer: the substrate for RF SoC applications?**
Jean-Pierre Raskin
Université catholique de Louvain, Microwave Laboratory, Louvain-la-Neuve, Belgium

15^{00} **(Invited) GeOI Technology**

H.S. Gamble, P.T. Baine, Y.W. Low, Y.H. Low, P.V. Rainey , R. Hurley, J.H. Montgomery, B.M. Armstrong, D.W. McNeill, S.J.N. Mitchell (Queen's University Belfast, N. Ireland)

School of Electronics, Electrical Engineering and Computer Science, Queen's University Belfast, N. Ireland

15^{30} **(Invited) ZnO films and nanocrystalls on bulk silicon and SOI wafers: formation, properties and applications**

E. Chubenko[1], M. Balucani[2], A. Belous[3], V. Malyshev[3], **V. Bondarenko[1]**
[1]*Belarusian State University of Informatics and Radioelectronics, Minsk, Belarus*
[2]*University of Rome "La Sapienza", Rome, Italy*

[3]*Research and Development Centre "Belmicrosystems", Integral Corporation, Minsk, Belarus*

16^{00} Coffee break

SOI Material and Devices Technologies

16^{30} **(Invited) Low temperature fabrication of germanium-on-insulator (GeOI) structure using remote plasma activation and hydrogen exfoliation**

Cindy Colinge[1], Ki Yeol Byun[1], Isabelle Ferain[1], Mark Goorsky[2]
[1]*Tyndall National Institute, University College Cork, Cork, Ireland*

[2]*Department of Material Science and Engineering, UCLA, USA*

17^{00} **The investigation on the interface characteristics of GeOI manufactured by low temperature wafer bonding**
Xuan Xong Zhang[1,2], Tian Chun Ye[1], Songlin Zhuang[2], Jiwei, Jiao[3]
[1]*Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China*
[2]*Shanghai Key Laboratory of Modern Optical System University of Shanghai for Science and Technology Shanghai, China*

[3]*Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences Shanghai, China*

17^{20} **(Invited) Fabrication and characterization of strained semiconductor materials on dielectric platforms D. Leadley**

University of Warwick, UK

17^{50} **SOI structures with nitrided buried SiO_2 layer: formation and properties**

I.E. Tyschenko, V. P. Popov
Institute of Semiconductor Physics, Novosibirsk, Russia

2nd day (Tuesday, April 27)
a.m.
Ukrainian-French Seminar

9^{00} **(Invited) Ohmic and Schottky contact CNTFET: transport properties and device performance using semi-classical and quantum particle simulation**
Philippe Dollfus, Huu-Nha Nguyen, Damien Querlioz, Arnaud Bournel and Sylvie Retailleau
Institut d'Electronique Fondamentale, CNRS, Université Paris-Sud, Orsay, France

9^{30} **(Invited) Confined and guided VLS growth of silicon nanoribbons: from nanowires to SOI-like layers**

A. Lecestre, **E. Dubois**, A. Villaret, T. Skotnicki, P. Coronel, G. Patriarche, C. Maurice

IEMN – UMR CNRS, Villeneuve d'Ascq, France

10^{00} **(Invited) Gold assisted growth of silicon nanowires**

A.I. Klimovskaya, P.M. Lytvyn, Yu. N. Pedchenko, A.T. Voroschenko, O.C. Oberemok, A.V. Sarikov, O.A. Stadnik, Yu.M. Litvin, I.V. Prokopenko

Lashkaryov Institute of Semiconductor Physics, NAS of Ukraine, Kyiv, Ukraine

10^{30} Coffee break

Ukrainian-French Seminar

11^{00} **(Invited) Engineering pseudosubstrates with porous silicon technology**

A. Boucherif, N. Blanchard, Ph. Regreny, A. Danescu, H. Magoarie, O. Marty, J. Penuelas, J-M Bluet, G. Guillot, V. Lysenko, and **G. Grenet**

Lyon Institute of Nanotechnologies, CNRS UMR, Université de Lyon, France

11^{30} **(Invited) Photo-electrical properties of SiGe quantum dots on SiO_X**

Yu.N. Kozyrev[1], N.T. Kartel[1], M.Yu. Rubezhanska[1], S.V. Kondratenko[2], Ye.Ye. Melnichuk[2], C. Teichert[3], V.S. Lysenko[4], Yu.V. Gomeniuk[4]

[1]Institute of Surface Chemistry, NAS of Ukraine, Kyiv, Ukraine
[2]National Taras Shevchenko University, Kiev, Ukraine
[3]Institute of Physics, Montanuniversitaet Leoben, Leoben, Austria

[4]Institute of Semiconductor Physics, Kiev, Ukraine

12^{00} **(Invited) Multilayers porous silicon – silicon structures for sensors and solar cells**

V.A. Skryshevsky, I.I.Ivanov

Institute of High Technology, Taras Shevchenko National University, Kiev, Ukraine

12^{30} **(Invited) 3D quantum simulation of elastic and inelastic scattering in Silicon nanowire FETs**

Marco Pala

IMEP-LAHC, INP Grenoble, Grenoble, France

13^{00} Lunch

p.m.
SemOI WORKSHOP
Physics & Technology of New SOI devices

14^{30} **(Invited) Junctionless transistors: physics and properties**

J.P. Colinge, C.W. Lee, N. Dehdashti Akhavan, R. Yan, I. Ferain, P. Razavi, A. Kranti, R. Yu

Tyndall National Institute, University College Cork, Cork, Republic of Ireland

15^{00} **(Invited) Floating body effects for SOI memories**

M. Bawedin[1], K-H. Park[1], K-Y. Na[1], Y-H. Bae[1,2] and S. Cristoloveanu[1]

[1]IMEP-LAHC, Grenoble INP Minatec, France

[2]Uiduk University, Gangdong, Gyeogju, Korea

15^{30} **(Invited) FinFETS and their futures**

N. Horiguchi[1], B. Parvais[1], T. Chiarella[1], N. Collaert[1], A. Veloso[1], R. Rooyackers[1], P. Verheyen[1], L. Witters[1], A. Redolfi[1], A. De Keersgieter[1], S. Brus[1], G. Zschaetzscha[1,2], M.

Erckena[1], E.Altamirano[1], S. Locorotondo[1], M. Demand[1], M. Jurczak[1], W. Vandervors[1,2], T. Hoffmann[1], and S. Biesemans[1]
[1]*IMEC, Leuven, Belgium*
[2]*Instituut voor Kern- en Stralingsfysica, K.U. Leuven, Leuven, Belgium*

16^{00} **Towards SemOI-based quantum computers**

S. Filippov[1] and **V. Vyurkov**[2]

[1]*Moscow Institute of Physics and Technology (State University), Russia*

[2]*Institute of Physics and Technology of the RAS, Moscow, Russia*

16^{20} Coffee break

Physics&Theory of New SOI devices

16^{50} **(Invited) Ultrathin single-gate and multiple-gate n-channel and p-channel SOI MOSFETs**

F.Gámiz, L.Donetti, C.Sampedro, A.Godoy, N.Rodriguez, F.Jimenez-Molinos

Nanoelectronics Research Group, Departamento de Electrónica, Universidad de Granada, Spain

17^{20} **(Invited) Quantum simulation of an FD ETSOI FET**

A. Orlikovsky, V. Vyurkov, and I. Semenikhin

Institute of Physics and Technology of the Russian Academy of Sciences, Moscow, Russia

17^{50} **(Invited) Some issues of modelling the double barrier metal-oxide-semiconductor tunnel structure**

B. Majkusiak and A. Mazurak

Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, Warsaw, Poland

18^{20} Break

19^{00} Poster Session & Buffet

3rd day (Wednesday, April 28)
a.m.

Ukrainian-French Seminar

9^{00} **(Invited) Single dopant and single electron effects in CMOS devices**

M. Sanquer

CEA-Grenoble, France

9^{30} **(Invited) Mobility characterization in advanced FD-SOI CMOS devices**

G. Ghibaudo

IMEP-LAHC, MINATEC, Grenoble, France

10^{00} **(Invited) Gate control of junction impact ionization avalanche in SOI MISFETs: theoretical model**

V. Dobrovolsky[1], **F. Sizov[1],** S. Cristoloveanu[2]
[1]*Institute of Semiconductor Physics, Kiev, Ukraine*

[2]*IMEP, ENSERG, Grenoble, France*

10^{30} Coffee break

SemOI WORKSHOP

Operation of Novel SOI devices

11^{00} **(Invited) Influence of atomic fluctuation on operation nanoscaled devices**
S. Roy
Univ. Of Glasgow, UK

11^{30} **(Invited) Investigation of tri-gate FinFETs by noise methods**
N. Lukyanchikova[1], N. Garbar[1], V. Kudina[1], A. Smolanka[1], E. Simoen[2] and C. Claeys[2,3]
[1]*V. Lashkaryov Institute of Semiconductor Physics, Kiev, Ukraine*
[2]*Interuniversity Microelectronics Centre, Leuven, Belgium*
[3]*Catholic University of Leuven, Leuven, Belgium*

12^{00} **(Invited) SOI MOSFET transconductance behavior from micro to nano era**
J.A. Martino[1], P. G. D. Agopian[1], E. Simoen[2] and C.Claeys[2]
[1]*LSI/PSI/USP - University of Sao Paulo, Brazil*
[2]*IMEC, Leuven, Belgium*

12^{30} **Hydrogen gettering in processed oxygen-implanted silicon**
A. Misiuk[1], A. Barcz[1,2], A. Ulyashin[3] and J. Bak-Misiuk[2]
[1]*Institute of Electron Technology, Warsaw, Poland*
[2]*Institute of Physics, Warsaw, Poland*
[3]*SINTEF, Oslo, Norway*

13^{00} Lunch

p.m.

14^{00} Excursion

18^{00} Banquet

4th day (Thursday, April 29)
a.m.

SemOI WORKSHOP
SOI Sensors and MEMS

9^{00} **(Invited) Top-down processed SOI nanowire devices for biomedical applications**
S. Ingebrandt[1], X.T. Vu[1,2], J.F. Eschermann[1,2], R. Stockmann[2], A. Offenhäusse[2]
[1]*Department of Informatics and Microsystem Technology, University of Applied Sciences Kaiserslautern, Germany*
[2]*Institute of Bio- and Nanosystems, Forschungszentrum Jülich, Germany*

9^{30} **(Invited) Universal sensing platform of SOI nanowire transistor matrix for femtomole electronic bio and chemical sensors**
V.P. Popov[1], O.V. Naumova[1], Yu.D. Ivanov[2]
[1]*Institute of Semiconductor Physics, Novosibirsk, Russia*
[2]*Institute of Biomedical Chemistry, Moscow, Russia*

10^{00} **(Invited) Conceptual foundations of engineering and technology design for SOI microelectromechanical sensors with an integral monolithic tensoframe**
Leonid V. Sokolov

Federal State Unitary Enterprise Institute of Aircraft Equipment, Russia

10^{30} **Non-standard FinFET devices for small volume sample sensors**

Michał Zaborowski[1], **Daniel Tomaszewski[1]**, Lidia Łukasiak[2], Andrzej Jakubowski[1]

[1]*Institute of Electron Technology, Warsaw, Poland*

[2]*Warsaw University of Technology, Warsaw, Poland*

10^{50} Coffee break

Novel SOI devices

11^{20} **(Invited) Carbon: the future of silicon nanoelectronics?**

Udo Schwalke

Institute for Semiconductor Technology and Nanoelectronics Technische Universität Darmstadt, Darmstadt, Germany

11^{50} **(Invited) Variable barrier resonant tunneling transistor: performance investigation of a steep slope, high on-current device**

Aryan Afzalian[1], Jean-Pierre Colinge[2] and Denis Flandre[1]

[1]*Laboratoire de Microélectronique, Université Catholique de Louvain, Louvain-La-Neuve, Belgium*

[2]*Tyndall National Institute, University College Cork, Ireland*

12^{30} **(Invited) Effects of high–energy neutrons on advanced SOI MOSFETs**

V. Kilchytska, J. Alvarado, O. Militaru, G. Berger, D. Flandre

Microelectronics Laboratory, Nuclear Physics Laboratory and Centre de Recherches du Cyclotron, Université catholique de Louvain, Louvain-la-Neuve, Belgium

13^{00} Lunch

p.m.

14^{00} Excursion with visiting of Institutes of National Academy of Sciences

Posters

1. **Silicon-on-insulator flicker-noise gas sensor**
   M.I. Makoviychuk
   Yaroslavl Branch of the Institute of Physics and Technology of RAS, Yaroslavl, Russia

2. **Ion-beam synthesis of two-dimensional photonic crystals in silicon-on-insulator structures**
   M.Yu. Barabanenkov[1], A.F. Vyatkin[1], A.I. Il'in[1], V.I. Zinenko[1], G.E. Daviduk[2], G.L. Myronchuk[2]
   [1]*Institute of Microelectronics Technology and superpure materials, Russian Academy of Sciences, Chernogolovka, Russia*
   [2]*Lesya Ukrayinka Volyn' National University, Lutsk, Ukraine*

3. **Influence hydrogen plasma treatment on a-SiC resistivity of the SiC/SiO_2/Si structures**
   S. Gordienko[1], A. Nazarov[1], A. Rusavsky[1], A. Vasin[1], N. Rymarenko[1], V. Stepanov[1], T. Nazarova[2], V.P. Bondarenko[3], K.I. Kholostov[3], E.B. Chubenko[3]
   [1]*Lashkaryov Institute of Semiconductor Physics, NASU, Kyiv, Ukraine*
   [2]*National Technical University of Ukraine "KPI", Kyiv, Ukraine*
   [3]*Belarusian State University of Informatics and Radioelectronics, Minsk, Belarus*

4. **Semi-analytical models of field-effect transistors with low-dimensional channels**
   A. Khomyakov and V. Vyurkov
   Institute of Physics and Technology, Russian Academy of Sciences, Moscow, Russia

5. **Research and development of technological processes of SOI for MEMS elements**
   S.P. Timoshenkov[1], V.V. Kalugin[1], L.V. Sokolov[2], **N.M. Parfenov**[2]
   [1]*Moscow Institute of Electronics Engineering (Technical University), Moscow, Russia*
   [2]*Moscow Aviation Institute (Technical University), Moscow, Russia Moscow Institute of Electronics*

6. **Diamond – graphite heterostructures formed by nitrogen and hydrogen implantation and annealing**
   V. P. Popov, L.N. Safronov, **O.V. Naumova**, Yu.N. Palyanov[2], I.N. Kupriyanov[2]
   [1]*Institute of Semiconductor Physics, Novosibirsk, Russia*
   [2]*Institute of Geology and Mineralogy, Novosibirsk, Russia*

7. **SOI heterostructures crystallographic features research**
   K.L.Enisherlova, A.V.Lutzau, E.M.Temper, V.G.Gorjachev
   Federal state unitary enterprise Science & Production enterprise "Pulsar", Moscow, Russia

8. **Investigation electrical parameters of SOS-structures with 0,3 μ silicon layer**
   K.L. Enisherlova[1], V.G.Gorjachev[1], E. L. Shobolov[2], V.A.Gerasimov[2]
   [1]*Federal state unitary enterprise "Science & Production enterprise Pulsar", Moskow, Russia*
   [2]*Federal State Unitary Enterprise "Federal Research-and-Production Centre Measuring Systems Research Institute named after Yu.Ye.Sedakov", Nizhny Novgorod, Russian*

9. **High temperature effect on harmonic distortions in submicron graded-channel MOSFETs**
   M. Emam[1], M. A. Pavanello[2], F. Danneville[3], D. Vanhoenacker-Janvier[1] and J.-P. Raskin[1]
   [1]*Institute of Information and Communication Technologies, Electronics and Applied Mathematics,*
   Université catholique de Louvain, Louvain-la-Neuve, Belgium
   [2]*Department of Electrical Engineering, Centro Universitário da FEI, São Bernardo do Campo, Brazi.*
   [3]*Institut d'Electronique de Microélectronique et de Nanotechnologie (IEMN), Villeneuve d'Ascq Cedex, France*

10. **Model of nonuniform channel for the charge carrier transport in nanoscale FETs**
    V. P. Popov, **M. A. Ilnitsky**
    Institute of Semiconductor Physics, Novosibirsk, Russia

11. **Double-gate voltage programmable silicon-nanowire-FETs**
F. Wessely, T. Krauss, U. Schwalke
Institute for Semiconductor Technology and Nanoelectronics, Darmstadt University of Technology, Darmstadt, Germany

12. **Fabrication process for applying high mechanical stress on monocrystalline silicon film**
Vikram Passi[1], Umesh Bhaskar[1], Thomas Pardoen[2], Jean-Pierre Raskin[1]
[1]*Institute of Information and Communication Technologies, Electronics and Applied Mathematics, Université catholique de Louvain, Louvain-la-Neuve, Belgium*
[2]*Institute of Mechanics, Materials and Civil Engineering, Université catholique de Louvain, Louvain-la-Neuve, Belgium*

13. **Polysilicon on insulator structures for sensors application at harsh conditions**
A.A.Druzinin[1,2], I.T.Kogut[3], Yu.M.Khoverko[1,2]
[1]***Lviv National Polytechnical University, SRC "Crystal"***
[2]*International Laboratory of High Magnetic Fields and Low Temperatures, Wroclaw, Poland*
[3]*Precarpathian university named after V. Stephanyk, Iv-Frankivsk Lviv National Polytechnical University, Lviv, Ukraine*

14. **3D SOI elements for silicon-on-chip applications**
I. Kogut[1], A.A. Druzhinin[2], V. I. Golota[1]
[1]*Precarpathian National University, Ivano-Frankivsk, Ukraine*
[2]*National University "Lvivska Politechnika", Lviv, Ukraine*

15. **A model of the evolution of the Au/Si droplet ensembles during rapid thermal annealing at high temperatures**
A. Sarikov, A. Klimovskaya, O. Oberemok, O. Lytvyn, O. Stadnik
V. Lashkarev Institute of Semiconductor Physics NAS Ukraine, Kiev, Ukraine

16. **High-frequency CMOS integrated circuits for quartz oscillators, and analog switches of control on SOI structures**
L.I. Samotovka[1], T.M. Virozub[1], V.L. Samotovka[1], A.F. Voschinkin[1], V.I. Zolotarevsky[1], L.V. Kobzar[1], V.G. Verbitsky[1], A.N. Nazarov[2], V.S. Lysenko[2]
[1]*State Enterprise "Research Institute of Microdevices", Kiev, Ukraine*
[2]*V. Lashkarev Institute of Semiconductor Physics NAS Ukraine, Kiev, Ukraine*

17. **Electrical properties of high-k $LaLuO_3$ gate oxide for SOI MOSFETs**
Y.Y. Gomeniuk[1], Y.V. Gomeniuk[1], A.N. Nazarov[1], P. Hurley[2], C. Cherkaoui[2], S. Monaghan[2], P.-E. Hellström[3], O. Engström[4]
[1]*V. Lashkarev Institute of Semiconductor Physics NAS Ukraine, Kiev, Ukraine*
[2]*Tyndall NI, Cork, Ireland,*
[3]*KTH, Stockholm, Sweden*
[4]*Chalmers UT, Göteborg, Sweden*

18. **Formation of Si nanocrystals in thin insulator SiO_2 by ion-plasma sputtering**
A. Evtukh, V. Litovchenko, **O. Bratus**
V. Lashkarev Institute of Semiconductor Physics NAS Ukraine, Kiev, Ukraine

19. **SIMOX technology with ultra-thin oxide layer and Si nanocluster inclusions**
B. Romanyuk, V. Litovchenko, V. Melnik, V. Popov, O. Oberemok, V. Nikirin
V. Lashkarev Institute of Semiconductor Physics NAS Ukraine, Kiev, Ukraine

20. **Charge trapping and retention in nanocrystal Non Volatile Memory structures**
V.I. Turchanikov[1], V.A. Evtukh[2], **A.N. Nazarov**[1]
[1]*V. Lashkarev Institute of Semiconductor Physics NAS Ukraine, Kiev, Ukraine*
[2]*Taras Shevchenko National University of Kyiv, Radio Physics Department, Kiev, Ukraine*