INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

Grant Agreement nº 216373

D3.8 Summary report related to all the executed training activities within EUROSOI+ in the third reporting period (M26-M42)

Due date of deliverable: 30-06-2011
Actual submission date: 30-06-2011

Start date of project: 01-01-2008 Duration: 42 months

Project coordinator: Prof. Francisco Gámiz, UGR
Project coordinator organisation: University of Granada, Spain Rev.1

Project co-funded by the European Commission within the Seventh Framework Programme (FP7)		
Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

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1. Introduction

One of the main objectives pursued by the network is the organization of a wide range of training activities. In this framework, different short-courses have been and will be organized addressing the following topics: SOI materials – SOI device physics – SOI Circuits – SOI for niche applications.

These one-day-courses were held at the same time as two important European electronics events, ESSDERC-2010 (Seville, Spain, September 13-17, 2010) and EUROSOI-2011 (Granada, Spain, January 17-19, 2011).

Relevant speakers were invited and the participation of members of the SOI industrial community was encouraged. After each event, the opinion, comments and suggestions of the participants is collected through written inquiries. This feedback will be used by the Management Board to design next events.

Short Courses

A. Tutorial "Silicon on Insulator: Materials to Circuit Design " Seville, Spain, September 13th, 2010

This tutorial was organized by Prof.Jean-Pierre Colinge., from Tyndall Insitute, Cork, Ireland, on September 13th, 2010, as a satellite event of the 40th European Solid State Device Research Conference, with the intention of embemding the tutorial in a well-known very big event as ESSDERC, to widen the number and quality of potential attendants.
ESSDERC is Europe's premier forum for leading-edge research into electronic, and nanoelectronic devices and processes ESSDERC 2010 run parallel to his sister conference ESSCIRC 2010, covering all aspects of modern solid-state systems, circuits and devices at a single event. In combination these two conferences provide a unique forum where technologists, device experts, and circuit and system designers can interact. The 2010 conference was held in Seville, Spain, at the Barceló Renacimiento Hotel, on the Isla de la Cartuja, an island located between two branches of the Guadalquivir river. It run September 14-16, 2010, preceded by a full day of Short Courses and Tutorials on Monday, September 13. ESSDERC 2010 drew presentations and attendees from industry, academia, and governmental agencies worldwide. No other meeting in Europe presents as much leading work in so many different areas of microelectronics, encompassing both silicon and non-silicon device and process technology, molecular electronics, nanotechnology, optoelectronics and MEMS (microelectromechanical system) technology.

Professor Colinge organized a tutorial with a wide scope embracing from material issues to end-user applications:

Silicon on Insulator: Materials to Circuit Design

1. **Smart-cut enabled materials** Cindy Colinge (Tyndall)
2. **Physics of SOI devices**. Jean Pierre Colinge (Tyndall)
3. **SOI MOSFET compact models**. Benjamin Iñiguez (URV)
4. **SOI Design: RF**. Jean Pierre Raskin (UCL)
5. **Analog SOI CMOS devices : figures of merit, design techniques and applications**. Denis Flandre (UCL)
6. **SOI design: logic circuits**. Philippe. Flatresse (STM)

September 13th, 2010

Tutorial

Silicon on Insulator: Materials to Circuit Design

Organized by: JP Colinge, Tyndall Institute, Cork, Ireland

In collaboration with:

EUROSOI: Thematic Network on Silicon on Insulator Technology, Devices and Circuits

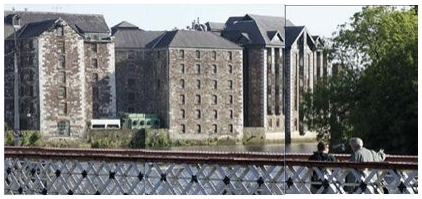
Lecture 1: Smart-cut® enabled materials

The simplicity and success of direct wafer bonding coupled with ex-foliation (Smart Cut®) has made it possible to transfer thin, single crystal materials to any substrate. An example of Smart Cut® is silicon on insulator (SOI) which is used for a variety of microelectronic applications. Furthermore, Smart Cut® enables the integration of exotic materials such as III-V semiconductors or Ge with any substrate. This lecture will discuss the basic Smart Cut® technique used for SOI and then describe other variations of Smart Cut® and their applications.

Instructor: Professor **Cindy Colinge** received her Bachelor of Science in Chemical Engineering 1983 from University of California, Davis, the Master of Science in Electrical and Electronic Engineering 1989 from California State University, Sacramento, and the Doctor of Philosophy in Electrical Engineering 1993 University of California, Davis working on bond and etch-back silicon on insulator. From August 1993 to 2009 she has held the position of Professor in the department of Electrical Engineering at California State University, Sacramento. She is currently at Tyndall National Institute in Cork, Ireland where she is studying interfacial properties of bonded heterostructures. Professor Colinge has written and presented over 50 articles on wafer bonding and has co-authored a textbook on "Physics of Semiconductor Devices. She is a Senior Member of IEEE since 2003 and a Member Electrochemical Society 1990. She has been and continues to be a member of the organizing committee for the Electrochemical Society's International Symposium on Semiconductor Wafer Bonding Science, Technology, and Application.

Smart-cut® Enabled Materials

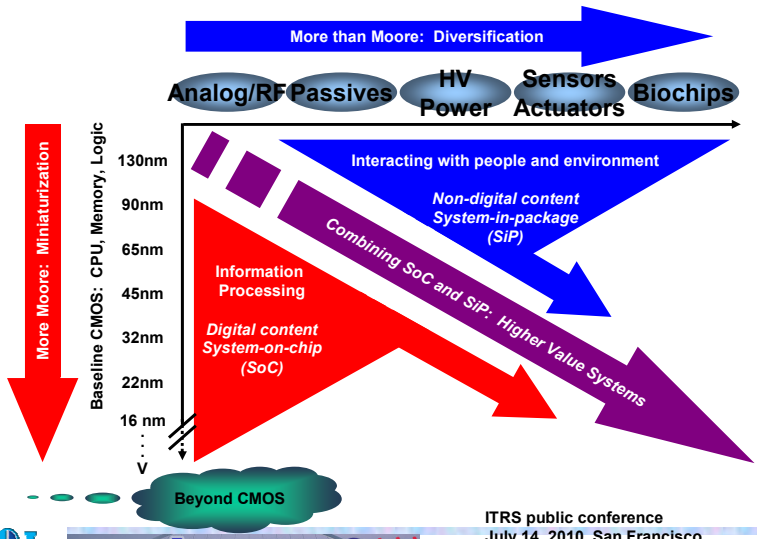
Tyndall National Institute
(formerly NMRC)



Cindy Colinge

Tyndall National Institute
Cork City
Ireland

International Technology Roadmap for Semiconductors (ITRS)



ITRS public conference
July 14, 2010, San Francisco

OUTLINE

SOI and Applications

- ➢Motivation for SOI
- ➢Fabrication of SOI
  - ➢Bonding and Hydrogen Exfoliation (Smart Cut®)
- ➢Ultrathin SOI
- ➢SOI for RF SOC
- ➢Outlook and Summary for SOI

New Materials and Applications

- ➢Ultimate CMOS Materials
- ➢Ge for Advanced CMOS
  - ➢Epitaxial Growth of Ge on Si vs. Bond and Exfoliation
  - ➢Challenges: Bonding Ge to Si and CTE Mismatch
  - ➢Other Applications: Photo Diodes
- ➢Examples of Smart Cut® for GaN and Applications
  - ➢Exfoliation Temperatures and Times
  - ➢GaN for LEDs, Power Devices, RF

Conclusion

Why SOI?

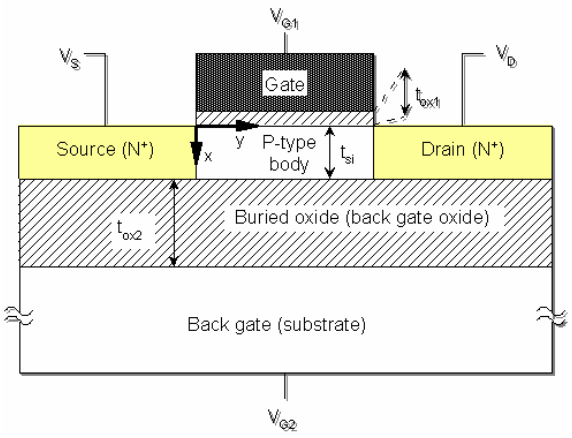
- Historical Motivation – radiation hardness
  - Small cross section for ionizing particles
- Past Motivation – enhanced performance
  - High speed and/or low power
- Present Motivation – extends device scaling beyond bulk Si
  - L_G scalability to 11 nm demonstrated
- Advantages of SOI CMOS
  - Low power, high speed, and/or lower V_{DD}: $P=I_{OFF}\ V_{DD} + \alpha\ f\ C\ V_{DD}^2$
  - Higher Packing Density
  - Crosstalk Reduction
  - Latchup Prevention
  - Soft Error Reduction

Lecture 2: Physics of the SOI transistor

This lecture will compare the physics of bulk MOSFETs, partially depleted SOI MOSFETs and fully depleted SOI MOSFETs. Emphasis is placed on the properties that make these devices interesting for particular applications. For instance, one can take advantage of PDSOI's floating-body effects to increase the speed of digital circuits. The superior linearity of FDSOI is excellent for analog applications, high-resistivity SOI wafers are well adapted to the fabrication of RF devices.

Instructor: Prof. **Jean-Pierre Colinge** received a BS degree in Philosophy, the Electrical Engineer degree, and the Ph.D. degree in Applied Sciences from the Université catholique de Louvain, Louvain-la-Neuve, Belgium, in 1980, 1980, and 1984, respectively. He worked at the Centre National d'Etudes des Télécommunications (CNET), Meylan, France, at the Hewlett-Packard Laboratories, Palo Alto, USA, at IMEC, Leuven, Belgium, where he was involved in SOI technology for VLSI and special device applications. From 1991 to 1997, Dr. Colinge was professor at the Université catholique de Louvain, leading a research team in the field of SOI technology for low-power, radiation-hard, high-temperature and RF applications as well as reduced dimension devices (thin double-gate and quantum-wire MOSFETs). He has published over 340 scientific papers and four books on the field of SOI as well as two books on semiconductor device physics. Prof. Colinge is currently Professor at the Tyndall National Institute, University College Cork, Ireland, where he is head of the Micro-Nano Electronics Centre and is conducting research on modelling, fabrication and characterization of advanced SOI MOS devices.

Physics of the SOI Transistor



JP Colinge

Tyndall National Institute
University College Cork
Cork, Ireland

Outline

1- Introduction

2- Bulk MOSFET *vs.* SOI MOSFET

3- SOI MOSFET fundamentals
- Types of SOI transistors
  - Partially depleted MOSFET
  - DTMOS/MTCMOS
  - Fully Depleted SOI

4- Unified body effect representation
- Simple and physics-based comparison of body effect between devices

5- Multi-gate FETs
- Short-channel effects
- Natural length

Lecture 3: Compact Modeling of the SOI MOSFET

The goal of this lecture is to present compact modeling techniques which have been applied for different types of thin film SOI and multiple-gate MOSFETs: Ultra-Thin Body SOI MOSFETs, Double-Gate MOSFETs, Gate All Around MOSFETs, Tri-Gate MOSFETs, and FinFETs. Long channel models areobtained by deriving a unified charge control model from the solution the 1-D Poisson's equation (considering volume inversion), and using an appropriate and self-consistent transport model. The final channel current, charge and capacitance models are written in terms of the charge sheet densities at the source and drain ends of the channel. The short-channel effects have to be incorporated to the compact models. Analytical and scalable models for the subthreshold swing, threshold voltage roll-off and DIBL have been developed by solving the 2-D or 3-D Poisson equation using a number of appropriate techniques. Quasi-static small-signal models, with analytical expressions for transconductances, conductances and capacitances, can be developed from the derived charge control model. Finally, using the active transmission line approach, the quasi-static compact models can be extended to the high frequency operation, in order to study the RF performance, including noise. Explicit expressions for the noise parameters can be developed.

Instructor: **Benjamin Iñíguez** received the B. S., the M. S. and the Ph. D. Degrees in physics from the University of the Balearic Islands (UIB), Spain, in1989, 1992 and 1996, respectively. His doctoral research focused on the development of CAD models for short-channel bulk-Si and SOI MOSFETs. From February 1997 to September 1998 he was working as a Postdoctoral Research Scientist at the ECSE Department, Rensselaer Polytechnic Institute (RPI), Troy, NY, in 1997-98, where he studied advanced devices, such as short-channel a-Si and poly-Si TFTs, GaN HFETs and heterodimensional MESFETs. From September 1998 to February 2001 hewas a Research Scientist (Postdoctoral Marie-Curie Grant Holder) in theMicroelectronics Laboratory, Université catholique de Louvain (UCL),Louvain-la-Neuve, Belgium, working on the characterization and modeling of thin-film and ultrathin-film SOI MOSFETs from DC to RF conditions. In February2001 he joined the Department of Electronic Engineering (DEEEA), UniversitatRovira i Virgili (URV), Tarragona, Spain, as Titular Professor. In 2004 he was awarded the Distinction of the Catalan Government for the Promotion of University Research. In 2007 he obtained the IET Premium Award for a paper about charge transport in organicTFTs. His current research interests are characterization and modeling of advanced electron devices, in particular nanoscale SOI and multiple-gate MOSFETs and organic and polymer TFTs. He is IEEE Senior Member from 2003, and IEEE EDS Distinguished Lecturer since 2004. In 2009 he obtained the ICREA Academia Prize. In 2010 he became Full Professor at the Universitat Rovirai Virgili (URV). HE has authored or co-authored more than 80 papers in international journals and a similar number in international conferences. He has participated in several European projects, and he is the leader of the "COMON" (Compact Modelling Network), an Industry Academia Partnership and Pathway funded by the 7th Framework Programme of the European Commission.

SOI MOSFET Compact Models

Benjamin Iñiguez

Universitat Rovira i Virgili
Tarragona
SPAIN

Goals

- Review of the main compact modeling issues in thin film SOI MOSFET modelling
- Review of the main compact modelling approaches in different types of thin film SOI MOSFET modelling
- Utilisation of models for technological and performance predictions

Outline

- Introduction
- General electrostatics
- Fully-Depleted (FD) SOI MOSFET
- Accumulation-Mode (AM) SOI MOSFETs
- Multi-Gate MOSFETs
- RF and noise modelling
- Conclusions

Introduction

- MOSFET scaling trend in near future will not be as straightforward as it has been in the past because fundamental material and process limits are imminent.
- In order to reach below the 32 nm technology node, implementation of advanced, non-classical MOSFETs with enhanced drive current and acceptable control of short channel effects are needed.
- Advanced thin-film SOI MOSFETs (e.g., single or multiple-gate MOSFETs) are very promising structures for the downscaling of MOSFETs below the 32 nm technological node.

Lecture 4: Analog SOI CMOS : devices figures of merit, design techniques and applications

Substrate insulation is responsible for SOI-specific MOS behaviour, whether advantageous (such as reduced body effect or capacitances) or detrimental such as static, dynamic and frequency-dependent floating-body effects or self heating. Their significant impacts on analog device properties and performance will be reviewed. The design and experimental results of low-power thin-film SOI CMOS analog blocks will be comprehensively presented and compared to bulk Si, targeting applications from micropower to very high-frequency, high-precision or high-temperature specifications and emphasizing SOI design tips and optimization opportunities. An Ultra-Low-Power (ULP) design technique will also be presented.

Instructor: **Denis Flandre** is Professor at Université catholique de Louvain (UCL), Louvain-la-Neuve, Belgium. Since 1986, he has been working on the modelling and characterization of SOI MOS devices and automated synthesis methodology for MOS analog circuits. He is now involved in R&D of SOI MOS devices, digital and analog circuits, as well as sensors and MEMS, for special applications (high-speed, low-voltage low-power, microwave, biomedical, rad-hard and high-temperature electronics and microsystems). He has co-authored more than 500 technical papers. He is co-inventor of 10 patents. He has organized or lectured many short courses on SOI technology, devices and circuits in universities, industries and conferences. He is director of the UCL Micro/nano-technology facility (Winfab.be), an executive of EU Networks of excellence (EUROSOI, HITEN (for High-Temperature Electronics), NANOSIL) and virtual institute (SINANO (on Silicon Nano-devices)), an IEEE Senior member, a member of the SOI Industry Consortium and a co-founder of CISSOID S.A., a spin-off company of UCL founded in 2000, focusing on SOI high-temperature IC solutions.

Analog SOI CMOS : devices figures of merit, design techniques and applications

Denis Flandre

UCL / ICTEAM
Louvain-la-Neuve
Belgium

Many thanks to :

Microelectronics / Microwaves Groups,
Research Center in Micro- and Nano-Scale
Materials and Electronics Devices (CeRMiN),
Université catholique de Louvain (UCL)
Louvain-la-Neuve, Belgium

Aryan Afzalian, Joaquin Alvarado, David Bol, Valeria Kilchytska,
Dimitri Lederer, Jean-Pierre Raskin and many others…

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& collaborations (B. Iniguez, M. Pavanello,
IMEC, STM, CEA-LETI, OKI, CISSOID…)

Table : Analog Mixed-Signal CMOS Technology Requirements						
Year of Production	*2010*	*2012*	*2014*	*2016*	*2018*	*2020*
Performance RF/Analog						
Supply voltage (V)	1,05	1,05	0,95	0,95	0,85	0,85
T_{ox} (nm)	1,2	1,2	1,10	1,10	1,00	0,90
Gate Length (nm)	38	29	22	17	14	12
g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$	**30**	**30**	**30**	**30**	**30**	**30**
1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	90	70	60		40	30
σ V_{th} matching ($mV \cdot \mu m$)					5	4
Precision Analog/RF Driver						
Supply voltage (V)	1,8	1,8	1,8		1,8	1,5
T_{ox} (nm)	3	3	3	3	3	2,6
Gate Length (nm)	180	180	180	180	180	130
g_m/g_{ds} at $10 \cdot L_{min\text{-}digital}$	**160**	**160**	**160**	**160**	**160**	**110**
1/f Noise ($\mu V^2 \cdot \mu m^2/Hz$)	360	360	360	360	360	270
σ V_{th} matching ($mV \cdot \mu m$)	6	6	6	6	6	5
Availability of optional analog / High-voltage FETs	limited	common	wide	wide	wide	wide
				switch to UTB FD or DG device		

Performances ?

Based on LSTP devices roadmap (for lower standby power and higher bias voltages than high performance (HP) or low operating power (LOP) CMOS) … but (analog / RF) devices into production 1 year later than LSTP digital (development of high-frequency models & other tools for RF and AMS design... LSTP logic gate length lags that of HP by ~2 years

OUTLINE

1. Amplifiers

   ("MOS transimpedance in saturation")

   - Figures of merit (Bulk vs FD illustration)
   - Design methods and performances
   - SOI specificities : PD, FD, UTB, FinFET

2. Non-Linear analog circuits :

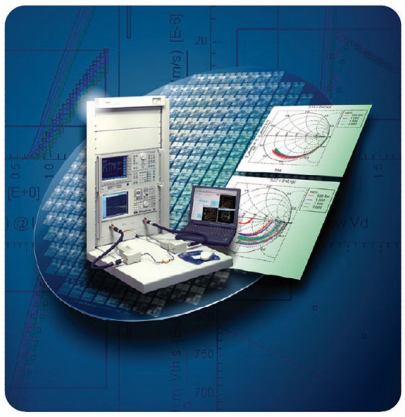
   ("MOS Id-Vd in large signal")

   - Switches / Diodes
   - ULP disruptive design

Lecture 5: SOI technology: an opportunity for RF designers?

Modern communication systems are very demanding; high frequency, high degree of integration, low power consumption, and they have to present good performance even under harsh environment. The integrability and power consumption reduction of the digital part will further improve with the continued downscaling of technologies. The bottleneck for further advancement is the analog front-end.
This last decade Silicon-on-Insulator (SOI) MOSFET technology has demonstrated its potentialities for high frequency reaching cut-off frequencies close to 500 GHz for nMOSFETs and for harsh environments (high temperature, radiations) commercial applications. Partially Depleted SOI is now massively serving the 45-nm digital market where it is seen as a low cost - low power alternative to bulk silicon. Fully depleted devices are also widely spread as they outperform existing semiconductor technologies for extremely low power analog applications.
For RF and systems-on-chip applications, SOI also presents the major advantage of providing high resistivity substrate capabilities, leading to substantially reduced substrate losses. Substrate resistivity values higher than 1 kO.cm can easily be achieved and High Resistivity Silicon is commonly foreseen as a promising substrate for radio frequency integrated circuits (RFIC) and mixed signal applications. Based on several experimental and simulation results the interest, limitations but also possible future improvements of the SOI MOS technology for RF applications are presented.

Instructor: **Jean-Pierre Raskin** received the Industrial Engineer degree from the Institut Supérieur Industriel d'Arlon, Belgium, in 1993, and the M.S. and Ph.D. degrees in Applied Sciences from the Université catholique de Louvain (UCL), Louvain-la-Neuve, Belgium, in 1994 and 1997, respectively. In 1998, he joined the EECS Department of The University of Michigan, Ann Arbor, USA. In 2000, he joined the Microwave Laboratory of UCL, Louvain-la-Neuve, Belgium, as Associate Professor. Since 2007, he has been a Full Professor and Head of the Microwave Laboratory of UCL. He was visiting professor at The University of Newcastle, Newcastle Upon Tyne, UK, for one year from September 2009. His research interests are the modeling, wideband characterization and fabrication of advanced SOI MOSFETs, micro and nanofabrication of MEMS/NEMS sensors and actuators as well as the characterization of intrinsic properties of materials at nanoscale. He is an IEEE Senior Member, EuMA Associate Member and Member of the Research Center in Micro and Nanoscopic Materials and Electronic Devices of the Université catholique de Louvain. He has published more than 150 articles in international journals and over 300 articles in conference proceedings.



SOI technology: an opportunity for RF designers?

Prof. Jean-Pierre Raskin

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Microwave Laboratory
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jean-pierre.raskin@uclouvain.be

Outline

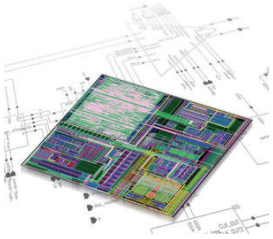
- State-of-the-art of RF **CMOS performance**
- **Limiting factors** for active and passive devices in Silicon technologies
- **Diversity of SOI technologies** (PD, FD, strained SOI, SON, MuG)
- **High Resistivity SOI** substrates: a key substrate for RF applications
  - Transmission lines
  - Crosstalk in mixed-mode ICs
  - Optical RF switches
  - Non-linearities for high power Si ICs
- Conclusions

Lecture 6: SOI design for low-power applications

The trade-off between performance and power consumption is the major challenge on the horizon for scaling of CMOS ICs. SOI technology offers solutions to this challenge and is receiving today strong interest from the semiconductor industry. However, the lack of design knowledge and IP libraries lead the list of missing pieces for a wide SOI adoption.
The lecture intends to show that a SOI digital design platform dedicated to low power applications can be derived from its bulk counterpart at a low cost design effort. The efficiency of such approach will be demonstrated on standard cells, SRAM, IO libraries and low power solutions ... Comparisons between SOI and BULK based on silicon measurements and circuit simulations will be presented, showing the advantages of SOI in the low power arena.

Instructor: **Philippe Flatresse** received the PhD degree in Microlectronics from the Institut National Polytechnique de Grenoble in 1999. During his thesis, he developed LETISOI spice model dedicated to partially depleted SOI circuits at CEA-LETI, the R&D laboratory from French Atomic Energy Commission, located in Grenoble. In year 2000, he joined STMicroelectronics Central R&D, Crolles, where is currently in charge of CMOS Design Platforms qualification and digital SOI design in Central CAD and Design Solutions department. Dr. Flatresse has coauthored more than 40 papers and filed 10 patents in advanced CMOS technologies.

Partially Depleted SOI Design for Low-Power Applications



Philippe Flatresse
Design for Qualification
Central CAD & Design Solutions
STMicrolectronics, Crolles, France

OUTLINE

- PD-SOI transistor optimization for LP Applications
- PD-SOI Design Platform
  - Standard cells Libraries
  - SRAM
  - ESD & IOs
- Leakage Power Management in PD-SOI
- Conclusion

B. Short course Granada-2011 EUROSOI Workshop

A fourth short course was organized by Prof. Francisco Gamiz (UGR) during 2011 EUROSOI Workshop held in Granada in January, 2011. Nanoelectronics has to provide smart solutions in the following years in several social domains (Health, security, transportation). These solutions mean higher performance at lower power consumption, and not only computational power and large data storage, but also interactivity with the environment. Silicon-on-Insulator technology is a perfect candidate to be used in the fabrication of these sytems.

Because of this, 2011 EUROSOI Short Course was focused on the opportunities offered by SOI technology to improve the performance of analog and digital applications, according to the following programme:

Silicon on Insulator technologies for future electronics
January 17th, 2011, Granada, Spain)

1. **SOI solutions for next technological nodes**
   Prof. Sigfried Mantl, FZJülich, Germany
2. **ETSOI Technology**
   Dr. Bruce Doris, IBM, USA
3. **CMOS---SOI---MEMS Imagers**
   Prof. Yael Nemirovsky, Technion, Israel
4. **SOI Low-power applications**
   Dr. N. Sugii, LEAP, Japan
5. **Memories on SOI**
   Dr.Malgorzata Jurczak, IMEC, Belgium
6. **SOI Photonics**
   Dr. Jean Marc Fedeli, LETI, France

Granada's Short Course was attended by more than 100 people (most of them students from EU) from Universities and European Semiconductor Industries

Silicon-on-Insulator technologies for future electronics

Francisco Gamiz

Granada, January 17th, 2011

Silicon-on-Insulator technologies for future electronics

1. **SOI solutions for next technological nodes**
   Prof. Sigfried Mantl, FZJülich, Germany
2. **ETSOI Technology**
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EurSOI

JARA Jülich Aachen Research Alliance

GEFÖRDERT VOM

Bundesministerium für Bildung und Forschung

JÜLICH FORSCHUNGSZENTRUM

SOI solutions for next technology nodes

Siegfried Mantl

Peter Grünberg Institut (PGI-9),

Forschungszentrum Jülich

in collaboration with

CEA-LETI, MINATEC, 17 Rue des Martyrs, 38054 Grenoble Cedex 9, France

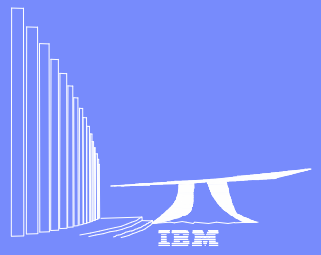
SOITEC, Parc Technologique des Fontaines, 38190 Bernin, France

Outline

- **Mobility enhancement:** basics
  stressors on SOI
  strained Si on insulator (SSOI)
  Quantum Well FETs:
  SiGe and Ge channels with high-k
- **Electrostatics** high-k dielectrics
  device geometry
- **Contacts** improved silicides
- **Future SOI solutions:** FDSOI on thin BOX
  FinFETs
  Nanowire transistors

FDSOI

Bruce B. Doris
IBM Research Division



Outline

- Introduction
- Device Design
- SOC Considerations
- Extendibility
- Summary

CMOS-SOI-MEMS Imagers

Y. Nemirovsky & Research Group
EE Dept., Technion-Israel Institute of Technology
nemirov@ee.technion.ac.il

Outline: Main Topics

- The enabling technology: CMOS-SOI-MEMS
- What is an imager and imager classifications
- CMOS-SOI Image Sensors for visible and near IR
- Thermal Sensors for thermal imaging
- CMOS-SOI-MEMS transistors as thermal sensors:
  - "TMOS": uncooled passive monolithic IR imaging
  - "TeraMOS": uncooled monolithic THz imaging
- Scaling CMOS-SOI technology from 1μm to 0.18 μm

Ultralow-Power SOI Device Technology

Low-power Electronics Association & Project (LEAP)

Nobuyuki Sugii

http://tia-nano.jp/English/index.html http://www.leap.or.jp

Outline

- Classical scaling rule and past trend
- Power consumption of LSIs
- Relationships between speed, power efficiency, and scaling
- Overview of low-power circuit technologies
- Issues on voltage scaling
- Factors to determine minimum V_{dd}
- Transistors for low-power technology
- Planar FDSOI devices with variable V_{th}
- FDSOI process technoogy
- Tradeoffs and integral system-circuit-device design to solve tradeoff issues
- Summary

MEMORIES ON SOI:

FLOATING BODY CELL MEMORY

TRAINING COURSE

EUROSOI

GRANADA, JANUARY 17, 2011

MALGORZATA JURCZAK

imec

OUTLINE

Introduction

- Memory market today
- Memory landscape
- Scaling trends

SOI in memory world

- SRAM
- DRAM: FBRAM
  - Principles of operation
  - FBRAM flavors
  - FBRAM device architectures
  - Performance Benchmarking

Summary and final conclusions

2011

Silicon photonics integration with electronic circuit.

JM. Fedeli

CEA, LETI, Minatec campus, Grenoble, France

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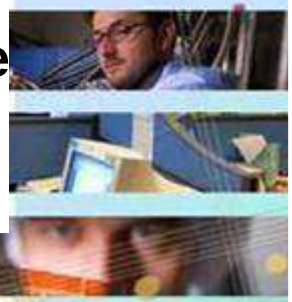

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Outline

- Waveguiding
- Hybrid laser
- Modulation
- Photodetection
- Integration with electronics
- ePIXfab service