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Section 1. Deliverable description.

The EUROSOI network embraces a broad range of research areas related to Silicon-On-Insulator technology (from materials to end-user electronic applications in traditionally strong European industrial sectors such as automotive, communications, space).

The aim of the EUROSOI network was to establish Europe as the international scientific leader in Silicon on Insulator (SOI) Technology, Devices, Circuits and Systems. EUROSOI has networked together the SOI related resources and expertise already existing in Europe and has successfully promoted different activities needed to reach the scientific leadership mentioned above. The final goal of EUROSOI was to provide the European Industry with easier access to the large amount of expertise and invaluable experience available in Europe, so that it will become the leading SOI player in the international arena. Therefore, the EUROSOI co-ordination efforts were focused on fostering those activities which contribute to improving the role of the European semiconductor industry with regard to SOI and to the knowledge that will enable Europe to compete internationally. These goals were realized by achieving the following objectives:

1) **Increase the knowledge and expertise about SOI technology in Europe by enhancing interaction and synergy between academic groups and industry.**

EUROSOI is a platform that promotes the exchange of knowledge and experience between its partners. To achieve this, we have created a virtual research centre to give answers to specific problems about SOI, and which can be found at www.eurosoi.org. It contains excellent resources, including different sections such as Landmark SOI publications, and links to abstracts for more than 1000 relevant articles in research journals around the world (EUROSOI Virtual Journal).

2) **Foster the exchange of knowledge between research groups working on materials, devices, circuits and electronic end-user applications, through the organization of Working Group meetings, and EUROSOI Workshops (UGR-Granada-2005, GRENOBLE INP-Grenoble-2006, IMEC-Leuven-2007, Tyndall-Cork-2008)**

This vertical integration is essential in order to ensure the co-evolution of technology and applications so that technology advances are exploitable in innovative products and services. Particular attention has been paid to users' needs and to usability and accessibility of SOI technologies and applications.

3) **Collect, filter and provide structured information about SOI in Europe**

During this first stage of EUROSOI running, we have elaborated the SOI State-of-the-Art (SoA) Report. This report gives a summary of the European expertise in relation to SOI activities ongoing worldwide.

4) **Elaborate the European SOI Roadmap**

The recommendations and conclusions of the SoA report have been used to identify scientific priority areas, and formulate research and development strategies about SOI technology, that is to say, to elaborate the European SOI Roadmap. This report will be used in this second stage as the starting point for the elaboration of proposals for advanced research projects and to promote their joint submission to the appropriate funding agencies. The SOI Roadmap is a helpful tool for European researchers since it identifies the future needs of SOI technology in EUROPE, foresees its physical limits, and provides, when possible, alternative solutions.

5) **Promote industrial participation in the Network activities**

We have informed industry about relevant progress in SOI technology and provided a feedback loop for industrial mid- and long-term interests. To achieve this objective, the key industrial partners in the field are members of the management board, and co-leads with another partner, the different working groups in which the area of interest of the network has been divided.

6) **Organize and advertise SOI events**

Special attention has been paid in the fast distribution of the results of the network through the organization and sponsoring of workshops, working groups, training courses and tutorials, project results, job opportunities, grants. 18 student grants have been given to attend EUROSOI Workshops.

7) **Manage funding for short technical visits to other labs**

We have also promoted the scientific exchange between partners through a unified management structure that encourages staff mobility, staff exchanges, and joint execution of research projects. Fourteen (14) short scientific visits have been carried out funded by EUROSOI.

8) **Interaction between existing SOI projects**

Along these years we have promoted:

i. The interaction between existing SOI projects at national and European levels, and facilitated the coordination of their work.

ii. The dissemination of available knowledge and pertinent results in new research projects to the industry.

iii. Through the elaboration of the EUROSOI "Who is Who" guide, organization of working group meetings and EUROSOI Workshop.

9) **Training activities for young scientists**

We have developed initiatives to retain qualified young scientists and engineers within Europe, thereby avoiding the brain escape. Two training courses have been organized, with more than 60 attendants and involving, as lecturers, the best specialists in SOI topics all over the world.

10) **Beyond microelectronics: Towards nanotechnology**

We have addressed and fostered initiatives beyond CMOS, taking advantage of the SOI knowledge to develop platforms for further technological development in nanotechnology and not only in microelectronics.

To achieve the objectives of this project it is necessary i) to promote interaction between scientists, ii) to take advantage of the existing experiences

within the research groups, iii) to join forces to maximize the synergy between the individual skills, thus obtaining the best achievable global results, and iv) to provide an appropriate communication channel between academic groups and industrial production centres.

One of the key deliverables of EUROSOI is the State of the art (SoA) report. The goal of this report is to provide an extended review of the past and present of Silicon-on-Insulator technology, based on the collective knowledge of researchers in the field (in this case, the partners of EUROSOI). The report wants to sum up the present situation of SOI technology, highlighting not only scientific advances but also weaknesses, i.e., those aspects which require more research effort. The main idea is to compile, filter and present data on SOI topics in a way that is easily accessible by industrial partners, so that they can decide whether or not to incorporate this information into their R&D work or production process. The work has directly involved the six WG leaders, but also the experience and expertise of the other partners has been fundamental.

- The report would have nine chapters.

Topic
SOI Materials.
Devices. Characterization.
Devices. Fabrication Technologies.
Devices. Physics.
Simulation and modeling.
Reliability of SOI devices and circuits.
Physics. Advanced Device Concepts.
Circuit design.
End-users and Industrial Applications.

- Each chapter should have
  - Introduction
  - Extended review of the past and present of Silicon-on-Insulator technology in the chapter area. Research projects related to SOI.
  - Identification of not only scientific advances but also weaknesses, i.e., those aspects which require more research effort. Main publications in the field.
  - All this should be done in a way that is easily accessible by industrial partners, so that they can decide whether or not to incorporate this information into their R&D work or production process.

Section 2. State of the Art Report

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SOI Materials

EUROSOI State of the Art Report

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Abstract

This section intends to list and update the main techniques existing today for the fabrication of SOI substrates on a commercial basis, as well as the main actors and Vendors. Key manufacturing steps and limitations will be reviewed for each process, calling for further improvements in some areas.

Introduction

This section intends to list the main techniques existing today for the fabrication of standard SOI substrates on a commercial basis, with a focus on the new events, main actors and remaining challenges for the future.

Many good books and review papers [1-6] already exist on the topic. In these documents, the reader will be able to find a thorough description of all the possible techniques to make SOI substrates. Here, we will focus first on those techniques that are used today to (or have the potential to) produce commercially large volume quantities of SOI materials with appropriate quality. In that respect, some very-well known techniques such as Zone Melting Recrystallization (ZMR), Epitaxial Lateral Overgrowth (ELO), Full Isolation with Porous oxidized silicon (FIPOS) etc … will not be addressed.

Consequently, mainly SIMOX and wafer bonding techniques (BSOI, Smart Cut, ELTRAN) will be reviewed, as well as some other more marginal but existing technologies such as SOS (Silicon On Sapphire) and SON (Silicon On Nothing).

This document will not describe all the details of those selected techniques but will give an overview of the main achievements and possibilities offered by each of them. Market applications targeted by each of them will be addressed mainly through the segmentation “thin/thick SOI products”.

Last, we’ll focus on the remaining challenges corresponding to each technique to identify the different R&D axes that need to be addressed in the future. All those technical challenges do not necessarily have to be tackled by European partners. Some recommendations will be given on which of those R&D activities should be supported, based on the picture of the strength and weakness of Europe.

1.1.1. SIMOX

Although many more steps are actually needed, two basic steps define this process. (1) Implantation of high dose of oxygen and (2) high temperature annealing (>1320°C) . Oxygen implantation is performed within a bulk substrate to separate (insulate) the active layer from the rest of the bulk substrate by the formation of an oxygen-rich silicon layer. High temperature annealing is afterwards performed to promote oxygen diffusion / precipitation for the buried SiO_2 formation / densification, and to cure the many crystalline defects created in the silicon by the implantation of heavy oxygen ion species.

The buried oxide (BOX) thickness is fixed by the oxygen dose. First generations of SIMOX materials (called “standard SOI”) had typical BOX thicknesses of about 4000 Å corresponding to ion dose in the range of $1.5 \cdot 10^{18}$ O+/cm². Thicker BOX is not available, which makes the use of SIMOX wafers difficult if not impossible for certain applications (Power applications for instance). Thinner BOX substrates are available or are in development, such as the so-called “low dose SIMOX” wafers. In this case 1000-1500 Å thick BOX can be achieved and is available commercially. One advantage for the SIMOX approach going to thinner BOX is the cost and throughput since the high dose implantation step is probably one of the most limiting factors of the process. The main risk with lowering the oxygen dose (hence the BOX thickness) is the existence of shorts through the BOX (discontinuities in the BOX called “pipes”). Last, it should be noticed that due to the narrow process windows for the BOX synthesis by the SIMOX process (limited process flexibility), such wafers are not available at any BOX thickness but only at some discrete values: for instance 3800, 2000, 1450, 1000Å depending also on the supplier.

The Si thickness is primarily fixed by the implantation energy. Standard dose SIMOX processes use energies in the 100-200keV range, which enable to realise SOI layers as thick as 2000Å. Thinner SOI (lower implantation energy) processes do exist. Adjustments to the SOI thickness may be done at the final stage: (i) towards thick films by growing a final epitaxial layer on the SOI or (ii) towards thin films by thinning the SOI (by sacrificial oxidation for instance).

Still those SIMOX wafers are in the “thin” SOI segment and address more particularly CMOS applications.

In order to improve both the BOX integrity (pipes, interface sharpness, breakdown voltage, ..) and the SOI quality (oxygen precipitates, dislocations, stacking faults, ..) many different improvements have accompanied the now long history of SIMOX:

- very high temperature anneals: 1320°C which is beyond temperature allowed by standard furnaces,
- ITOX (Internal Oxidation) process consisting of growing further the already formed buried oxide layer: a very high temperature oxidation (1320°C) allowing oxygen atoms to penetrate and diffuse through the SOI to react with the SOI/BOX interface
- Control of temperature during implantation: especially heating around 600°C prevents too many crystalline defects to form, which in turn leads to lower final dislocation densities
- multiple implantation steps performed at different temperatures, with or without

intermediate annealing steps
- etc …

On the process side, further improvements are still necessary to improve thickness control and uniformity, roughness, pipes and BOX integrity, SOI defectivity (HF defects, dislocations, …), Light Point Defects, interface sharpness (SOI/BOX and BOX/handle substrate), thin BOX substrates (below 800 Å).

Beyond the needs for quite specific furnaces (1320°C, in large diameters), the high dose oxygen implanter is the critical and non-standard equipment limiting a broader diffusion of this technology. Among others, the specifics are:

- Need for oxygen species implantation,
- High dose (first throughput limiting factor of the process),
- Dose uniformity (as thickness uniformities and pipe densities directly depend on them),
- Heating and temperature control during implantation (500-700°C),
- Importance for such high doses of sputtering of internal implanter walls and parts, generating metallic contamination and particles (which in turn play a critical role on BOX homogeneity).

Basically two main suppliers are addressing this equipment market: IBIS Technology Corp. in the US and Hitachi in Japan.

Concerning the industrial exploitation of the SIMOX process and the associated SOI wafer market:

Europe is absent. Only SOITEC (supported by CEA-LETI) used to exploit this technology with a leading position up to the mid 90's before switching to a wafer bonding technology: Smart Cut™).

In the US, IBIS Technology Corp. [8] has been the main and only US supplier with a strong position worldwide. Their business model until the summer 2004 was to develop the implanters and to commercialize the SOI wafers. During the summer 2004 however, they announced that they exit the wafer business to focus on their equipment business [9]. Their SIMOX deal with MEMC was also announced at the same time to be terminated [9]. Indirectly, one of the main players for SIMOX material in the US (with a worldwide leadership) has been IBM [10] who had a leading position for the development of further generations of SIMOX material (see for instance late "MLD: Modified Low Dose" processes). IBM has been manufacturing internally such wafers for some of their needs, starting in its early device R&D phases. This material technology had also been licensed to IBIS.

In Japan, SUMCO (Sumitomo Metals + Mitsubishi Materials) is probably the leader today for the supply of SIMOX materials [11]. Komatsu and Nippon Steel have also had in the past some SIMOX material related activities.

In China, SIMGUI, a company recently created by the Shangaï Institute of Metallurgy is also proposing SIMOX wafers [12].

1.1.2. Wafer Bonding

Although it has been known and studied for several decades now, wafer bonding technology is quite a new manufacturing module that has been industrially introduced only recently, driven in particular by SOI material technologies as well as by MEMS. It is a tool that is used in very similar ways for several different SOI material manufacturing processes. Several excellent books and review exist on the science and technology of wafer bonding: see for instance [1-7].

Those techniques also basically share the way the buried oxide is formed. In general, a standard oxide layer (thermal or deposited oxide) is formed on the surface of at least one of the two surfaces to be bonded. In this respect, the final BOX thickness value is much more flexible than for the SIMOX process. It can vary continuously from hundreds of Å (and even below in theory) up to many micrometers.

The different SOI manufacturing techniques based on wafer bonding are characterized and differentiated by the technology used to thin down the top substrate (donor substrate) into a (more or less) thin SOI layer. Such thinning techniques can be real material removal techniques such as grinding/polishing/etching (BSOI, BESOI). They can also be based on a splitting/detachment along a certain layer introduced into the donor wafer to delineate the thin Si layer, which will become the SOI layer.

1.1.2.1 BSOI/BESOI

After bonding, the thinning is realized by real material removal techniques such as grinding/polishing/etching. The obtained BSOI wafers are well known to suffer from thickness uniformity limitations: one needs to realize that µms thick SOI layers are obtained as the result of the removal of hundreds of µm from a bulk donor substrate. In most of the cases, those techniques are addressing thick SOI markets: typically 5-50µm, with some possibilities to extend in the1 to 5 µm range of thickness. In this respect they address perfectly applications such as power applications. This situation can be improved if an etch stop layer (Boron doping, SiGe layers, porous layer, ..) is previously added within the donor substrate (BESOI approach). Then a final selective etch is used to achieve much better thickness uniformities.

Beyond thickness related limitations, such technologies are quite simple and processing is cost-competitive for thick products. However, a disadvantage compared to the techniques that will be addressed later in this document is the cost of the starting wafers: the donor substrate is sacrificed in the process, leading to a consumption of 2 bulk wafers for the realization of one final SOI wafer.

Several BSOI/BESOI suppliers exist today.
In Japan, historically one of the oldest players in bonded SOI is SEH (N°1 worldwide for bulk Si wafers), which is still proposing such wafers for specific applications [13].
In the following sections, it will be explained that SEH is also pursuing other technological ways to address thin SOI material for mainstream CMOS.
In Europe, BCO Technologies in Ireland, used to produce such wafers. After a period in the Analog Devices group, all activities related to the SOI substrate business have disappeared. UMICORE in Belgium [14] and Okmetic in Finland [15] are also proposing SOI substrates based on such a technology. A new start-up originating from CEA-LETI, TRACIT Technologies, has been created in Grenoble (FR) and it offers different services based on wafer bonding such as BSOI specific wafers [16].

In the US, only small companies, as is also the case for most of the European companies in the field, are proposing such wafers like Virginia Semiconductors and

Isonics.

As a conclusion, Europe has a competitive position in the field of BSOI/BESOI substrates, which however is limited to marginal business segments markets, mainly because it can not address mainstream CMOS applications but only niche applications (where they still have to compete with other techniques). These companies however have a good knowledge and experience in wafer bonding on an industrial level and are also generally addressing other wafer bonding based activities and services (application specific substrates, MEMS, dissimilar materials integration, processed layer transfers, packaging solutions, …).

Little R&D is done in the field of blanket BSOI/BESOI wafers, except regular engineering developments at industrial substrate suppliers to improve regularly the general quality of the SOI wafers. The field of patterned and / or other specific BSOI/BESOI wafers is addressed in the next section: New SOI-like materials.

1.1.2.2 Layer transfer based on Porous silicon layers (ELTRAN™)

This technology is based on the transfer of an epitaxial silicon layer grown initially on a porous silicon layer. It has seen several evolutions. At the origin, one of the main goals of the porous layer was to supply an etch-stop layer in a BESOI-like configuration. The porous silicon layer, the last layer to be removed before reaching the final non-porous SOI layer, is etched very fast compared in comparison [17]. Recent evolutions have consisted of using this intermediate porous layer as a fragile layer for a wafer scale fracture [18]. Along this layer splitting is performed thanks to mechanical efforts. In particular, CANON has demonstrated the use of a water jet technique [19, 20] to apply appropriate mechanical stress. Probably due to the necessity to limit the damage to the active layer, the porous layer became a double porous layer in the last CANON publications in order to better localize the splitting surface [19, 20].
The remaining porous material on the resulting SOI is selectively etched away after splitting, leaving the initial epitaxial layer transferred to the buried oxide. The SOI thickness control relies on the ability to form good epitaxial layers on porous silicon and enables then good results for thin films. Like in the case of Smart Cut™ (another splitting technology), the remaining donor wafer can be reclaimed and re-used in a subsequent process. ELTRAN™ is a trademark owned by CANON.

There are several key steps in this process. The first of them is the ability to form good quality, low contamination porous silicon layers. Another is the epitaxial deposition of single crystalline silicon layers on such porous layers. The technical challenge related to this task can be measured when referring to the critical importance of surface preparation before epitaxy (and in particular when this surface consists of porous Si). The generation of macroscopic crystalline defects such as hillocks and stacking faults, very sensitive to these surface preparations, can not be tolerated as they would be detrimental to the wafer bonding operations. Yield issues may become critical as small defects before bonding may lead to millimetric voids after layer transfer. Another key step concerns the controlled fracture along the porous layer by mechanical means without damaging the adjacent thin silicon layers. The double porous layer developed by CANON reflects clearly the difficulties related to this step. Last, the finishing step of the wafer consisting in removing the porous layer still needs to be well controlled as it leaves afterwards the final surface of the SOI layer, which needs to be of high quality (roughness, pitting, uniformity, etch pits, particles, ..).
Many R&D efforts are clearly required to accompany the evolution of this technology along with the ITRS roadmaps requirements.

One main actor is involved and has a strong position (patents, ..) with this process: CANON [20]. Other players are limited and have only been involved in limited demonstrations of the process.

1.1.2.3 Layer transfer based on ion implantation (Smart Cut^{TM})

This technology is based on the use of an ion implantation step to define within a donor wafer a damaged layer that will serve as a splitting layer. Hydrogen species implantations are preferentially used but other species can also be used. In order to realize SOI wafers, the implanted donor wafers are bonded to handle substrates, which act also as stiffeners in the process. Right after splitting and layer transfer, the SOI shows generally some roughened/damaged surface. Some surface finishing steps are used to recover a surface comparable to that of a bulk substrate. Polishing (CMP) is one of the most extensively used techniques today for that purpose. For more details on this process, see for instance [5, 6, 21, 22].

As in most of the wafer bonding techniques, the buried oxide layer thickness is formed before bonding on either one of (or both) the surfaces to be bonded, and is therefore quite flexible. The SOI layer thickness is primarily given by the implantation energy. With standard industrial implanters (limited at around 200keV), and considering H+ ions as the implanted species, SOI as thick as 1.5µm are possible. Thicker SOI may also be obtained with an additional epitaxial step formed afterwards. Thinner SOI may be obtained by decreasing the implantation energy and/or by using thinning techniques (sacrificial oxidation, etching, polishing, ..).
SOI thickness non-uniformities, one of the main challenges in CMOS SOI, especially for Fully Depleted technologies, are induced by the combination of several steps in this process: the ion implantation energy uniformity, the thickness uniformity of the oxide layer formed on the donor wafer before implantation, the surface finishing technique uniformity (CMP, ..), and to a lesser extent by splitting conditions. Nevertheless, overall SOI thickness uniformities achievable with this technology are much better than what can be achieved by any BSOI/BESOI techniques. In that respect they are more suited to thin SOI wafers, in the submicron thickness regime.

Among the other advantages of this technology are:

- the possibility to reclaim the donor wafer,
- the fact that epi layer does not need to be grown on the donor wafer, and
- the fact that it uses only standard equipment (no development at the equipment level, easy extension to large diameters, such as 300mm).

As opposed to SIMOX (for instance), it should be noticed that this technology has a generic nature in the sense that it can be applied to (1) other materials than silicon for the active layer or handle substrate, (2) other buried insulators than SiO_2 (and even multiple layers of insulators) and (3) also structures containing patterned layers as well as several levels of SOI (double SOI, etc). Those aspects are addressed in the following sections.

Variations and developments related to this technology have focused on the implantation step (co-implantation with other species such as He, temperature during implantation,…), the impact of the donor wafer properties (doping types and levels, crystalline orientation, …), the splitting zone evolution as a function of different parameters, the fracture parameters and the post splitting surface finishing processes.

Another effort that has been (and that should be kept) high priority is defect reduction. It has been understood for a few years that the quality of the final SOI was more and more limited by the quality of the starting bulk silicon: especially bulk crystalline defects such as COPs (Crystal Originated Particles) coming from the ingot growth. This became a more serious problem when the thickness of the useful layers reached the order of such nano-defects (100nm scale and below). Since then high quality incoming wafers have been used for those most demanding applications such as advanced CMOS. The apparent "cost penalty" associated with those more expensive substrates is balanced by the fact that they are reclaimed and re-used.

Considering the actors worldwide, Europe is clearly leading in this field. This technology has been invented in CEA/LETI and industrially developed by SOITEC (in collaboration with CEA/LETI). With this technology, SOITEC is today the worldwide leader in the thin SOI material market. Smart Cut™ and UNIBOND™, two trademarks owned by SOITEC, correspond respectively to the technology and the SOI wafers made by the technology. The power and potential of this technology has been recognized by major actors worldwide: Shin Etsu Handotaï (SEH) in Japan, N°1 in the bulk Si market has adopted this technology with an agreement signed in 1997 with SOITEC. SEH has started to offer such wafers on a commercial basis. In Europe, Wacker-Siltronic, N°3 worldwide in bulk Si, has recently signed with SOITEC an agreement concerning the licensing of this technology for the manufacturing of SOI wafers. On the R&D side, some public labs are also present in Europe. For instance, MPI-Halle (D) is having activities in the field of Smart Cut in addition to their strong activities in wafer bonding in general [23]. VTT in Finland has also used hydrogen implantation splitting with a focus on Low temperature splitting to realize different structures such as SOI and silicon on glass (SOG) [24].

Outside Europe, strong R&D activities are a proof of the recognized and strategic importance of this technology. Mostly in the US, but also in Asia, both large IC companies, smaller private companies (including some start-up), and public labs/universities work in this area, sometimes with some support from national institutions (DARPA, DoE, NSF..). Concerning the large companies, IBM for instance has made several demonstrations of the Smart Cut™ technology to realize specific SOI structures (strained SOI, etc ..) [25]. Among the small companies, SiGen (Silicon Genesis Corp.) in the US has been working and publishing actively on such technology for several years [26], with a specific focus on some steps and options (hydrogen plasma implantation, low T splitting, plasma activated bonding, variations of combinations of finishing steps. They recently announced a change in their business model: giving up the SOI wafer sale side to focus on a pure IP company model. Many other labs outside Europe also have been active in the field such as for instance the US Naval Research Laboratory (NRL), Duke University, Lucent Technologies.

Overall, although Europe has been pioneering in the field, the situation today is that many actors have entered into the arena, and have engaged significant resources. As a result, especially on the Intellectual Property side, many patent applications (more or less sensible) have been filed on many topics related to such a technology. Europe's leading position here is being threatened.

Concerning the technical challenges, in the short term they are addressing:

- Continuous improvement of material quality in line with the industry roadmaps (ITRS, etc ...)
- Thickness reductions towards sub-10nm dimensions and a strong focus on thickness uniformities at large diameter wafer scales. In that field major progress have been done in 2008-2009 and today the state of the art in term of

SOI thickness uniformity is 150Å ±5Å.

- Technology cost and technology yield improvements through a better control of each of the key steps of the technology (wafer bonding, splitting, surface finishing, ..)

On the longer term, many other key developments do exist to build the next generations of SOI wafers. They will be treated in the following sections; they include high mobility in SOI thanks to strained-Si or Ge-On-Insulator, changing the buried insulator for better thermal management purposes, incorporating patterns into or below the transferred layers. Other developments will consist in adapting the SOI wafers for some specific applications (which do not rule out high volume). For instance, RF applications require high resistivity substrates. Wafer bonding techniques, among them Smart Cut™, enable specific solutions consisting in placing high quality transistor grade silicon film onto high resistivity silicon. Other specific substrates may be optimized for high power devices, MEMS, and for Opto devices.

1.1.2.4 Basic wafer bonding process and evolution trends

The focus of this section is on direct wafer bonding techniques used for SOI-type material fabrication. Gluing and similar approaches are not discussed.

Wafer bonding is a key technology in SOI material formation, at least for those techniques based on layer transfer such as addressed in this section. It is known that this technological step is very sensitive to parameters such as particle density, organic contamination, flatness, roughness, and surface chemical activity. Those aspects are addressed in detail in some books/papers [1-7, 27-29]. Severe defects (sometimes mms wide and even larger) are often associated with a lack of control of some of these parameters. In that respect, not only the geometrical parameters of the initial bulk wafers are of importance but also the final preparation of the wafers before bonding. Today, most of the final preparations are based on wet chemistry, such as (more or less modified) RCA cleanings. As far as industrial scale is concerned, these cleanings are usually performed in separated industrial wet benches of the same type than those used in Si-based IC manufacturing. Wafer bonding, easily done manually in a research setting, is performed in automated machines when manufacturing is considered; Europe counts two leaders in wafer bonding equipment: EVG in Austria [30] and Karl-Suss [31] in Germany. However this industry is quite young and is subject to further developments. In the field of science and technology of wafer bonding based on wet chemistry, Europe has a position of leadership with several labs (CEA-LETI, MPI-Halle, VTT Finland, Queen's Univ. Belfast, Chalmers Univ.,) and several industrial end-users (SOITEC, Okmetic, TRACIT Technologies, Umicore,…).

Usually a wafer bonding preparation based on wet chemistry pre-cleaning is associated with a post-bonding high temperature annealing (>1000°C) to transform low/medium bonding energy into a strong covalent one. The wafer contacting and bonding step is usually performed at room temperature. While lower energies can be tolerated for some applications, SOI wafer processing in general cannot afford it. For future evolutions of SOI materials, there is a need to go to high bonding energies, using processes without the use of high temperature anneals: the so-called Low T° wafer bonding processes (Low T refers to the maximum temperature used in the post bonding annealing).

Low Temperature processes

The possibility of increasing surface energy of bonded interfaces at low annealing temperatures or even at room temperature is of importance in the application to dissimilar materials (i.e novel dielectrics in SOI) and for future applications of layer transfer techniques. There are several ways to reach an increased mechanical stability of the bonded interface after exposure to low or moderate thermal budgets. They all include various modifications of the surfaces. Only extending the annealing time at low temperatures after conventional wet cleaning does not improve the situation more than marginally. Modifications reported to increase the surface energy at low temperatures include:
-Plasma treatment (most of the time oxygen or nitrogen) of the surfaces to form a low density subsurface layer increasing the diffusion of water from the interface. Works at room temperature or with 100-200°C annealing temperatures. The increased water diffusion rate as an effect of the plasma treatment is generally agreed. However, reported results are very scattered, pointing at the fact that the structure of the surface layer is very dependent on the detailed conditions (and chamber geometries, etc) during plasma treatment.

- Non-standard chemical treatments combined with low temperature annealing.

- Ion bombardment or UHV treatments to atomically clean surfaces before bonding.
The challenge of most of the methods is to increase the reactivity (normally the density of silanol groups or the diffusion constant of water in the interfacial region) without detrimentally damaging the materials.

It should be noticed that low T° wafer bonding is also of major interest in the field of Microsystems where wafer bonding is an enabling step to form complex structures. Temperatures and thermal budgets have most of the time to be limited there. Some common interest does exist between the 2 fields of applications SOI and MEMS.

Most of the European labs involved in wafer bonding have also high energy bonding programs. In the field of low T° wafer bonding, Europe today is running in a strongly competitive domain, with strong contributions in the US and Japan. Low T° wafer bonding is important for the future and should be addressed carefully, for instance by gathering together the many rich but elementary activities spread across Europe.

1.1.3. Others (SOS, SON)

SOS

The advent of reliable 100% silicon based SOI wafer manufacturing process has pushed SOS substrates into narrowly defined applications. One of them, probably the most important is about RF applications. For these applications, insulating (or high

enough resistivity) substrates are required. This improves passive component performance (high Q inductors for instance) making above IC architectures possible, and also reduces detrimental cross-talk effects. High resistivity versions of silicon materials enable certainly to address a large part of RF applications but their limited maximum resistivity (typically below a few kΩ.cm) leaves some room for truly insulating substrates such as sapphire.

Today, SOS activities on the material realisation side are close to zero in Europe. The main actors are based in the US as far as materials are concerned (Peregrine Semiconductors and some labs often linked to Defense organizations) [32]. The process used for the material manufacturing is based on epitaxy, and one key element is the control of the hetero-epitaxial growth of Si onto sapphire, as well as metallic contamination control from sapphire.

SON

Silicon On Nothing (SON) is usually obtained through the selective etch of a buried epitaxial layer (for instance a buried SiGe embedded in a silicon matrix). For enabling the selective etchant to reach the buried layer to be etched away, patterning is necessary. This makes this approach more suitable for local SOI structures than for full blanket wafers. As *Nothing* may not have the best insulating properties, and since *Nothing* does not behave properly during IC manufacturing process, the emptied buried layer may be selectively filled by another material, such as SiO_2. The thickness control is a combination of epitaxial and etching step control. When filling the cavities is considered, lateral filling of those horizontal buried cavities is the limiting factor for the width and homogeneity of such structures. Europe has a pioneering position in this area with ST's already long experience [33].

It should lastly be noticed that other approaches have been evaluated to create SON. For instance the "Toshiba approach" uses a combination of deep trench formation by etching and subsequent capping by silicon surface reconstruction thanks to smoothing anneals (hydrogen anneal). To the authors' knowledge, this is so far not reported to be industrially exploitable.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Leadership on wafer bonding science and technology (MPI-Halle, CEA-LETI, SOITEC, EVG, Karl-Zuss, QUB, VTT, Okmetic, Chalmers , …)	Key for most of the SOI material techniques (except SIMOX) but also µ -microsystems.	Aggressive competition outside Europe
Leadership on wafer bonding tools (EVG, Karl-Zuss)	Key for industrial application of wafer bonding	
Leadership based on the Smart Cut process (SOITEC, CEA-LETI) for industrial exploitation (MPI-Halle, CEA-LETI, VTT) for basic research	Pioneering based on the Smart Cut process	Aggressive competition outside Europe
Contributors in BSOI (Tracit, UMICORE, Okmetic)		
Follower in combination of wafer bonding and other than Smart Cut splitting/thinning techniques		Very small activity in other approaches than wafer bonding + Smart Cut
Nothing for other approaches such as SIMOX, SOS		
Leadership in SON (ST)	SON (ST leadersdhip)	No (or almost no) activity in SIMOX, Porous silicon splitting, SOS
Comments: Leading activities in combination of wafer bonding and porous layer splitting in Asia (Canon). Strong contributions on combination of plasma bonding and Smart Cut alike techniques in the US. Strong contributions on wafer bonding in the US (NRL, EVG) and Asia (Tokyo)		

Conclusions and recommendations

- Almost no SIMOX material activity in Europe: Closing the gap would be too expensive and SIMOX is not the present European solution.
- European overall leadership in wafer bonding science and technology
- Importance of wafer bonding technologies for most of the techniques available in Europe
- Thin SOI market potential much bigger than thick SOI due to the perfect match with mainstream CMOS needs
- European leadership in thin SOI material market with Smart Cut

- European activities behind international efforts in some combinations of wafer bonding and wafer splitting/thinning techniques (ex. Porous Si)
- A further integration of European activities through joint projects necessary.

➔ Focus resources on keeping leadership in wafer bonding, Smart Cut and thin SOI material market to keep pace with US and Asia in terms of innovation, IP, ...

EUROSOI State of the Art Report

Chapter 1. SOI Materials
Section 1.1 Commercially available SOI substrates and key manufacturing steps
Subsection 1.1.4. CVD-epitaxy for SOI

Date of Issue: Jul – 2009	**Partner: IMEP**

Abstract

CVD selective epitaxial lateral overgrowth was successfully demonstrated in thin SOI films.

Introduction

Numerous attempts were made to fabricate transistors in varying films made by sputtering, zone-melt recrystallization, and different epitaxy reactor geometries. The work by Philips SC [1] was the first to demonstrate a fully-depleted MOSFET with two individually controllable gates. Recently three-dimensional (3D) thin-film transistors (TFTs) have been intregated forming static random access memory (SRAM). The technique to grow selective epitaxial Si films through the seeding contact hole was successfully developed with a single-wafer-type chemical vapor deposition (CVD) and dichlorosilane gas with HCl in H_2 carrier gas. The electrical characteristics of the cell TFTs made on the selective epitaxial growth (SEG) Si films are very close to those of the bulk transistor. 72 Mbit SRAM was successfully developed with this SEG technique and 3D S_3 SRAM cell technology.

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
Leadership: first successful full-depletion device **Comments:** Issues around gate-oxide grown on polycrystalline silicon and on interface-states on silicon grown on oxide had to be resolved.	Full depletion, almost symmetric gates	Slow growth rate and very high costs. No industrial acceptance.

Conclusions and recommendations

No commercial solutions.

EUROSOI State of the Art Report

Chapter 1. SOI Materials
Section 1.1 Commercially available SOI substrates and key manufacturing steps
Subsection 1.1.5. Liquid-phase epitaxy for SOI

Date of Issue: Jul – 2009	**Partner: IMEP**

Abstract

Devices made in SOI film fabricated by liquid-phase epitaxy (LPE) are characterized.

Introduction

Gas-phase epitaxy for local overgrowth has the disadvantage of slow growth rate and high cost (large consumption of high-purity super-dry hydrogen and heat energy). Liquid phase epitaxy has the advantage that the solvent (Ga or In) can be re-used and the temperatures are lower [1].
Liquid-phase epitaxy allows the islands grown from different orientation seeds. To do so, single-crystalline Si wafers are used as seeds for the location-controlled grain growth with μ-Czochralski process during excimer laser crystallization (ELC). With an enough energy density, Si wafers seeds liquid epitaxial growth and grains with arbitrary orientation can be obtained at the predetermined positions [2].

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
Leadership: only some institutes working on LPE.	Cost advantage	No industrial acceptance

Conclusions and recommendations

No commercial solution.

EUROSOI State of the Art Report

Chapter 1. SOI Materials
Section 1.2. New SOI-Like materials in development
Subsection 1.2.1. High mobility SOI
1.2.1.1. High mobility I: Strained Si on Insulator Wafers

Date of Issue: Nov – 2009	**Partner: SOITEC, CEA-LETI.**

Abstract

Improved versions of SOI material tend to incorporate high carrier mobility layers on Insulator: Strained Si and/or SiGe layers on Insulator are considered in a first version.

Introduction

Improving the carrier mobility, in addition to adopting SOI architectures, is becoming a priority if one wants to meet the next challenges raised by the ITRS roadmap for the sub 65nm nodes (drive current, ION/IOFF trade-off, …). Strained Si in a "bulk" configuration is already considered by some actors for the 90nm node. Combining strained Si and SOI will more precisely address 65nm and below nodes, depending on the applications. High performance devices (logic applications, ..) will be the first to benefit from / require such evolutions.

Strained Si

One known way to modulate carrier mobilities in semiconductors is to apply strain to the material. Applying tensile strain to silicon is known to increase electron mobilities for moderate strain values but also hole mobilities if strong enough strain is applied. To extend the capabilities of silicon in terms of mobilities, the use of strained Si is a solution of choice because it remains a silicon based solution and does not require to revisit completely the transistor fabrication processes (unlike the migration towards other semiconductors such as Ge for instance).

Several ways exist to realize controlled strain induced into silicon. These have generally been initially developed for "bulk" solutions. In this section one should consider whether (and at which price) these solutions can be combined with SOI architectures. Today, two main approaches are investigated for introducing strain in CMOS transistor channels.

The first approach, often referred to as "local strain" or "process-induced strain", is based upon the local strain (generally uniaxially oriented) that is introduced during the CMOS manufacturing steps such as epitaxial SiGe source/drain pocket formation, nitride spacer deposition, gate encapsulation, shallow trench isolation (STI). It has proven very successful and leading edge IC makers have implemented it in 90nm technology manufacturing. These approaches have as advantage that they do seem to depend only on the fine but a priori easy tuning of some basic deposition or etch steps. On the other hand however, one could remark that scalability is a tricky point to control as reducing the lateral dimensions of the transistors affects definitely the efficiency of the induced strain. Strain engineering needs to be taken into account at the transistor level and may limit the flexibility and complexity of transistors architectures. Flexibility

can be limited as each new transistor needs a redesign at a technological level in terms of the strain that needs to be initially applied and the way it transfers to the point of use. Defectivity is another unknown parameter today. The presence of strong strain gradients associated with the local strain approach may indeed raise questions as to the formation of crystalline defects such as dislocations to release the strong gradients of strain. The evolution and impact of such defects on transistor performances and overall yield is not very well known at the moment. Although initially developed for "bulk" solutions, this approach can be combined with the use of SOI substrates [1], with a priori no specific development required at the SOI substrate level.

The other approach ("Global strain" at the material level) transfers the strain building and engineering concerns at the starting material level, adding definitely some value in the substrate. Once the strain is incorporated in the substrate, the device engineers are relieved from additional constraints that limit their flexibility, except maybe to avoid global strain relaxation induced by too aggressive manufacturing steps. The general bi-axial symmetry of the strain associated with this approach makes the impact of the transistor width and length equivalent. A key element here is then the formation of the substrate, a SOI wafer integrating the strained Si active layer. There is definitely room in this field for key and innovative developments on the material side. Europe today has a leading position on the field (see below) and should stay well positioned in that respect.

Initially the two approaches (local versus global strain) appeared as two competitive solutions that several companies and labs worldwide were evaluating in parallel (IBM, TOSHIBA, MIRAI consortium in Japan, MIT, ...). However, instead of pure competition, global strain shall be considered as a further step in strain engineering to further boost device mobility and current drive. It helps overcome the limitations of uniaxial techniques, and its combination with local strain techniques is proposed to maximize performance for the future technology nodes. Global strain is not only an alternative but can be combined with process induced strain to enable the optimization of both NMOS and PMOS transistors.

Competitive solutions at the substrate level for the "Global strain" approach

Still corresponding to the same spirit of introducing the strain at the substrate level in a SOI configuration, alternative ways of creating those high added-value substrates exist.

Probably the oldest (and still competitive) way to form strained Si for "bulk solutions" relies on the hetero-epitaxy of silicon onto relaxed $Si_{1-x}Ge_x$ layer, the final strain being an increasing function of the Ge content (x) and the relaxation rate (R) of this layer (R= 0 for fully strained and =1 for fully relaxed). Since bulk SiGe substrates and ingots do not exist (or only for low diameters, low Ge content, high defectivity), virtual SiGe substrates are formed by hetero-epitaxy onto bulk Si with the help of different sorts of buffer layers (graded buffers etc …).

For the case of SOI architectures, it appears that most of the different classes of substrates that can be obtained contain at least one thin relaxed SiGe layer (but without any additional buffer layer that would be detrimental to the transistor behaviour) in addition to the strained Si layer. Correspondingly, an intermediate substrate is obtained: SiGeOI. In a second phase, this intermediate substrate is used as template for a final strained Si epitaxial deposition step. This approach is called "SGOI". Only in

a very few and specific cases can the final substrate be free of any SiGe layer (see below). In this case, a strained Si layer directly lying on the buried insulator forms the whole structure. Such a structure is named “sSOI”. The two versions, SGOI and sSOI, have already been demonstrated as can be seen hereafter.

Several elements enter into the comparison between the two sSOI and SGOI versions. One is that Ge may be seen by some end-users as a contamination element. Using sSOI substrates becomes therefore a critical advantage for IC makers that are not willing to handle Ge cross contamination issues in their fabs. Another element address the stability and range of uses of such wafers. Since it is relying mainly on the bonding interface to maintain the strain, the sSOI substrates may be more prone to loose part of their strain when submitted to aggressive steps (high temperature treatments, trench isolation or implantation steps associated with transistor manufacturing for instance). First test however have shown that the strain was quite efficiently maintained [3-5] although further work on reliability shall be clearly performed. Last, thickness considerations need to be performed as it directly address the compatibility of such wafers with Partially of Fully Depleted technologies. For SGOI, the total thickness of surface semiconductor is the sum of the SiGe layer thickness, typically 20-50nm, plus the strained Si layer (typically 10-20nm depending on the initial Ge content). The sum makes a value in the 30-70nm range, which renders this structure adapted for Partially Depleted technology only. On the other hand, the sSOI thickness (typically 10-20nm) are perfectly matched with Fully Depleted technologies. Thicker versions of sSOI may also be developed to address Partially Depleted applications as well.

The most common routes to strained Si on Insulator (SGOI and sSOI) that have been tested are:

Growth of SiGe on “standard” SOI and looking for a possible relaxation mechanism during or after growth of the SiGe layer. On some experiments, such a relaxation has been expected to happen thanks to a possible compliant effect coming from the buried layer of the SOI substrate. The final results both in terms of relaxation efficiency, reproducibility and defectivity are not definitely clear. Other attempts have used specific SOI substrates characterised in that the buried oxide were made of low viscosity insulators (BPSG for instance). After the SiGe deposition, the use of high enough temperature thermal treatment is used to make the BPSG layer to flow provoking a relaxation of the strained SiGe layer [6]. Successful relaxation occurs but what is observed is not only a favourable lateral expansion to relax the strain but also buckling of the layers. One solution that the authors have used to prevent buckling is to pattern the layer. If lateral dimensions are below tens of µm (depending on strain, thickness etc ..), the buckling contribution can be minimised. Such a patterning however may not be convenient for any application and different end-users. Post SiGe deposition relaxation has also been shown to be possible thanks to the use of a H or He implantation through the SiGe layer [7]. This implantation concept applied to a SiGe layer grown on a standard SOI leads to complex SOI architectures containing in particular close to the active area a defective layer associated with the defects having provoked the relaxation. Such a technique is also considered in the layer transfer techniques described below, as it appears on the other hand more adapted for the realisation of “bulk” relaxed SiGe donor wafers for layer transfers operations.

SIMOX technology. In a similar manner than for standard SOI manufacturing by SIMOX, high dose of oxygen is implanted within a substrate to separate the active layer from the rest of the bulk substrate but at this time, an additional epitaxial SiGe layer is

preformed before the oxygen implant [8]. Usually in SIMOX, a high temperature

(>1300°C) annealing is finally performed to promote oxygen diffusion / precipitation for the buried oxide formation / densification, and cure the many crystalline defects created in the top silicon layer. For SGOI formation this final high temperature anneal is still necessary and limits severely the initial Ge content of the SiGe layer: its melting point is a strong decreasing function of Ge content. It should also be noted that the overall process enables (although not well understood) a relaxation of the SiGe layer. Such a process does not seem to be the object presently of many activities, which may be explained by the emergence in parallel of other approaches, such as the following.

"Ge condensation effect" [9]. The approach starts with a "standard "SOI substrate on which a SiGe layer is deposited. Following a subsequent sacrificial oxidation treatment, Ge diffusion (from the SiGe layer) into the SOI layer occurs while the buried oxide blocks any further diffusion into the rest of the substrate. This leads to a Ge enrichment of the SOI layer and ultimately to a thin relatively uniform SiGe single layer on SiO_2, with some relaxation of the SiGe layer in the same time. On such a SiGeOI substrate, a strained Si layer is afterwards formed. Several teams are evaluating this approach which has the theoretical advantage to start with standard commercially available SOI wafers. Defectivity (especially dislocation densities) and strain relaxation efficiency in the SiGe layer are among the points that need to be improved. This approach is based on Ge enrichment and does not appear consequently to be compatible with the realisation of Ge-free sSOI substrates.

Layer transfer techniques. Different options of layer transfer techniques (at least the BESOI and Smart Cut™ technologies) have been used to demonstrate the realization of SGOI wafers [3, 4, 10 et 11]. Basically, the main difference when compared to the realisation of standard SOI wafers is that the donor wafers differ in that they now contain pre-formed relaxed SiGe and/or strained Si layers. The Smart Cut™ technology keeps among other advantages the opportunity to save and reclaim the donor substrate (including possible additional layers forming an epitaxial buffer), which from an economical point of view is important. Such a layer transfer based on the fracture of porous Si layers (see CANON's ELTRAN™ technique) have not been reported to the knowledge of the authors. The final quality of the strained Si On Insulator substrates depends critically (especially in terms of dislocation density but also thickness uniformity) on the epitaxy steps involved in the realisation of the relaxed SiGe donor wafer. Several ways of creating the donor wafer are possible and in competition. One family of solutions is based on the existence of different sorts of buffers realised during the epitaxial growth ("graded buffers", low temperature buffers,...) in order to accommodate the lattice mismatch while enabling relaxation of the SiGe layer. In a second family of techniques strained SiGe layers are initially grown and subsequently relaxed (use of H or He implant and anneal for instance [7], …).

Beyond the fact that such layer transfer techniques have already been proven to be volume manufacturing compatible for standard SOI wafers, they present the unique opportunity to realise Ge-free strained Si On Insulator substrates [3, 5, 12]. For this, an additional final strained Si layer formed on the donor substrate is transferred to end-up directly onto the buried oxide of the final substrate. Any remaining SiGe layer that has been used to build the strain in the silicon layer is removed afterwards when the layer transfer has been realised. The strain is from now on maintained by the wafer bonding interface [3, 5, 12].

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European Contribution on the Field	Current Situation	
European Groups	**Strong Points**	**Weaknesses**
Leadership for strained Si On Insulator wafers developments by layer transfer techniques (SOITEC on the industrial side, CEA-LETI, MPI-Halle, QUB for institutes)	++ sSOI and SGOI manufacturing process by the Smart Cut technology; sSOI unique solution for Ge-Free strained Si on insulator substrates	
Follower for other approaches (condensation, SIMOX, …)		- No SIMOX actor Japan and US leaders in condensation approach
Comments: - For layer transfer techniques, the donor substrates (epitaxial layers) are also of prime importance. There is a large number of leading actors in Europe involved in Relaxed SiGe/strained Si epitaxy - Degree of combination of local strain approach with standard SOI and/or sSOI/SGOI to be determined.	++	

Conclusions and recommendations

- Strained Si + SOI architectures is a strategic topic (on the ITRS roadmap!)
- Represents a source of innovative and key developments on the material side (high added value materials)
- Technology leaders and key actors in Europe
- Strength of Europe relying on layer transfer (Smart Cut™ technology, ..), not SIMOX, condensation and other competitive techniques
- Good background and large number of leading actors in Europe involved in relaxed SiGe/strained Si epitaxy but also innovative relaxed SiGe formation techniques
- Strong competition around the world (US, Japan)
- This emerging European leadership in such a key and emerging area shall be maintained and reinforced.

EUROSOI State of the Art Report

Chapter 1. SOI Materials
Section 1.2. New SOI-Like materials in development
Subsection 1.2.1. High mobility SOI
1.2.1.2. High mobility II: Ge on Insulator Wafers

Date of Issue: June – 2009	**Partner: SOITEC, CEA-LETI.**

Abstract

Improved versions of SOI material tend to incorporate high carrier mobility layers on Insulator: Pure Germanium on Insulator is considered on the long term, and addresses sub 32nm nodes.

Introduction

Improving the carrier mobility, in addition to adopting SOI architectures, is becoming a priority if one wants to meet the next challenges raised by the ITRS roadmap. Beyond strained Si evolutions, the use of pure germanium as the active layer is regaining a significant attention. At first, both electron and holes mobility enhancements are expected: from x2 for electrons to x4 for holes. But also, its compatibility with emerging high-K materials for gate insulators (better than Si compatibility which tends to form parasitic oxides) makes of Ge an even more serious candidate for the future. Today GeOI substrates are not available on regular commercial basis and should be developped.

Other applications than pure CMOS may be concerned by GeOI developments. Today pure bulk Ge is used as templates for GaAs and other III-Vs epitaxial growth for opto (photodiodes, lasers, LEDs) and solar cells applications. GeOI substrates can also penetrate these applications by supplying solutions to different problems: mechanical properties and cost issues linked to pure bulk Ge.

Last, it may bring innovative solutions to enable III-V integration onto silicon, thanks to an intermediate Ge layer (on which III-V materials can be grown thanks to better matching).

Bulk Ge

Bulk Ge is obtained similarly than bulk Si by CZ crystal pulling and transforming such ingots into wafers (slicing, grinding, etching, ..). Compared to Si however, bulk Ge is much less mature and is some generations behind. The number of applications presently addressed by crystalline Ge, as well as the number of vendors, is much more limited (which is besides one of the reasons at the origin of the shift with bulk substrates Si and Ge technologies). The major and almost unique vendor today is located in Europe: UMICORE in Belgium. Recently, bulk Ge developments have accelerated, driven at least by the regain of attention for pure CMOS applications demanding of large diameter substrates. The first 200mm wafers have been made available recently on limited quantities by UMICORE. It has been reported that, as opposed to the case of silicon, the availability of raw material for Ge is much more limited. Recycling and saving Ge material is a potential critical concern if it has to

come to mainstream CMOS devices on bulk Ge substrates. Using layer transfer techniques enabling reclaiming of the donor wafers are here particularly relevant: the same bulk Ge substrates may be used several times as donor wafers to make several GeOI substrates (bulk Si handle substrates).

Epitaxial Ge

Another "common" way to realize crystalline Ge material is to grow those layers epitaxially. Ge epitaxy on standard silicon substrates however suffers from the large mismatch between Ge and Si properties. Beyond the necessity of realizing adequate buffer/adaptation layers, the strong lattice parameter mismatch in particular accounts also for the presence of high densities of remaining threading dislocations. As opposed to bulk Ge substrates however, scalability with large diameters appears to be much less of a problem since standard bulk Si substrates on one hand and "standard" epi tools on the other hand are concerned. This does not rule out that adequate / industrial epitaxial recipes will have to be developed. Ge epitaxial layers also can be used as donor wafers for layer transfer operations.

GeOI

So far the techniques the most frequently reported to realize GeOI substrates have been among the layer transfer techniques: both BESOI techniques as well as the Smart Cut process. A comparison between these two would probably remind the same comparison than can be made for standard SOI. The first is mostly adapted to "thick" GeOI substrates. Smart Cut on the other hand is more adapted to thin and uniform GeOI layers (submicron thickness). Another advantage of the Smart Cut process concerns the possibility to save and reclaim the donor wafer. This advantage is even more critical in this case where bulk Ge are even more "precious".

Another interesting technique that has been demonstrated for the realization of GeOI substrates is based on the condensation effect that has emerged for SGOI and strained Si On Insulator developments (see corresponding section 1.2.1.1). Here the Ge enrichment mechanism is pushed to its limits to end-up with a Pure Ge On Insulator structure. This approach is quite new, especially when applied to pure Ge and needs to be further investigated.

Additional challenges related to Ge

While early demonstrations concerning the realization of GeOI substrates have been done, it still happen that Ge is definitely another material than silicon and that it will require in that respect several profound process module developments (Ge cleaning, passivation, annealing, etching, …). In that respect, any experience and background activity related to Ge processing is an added value. Several teams in Europe are pioneering in this field (CEA-LETI, IMEC, UMICORE, ..), but significant efforts still have to be devoted to these developments and today no clear solution came up for the NMOS devices

Due to its small bandgap, leakage currents are quite high and ultra-thin GeOI layers have to be used in order to limit this current. Another alternative is to use SiGe materials with a Ge concentration between 50 and 70%. Indeed, for these concentrations, the bandgap is larger than Ge and hole mobility is enhanced compared to Si. This type of material is thus a good compromise between leakage current and carrier mobility.

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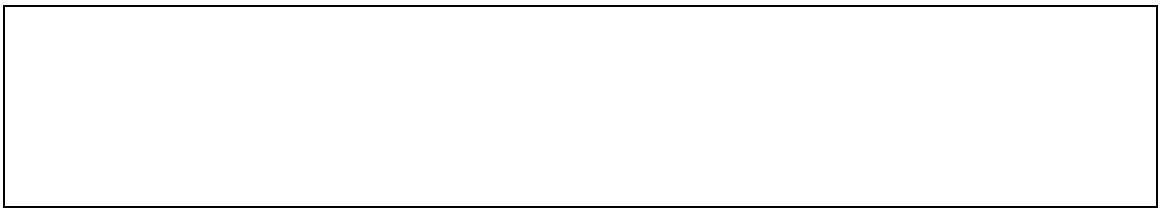
European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Leadership for bulk Ge (UMICORE)	++	
Leadership for Ge On Insulator wafers developments by layer transfer techniques (SOITEC, CEA-LETI, UMICORE)	++	
Leadership on Ge processing (CEA-LETI, IMEC, UMICORE)	++	
Follower for other approaches for GeOI manufacturing (condensation)		Only early demo in Japan
Comments: For layer transfer techniques, the donor substrates may also be made of epitaxial layers. In addition Ge is a very specific material compared to Si, and will require specific process module developments. Several teams have some experience of Ge epi and Ge processing in Europe (CEA-LETI, ST, IEF, …)		

Conclusions and recommendations

- Ge is a Strategic topic for the long term part of the ITRS CMOS roadmap (<32nm)
- Thin films Ge on Insulator are needed if Ge wants to become mainstream
- Represents a source of innovative key developments on the material side (high added value materials)
- Technology leaders and actors in Europe (bulk, epitaxy, layer transfer, smart Cut technology, Ge process module)
- This emerging European leadership in such a key and emerging area shall be maintained and reinforced.



EUROSOI State of the Art Report

Chapter 1. SOI Materials
Section 1.2. New SOI-Like materials in development
Subsection 1.2.1. High mobility SOI
1.2.1.3 Crystalline orientation effect and Hybrid orientation SOI

Date of Issue: Oct – 2009	**Partner: Chalmers, SOITEC, CEA-LETI.**

Abstract

Improved versions of SOI have manipulated semiconductor films to improve carrier mobility (i.e. strain). A variation on improving carrier mobilities in SOI materials is to use crystalline orientation variations to optimize either pMOS or nMOS transistors. A further new concept has been emerging to combine different crystalline orientations on the same substrate to address both and independently pMOS and nMOS transistors (hybrid orientation SOI).

Introduction

For future CMOS there is a strong driving force to form substrates with improved carrier mobility as compared to bulk (100) silicon. Some of the solutions take advantage of strain or alloy (SiGe, strained-Si). Another approach is to take advantage of the fact that carrier mobility is crystal direction dependent (different dependencies for electrons and holes). Historically, (100) oriented bulk substrates with flat or notch location defining the <110> axis have been the universal standard in the IC industry: see for instance SEMI standards for 200mm and 300mm polished monocrystalline silicon wafers [SEMI M1.9-0699 and SEMI M1.15-0704 respectively]. The reasons behind this choice were to maximize electron mobility, with (100) surfaces having the additional advantage of forming good quality gate oxides.

Looking at the effect of different crystalline orientations on the hole mobility, it could be seen that this choice is not optimum for PMOS.

In a SOI configuration, especially when wafer bonding based techniques are concerned, combining two different orientations on the same substrate can be “easily” achieved: one of them is fixed by the handle substrate and the other is fixed by the donor substrate. For instance, making 45° rotation of the donor substrate (active layer) compared to the handle substrate is something that enables a 10-20% gain on hole mobility and which can be achieved easily : either by rotating one wafer compared to the other prior to bonding, or using early specific wafering steps (notch/flat formation) by rotating the donor bulk wafer. This enables to keep standard orientation for the handle substrates, maintaining for instance the way the wafers will cleave during die separation, while optimizing carrier mobilities at the transistor level. Another example is based on the use of 110 Si wafer for the donor substrate while the base substrate is left unchanged (regular 100 wafer). Such wafers have been already demonstrated by the Smart Cut process. These combinations can also be easily made by BSOI/BESOI techniques.

So far, these considerations seem to be limited by the unique choice of one single crystalline orientation for the donor layer and therefore common choice for both N and P MOS transistors. A compromise between both has to be found: in some cases improving one channel type transistor may be at the expense of the other type.

A further new concept has been emerging to combine different crystalline orientations on the same substrate to address both and independently pMOS and nMOS transistors (hybrid orientation SOI). Thanks to the flexibility of wafer bonding and layer transfer techniques, it combines the conventional (100) orientation (notch oriented towards <110> direction) to address NMOS and a (110) orientation for PMOS. In one case the (100) oriented layer is the SOI film (NMOS SOI) while the bulk PMOS is built on a (110) layer grow epitaxially from the handle substrate. The inverse crystal orientation combination results in (110) SOI PMOS and (100) bulk NMOS.

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European Contribution on the Field	Current Situation	
European Groups	**Strong Points**	**Weaknesses**
SOITEC, CEA-LETI : Demos with Smart Cut Outside Europe: IBM as leader in Hybrid Orientation activities	Wafer bonding + layer transfer have a strategic advantage to allow for mixed orientations; Smart Cut preliminary demo already done (100, 110, 111, ..)	Wafer and process cost.

Conclusions and recommendations

- Improved mobility and SOI architecture is a strategic topic
- Wafer bonding + layer transfer techniques have as strategic advantage to be very flexible for Crystalline orientations control and mixing

Balancing the relatively low difficulty of implementation with the potential huge benefit, exploration and development of these solutions shall be a priority.

EUROSOI State of the Art Report

Chapter 1. SOI Materials
Section 1.2. New SOI-Like materials in development
Subsection 1.2.2. New buried insulators

Date of Issue: Oct – 2009	**Partner: Chalmers, SOITEC, CEA-LETI.**

Abstract

Potential improvements in SOI circuits can be achieved by replacing the buried silicon dioxide (BOX) layer by another insulating material. One example concerns thermal management issues that can be addressed more efficiently if a thermally more conductive material is chosen to replace SiO2. This section will describe work on non-SiO_2 BOX materials.

Introduction

Self-heating effects is in many applications a major limitation for SOI CMOS performance [1,2], degrading mobility, threshold voltage, subthreshold swing, leakage currents etc... The low thermal conductivity of the silicon dioxide BOX limits thermal transport to the substrate as well as thermal spreading from hot spots. Wafer bonding and layer transfer in principle allows SOI materials with any buried insulator material to be manufactured. Possible BOX materials include Si_3N_4, Al_2O_3, AlN and diamond, with Al_2O_3 probably having the largest potential for incorporation in commercially SOI materials. These materials have orders of magnitude higher thermal conductivity as compared to SiO_2. The largest potential can probably be found for AlN and diamond. The formation of SOI materials with alternative buried insulators has been studied since at least 1990, having a profound increase in interest during the last years. The challenges are found in forming the advanced highly thermally conductive SOI materials without degrading electrical performance. Another problem is related to the stability of the buried oxide upon device processing in the SOI material. AlN and diamond may be oxidised during processing, causing minor problems with decreased thermal conductivity for AlN and catastrophic scenarios for diamond.
Today, first demonstration of 'Silicon on Diamond' (SOD) substrates has already been demonstrated by CEA-LETI [3] and preliminary devices have been processed. Thin diamond layer (100nm) have been used in order to limit the surface roughness. Due to its thin thickness, the thermal conductivity of diamond is degraded compared to Bulk diamond, but thermal measurments at device level have shown similar values to those obtained on UTBOX (see section 1.2.3 for UTBOX).
Another "more mature" candidate to replace SiO2 is Si3N4. Some early demos have already been reported [4], showing that beyond a single replacement the move to multilayered composite insulating stacks (SiO2/Si3N4) can be realised. Thermal conductivity again can be improved but other device parameters optimization may also be concerned: breakdown voltage, global wafer bow and warp, buried insulator charge trapping properties, specific etch stop layer.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
CEA-LETI, SOITEC, Chalmers Leadership in Si3N4 Diamond and Al_2O_3 based buried insulators for SOI materials Follower in other buried insulator	Strong advantage of layer transfer techniques. Combinations with Smart Cut and or BSOI/BESOI for high quality SOI materials	Small activity on AlN. Applications for Si3N4 not really clear today.

Conclusions and recommendations

- European groups have already a good position in the field and should be able to strengthen it.
- This type of SOI materials may be a potentially important product in the future, for different reasons (thermal management, bow/warp, buried insulator charge trapping properties, ...)

EUROSOI State of the Art Report

Chapter 1. SOI Materials
Section 1.2. New SOI-Like materials in development
Subsection 1.2.3. Ultra-Thin buried oxide

Date of Issue: June – 2009	**Partner: CEA-LETI.**

Abstract

Thinning the buried oxide thickness offers many advantages compare to standard thick buried oxide. Among all the advantages, we can mention [1]:

- Thermal conductivity improvement
- Improvement of the electrostatic control of the transistors
- Re-use of the Back-bias control, like in Low Power Bluk technologies
- Modulation of the front channel threshold voltage (hence the circuit consumption) through a Ground Plane implementation

Introduction

When using a thick buried oxide, many various physical effects occur and limit the transistor performance: due to its poor thermal conductivity, the buried oxide induces an increase of the device temperature during its operation, leading to a slow down of the drive current and associated circuit speed. Fringing fields from the drain through the buried oxide also increase the short channel effects, which limits the scalability of Fully Depleted SOI devices.
Thinning down the buried oxide solves the two previous problem, making FDSOI devices suitable for technological nodes down to 11nm [2, 3].
In addition, this thin buried increases significantly the coupling effect between front and back interface. Coupling coefficients, comparable to the body factor measured on Bulk technologies, are thus measured. This enables circuit designers to re-use all the IPs related to Low Power circuit design. Multiple VT can also be addressed by adding highly doped Ground Plane below the Buried oxide. Thanks to the coupling effect, the front channel VT can be easily tuned, enabling its use for System On Chips applications.
Ultra-thin Buried oxide materials have already been demonstrated, with functionel devices and circuits. Buried Oxide thicknesses of 30, 20 and 10nm have been demonstrated using the Smart Cut™ technology. Standard process have been modified to take into account the specificities of the thin buried oxide.
Today, no clear evaluation of the dynamic performance has been done at the circuit level. This last point will be key for the targeted Low Power applications.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
SOITEC, CEA-LETI Leadership in UTBOX substrates fabrication	Strong advantage of layer transfer technique: high quality UTBOX substrates already available	Parasitic capacitances to be evaluated at circuit level

Conclusions and recommendations

- European groups have already a good position in the field and should be able to strengthen it.
- This type of SOI materials may be a potentially important product in the future.

EUROSOI State of the Art Report

Chapter 1. SOI Materials
Section 1.2. New SOI-Like materials in development
Subsection 1.2.4. Complex SOI structures

Date of Issue: Dec – 2009	**Partner: QUB**

Abstract

This section describes some of the complex SOI structures that can be formed, often associated with the introduction of new layers, new materials or local structures.

Introduction

Substrates for Self Heating optimization

Silicon dioxide as the insulator in SOI substrates is an excellent electrical insulator, but is also a very good thermal insulator. It is therefore difficult to remove heat from ICs on SOI substrates and devices can suffer from self-heating affects. One obvious solution to this problem is to replace the buried oxide layer with a dielectric, which is a good electrical insulator, but a good thermal conductor. However, the use of non-standard IC materials in the substrate is seriously frowned on by IC manufacturers from a contamination viewpoint.

See section 1.2.2 for solutions based on “New buried insulators”.

To overcome the heat removal problem some researchers have etched vias through the buried oxide through earth nodes in the circuit and provided metal paths to the substrate. For thin SOI the thermal conductivity of single crystal silicon drops rapidly and so lateral heat flow in the SOI layer to these metallised vias is limited. The optimum location for thermal vias through the buried oxide is directly below the heat generation regions. Electrical isolation is still required in these areas, but in many cases the thickness of the dielectric is controlled by the desired maximum capacitance rather than by the electrical breakdown. For these applications vias filled with an undoped polycrystalline silicon layer sandwiched between thin silicon dioxide layers have been employed. The polycrystalline silicon, which has a thermal conductivity of 20 times that of silicon dioxide, will behave as a dielectric at high frequencies and provide planarity for the vias. The thin silicon dioxide layers could be replaced with higher thermal conducting silicon nitride.

Silicon on Silicide on Insulator (SSOI)

The employment of SOI substrates and trench isolation greatly reduces the collector-substrate capacitance of bipolar transistors, reduces leakage currents and increases packing density. Metal silicides have been employed for extended base and emitter connections to minimise series resistance. Further optimisation of the device can be achieved by minimising the collector series resistance. The incorporation of a metal silicide between the active silicon and the buried oxide is being investigated. The metal or metal silicide is deposited on the active wafer before bonding to an oxidized handle wafer. A refractory metal is therefore employed as it will have to withstand the high temperature post bond anneal and the IC processing cycles. Titanium disilicide with a low resistivity of 16 $\mu\,\Omega$-cm was the initial choice. In this case the titanium metal

was sputter deposited on the active wafer and a thin layer was deposited on the oxidized handle wafer. By annealing the contacted wafers at 600°C or above, the titanium reacted with the active silicon and the polycrystalline silicon to form titanium silicide and thus bonding the two wafer together. However, it was found that after prolonged high temperature anneals the sheet resistance of the silicide layer increased from 1 Ω/□ to 150 Ω/□. This was attributed to a reduction of the silicion dioxide layer by the titanium to form a titanium oxide and thus decreasing the titanium silicide thickness.

Sputtered layers of tungsten were then used in a similar process to the titanium. Higher temperatures were required to form the tungsten silicide but successful bonding of the wafers was usually obtained. However, on a few wafers the layers delaminated not at the bonded interface, but at the active silicon tungsten interface. It was found that in some cases the tungsten-silicon reaction would start at localised sites and that the silicon would rapidly diffuse into the tungsten leaving voids in the silicon. Silicon atoms diffused rapidly along the surface of the voids to satisfy the tungsten and creating semispherical cavities in the silicon. In some cases the problem was so severe that these semispherical cavities overlapped and the wafer delaminated. To overcome these problems CVD of tungsten silicide was investigated. Tungsten silicide can be deposited at around 400°C by the reduction of tungsten hexafluoride by hydrogen and/or silane. The layers were deposited silicon rich so that they would be stable in a silicon environment. Tungsten silicide deposited and annealed has a resistivity of 40 μΩ-cm given a sheet resistance of 2 Ω/□ for a 0.2 μm thick layer. To ensure an ohmic contact between the tungsten silicide and the single crystal silicon, the latter is ion implanted before deposition of the silicide.
The surface of the tungsten silicide is too rough to bond so it is covered with a thin layer of polycrystalline silicon, which is subsequently polished. The bonding of the two wafers is thus a silicon to oxide bond. After the post bond anneal the active wafer is ground and polished back to a thickness of 2 μm. MOS capacitor and p-n junctions formed on the active silicon of these SSOI substrates yield carrier lifetimes similar to that of the bulk silicon wafers. The diodes showed seven orders of exponential behaviour illustrating the low series resistance available with this technology. Bipolar transistors fabricated on SSOI substrates by MEDL Ltd, England showed no adverse effects from the buried tungsten silicide layers. Cross-sectional analysis by HRSEM and an ultrasonic technique confirm that the WSix is stable up to 1100°C.

These thick SSOI substrates can also be used with Smart-power circuits where vertical DMOS transistors are employed. The buried silicide will reduce the Drain series resistance. A further reduction in collector/Drain resistance is possible by replacing the diffused sinker contacts with tungsten silicide or tungsten filled trenches.

There would be an advantage in using thinner SSOI layers for low power high frequency bipolar transistors provided the thickness uniformity of the SSOI layer could be improved. These advantages include the elimination of epitaxial layers, reduced capacitance and shallower isolation trenches. Directly employing the Smart-cut process gives layers whose silicon thickness is controlled more by the uniformity of the CVD silicide than by the ion implantation. Thin SSOI layers have been produced by starting with an SOI wafer. The tungsten silicide and polycrystalline silicon are deposited on the SOI wafer before bonding to another oxidised handle. After the bond anneal the handle wafer of the original SOI wafer is removed. Thus the silicon layer uniformity is that of the original SOI wafer. The disadvantage of this process is that two silicon wafers are required to produce one SSOI wafer.

SSOI wafers offer significant promise for the production of complementary bipolar

transistors. The buried collectors of the p-n-p transistors will have the same sheet resistance as the n-p-n transistors of 2 Ω sq-1. It has also been proposed to use the tungsten silicide as a dopant conduit as it is reported to have a high diffusivity of impurities. This would enable the doping of the buried collectors to be carried out after wafer bonding, eliminate the need for an epitaxial layer and allow individual process control of the p-n-p and n-p-n transistors to achieve optimum matching. The technique could also reduce the number of photolith and processing steps.

SSOI substrates with HR-Si handles also offer promise for MMICs with active silicon devices. The buried tungsten silicide layer can be employed to minimise the series resistance of active devices, but removed over other areas to allow CPW lines, inductors etc to be located over the HR-Si substrate.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Leadership in SSOI and SOI with Thermal Visa, QUB	MITEL (ZARLINK) fabricated bipolar transistors on SSOI substrates and found wafers to be process compatible	Refractory metal present early in the process QUB Limited to 150mm substrates
Significant Contributor, SOTON, LIVUNI	SiGe HBTs have been successfully fabricated on SSOI and on TVSOI by SOTON	Partial SOI
Follower, CHALMERS		

Conclusions and recommendations

- Unique, complex and high added value possible with layer transfer techniques.
- Pioneering position of Europe in the field.

Europe shall strengthen and take advantage of its leading position in the field.
Those developments, often related to specific device problems or specific applications shall be developed in close collaboration with end-users.

EUROSOI State of the Art Report

Chapter 1. SOI Materials
Section 1.3. Material characterization
Subsection 1.3.1. Electrical characterization

Date of Issue: Dec – 2009	**Partner: IMEP**

Abstract

The main techniques for electrical evaluation of the SOI wafers are reviewed. We focus on the pseudo-MOSFET which is a very powerful and original tool for rapid characterization of the film, interface and buried oxide.

Introduction

The electrical properties of the starting SOI wafer determine the performance of the integrated circuits. The optimization of the wafer fabrication requires rapid feedback from characterization, which implies on-wafer measurements rather than time-consuming device-based information. However, the electrical characterization of SOI wafers is a difficult task due to the thinness of the film and complexity of the stacked structure.

The pseudo-MOS transistor (Ψ-MOSFET) is a unique SOI device which does not need any technology at all. It is based on the upside-down MOS structure that is inherent in all SOI materials. The Si substrate is biased as a gate to induce a conduction channel (inversion or accumulation) at the interface. The buried oxide plays the role of a gate oxide and the Si film represents the transistor body. Low-pressure probes are placed on the film and form source and drain point contacts. Very pure MOSFET-like characteristics are obtained, which in turn deliver invaluable information on the material parameters. The slope of $I_D/g_m^{0.5}$ vs. V_G curves yields the mobility of electrons and holes, whereas the intercept with V_G axis gives the threshold (V_T) or the flat-band (V_{FB}) voltage. The density of traps at the film-BOX interface is calculated from the subthreshold slope in weak inversion, the fixed charge density from V_{FB}, and the film doping from the difference (V_T - V_{FB}). The carrier lifetime is evaluated by recording the transient drain current after the gate is pulsed in strong inversion. The method was successfully applied to SOI films of variable thickness (from a few microns down to 10 nm) and is currently used to optimize the process and monitor the quality of SOI wafers with SiGe and strained films. The Ψ–MOSFET can also be operated in circular, Corbino-like configuration, by using mercury probes; the device is named Hg-FET.

Other measurements. In principle, the Hall effect provides the carrier mobility and film doping. However, thin films have a very large sheet resistance and can be fully depleted. The solution is to use the substrate bias, like in the Ψ–MOSFET, for separating the contributions of the film volume and interface. Same limitations apply to four-probe measurements of the average resistivity, spreading resistance for the resistivity profiling, and photo-conductivity. The Surface Photo-Voltage measurement can be used to determine the diffusion length of minority carriers.

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Key contributors: IMEP, LETI, SOITEC, IBM, Kansai Univ. Osaka, etc

European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
IMEP – Leadership SOITEC – Leadership LETI – Significant contributor Univ. of Athens – Significant contributor	Development of new techniques for SOI wafers. Many samples available.	Models needed for ultra thin films.

Conclusions and recommendations

- The expertise and leadership of European labs is recognized. Support is needed to solve urgent issues related to the characterization of sub-10 nm thick films. In particular, models are needed for parameter extraction with pseudo-MOSFET in ultra-thin films.
- Define a methodology for wafer inspection.
- Correlate the pseudo-MOSFET and Hg-FET data in thin films.
- Extend the principle of pseudo-MOSFET for other types of measurements: C-V and spreading resistance. Investigate the possibility of contactless measurements combining pseudo-MOS with optical methods (SHG or ellipsometry).

CHAPTER II

Devices. Characterization

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.1. C-V measurements

Date of Issue: October – 2009	**Partner: Chalmers**

Abstract

The use of Capacitance vs. Voltage (C-V) techniques, including Zerbst and Deep Level Transient spectroscopy-alike methods for characterisation of SOI materials is described.

Introduction

C-V techniques can be used to characterise interface states and oxide charges both in the SOI material itself and using MOS capacitors fabricated in the SOI film. When measured directly on the SOI material (the S-I-S structure) the top Si film is patterned in islands to define the capacitors. Capacitance measurements can be used to determine fixed oxide charge and interface states densities at both interfaces of the buried oxide. Generally interpretation of C-V data is fairly straight-forward using bulk theory in thick-film partially depleted materials, while fully depleted materials require modifications in the theory.

Using the Zerbst technique (C-t), where capacitance transients are measured when the interface to be studied is pulsed from inversion to depletion, the average generation lifetime in the SOI material can be estimated. A limitation of the Zerbst technique cannot give generation lifetime profiles in the material, where more complex techniques need to be used.

Deep Level Transient Spectroscopy can be applied to SOI materials, although the straight-forward conventional capacitance DLTS technique does not give reliable results on SOI materials, due to the high series resistance. Approaches to overcome this to give more accurate estimates of traps and states include conductance or current DLTS methods. Energy-resolved DLTS techniques may be necessary due to the continuous energy spectrum of the interface states and high levels of generation-recombination centres.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Many groups IMEP-LAHC – Leadership	Model, adaptation and application to SOI devices	

Conclusions and recommendations

The uses of C-V and C-t techniques are widely spread in Europe. Refinements may be needed for ultra-thin SOI films and non-standard SOI.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.2. Diodes: Lifetime characterization

Date of Issue: October – 2009	**Partner: UCL, ISP**

Abstract

Carrier lifetime is one of the key parameters for technology (as it indicates the material quality) and for MOS and bipolar devices operation (as it defines the p-n junction leakage current, floating body effects, bipolar gain, etc.). This parameter has become of crucial importance since it can determine the retention time in floating-body capacitor-less SOI memories.

Introduction

In SOI devices the generation (recombination) lifetimes are generally obtained from transient characteristics [1, 2]. In the last decade, the gated-diode technique, traditionally used for lifetime extraction in bulk Si devices, became more and more applicable for SOI devices [3-8]. This technique is the only one, which allows to extract lifetime parameters directly from measurements on thin-film FD devices, which is of great interest for low-voltage, low-power applications. The great advantage of this method is also the possibility to separate the impact from volume and interfaces, and so to extract both volume generation (recombination) lifetime and surface velocities for top and bottom Si film interfaces.
However, in spite of apparent simplicity of this method, the interpretation of the results is not trivial in the case of SOI devices and obtained curves differ strongly, depending on the SOI technology (i.e. depends on the generation/recombination mechanism which dominates in each concrete case) [3]. Great efforts in numerical simulations and modelling have been undertaken to clarify the SOI specific features of this technique [3, 5-7]. Measurements conditions, at which analyses can be simplified and different components can be discriminated, have been derived [3, 7].
Moreover, this technique should be considered as even more attractive at high temperatures [7, 8], where other techniques (Zerbst-like pulse methods) become unpractical due to strong decrease in relaxation times with temperature increase.
This technique can be also used to investigate the hot-carrier (or radiation) degradation of the Si-film-oxides interfaces [4].

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
ISP (Kyiv, Ukraine), IMEP-LAHC (Grenoble, France), UCL (Louvain-la-Neuve, Belgium) **Comments:** The scientific know-how and research groups possessing large expertise in this field exist in Europe.	Applicable to thin-film FD SOI devices. Allows to separate contributions from volume and from interfaces. Applicable at high temperatures.	Needs for specific structures (i.e. gated diodes, or MOSFETs with body contact); Non-trivial interpretation in the case of SOI

Conclusions and recommendations

Gated-diode technique for extraction of carrier lifetime opens many perspectives, as it is applicable to thin-film FD devices, can be used at high temperature and allows to separate contribution from volume and surfaces generation (recombination). While the method appears rather simple for realization, the interpretation of results is not so simple in the case of SOI devices and demands a good background in this field.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.3. MOSFET characterization and parameter extraction methods

Date of Issue: Sept – 2009	**Partner: IMEP**

Abstract

The SOI MOSFET characteristics represent an extremely rich source of information on the intrinsic material properties, device physics mechanisms and technology performance. Key techniques for parameter extraction are described.

Introduction

The typical configuration of SOI transistors requires an adaptation of the conventional techniques used in bulk silicon MOSFETs and, in some cases, the development of new methods. We briefly enumerate the main techniques.

- **Drain current vs. gate voltage curves.** These curves, measured at low drain voltage, provide the subthreshold slope, leakage current, and threshold voltage (determined either from linear extrapolation or position of the double derivative peak). The transconductance peak yields the carrier mobility. The impact of series resistances on mobility and threshold voltage can be evaluated by using the linear plot of $I_D/g_m^{0.5}$ vs. V_G or more evolved methods. The characterization above is performed for both the front and back channels. For the case of ultrathin devices new methods must be investigated to disclose the intrincated particularities and effects of the confined SOI structure.
- **Saturation characteristics.** Increasing the drain voltage, one can monitor the breakdown voltage, the impact ionization effect leading to kink effect, hysteresis and parasitic bipolar action, the drain-induced barrier lowering (DIBL), the gate-induced drain leakage (GIDL), etc.
- **Floating body effects.** These typical SOI effects (kink, bipolar action, hysteresis, latch, transients, etc) may be disabled by using MOSFETs with body contact. In such transistors, it is useful to monitor the body potential.
- **Coupling effects.** In fully depleted SOI MOSFETs, the properties of one channel vary as a function of the bias applied to the opposite gate. For example, the threshold voltage, mobility and swing of the front channel should be monitored as the back gate goes from accumulation to depletion and inversion. One channel can be discriminated by accumulating the opposite one. This is no longer valid in extremely thin films where volume inversion, super-coupling and quantum effects occur.
- **Edge effects.** The lateral edges of SOI transistors represent a parasitic conduction path, the importance of which depends on the isolation technique (STI, LOCOS or mesa). Edge effects are assessed by comparing devices with variable width.
- **Short-channel effects.** The charge sharing between the gates and the source-drain terminals, the DIBL and the influence of the fringing field from the drain into the buried oxide (drain-induced virtual substrate biasing or DIVSB) are the key effects detrimental in short transistors. They are measured by comparing devices with variable length.
- **Ultra thin gate oxide effects.** The gate tunneling current gives rise to gate-

induced floating body effects (GIFBE) which affect primarily the transconductance, the noise and the transient/history effects. It is necessary to monitor the gate current and, when possible, the body potential.

- **Reliability aspects.** The shift in device characteristics is monitored during radiation (charge trapping in the buried oxide), hot carrier stress (interface state generation and trapping in the gate oxide) or high temperature operation. The drain, gate and substrate current are measured as a function of the degradation time and bias.

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Key contributors: LETI, IMEP, IMEC, UCL, George Mason University (USA), STMicroelectronics, Infineon, Motorola, Toshiba, Univ. of Berkeley, etc.

European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
IMEP – Leadership LETI – Leadership IMEC – Significant contributor UCL – Significant contributor STMicro – Significant contributor Many other contributors	Development of adequate techniques and models, new mechanisms, reliability studies. Some advanced devices are being fabricated.	

Conclusions and recommendations

The European groups are very present in the international arena, where the competition is active. More focus is needed on extremely thin and short devices. New mechanisms emerge continuously and require revisited techniques. A European SOI characterization network, sharing state-of-the-art devices and appropriate techniques, is recommended.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.4. Transport measurements in MOS-like devices.

Date of Issue: October – 2009	**Partner: IMEP-LAHC**

Abstract

Typical transport measurements in SOI transistors are briefly described by showing the information that can be extracted. The main issues of current interest are the mobility behaviour both for electrons and holes the subband splitting in ultra-thin films and the accurate effective field determination.

Introduction

Transport measurements are essential for the analysis of the carrier mobility, doping behavior, band structure, quantum effects, etc. These measurements are difficult in thin SOI films (even impossible in fully-depleted films), without the use of a MOS structure which enables the modulation of the carrier concentration. In general, long-channel MOSFETs are inspected in several respects:

- **Room-temperature experiments:** mobility variation with effective field, strain effects on electron and hole mobility, thickness effects, etc.
- **Low/high temperature measurements:** analysis of the carrier scattering mechanisms (which govern the mobility), impurity freeze-out and activation, strain effects, etc.
- **High magnetic field measurements:** Shubnikov-de-Haas oscillations revealing the subband structure, magnetoresistance effect providing the mobility value, etc.
- **Combination with capacitance measurements:** split-CV method for mobility extraction (universal curves).

A more sophisticated device is the MOS-Hall transistor, where additional lateral contacts allow performing Hall effect measurements. The advantage is that the carrier density and mobility are extracted independently and accurately. Moreover, accumulation-mode Hall MOSFETs served to determine the in-depth profiles in early inhomogeneous SOI films. The idea is to gradually deplete the film, hence reducing the thickness of the active transport layer. A procedure based on differentiation yields the transport parameters at the limit between the depletion and active regions.

The geometric magnetoresistance technique in short-channel MOSFET has been recently introduced to measure the carrier mobility without the need of a precise determination of the channel length [4]. The presence of magnetic field, *B,* perpendicular to the transport plane does not affect the electron confinement. The magnetoresistance mobility, μMR, is obtained by computing the channel resistance for different values of the magnetic field. This procedure can be extended for a deep insight into the transport mechanisms that are hard to reveal with conventional techniques.

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Key contributors: IMEP, LETI, IMEC, UC Louvain, Univ. of Tokyo, MIT, Berkeley, Toshiba, STMicroelectronics, etc.

European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
IMEP-LAHC – Leadership LETI – Leadership IMEC – Leadership UCL – Key contributor Univ. of Udine – Key contributor	Development of new techniques adapted to SOI devices. Good experimental facilities.	Limited sample availability and circulation between laboratories.

Conclusions and recommendations

The expertise of European labs is well known. Support is needed to solve urgent issues before the competitors (very active) succeed: accurate mobility characterization in sub-10 nm films, impact of quantum confinement and strain effects, optimization of thinning techniques, strain transfer methods, etc.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.5. Phonons in SOI.

Date of Issue: Dec – 2009	**Partners: University College Cork (NMRC) and VTT**

Abstract

Phonons play and important role in thermal and electrical conduction in all semiconductors. They are also relevant in characterisation of the built-in strain in semiconductors. Here the most recent work on phonons in SOI is summarised.

Introduction

Phonons in SOI are known to (i) determine the mobility limits at low temperature (acoustic phonons) and at room temperature (optical phonons) via electron-phonon scattering, (ii) act as probes for built-in strain due to lattice mismatch at the various interfaces: planar and around clusters and or grains, and (iii) to play a key role in thermal conduction.

The nature of the SOI thin layer structure means that thermal conduction becomes an increasing challenge to control since (a) the BOX layer is already a poor conductor and (b) the thickness of the SOI layer coupled to the acoustic mismatch of the SOI and oxide layers, leads to bound acoustic phonons. The latter means that the density of states of phonons is changed with consequences for the electron- acoustic phonon scattering arising from a strong deviation from the continuum of phonon energies. The thermal conductivity was predicted to be affected in Silicon quantum well of thickness below about 40 nm [1] due to confinement of acoustic phonons. While this is welcome for an increase in the thermo-electric figure of merit, it becomes is a major challenge for thermal conduction in terms of removing heat from the active part of the SOI structure as well as in the modelling of electron-phonon scattering in SOI device simulators.

The first indications of confined acoustic phonons [2] came from inelastic light scattering experiments in a BESOI structure, although the authors found that the assignment of peaks was incomplete. Prior to this work, Brillouin scattering in a SIMOX structure with SOI thickness of 350 nm had been reported from the perspective of surface acoustic waves [3]. Recently, Raman scattering studies of acoustic phonons in free-standing SOI membranes have shown that acoustic phonons in an air-SOI-air phonon cavity are confined, with the peak energies increasing with decreasing SOI membrane thickness and the peaks becoming more spaced out with decreasing thickness [4].

Acoustic phonon confinement has also been invoked in the interpretation of low temperature transport experiments in 70 nm SOI structures, when measuring the electron-phonon coupling measurements [5].
From the materials characterisation perspective, Raman scattering by optical phonons was successfully used to determine the strain fluctuation in SOI layers as a function of thickness of both the SOI and the buried oxide layer by monitoring the optical phonon frequencies and the peak line width [6].

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Leader: Univ. Montpellier II on strain in SOI assessment. Leaders: Univ. College Cork (NMRC) and VTT on acoustic phonons in device-like SOI structures. Contributors: Politechnico di Milano, Univ. Paul Sabatier. **Comments:** There are very few laboratories working in this field. Critical mass has not been reached. Thermal conductivity in nanostructures is an emerging field in nanotechnology with potentially huge impact in simulations of devices and circuits.	Probably world-level leadership but effort too small to retain it.	Insufficient comparison of theory and experiment in device-like structures to extrapolate into device simulation. No experimental work in actual devices to determine thermal conductivity directly.

Conclusions and recommendations

Acoustic phonon studies of SOI structures is an emerging field needing strong support to harvest the benefits to improved SOI device performance based on phonon engineering.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.6. Interface characterization by Charge Pumping.

Date of Issue: Sept – 2009	**Partner: IMEP-LAHC**

Abstract

The Charge Pumping method is briefly described in the context of SOI MOS devices. It provides the density of interface traps as well as the additional damage induced by radiation and hot carrier degradation.

Introduction

Charge pumping measurements are widely used to characterize interface state densities in MOSFET devices. This type of measurement is especially useful for thin gate materials that have relatively large gate leakege currents when accurate removal of the gate leakage is done. Such leakage makes it difficult, if not impossible, to collect simultaneous quasiestatic high frequency C-V measurement data to estimate state densities. The principle of conventional CP in MOSFETs is to repeatedly switch the gate from inversion to accumulation and vice-versa, while keeping the source and drain contacts grounded or slightly reverse biased. In inversion, some of the minority carriers provided by the source and drain reservoirs are trapped on the interface states. During the falling edge of the pulse, the trapped carriers recombine with majority carriers provided by the body contact. This recombination gives rise to a CP current, which is a frequency-amplified measure of the density of interface states. Recent developments include: 3-level pulses, profiling of the trap distribution, impact of gate tunnelling currents.

The adaptation of CP to SOI transistors requires a contact to the Si film (since the original method involves measurements of the substrate current while applying voltage pulses): either 5-terminal MOSFETs or gate-controlled p-i-n diodes may be used. In fully depleted devices, special SOI coupling effects occur: the pulsing of the front gate results in a scanning of the back surface potential which enables the pumping of some of the back interface traps. Another parasitic CP current is due to `dimensional effects'', which happen in long devices or if the rise/fall times of the pulse are too short.

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Key contributors: IMEP-LAHC, IMEC, Yale University, George Mason University (USA)

European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
IMEP – Leadership IMEC – Leadership	Model, adaptation and application to SOI devices	

Conclusions and recommendations

The CP technique is available in Europe. Developments are needed for extra thin SOI films and gate oxides and for measuring the buried interface properties from front-gate CP experiments.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.7. Electro-luminescence techniques.

Date of Issue: Aug – 2005	**Partner: UNIUD**

Abstract

Measurements of the hot carrier and carrier recombination induced light emission are a contact-less technique to characterize the carrier distribution function in semiconductor devices. In SOI MOSFETs, where the substrate current cannot be measured without perturbing the device behaviour, it provides a valuable alternative monitor of hot carrier and carrier recombination effects.

Introduction

Carriers in semiconductors can relax to lower energy states through microscopic processes that can lead to photon emission. Some photons are reabsorbed in the substrate with the possible creation of electron-hole pairs (with holes flowing toward the substrate terminal and electrons toward the closest high voltage terminal, if these are present and connected); others are absorbed in the top layers; others escape from the device and can be measured directly.

Measurements:
Typical measurement set-up are based either on photomultiplier tubes or on CCD cameras and image intensifiers. The measurement systems can provide essentially two types of information: i) spatial distribution of the emitted light intensity; ii) bias and photon energy dependence of the emitted light. Commercial equipment (Photon emission microscopes) to measure the spatial distribution of EL integrated over relatively large energy bands is available, e.g., from Hamamatsu. This equipment, however, is not very well suited for detailed spectral analysis and most research level setup are typically at least in part home made.

Relevance of the technique:
The photon emission spectrum is partly correlated to the carrier distribution function and represents a powerful mean to study electronic transport and the shape of the distribution function in energy [10]. The bias dependence of integral light emission intensity in given energy bands, instead, is tightly correlated to the most common monitors of non equilibrium transport (drain, substrate and gate currents in bulk devices). In the specific case of SOI devices, Electro-Luminescence (EL) techniques provide unique advantages in that they allow to monitor hot carrier transport effects and carrier distribution functions without the need for additional, perturbing terminals (e.g. body).Relevant extensions of the technique to the analysis of integrated circuits (not necessarily on SOI) have been recently reported in [11-13].

Electro-Luminescence (EL) Modelling:
Hot carrier luminescence and photo-generated current modelling for silicon devices has been mostly developed in [1, 15]. The model incorporates what are believed to be the most relevant light emission mechanisms for MOS devices. However, the model, well verified in Bulk MOSFETs, has been never specifically applied to SOI devices.

Applications to SOI devices and circuits:
EL has been used to analyse in detail hot carrier effects in SOI technologies [2, 3, 4, 7] and to compare hot carrier effects in bulk and SOI technologies [2, 12]. The relationship with hot-carrier degradation has also been studied in [9, 15]. Self heating in SOI has been analyzed with EL in [6].

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
DIEGM, Univ. of Udine, Italy Dept. of Physics, Univ. of Parma, Italy.	Spectrally resolved characterization and physically based photon emission simulation capabilities at the device level	
DEI, Politecnico di Milano, Italy IBMT.J.Watson Research Center, USA	Spatially resolved ultrafast circuit imaging. Circuit	

	design testing and failure analysis.	
IMEP, Grenoble, France	Integral light intensity characterization at the device level	

Conclusions and recommendations

In recent years, voltage scaling has reduced the emphasis on hot carrier effects as the source of the dominant MOSFET (including SOI) reliability concerns. However, hot carriers are still present in modern technologies and they are relevant for PD and FD SOI's also as the source of substrate holes. EL measurements have been historically exploited mostly in relation to hot carrier and degradation analysis. However, the technique is much more general and represents a valuable source of data to verify and calibrate carrier transport models in semiconductor devices. EL studies can help device analysis as a mean to characterize carrier distribution functions, in particular in the low voltage, presumably quasi- ballistic regime. The relative importance of different emission mechanisms at low voltage and in particular in SOI devices is not yet fully assessed. From the experimental point of view, sensitive detectors for the energy range below 1eV would be desirable in view of the reduced supply voltages of present and future devices.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.8. Noise and fluctuations.

Date of Issue: Sep – 2005	**Partner: IMEP**

Abstract

The main sources of noise in SOI transistors are briefly described. The noise stands as a powerful tool for defect characterization as well as a figure-of-merit for circuit performance.

Introduction

The noise reflects the current fluctuations brought about by random variations in carrier number and/or mobility. Each physical mechanism involved in current fluctuations has a distinct noise signature or spectrum.

1. The 1/f noise of MOS transistors originates from the carrier trapping in slow oxide traps located close to the Si-SiO_2 interface. The normalized drain current noise S_I/I_D^2 is measured as a function of gate voltage in order to extract the density of slow traps.
2. The generation-recombination noise features a Lorentzian spectrum: plateau at low frequency, followed by a $1/f^2$ decrease. The cut-off frequency gives the carrier lifetime.
3. The thermal noise has a white spectrum and is induced by several resistors (channel, body contact, measurement system, etc).
4. The Random Telegraph Signal (RTS) is observed in very small area devices. The trapping of one carrier is detected in the time domain as a small pulse super-imposed on the average current. The pulse duration yields the time constant of the trap.

The downscaling of ULSI devices necessitates the introduction of new architectures and new materials with reliable performance and also low power consumption. SOI CMOS with high-k dielectrics (HfO_2) is a one of the most promising candidates for future SOI technology.
However, the implementation of high-k materials usually involves problems for the silicon/dielectric interface quality, for which the low frequency (LF) noise is a diagnostuc tool. The LF noise behavior of TiN/HfO_2 Fully-Depleted (FD) devices for different front and back gate voltages needs to be deeply studied.
Excess noise in SOI transistors can be generated also by the floating body effects, induced by either impact ionization or gate tunneling current (GIFBE). Another special feature in SOI is the interface coupling which may result in a superposition of noise generated at both interfaces. The appropriate biasing of the front and back gates enables to isolate a particular mechanism or a region from the surroundings, in order to measure the noise generated solely by that source.

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- etc gifbe

Key contributors: IMEP, IMEC, Institute of Semiconductors (Kiev)

European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
IMEP – Leadership IMEC – Leadership Inst. Semiconductors, Kiev - Contributor	Models, adaptation and applications to SOI devices. Recent developments.	

Conclusions and recommendations

The noise spectroscopy is an elegant method to discriminate various defects and mechanisms. This technique is available in several European labs which maintain an active leadership. New developments (extra thin SOI films, tunneling gate oxides, quantum related transport, etc) deserve being supported.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.9. Transient and history effects.

Date of Issue: Sept – 2009	**Partner: LETI**

Abstract

This section shows the state of the art of the existing methods for the characterization of the transient effects and the related history effects that occur in the SOI transistors and circuits respectively. European teams contributions is highlighted.

Introduction

Interest: In case of Partially depleted transistors, the internal floating body potential can not be externally fixed, as for Bulk or Body-contacted SOI transistors. This means that the body charge (and hence its potential) is fixed by the voltages applied on the external nodes, and by considering the Kirschoff law at the internal floating body node. This body potential is thus dependent on the external biases applied and is also time related. This leads to the well known 'transient and history effects'. The threshold voltage of the SOI MOSFET (and hence current, transconductance and, definitely, the performance) being modified by the body voltage, it becomes obvious that an accurate modelling of this internal body potential is essential for the correct modelling and design of SOI transistors and circuits. This floating body potential is fixed by a balance between generation and recombination mechanisms in the transistor body. Excess or lack of carriers occurs in the internal body region during the device operation. It is thus important to correctly characterize the lifetime of the carriers.

These effects have been clearly analyzed and explained in Europe ([1], using Partially Depleted SOI technology. By applying the correct voltage drop on the front or the back gate, we can generate generation or recombination transients on the drain current. In a MOS transistor, carrier generation occurs in the space charges of the junction and near the drain through impact ionization or band to band tunnelling (GIDL). Recombination mechanisms occur in the space charge of the junction. The generation transient is due to a lack of majority carriers in the body, whereas the recombination transient is due to an excess of majority carriers. Using Zerbst-type equations, it is possible to extract the lifetime of the carriers, when the transistor is completely processed. Using such method, we can compare different transistor architecture (pocket versus no-pocket, different silicide), and different SOI substrates, in term of carrier lifetime. Keeping in mind that the larger will be the carrier lifetime, longer will the transient (hence faster will be the transistors), this method offer an easy way to analyze the relation between process and circuit performance.

One of the most significant consequence of the transient effects is the well known 'history effect' that illustrates the variation of the body charges of the transistors during the operation of the circuit. In a circuit, each transistor has its own DC body voltage. During the circuit operation, dynamic charges and static charges (due to impact ionization, gate leakage, GIDL/Band to Band tunneling, junction leakage currents...) are injected into the internal floating bodies. Those injections modify the body voltage values and thus during all the operation of the circuit. If the duration of the operation of the circuit is long enough, a steady state condition can be reached. In such case, the floating

body potentials are no longer dependent on the history of the circuit. So, history effects mean that the performance of the circuit are time related. Extreme conditions are reached during the operation of the circuit. Margins have to be taken into account during the design of circuit: those margins must be defined in accordance with the magnitude of the history effects. Their characterization is therefore very important for the layout of the design. IBM ([2]) was the first company to characterize the history effects. Their method was quite simple and based on the first switch/second switch concept. LETI has made effortson the characterization of such effects [3]. They have worked on the experimental analysis of the history effects, analysis coupled with SPICE simulations. They have designed specific structures, in which the four fundamental propagation delay times can be extracted. They have shown that the 'first switch/second switch' concept of IBM is not sufficient to completely characterize the history effect of digital circuit. ST microelectronics design folks have developed their own internal methodology ([4]). Their method can easily, accurately and quickly evaluate the history effects of all their digital cells. They are able to identify the worst case condition for the input signal. IMEP-ST-CEA-LETI has been focussed to exploit the the challenge of history effect characterization in standard cells after static equilibrium and during transient operations. In this study, time efficiency and/or accuracy limitations of standard methodologies, based on gates inputs initialisation, are discussed. A new circuit initialisation technique [5] at transistor level is proposed to overcome the issue of industrial standard cells library characterization. In the proposed solution the polarizations of each transistor of a logic gate are determined by considering all possible input vectors.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
IMEP: Significant Contributor LETI-LAHC: Significant Contributor ST: Significant Contributor	+ History effects on Partially depleted technology	- History effects on advanced single and Multiple-gate Fully depleted technologies.

Conclusions and recommendations

European groups contribute significantly on the field of transient effects and history effects characterization for Partially Depleted technology. Only few analyses are performed on single-gate and multiple-gates Fully Depleted technologies. This last point should be developed significantly.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.10. Floating Body effects (including gate-induced FBE and Meta-Stable Dip effect)

Date of Issue: Sept – 2009	**Partner: LETI**

Abstract

This section shows the state of the art of the existing methods for the characterization of the floating body effects in SOI transistors, including the new floating body effects due to the gate leakage current. European teams contributions is highlighted.

Introduction

Due to the fact that the internal floating body potential can not be externally biased in SOI transistors, its value is fixed by all the carriers injected in the body region. Balance between impact ionization current, Gate Induced Drain Leakage current, junction currents determines the value of this body potential by applying the Kirschoff law in DC mode. In transient mode, dynamic currents contribute to the injection of charges in the body, modifying the body potential value. All the previous mentioned currents must be accurately characterized and modelled, in order to correctly simulate the floating body voltage that reflects the performance of SOI transistors. The initial work on the characterization of Floating Body effects has been mainly done in US. Most of this work was done around the kink effect, i.e. balance between impact ionization and junction currents. At that time, one of the most significant contributions in Europe (in collaboration of University of Florida) was to show that the floating body effects are not only seen in Partially depleted SOI transistors: they can be observed in fully depleted SOI devices [1]. Strength in Europe is related to the characterization of the activation of the parasitic bipolar transistor [2]. Specific methods have been developed to quantify the gain of this bipolar, and to evaluate its variation as a function of SOI film thickness, temperature, gate length. Labs in Europe (especially at IMEP) have done a lot of work on the bipolar characterization. Most of the methods are quasi-static or DC methods. University of Southampton is almost the only one in Europe that publishes on dynamic characterization of floating body effects [3]. Such type of method is cumbersome, but it is the only way to evaluate the time constant of floating body effects and use those data for the small-signal model of floating body effects.

More recently, due to the scaling of the size of the transistors, a new floating body effect appeared in advanced SOI transistors: the so called gate-induced Floating Body effect. This new effect is induced by the gate oxide leakage current that injects carriers in the floating body. This new effect has been carefully characterized and analyzed at IMEP, LETI, ST ([4]) in 2002 and also more recently at IMEC [5] in 2003 on 130nm Partially Depleted technologies. In 2003, LETI [6] has also shown that such effect can be observed on Fully Depleted transistors, when the amount of injected charges is large enough to ensure a transition between full and partial depletion. Such characterization and modelling is very important, because it directly impacts the simulation and the design of the circuit, by modifying the well known history effect. Body pre-charging (or discharging) occurs in circuits, due to gate current: speed and consumption can be significantly changed.

Several European groups in collaboration with Kumamoto National College of Technology have developed a new method [7] for body potential estimation of ultra thin gate oxide fully-depleted silicon-on-insulator MOSFETs in accumulation mode operation. The impact of the back gate voltage, gate length and drain voltage on the body potential has been deeply investigated.

The Meta-Stable Dip effect (MSD) is a new mechanism reflected by a hysteresis in transconductance and current. The MSD effect has potential for developing capacitor-less DRAMs [7].

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
IMEP: Significant Contributor IMEC: Significant Contributor LETI: Significant Contributor	+ characterization methods for bipolar transistors	- Mostly only quasi-static characterization of FB effects: not enough dynamic characterization.

Conclusions and recommendations

European groups contribute significantly on the field of floating body effects characterization for partially depleted and fully depleted SOI technologies. Most of the characterizations are quasi-static methods, where the time constants are quite long. University of Southampton is the only one to publish on dynamic characterization of floating body effects. Those kinds of methods must be developed in Europe. The MSD effect should be systematically investigated with the aim of developing capacitor-less DRAMs. This action should be encouraged as being industrially viable.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.11. Ultra-thin film effects in MOSFETs

Date of Issue: Nov – 2009	**Partner: LETI**

Abstract

This section shows the state of the art of the existing methods for the characterization of ultra-thin SOI film effects. European teams contributions is highlighted.

Introduction

The scaling of Fully Depleted SOI transistors induces a thinning of the SOI layer. A ratio of 3 to 5 is commonly adopted to ensure good performance for the transistors. This means that SOI films as thin as 5nm must be used for gate length as short as 30nm. Such thin layer modifies significantly the electrical properties of the SOI transistors. Firstly, a mobility reduction has been observed when we reduce the SOI thickness below 10nm. A lot of work has been done at Udine university on the characterization of the mobility in Ultra-thin SOI films [1]. The mobility reduction has been also shown at IMEP using experimental data [2].

Secondly, quantum effects occur in thin SOI film. First evidence of such effect has been done in Japan (Omura, NTT). They have shown that quantum confinement increases the threshold voltage of transistors. LETI researchers have worked on the experimental and modelling analysis of the impact of the quantum effects on the front and back interfaces coupling effects [3]. This new model allows an accurate modelling of coupling effects in thin SOI layers, as well as an accurate extraction of the SOI film thickness.
IMEP-LAHC has investigates [4] the carrier mobility in ultrathin SOI MOSFETs with thin SiO_2 gate oxide by comparing the front and back channels. The front-gate split *CV* method has been used at large substrate voltages to determine the carrier density and mobility in the back channel. The implementation of the split *CV* technique in ultrathin SOI films it has been described and is now available in Europe. This method is also efficient for determining the threshold voltage of the back channel.

References

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
IMEP: Significant Contributor LETI: Significant Contributor	+ coupling effects in thin SOI layers	- Not enough activity on quantum related effects.

Conclusions and recommendations

The contribution of European groups is not a leadership activity. Main contribution is still coming from Japan, where ultra-thin transistors are available since many years. Experimental characterization of quantum related effects must be increased in Europe, as experimental transistors are now available in Europe with SOI layer thinner than 10nm.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.12. Self-heating (+ High Tº)

Date of Issue: Sept – 2009	**Partner: Chalmers**

Abstract

Techniques for characterisation of self-heating effects in SOI materials and devices are described.

Introduction

The dielectric isolation (when SiO_2 is used as buried insulator) gives rise to a drawback due to the low thermal conductivity of the buried insulator. As a consequence the temperature in SOI devices may rise to values higher than in bulk devices due to self-heating effects. Both the limited thermal conduction from the SOI film to the substrate heat sink and the reduced capacity for lateral heat spreading may affect the device performance due to reduced mobility. For instance a negative resistance can be seen in the output characteristics of SOI MOSFETs. Also bipolar transistors on SOI can be largely degraded by self-heating effects. Technical solutions may be found by replacing the silicon dioxide material by other insulators exhibiting higher thermal conductivity.

Characterisation of the thermal properties of SOI materials can be made by using simple metal lines on the silicon surface or MOSFETs in the SOI films. Heat is generated in one part of the measurement structure (a metal resistor or a transistor) and the temperature rise is monitored in the sensing part of the measurement structure by a change in current or resistance. Extraction of reliable thermal parameters can be of considerable difficulty.

Time-resolved photon emission microscopy can be used to study self-heating effects, by measuring temperature-dependent luminescence. The technique gives the temperature of the device channel independent of surrounding materials or interconnects.

Self-heating effects can be avoided during measurements on MOSFETs by using pulsed techniques to minimize the power dissipated in the device under test.

References

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Philips Research Leuven - Strong contribution/leadership Uppsala University and Chalmers University - contributors IMEP/LETI Queen's University **Comments:** Strong IBM activity	Extraction of thermal parameters Self-heating in power devices Novel SOI materials	The total European activity is in volume small and therefore vulnerable

Conclusions and recommendations

There are fairly good European activities both on materials manufacturing and characterisation and on device characterisation. An increased collaboration between the groups would probably considerably strengthen the European activity. Techniques for measuring the thermal conductivity of various buried insulators should be developed.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.13. Special device characterization (multiple gates, high voltage FETs, ...)

Date of Issue: Dec – 2009	**Partner: IMEP + LETI**

Abstract

This section shows the state of the art of the existing methods for the characterization multiple gate and high voltage FETs

Introduction

Non planar multiple gate SOI transistors appear to be one of the most interesting device for the future [1,2]. Such kind of transistor will only replace the standard planar transistors, if the quality of the vertical channels is as good as the one of the planar transistors. So the vertical edges of the Fin must be carefully characterized in terms of carrier mobility and interface quality. Specific methods have been developed at IMEP to separate the conductions of the vertical and the planar channels and to extract the mobility of the vertical channel [3]. Such method is very important, because it allows a correlation between the Fin process and the resulting electrical performance. Special characterization methods have also been developed for the case of planar double-gate and four-gate transistors. Low-frequency noise is also a useful tool commonly employed in the characterization of these novel devices [4].

References

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
IMEP: Significant Contributor	+ coupling effects in FinFET + 4-gate transistor	- Not enough transistors available for electrical characterization.

Conclusions and recommendations

The contribution of European groups is not a leadership activity. The process of FinFET transistors in Europe should help significantly the development of characterization methods. The coupling effects in multiple-gate transistors should be investigated for devising conceptually new digital and analog circuits.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.14. SOI High Voltage Transistor Characterization.

Date of Issue: Sept – 2005	**Partner: X–FAB**

Abstract

High voltage MOS transistors formed by a gate and a drain drift region. Due to the electrical properties of the drift region modeling of the characteristics is not trivial. We use a BSIM-MOS model with a drain resistance subcircuit for modeling the drift region effects.

Introduction

Accurate modeling is mandatory for developing circuits. The subcircuit model shows more exact dc-characteristics as the BSIM model on its own. The drift zone characteristics are modeled by a resistor and a behavioral current or voltage source. This takes the mobility-reduction and saturation effects into account and leads to a more correct behavior of the output-characteristics. For nDMOS transistors a better simulation of the gate drain capacitance is given by an additional capacitance between gate and drain. This capacitance has a nonlinear dependence from the gate- drain voltage but this is not entirely taken into account for the model. The drain-bulk diode is represented as a component in the subcircuit rather than using the intrinsic diode of the BSIM model.
The subcircuit model shows a more accurate representation of the device than the simple compact BSIM model.

References

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
Automacs IST-project Advanced Unified Lateral DMOS Transistor Model for Automotive Circuit Simulation (partners: AMI Microsystems, Belgium; Bosch GmbH, Germany; IMEC, Belgium; SILVACO, France) Many companies offering high-voltage/ high-power MOS devices	Accurate model. Models and extraction strategies available for several technologies.	Simulation time. Complexity.

Conclusions and recommendations

High voltage modeling is well understood. Support is needed for a more compact formulation of the models and further development for advanced simulation techniques.

EUROSOI State of the Art Report

Chapter 2. Devices. Characterization.
Section 2.15. High Voltage Characterization During Production

Date of Issue: Sep – 2009	**Partner: X–FAB**

Abstract

The main techniques for electrical evaluation of the SOI wafers under productions conditions are introduced. Typical high voltage characterization parameters where collected on test devices within standard Process Control Measurement (PCM) procedures.

Contents

The requirement to measure high voltage comes from SOI high voltage technology providing drain to source breakdown voltages of more then 700V. To secure the quality of each wafer and to monitor the technological process a enhanced high voltage monitoring test systems is available within standard production environment. The system characterized at least 5 chips per wafer. Beside standard test (VT, RON, resistors, contacts, yield) special high voltage test are installed to measure high voltage parameters. The characterization tests do not require engineering supervision during the phase of wafer handling and measurement. Data is collected automatically and saved in a database. These statistical data is used to improve transistor models, especially regarding worst case modeling and model verification. Because of production always requires big wafer throughput on low cost level the high voltage routines must be optimized in measuring time.

References
(none)

European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
XFAB	Development of new techniques for SOI wafer production measurements.	Add more characterization parameters to automated test. Be sure, that the required measurement time is optimized.

Conclusions and recommendations

The installation of novel characterization methods within standard production environment is used for characterization work of high voltage devices and can replace time expensive manual characterization. Time optimized routines are required.

CHAPTER III

Devices. Fabrication Technology.

EUROSOI State of the Art Report

Chapter 3. Devices. Fabrication Technology
Section 3.1. SOI CMOS Technology
Subsection 3.1.1. Field isolation: LOCOS, mesa, trench isolation

Date of Issue: June – 2009	**Partner: UGR**

Abstract

In this section the most common SOI field isolation techniques are discussed. The vertical device isolation is intrinsic to SOI technology, this is one of the main reasons why SOI technology is gaining momentum with respect to the conventional bulk silicon technology. Therefore, the techniques presented here are the lateral device isolation solutions that are necessary to fullfil the complete isolation of devices needed in IC (LOCOS (Localized oxidation of silicon), MESA, Trench Isolation (TI)).

Introduction

The three main isolation techniques used are: LOCOS (Localized oxidation of silicon), MESA, Trench Isolation (TI). Each of these techniques has different narrow channel effects due to different stress effect on the device.

LOCOS

The local oxidation of silicon (performed in wet conditions, 900°C – 1000°C) is undergone using nitride hardmask to prevent oxidation of active silicon islands. Few interesting features of this technique are: a smooth surface topology which facilitates further etching steps and the fact that it is easy to implement and its cost is low.

The main issues to address in relation to this technique are the following:
1) Bird's beak:
- width loss reduces integration density (for SOI technology using thin films, the bird's beak extension is somewhat reduced)
- sidewall parasitic conduction, requires channel stop implants.
2) Generation of defects on silicon because the high temperature (1000ºC) applied on SiNx/Si.
3) High tensile nitride stress can generate dislocations in the silicon: therefore it can be considered the use of pad oxide (trade-off between less stress for thicker pad oxide and increased lateral encroachment of the oxide).

MESA ISOLATION

The mesa etching processes are used to isolate masked areas from one another to avoid short circuiting the fabricated devices via conducting layers. In order to form the mesa structures, highly anisotropic etching is wanted that implies no width loss and allows high integration density. Good etching profile is needed to produce a well isolated mesa islands.

The main issues to address in relation to this technique are the following:
1) Sidewall parasitics: sidewall additional charges or charge sharing with the front interface
2) Gate dielectric integrity at mesa sharp corners (rounding corners techniques might be necessary)

3) Gate over-etching may be required to avoid gate material residues at mesa dejes

TRENCH ISOLATION (TI)

This technique can be seen as a series of steps: a dry anisotropic trench etch + sidewall oxidation + trench fill + Chemical mechanical polish (CMP)
Few features worth mentioning are the following:
-Sidewall liner oxidation can be performed to: smooth silicon surface and improve interface quality and round corners and improve gap fill.
-Allows tighter active area pitch
-Creates more planar front-end

The main issues to address in relation to this technique are the following:
1) Control of over and under polish: overpolish of isolated features (tiling or reverse mask technique)
2) Micro-scratches and gouges
3) More expensive but most widely used in CMOS applications!
4) Mechanical stress induced by trench isolation (TI) may affect the performance of CMOS devices since it may change work function, effective mass, carrier mobility, and junction leakage

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
CEA-LETI (France) IMEC (Belgium) VTT (Finland) STMicroelectronics	**LOCOS** Smooth surface topology. Easy to implement and its cost is low. **MESA ISOLATION** No width loss. Allows high integration density. **TRENCH ISOLATION** Sidewall liner oxidation can be performed Allows tighter active area pitch Creates more planar front-end	**LOCOS** Bird's beak. High tensile nitride stress can generate dislocations in the silicon. **MESA ISOLATION** Gate over-etching Gate dielectric integrity at mesa sharp corners Sidewall parasitics **TRENCH ISOLATION** TI strain-induced device degradation Micro-scratches and gouges Control of over and under polish

Conclusions and recommendations

The techniques presented here are the lateral device isolation solutions that are necessary to fullfil the complete isolation of devices needed in SOI IC (LOCOS (Localized oxidation of silicon), MESA, Trench Isolation (TI)). The vertical device isolation is intrinsic to SOI technology. The main difficulties found in relation to these techniques are: LOCOS (bird's beak, high density of defects produced by high temperatures, high tensile nitride stress can generate dislocations in the silicon). MESA ISOLATION (gate over-etching, gate dielectric integrity at mesa sharp corners, sidewall parasitics). TRENCH ISOLATION (TI strain-induced device degradation, micro-scratches and gouges, control of over and under polish)

EUROSOI State of the Art Report

Chapter 3. Devices. Fabrication Technology
Section 3.1. SOI CMOS Technology
Subsection 3.1.2. Channel doping and mobility enhancement techniques

Date of Issue: June – 2009	**Partner: UGR**

Abstract

Increased doping concentration in bulk or PDSOI devices to further scale down the gate length results in degradation of mobility. Reduction of the supply voltage to prevent increased field and non scalability of VT and Tox to maintain stand-by power requirements reduces the gate overdrive Cox(VDD-VT). High–k dielectric likely will further degrade the transistors performance. Thin film devices such as FDSOI or DG SOI uses very thin silicon film with reduced mobility due to increased surface roughness scattering. Undoped films make the transistors operate at lower electric field and somewhat compensate for the mobility loss. Few techniques used to increase the channel mobility are the following:
- Strain engineering: process- or substrate-induced strain
- Crystal orientation effects
- New channel materials such as Ge
- SiGe SD stressor

Introduction

Process-Induced Strain
Shallow Trench Isolation (STI)-induced strain: compressive stress from STI results in nMOS performance degradation, depending on transistor layout. Both, decrease of source/drain width (channel direction, x) and device width (y direction), result in nMOS degradation. Narrow-width pMOS are affected by compressive STI as well.
Silicide-induced strain: tensile strain in the channel direction due to silicide improves both nMOS and pMOSFETs. Scaling down the S/D dimensions further increases the stress.
Nitride cap layer such as contact etch stop layer: highly tensile cap layer can improve nMOS devices but degrades pMOS while highly compressive cap layer does the opposite. Ge implant can be used to selectively relax the stress of the capping layer.
Combination of these process-induced strain and others can lead to benefits to both nMOS and pMOS devices. Advantages of this technique are:
- Easy implementation (low cost).
- Potential for improved circuit performance increases as the gate length is further reduced.

Strained Channel on SOI
The use of strained-Si layers instead of conventional relaxed ones increase the mobility of the carriers both electrons and holes in the devices. This technique can be used to increase the mobility to a 20-30 %. The quality of the silicon layers, however, can be worse than the conventional ones. Other materials in addition to silicon can be employed. For all these materials, uniaxial stress offers advantages over biaxial stress.

Crystal Orientation Effects

Inversion layer mobility depends on the surface orientations and current flow directions:
For holes, mobility is 2.5x higher on (110) surface compared to standard wafer with (100) orientation.
For electrons, mobility is highest on (100) substrates.

To fully take advantage of the carrier mobility dependence on surface orientation, fabrication of CMOS on hybrid substrates has been demonstrated. The hybrid substrate is obtained using a layer transfer technique in which the bonded wafer and the handle wafer have different crystal orientation. An additional photo step is used to etch through the SOI and BOX and expose the surface handle wafer to perform SEG.
The main issues to address in relation to this technique are the following:
- Limited scalability of bulk devices.
- Increased process complexity.

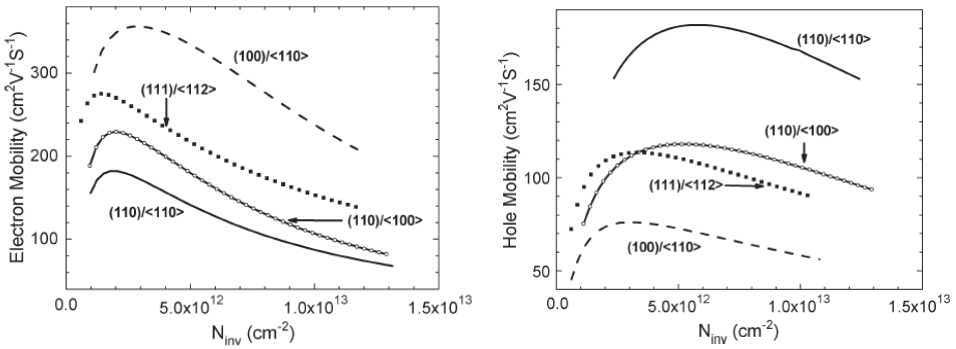

Figure: *Electron and hole mobility in MOSFETs fabricated on silicon substrates with various crystal orientations as a function of inversion charge density. Gate oxides were grown at 800ºC in an N2O ambient, and are on the order of 2–3 nm. The devices are 10 × 10μm. The optimum surface orientation for electron mobility is on the (100) substrate, and for hole mobility is on the (110) substrate with a <110> channel direction. [Figure taken from Ref. [6]]*

Germanium On Insulator
Ge offers 2x higher electron mobility and 4x higher hole mobility.
The main issues to address in relation to this technique are the following:
- Compatibility with a stable gate dielectric.
- Influence of the crystal orientation on the carrier mobility performance on GOI.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
CEA-LETI (France) IMEC (Belgium) VTT (Finland) STMicroelectronics	Techniques available to increase the channel mobility -Strain engineering: process- or substrate-induced strain. -Crystal orientation effects. -New channel materials such as Ge and III-V. -SiGe SD stressor.	Compressive stress from STI results in nMOS performance degradation. The quality of the strained-Si silicon layers, however, can be worse than the conventional ones. Inconsistent evidences of Coulomb mobility dependence on strain. Increased process complexity (HOT) **Germanium On Insulator** Compatibility with a stable gate dielectric.

Conclusions and recommendations

- Very high European Research Activity in high-mobility channels.
- Processing issues specific to the strained and Ge, or C, containing material, will need to be addressed:
  - ultra-thin (1 nm) gate oxides, effects of strain and Ge content on oxidation rate and reducing gate leakage
  - laser doping for ultra shallow junctions, lateral channel profiling
  - device isolation: STI, self aligned STI
  - smart-cut and wafer bonding processes for SSOI
- Hard work still necessary in the characterization and simulation of these devices.
  - Material and device characterisation are crucial to understanding, and vital for making progress.
  - New scattering models have to be developed (e.g.: Coulomb mobility has significant stress dependency).
- These devices with new materials (Ge and III-V) must be incorporated into standard CMOS production. Within Europe there is considerable experience of putting research material through standard process lines and developing new process modules.

EUROSOI State of the Art Report

Chapter 3. Devices. Fabrication Technology
Section 3.1. SOI CMOS Technology
Subsection 3.1.3. Source and drain engineering: silicide source and drain, elevated source and drain

Date of Issue: April – 2009	**Partner: UGR**

Abstract

This point is related to the fabrication of source/drain structures. In particular the features concerning SOI technology difficulties and the solutions that have been implemented.

Introduction

Film thinning is required for SOI CMOS devices to:
- Realize fully-depleted MOSFETs (To maintain control of SCE at very small gate length, very thin silicon is required).
- Improve performance of partially-depleted SOI devices through reduced SD sidewall junction capacitance.

Consequences of silicon film thinning are:
- Voids formation during silicidation (Ti, Co, Ni) due to diffusion of silicon from underneath the gate oxide into the silicide once all the silicon is consumed.
- Increased SD junction resistance when the silicide thickness reaches the silicon film thickness due to reduction of the effective contact area (horizontal area underneath the silicide is no longer available for contact) ~80% of silicided film is optimum.

For very thin films (300Å or lower) thinner silicide (Ni) and increased SD silicon thickness is required.

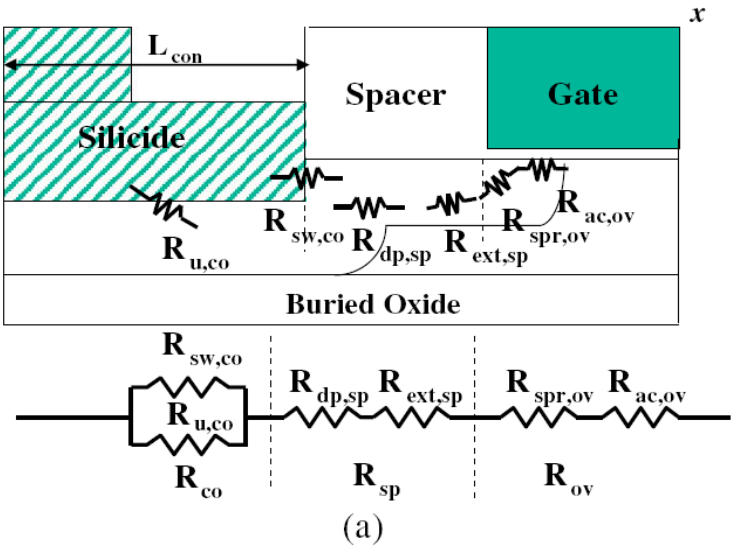

Figure: *Cross-section diagram of total source/drain resistance components including gate/extension overlap resistance, spreading resistance under the spacers, and contact resistance [Figure taken from Ref. [5]],*

Recessed channel technique or elevated S/D performed by means of Selective Epitaxial Growth: Deposition of silicon (or SiGe) epitaxial layer on Si substrate without the simultaneous growth of α-Si on oxide or nitride surfaces makes use of SiCl4, SiH4 or SiH2Cl2 gases and HCl to increase the selectivity of the process.

The main issues to address in relation to this technique and its use in ultrathin SOI films are the following:
Very thin Si films are quasi-stable and their shape changes after thermal treatment. Hence, they agglomerate into silicon islands to reduce their interface energy. It is unclear for crystalline silicon where the agglomeration starts and what causes it.
Silicon shrink, silicon islanding or agglomeration.

In the specific case of UTB SOI devices the parasitic source/drain series resistance can seriously limit the device and circuit performance. Hence sophisticated S/D selfaligned silicide contact technologies using elevated S/D or fan-out S/D structures are highly required. It is thought that as the silicide consumption of silicon increases, the contact series resistance is susceptible to increase due to the decrease in active dopant concentration at the silicide/Si interface or increase in sheet resistance underneath silicide. Numerical simulation predicted that the silicide-to-silicon thickness ratio should be less than 80% to achieve a low series resistance for sub-0.2 μm SOI MOSFET's.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
CEA-LETI (France) IMEC (Belgium) VTT (Finland) STMicroelectronics	Elevated S/D reduces SD junction resistance. Less voids formation	Optimization of the series resistance of silicide contact structure in UTB SOI MOSFETs. Silicon shrink agglomerate into silicon islands. Their shape changes after thermal treatment.

Conclusions and recommendations

The fabrication of source and drain structures in SOI devices is a very important issue. The fabrication in partially depleted devices implies the use of techniques different to the ones used in the case of fully depleted devices. Silicide and elevated source and drain are the main proposals to deal with the difficulties found in the fabrication of SOI devices. However there are several open questions that have to be addressed such as: voids formation during silicidation, increased SD junction resistance when the silicide thickness reaches the silicon film thickness, very thin Si films are quasi-stable, agglomerate into silicon islands.

EUROSOI State of the Art Report

Chapter 3. Devices. Fabrication Technology
Section 3.1. SOI CMOS Technology
Subsection 3.1.4. Gate stack, gate electrode materials, gate dielectric

Date of Issue: June – 2009	**Partner: UGR**

Abstract

In the context of the issue raised in this section it is important to highlight that down to 90nm gate length, N+ and P+ polysilicon gate was used for CMOS integration compatible with oxide or oxynitride gate dielectric. However, due to the aggressive scaling of the gate dielectric, the gate leakage is becoming unacceptably high (> Ioff), requiring the use of high-k dielectric. Therefore, taking into account that due to the incompatibility of polysilicon gate with high k dielectric (Fermi pinning, large VT, mobility degradation) and the need to boost performance (elimination of polydepletion, boron penetration,…), metal gate electrodes will likely be needed. For bulk or PDSOI technologies, two metals with work functions close to the bandgap edges are needed (high channel doping required to control SCE). For FDSOI or double-gate devices, work functions within 250meV from midgap are preferred, requiring more complex integration. Two integration approaches are considered: gate-first or gate-last. High-k dielectrics are also discussed.

Introduction

High-k Dielectrics

For oxide thicknesses below 20A, gate leakage current becomes higher than off-state leakage current. High-k dielectric can reduce gate leakage current by 3-4 decades. High-k dielectrics such as HfO2, ZrO2, Hf-based or Zr-based, LaO2, Al2O3,… can be deposited by ALCVD or MOCVD. Pre-deposition clean and post deposition anneals affect the quality of high-k. Making use of these dielectrics Fermi pinning at the poly Si/metal oxide interface occurs. Fermi pinning also occurs for metal gate electrodes.
The main issues to address in relation to this technique are the following:

- Mobility degradation (many publications have reported mobility degradation using high-k dielectrics, possible cause is coupling of soft optical phonons in high-k with inversion channel charge carriers).
- VT instabilities and reliability issues.
- Large k and large dielectric thickness result in Fringing field (FIBL) and loss of control of the channel by the gate.

Metal Gates

The use of metal gates provides flexibility in adjusting the gate workfunction and transistor VT.
• As Tox is scaled down, poly-depletion issue becomes more significant.
• Metal gates can decrease gate resistance as gate height is scaled.
• Eliminates boron penetration problem.
Integration schemes use two general approaches: gate-first or gate-last.
1) Gate-first approach: FE tool contamination, metal etching, high temperature anneal.
2) Gate-last approach (replacement gate): dummy gate removal and replacement, gate dielectric integrity.
CMOS requires separate work functions (WF) for NMOS and PMOS devices and

therefore 2 different metal gates. Some approaches proposed:
• Single metal for one transistor + an alloy of the same metal formed from an additional layer for the other transistor type. [I. Polishchuk et al., EDL, 2002]
• WF tuning by adjusting the nitrogen dose implanted and the anneal temperature in a single metal. (Mo) [Q. Lu et al., Symp. VLSI, 2001 and P. Ranade et al., IEDM 2002]
• WF tuning of TiN was demonstrated by controlling the N content of the film or by changing the TiN film orientation from {111} to {200}. [K. Nakajima et al. VLSI, 99]
• WF modulation by varying the thickness of the metal electrode. This uses a sandwich of two metals. A thick bottom metal results in the bottom metal bulkWF.
• Thinner bottom metal layer allow the top metal to affect the overall WF. [W. Gao et al., MaT; Res. Soc. Symp., 2003]
• Two different metals: One metal deposited for one transistor and then selectively etched away from the other transistor's active region before depositing the second metal.

Totally-Silicided Gate: WF Modulation
Adjustment of work function by:
1) Implantation of substitutional dopants such as B, As, or P
2) Mix of Co and Ni silicides
The main issues to address in relation to this technique are the following:
• Incomplete silicidation: not enough Ni or low T^a anneal can result in non-uniform silicidation.
• Local silicidation rate can vary highly depending on nucleation conditions, polySi grain structure, and high dopant concentration.
• Phase uniformity of the NiSi throughout the structure: Ni-rich phase does not result in dopant pile-up at the dielectric interface. Over supply of Ni and high silicidation T lead to Ni-rich phase trade-off.
• Large dose of dopants (> 4E15cm^{-2}) results in weakened interface bonds and increased delamination.
Its compatibility with high k dielectric is also uncertain and the gate dielectric reliability: not fully investigated at this time.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
CEA-LETI (France) IMEC (Belgium) VTT (Finland) STMicroelectronics I	**High-k Dielectrics** High k dielectric can reduce gate leakage current by 3-4 decades. **Metal gates** Eliminates boron penetration problem. Metal gates can decrease gate resistance as gate height is scaled.	**High-k dielectrics** Mobility degradation. VT instabilities and reliability issues. Large k and large dielectric thickness result in Fringing field. **Totally Silicided gate** Incomplete silicidation. Local silicidation rate can vary highly depending on nucleation conditions. Gate dielectric reliability.

Conclusions and recommendations

Due to the aggressive scaling of the gate dielectric, the gate leakage is becoming unacceptably high (> Ioff), requiring the use of high k dielectric.
Key materials issues that complicated the introduction of high-κ dielectrics are: reduced electron mobility, oxygen-based thermal instabilities, absence of thermally stable dual-metal electrodes, fringing field (FIBL) and loss of control of the channel by the gate, VT instabilities and reliability issues.

Metal gate electrodes will likely be needed on next technological nodes for the elimination of polydepletion and boron penetration. The main difficulties to be solved in this field are: gate dielectric reliability, phase uniformity of the NiSi throughout the structure, local silicidation rate that can vary highly depending on nucleation conditions, etc.

EUROSOI State of the Art Report

Chapter 3. Devices. Fabrication Technology
Section 3.2. High Voltage Devices
Subsection 3.2.1. LDMOS processes

Date of Issue: April - 2009	**Partner: CNM Barcelona**

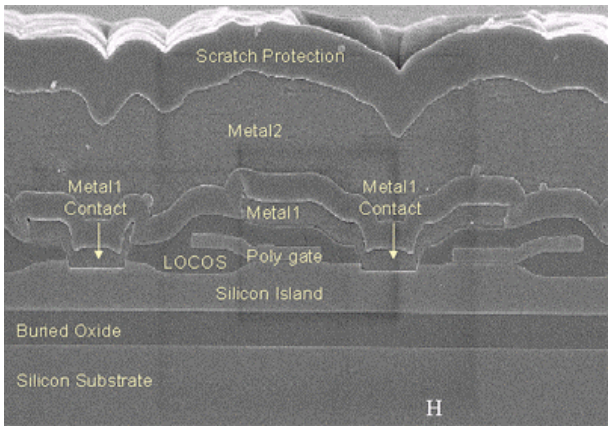
Abstract

European industry (Philips Semiconductor), has a leading position for versatile high-voltage SOI-LDMOS processes. The use of thin-film SOI-layers results in record-low specific on-resistance versus breakdown voltage.

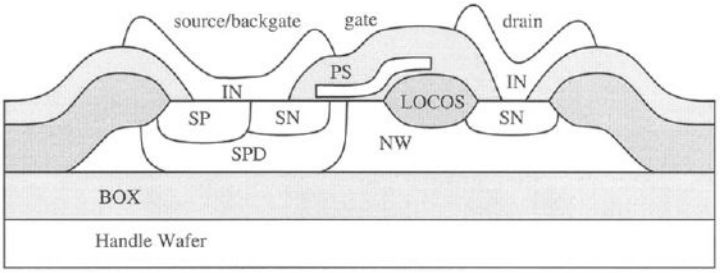
Introduction

A strong driving force in the field of microelectronics is to increase the functionality of the chips by integration circuits and devices with different functions. SOI technology enables easier integration of high voltage devices and low voltage circuits on the same silicon chip. One field that can take advantage of this is the automotive electronics, where there is a strong trend to increase the level of integration.

In order to combine both high-voltage devices and low voltage circuitry on the same piece of silicon, one approach is to integrate high-voltage LDMOS transistors on thin SOI-layers, isolated from the low-voltage devices by trenches.



SEM image of a Phillips SOI A-BCD technology



HV-DMOS integrated in the A-BCD technology

Philips Semiconductors has developed several generations of a thin-film SOI BCD process intended mainly for automotive applications [1]. This type of process uses lateral high-voltage devices. The process offers several types of devices, such as 5V NMOS and PMOS, medium voltage (12-25V) DMOS and high-voltage (100V) complementary DMOS transistors, as well as passive devices. It is therefore easy to integrate power, analog and digital functions on the same chip. The latch-up free substrate with improved EMC performance and its high temperature operation makes it especially well suited for automotive applications.

Later generation [2], which uses wafer-bonded SOI-substrates (1.5μm device layer thickness) and trench isolation, provides high-voltage LDMOS transistors with breakdown voltage up to 120V and 180V. That voltage rating is sufficient for almost all 42V automotive applications. Higher voltage, up to around 500V, is necessary for the semiconductor switches, normally IGBTs, which are used in the ignition circuits. By optimizing a lateral thin-film SOI technology, e.g. by using a graded [3] or retrograde [4] drift region doping profile, LDMOS and LIGBT [5] can reach breakdown voltages up to around 1000V. Extremely competitive performance regarding specific on-resistance versus breakdown voltage has been reported for the thin-film SOI LDMOS transistors, such as 0.1μmmm^2 for a 120V device [2].

In spite of the advantages of SOI technology comprising the latch-up free operation, the less leakage current and high packing density, the combination between SOI and high-power densities in SOI LDMOS transistors causes a significant self-heating that can eventually degrade the electrical performances [6].

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Philips Semiconductor - leadership **Comments:** Overall rather small academic activity in the field in Europe	Major European industrial player, with mature SOI-LDMOS processes. Market share in automotive electronics and audio amplifiers	Small academic activity, compared to USA and Korea

Conclusions and recommendations

Although the future systems integrated on a single SOI chip will require advanced LDMOS transistors, European academic research can be strengthened in this field. It may be worthwhile to exploit the RF-performance of SOI-LDMOS transistors. A complete integrated (CMOS/LDMOS) front-end power amplifier for wireless communication might be possible using SOI-technology.

EUROSOI State of the Art Report

Chapter 3. Devices. Fabrication Technology
Section 3.2. High Voltage Devices
Subsection 3.2.2. Vertical SOI High Voltage Processes

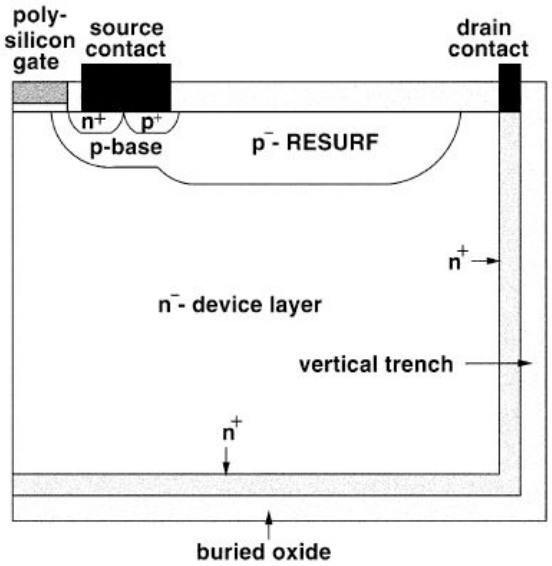
Date of Issue: June – 2009	**Partner: CNM Barcelona**

Abstract

European groups and industries have successfully integrated vertical high-voltage (>650 V) devices on thick SOI-layers. Increased level of integration is therefore possible.

Introduction

A strong driving force in the field of microelectronics is to increase the functionality of the chips by integration circuits and devices with different functions. SOI enables easier integration of high voltage devices and low voltage circuits on the same silicon chip. One field that can take advantage of this is the automotive electronics, where there is a strong trend to increase the level of integration.



Vertical DMOS transistor on SOI

In order to combine both high-voltage devices and low voltage circuitry on the same piece of silicon, one approach is to integrate vertical high-voltage transistors on thick SOI-layers, isolated from the low-voltage devices by deep trenches. With this approach the low voltage devices, such as CMOS, are very similar to ordinary bulk devices. Thus, those devices will not require any special processing modification. It is however worth noting that CMOS devices on thick SOI do not have the performance advantages of the thin-film SOI fully-depleted or partly-depleted CMOS devices. In this thick-SOI type of technology the maximum voltage rating for the high-voltage devices determines the thickness and the doping level of the SOI-layer. It will also determine the required thickness of the buried oxide (BOX) and the dimensions of the trench isolation, i.e. the thickness of the liner oxide.

The major process challenge with this vertical approach is to realize a low-ohmic conduction path to the drain contact at the surface, which for vertical bulk devices normally is at the backside of the wafer. This is accomplished by utilizing buried implanted layers just above the BOX and by dopant diffusion along the trench side-walls. Furthermore, since the high-voltage drain side is at the surface, a lateral high-voltage design is also needed. Another critical process step is the dry etching of the deep trenches, which is complicated both by the extended depth and the oxide etch

stop. There are special dry etch processes developed for this purpose.

Vertical SOI technology has been used to realize both high-voltage (500V) DMOS transistors on 50µm SOI-layer [1,2] and 600V bipolar devices with a 60µm layer thickness [3]. Recently X-FAB [4] presented its XT06 series that completes X-FAB's 0.6 Micron Modular Mixed Signal Technology. XT06 uses dielectric isolation on SOI wafers allowing unrestricted 60 V high and low side operation of all devices. The process offers reduced parasitics which results in smaller crosstalk, reduced noise and better EMC characteristics. Thus XT06 allows innovative circuit design with reduced circuit complexity. CMOS as well as Bipolar Transistors are available with breakdown voltages up to 110V.
Moreover, 650V devices are integrated with 1µm CMOS in a modular BCD-process [4].

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
X-FAB - commercial high-voltage SOI processes (leader) Uppsala University – process and device development. **Comments:** Overall rather small activity in the field both in Europe and worldwide	European foundry exists. Lot of academic knowledge has been built up.	Limited commercial interest as of today.

Conclusions and recommendations

The field might be promising for further exploitation by European industries in the field. In particular the following commercial applications may be targeted:

- Automotive electronics, communication, industrial and consumer market
- Low-power mixed signal circuits
- High precision mixed signal circuits
- Power management circuits
- Mixed signal embedded systems; systems on a chip (SOC)
- Analog front ends for sensors
- Circuits with integrated high voltage I/O's and voltage regulators

EUROSOI State of the Art Report

Chapter: 3. Devices. Fabrication Technology
Section 3.2. High Voltage Devices
Subsection 3.2.3. Bipolar SOI processes

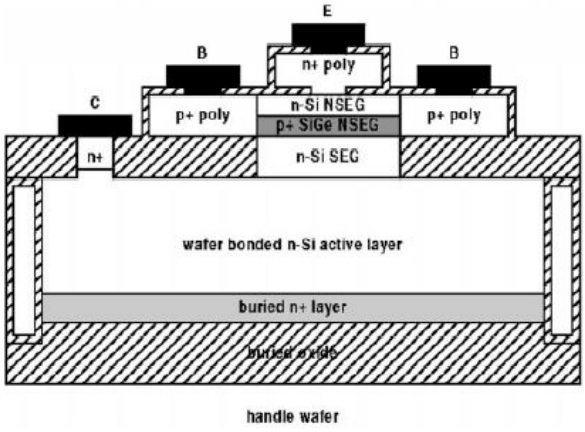
Date of Issue: June – 2009	**Partner: CNM Barcelona**

Abstract

This section focuses on different state-of-the-art bipolar SOI designs and technologies, states different solutions to self-heating and cross-talk problems of standard SOI substrates and outlines major challenges facing SOI BiCMOS integration.

Introduction

In bipolar technology, the use of SOI substrate eliminates parasitic substrate transistors and associated latch-up, and has the ability to reduce crosstalk. A significant reduction in the collector-substrate capacitance is achieved for bipolar transistors on SOI. When combined with trench isolation, a further reduction in capacitance and increased packing density can be obtained. This results in higher frequency performance and/or lower power dissipation. Various technological SOI bipolar concepts have been reviewed recently [1] with special emphasis on the state-of-the-art SOI SiGe HBT devices in vertical and lateral design. Here, we give a brief overview focusing on the state-of-the-art results.

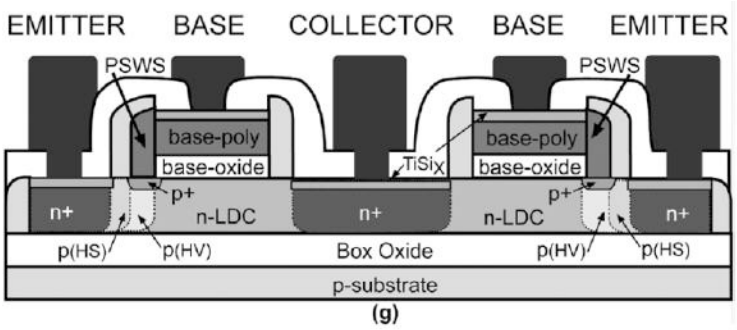


SiGe on bonded wafer substrate

Hitachi has fabricated SOI/HRS (high resistivity substrate) SEG SiGe HBT/CMOS technology targeting applications in wireless communication systems and optical-fibre-link systems [2]. NEC has developed super self-aligned SEG SiGe-base (SSSB) bipolar technology, suitable for application in 20-Gb/s optical transmitter IC's [3]. IBM has used the concept of fully-depleted-collector to produce polysilicon-emitter SiGe HBTs on SOI, particularly to facilitate higher voltage applications and to integrate high-performance HBTs and SOI CMOS on the same chip [4]. A UK consortium (comprising the Universities of Liverpool, Queen's Belfast, Southampton, Surrey, and the Imperial College (with industrial partners)) has fabricated SiGe HBTs on wafer bonded SOI substrates [5]. Bonded wafer technology was developed to allow incorporation of buried silicide layers both above and below the buried oxide. New electrical and noise characterisation results pointed to reduced 1/f noise in these devices compared to bulk counterparts [6]. The lower noise is purported to arise from strain relief of the device structure due to the elasticity of the buried oxide layer during the high temperature epitaxial layer growth. The novel concept of the silicide SOI (SSOI) SiGe HBT technology (Queen's University Belfast, UK) was developed for targeting a reduction in collector resistance, as well as for suppressing the crosstalk [7]. The buried tungsten silicide layers were found to have

negligible impact on junction leakage. A 20 dB reduction in crosstalk – superior performance to any other crosstalk suppression strategy – was achieved with this technology [8]. Recently STMicroelectronics in cooperation with Bordeaux University demonstrated for the first time integration of a high performance SiGeC HBT (f_T/f_{max}=102GHz/154GHz) on a thin film SOI substrate [9]. The SOI substrates feature a 160 nm silicon layer on top of a 400 nm buried oxide (BOX). The fabrication of this device required addition of only four masking steps to the 0.13µm SOI CMOS process. The f_Tx BV_{CEO} products were found to be above 200GHz x V.

In lateral design, the-state-of-the-art LBTs (Lateral Bipolar Transistors) on thin film SOI are fabricated by Toshiba [10] based on the spacer technique. With a small emitter size of 0.12x3.0 μm^2, a low base resistance of 270 Ω due to a novel Co silicided base electrode, and low base-collector parasitic capacitances of 1.4 fF due to SOI material, the device achieved the f_T=12 GHz and highest f_{max} of 67 GHz among the lateral SOI bipolar transistors.



LBJT in SOI for RF applications

Recently [11] the University of Toronto (Canada) with Asahi Kasei Microsystems (Japan) has reported a novel concept for fabricating CMOS-compatible LBTs on SOI. This technology required polysilicon side-wall-spacer (PSWS) structure and only five lithography masks to realize high-performance LBTs. This is the first functional bipolar transistor that has emitter current injection in multiple planes, an idea currently explored by cutting-edge CMOS devices. The experimental f_T/f_{max} of the high-speed device are 17/28 GHz, and for the high-voltage device, the measured f_T/f_{max} of 12/30 GHz and BV_{CEO} of over 25 V produces a Johnsons product well above 300 GHz·V – this is the highest reported for Si bipolar transistors, exceeding not only LBTs but vertical bipolar transistors that incorporate smaller lithography and epitaxial base process as well.

The Indian Institute of technology has reported [12] the highest collector breakdown voltage (12x higher than the conventional) for a lateral Schottky Collector Bipolar Transistor (SCBT) on SOI. The improvement in breakdown voltage was found to be due to the spreading of the electric field away from the Schottky collector metal-base interface into the depleted low doped base and due to the suppression of vertical breakdown at the Schottky metal-buried oxide interface by the extended BOX. This structure is expected to have wide applications for the new generation analogue circuits such as the low power RF amplifiers, current and voltage precision circuits, bandgap reference circuits.

The University of Southampton, UK was recently the first to report [13] lateral SOI SiGe HBT based on a CLSEG (confined lateral selective epitaxial growth) process. The simulation results have shown that the transistor can achieve a maximum f_T of 22 GHz at 34 µA, and an f_{max} of 14 GHz.

Two of the main disadvantages of standard SOI substrates are that (i) the buried oxide layer has poor thermal conductivity and so, self-heating can be a problem, and (ii) at high frequencies the buried oxide is electrically transferred resulting in signal transmission losses and crosstalk problems. A further disadvantage is large collector

resistance. As a viable compromise between high performance and low self-heating, a technological approach that employs a high-energy implantation (HEI) has been developed (Agere Systems, USA) [14]. The HEI is used to simultaneously form the sub-collector while also doping the silicon region below the buried oxide. The formation of a pn junction below the buried oxide results in a lower collector-to-substrate capacitance (C_{CS}). A further reduction in C_{CS} could be obtained by combining the use of SOI with deep trench isolation, but it was shown [14] that this option resulted in a much more dramatic degradation of thermal conductance. The HEI approach has a lower fabrication cost with respect to an epi buried layer. The self-heating effects of bipolar transistors on SOI substrates are discussed in detail through measurements and simulations ([15],[16]). A recent study by the Royal Institute of Technology, Kista, Sweden and Infineon Technologies, Sweden focuses on the examination of devices with three different isolation schemes (STI, DTI+STI, and SOI+DTI+STI) from both an experimental and simulation perspective [15]. The inclusion of heat removal through the dielectric isolation, vias and metallization was found to be important, especially for the SOI+DTI+STI isolation structure. In the device with full dielectric isolation (deep polysilicon-filled trenches on an SOI substrate), accurate modelling of the heat flow in the metallization was found to be crucial.

BiCMOS circuits are one of the key technologies to overcome the total power consumption of bipolar VLSI's circuits. BiCMOS technology allows both digital and RF circuits on the same chip. The α-particle induced soft error and latch-up are also a major concern for high density memory circuits as well as for bipolar logic circuits. SOI substrates offer the solutions to these problems. SOI/BiCMOS also holds the possibility of further lowering the power dissipation, if the digital block is in static CMOS logic. BiCMOS on SOI is the best solution to reduce the noise coupling. The main advantages of BiCMOS on SOI technology are that SOI CMOS allows higher performances than classical CMOS and also high performance PNP at low cost. The major constraint for bipolar design on thin film SOI is the low thickness for the device to be integrated. This design constraint modifies the familiar bipolar structure. To get deeper insight into the device operation, physical simulation device optimisation studies have been performed for HBTs on SOI (Bordeaux University and STMicroelectronics, France) [17].

The demand for increased functionality, lower cost, and more efficient design solutions for RF-applications have increased the use of system-on-a-chip (SoC). These one-chip solutions necessitate efficient isolation of the different circuit blocks. To reduce the transmitted noise through the substrate (crosstalk) various methods have been suggested. SOI on high resistivity (HR) ($\rho \geq 3k\Omega cm$) substrate is a promising solution, but is known to suffer from surface effects and resistivity degradation near the insulating oxide. The crosstalk for HR-SOI is sensitive to excess charges under the BOX layer. For high frequencies, HR-SOI is limited by the silicon relaxation capacitance that causes a frequency dependent contribution. Furthermore, high voltage devices may under normal operation cause an inversion or accumulation layer under the BOX, which strongly affects the device performance. A new technique to passivate the substrate surface of HR silicon wafers and avoid effective resistivity degradation in oxide-covered HR wafers has been recently presented by the University of Louvain, Belgium [18]. The proposed method consists in the LPCVD-deposition of amorphous silicon followed by Si-crystallization at 900ºC with a RTA. A successful bonding of this layer with an oxidized substrate was achieved, showing that this new passivation technique could be introduced at reduced cost inside a smartcut or BESOI process in order to fabricate SOI wafers with enhanced resistivity, i.e. higher than 10 kΩcm. Also, the same research group has shown [19] that the severe effective resistivity degradation effect can be annihilated by depositing a trap-rich 150 nm-thick (or thicker) polysilicon layer at 625°C between the buried oxide and the Si substrate

prior wafer bonding, leading to quasi-lossless HR SOI wafers. Also a 4h30min-long thermal anneal in neutral ambient could increase the effective resistivity of the wafers to even higher values [19].

Including a metal, or metal silicide, ground plane (GP) under the BOX is another method to reduce crosstalk utilizing SOI [20]. This method is based on shunting the current to the ground instead of reducing the current injected into the substrate, as in the case of HR-SOI. The GP-SOI solution has shown high suppression of crosstalk but the manufacturing is complicated and expensive. A new SOI technology on HRS handle wafers has been proposed by Queen's University Belfast, UK [21] for the suppression of crosstalk in SoC applications. The inclusion of a polysilicon layer under the BOX in SOI wafers to provide trap sites for mobile charge carriers has been shown to achieve near ideal crosstalk suppression in both p-type and n-type HRS substrates. The crosstalk suppression performance of these novel substrates with 300 nm BOX layers was as good as that provided by silicon-on-sapphire (SOS) technology. The proposed technology is fully compatible with wafer bonded SOI wafer production and offers a low cost silicon based solution to crosstalk in mixed signal integrated circuits.
As an alternative solution for substrate crosstalk reduction Uppsala University, Sweden has demonstrated ([22],[23]) for the first time the use of a very low resistivity (LR) SOI substrate. The LR-SOI substrate does not suffer from the problems associated with HR-SOI nor does it demand any additional manufacturing steps as GP-SOI. The low crosstalk for the LR-SOI is the result of effective shunting of the signal to ground through the low resistive substrate, which means an effective substrate ground is crucial. An additional advantage of the LR substrate is that the crosstalk is insensitive to relaxation effects, due to the high doping level. The measurements show an improvement in the range of 20–40 dB.

The major challenge for SOI BiCMOS integration lies in the different layer thicknesses needed for HBTs and CMOS. The silicon thickness of about 1 μm required for previously demonstrated high-performance HBTs on SOI is incompatible with advanced SOI CMOS. On the other hand, the performance of HBTs on thin SOI is limited by an increased collector resistance. A new approach to integrate high-performance SiGe HBTs on thin SOI substrates has been reported by IHP, Germany [24]. The thickness incompatibility problem of SOI CMOS and high-performance SiGe HBTs was solved by forming HBTs on Si islands in the BOX using implanted collector wells below the BOX. SiGe:C HBTs with f_T/f_{max} values of 220 GHz/230 GHz and a BV_{CEO} of 2V and fully-depleted CMOS transistors with 90 nm gate length were integrated on thin-body SOI wafers with 30 nm Si thickness. This technology does not use an epitaxially-buried subcollector or deep trench isolation, and thus facilitates an easy BiCMOS integration in a cost-effective manner. The thermal resistance of the HBTs is not increased by the use of SOI wafers due to the absence of the BOX below the active HBT regions. This is in contrast to previous approaches to SiGe HBTs on SOI which showed a significant increase of the thermal resistance due to the low thermal conductance of the buried oxide. This new scheme opens the way for BiCMOS technologies combining state-of-the-art SOI CMOS and bipolar performance.

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
Significant Contributor: UK consortium – SiGe HBTs on wafer bonded substrates Leadership: Queen's University Belfast, UK –crosstalk suppression (GPSOI, silicide SOI etc.) Significant contributor: Southampton University – lateral SOI SiGe HBTs STMicroelectronics, France + Bordeaux University – SiGeC HBTs and SiGe HBT on a thin film SOI Royal Institute of Technology, Kista, Sweden + Infineon Technologies, Sweden – work on different isolation schemes The University of Louvain, Belgium - work on passivating the substrate surface of HR Si wafers Uppsala University, Sweden – LR-SOI IHP, Germany – SOI BiCMOS. **Comments:** Significant work on cross-talk suppression (GPSOI, HR-SOI, LR-SOI)	• Crosstalk suppression techniques. • Thermal vias and smart substrates for heat removal. • Collaborative project (UK consortium) on bonded SOI SiGe HBTs: basic platform process established.	• Lack of continuity and funding • Uncertainty about take-up from industry
Conclusions and recommendations Pockets of expertise on SOI-HBT and related technology exist in Europe but greater engagement with industry is required for any exploitation other than generic training.		

EUROSOI State of the Art Report

Chapter 3. Devices. Fabrication Technology.
Chapter 3.3. RF and Power Devices.
Section 3.3.1. SOI LDMOS RF–Power Transistors

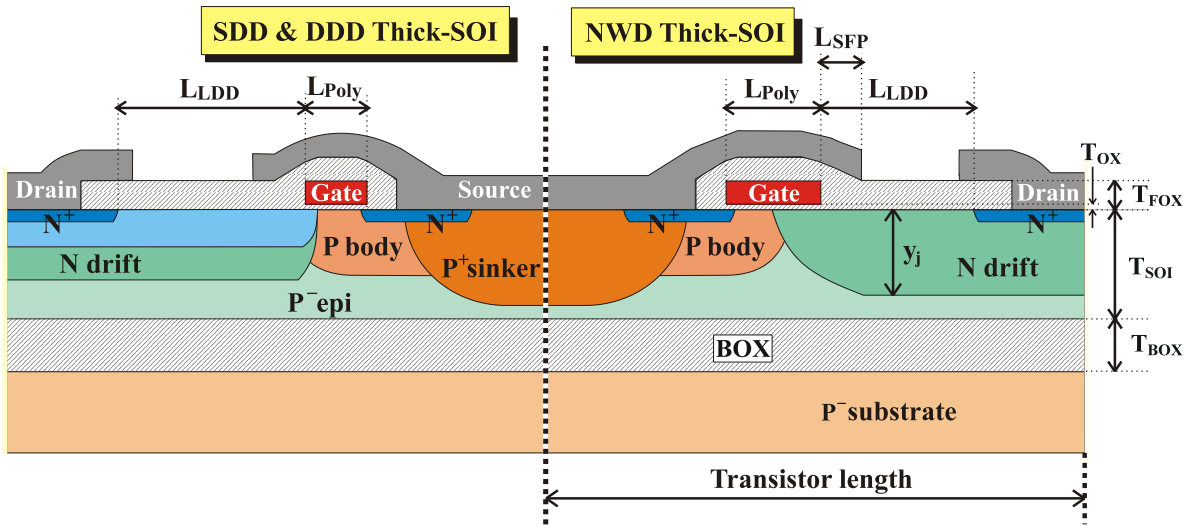
Date of Issue: July – 2009	**Partner: CNM Barcelona**

Abstract

SOI LDMOS transistors are promising for RF-applications, due to potentially better performance and offering higher level of integration. However, European activity in this field is small.

Introduction

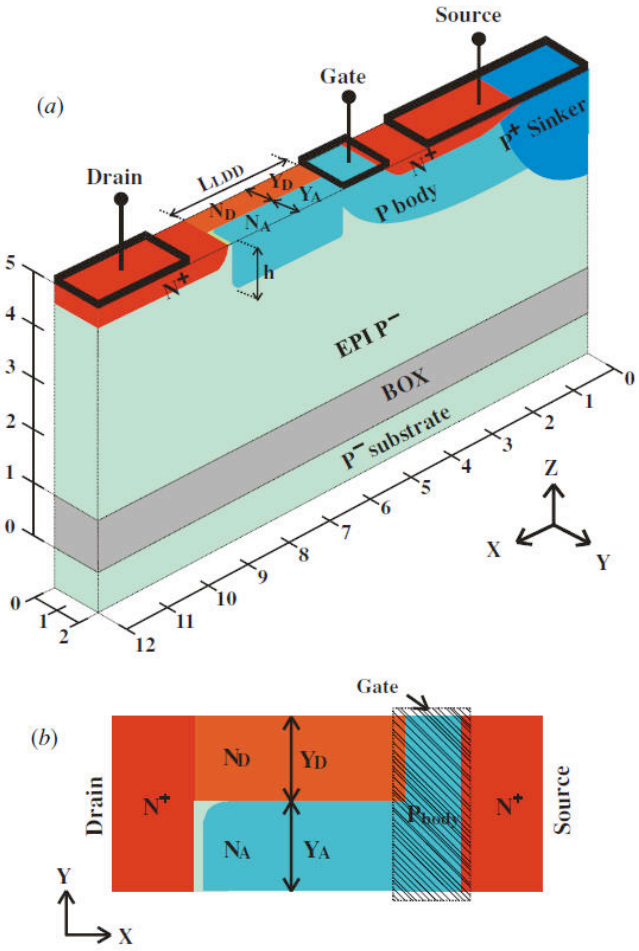
Silicon LDMOS transistors have a dominating position as power amplifiers in base stations for mobile communications. Normally dedicated LDMOS processes are used to produce discrete power transistors.



Advanced SOI LDMOS structures for RF base station Applications with a voltage capability of 80 V.

Today, power amplifiers for RF cellular base stations are implemented with lateral double diffused MOS (LDMOS) transistors due to their good linearity, high power gain, high drain effciency, negative temperature coefficient and low cost.

The need of reduced parasitic elements forces the monolithic integration of the whole RF amplifier in a single chip. SOI technology o□ers a large number of advantages in terms of reduced capacitances, less cross-talk and high integration density. The buried oxide reduces capacitive coupling to the substrate, which improves the power e□ciency, and also provides good isolation between low and high power stages. Finally, SOI wafers with high resistivity substrates allow the monolithic integration of high Q inductors. All these benefits have favoured the fabrication of RF power amplifiers on Thick SOI technology.



Three-dimensional view (a) and top view (b) of a Super Junction thick SOI RF LDMOS structure.

LDMOS transistors on SOI-substrate, on the other hand, have the potential to offer both better RF-performance (especially in terms of power efficiency), but also a higher level of integration, thereby enabling one-chip radio power-modules. Direct comparison between bulk and SOI-LDMOS, show better efficiency for the SOI devices due to reduced parasitics [1]. However, the use of high-resistivity SOI substrates also results in bias dependent RF-performance of LDMOS transistors due to charge inversion/accumulation under the buried oxide [2]. A Korean group has demonstrated an SOI LDMOS/CMOS/BJT technology for integrated power amplifiers used in wireless transceiver applications [3]. The LDMOS transistors had breakdown voltage of 21 V and f_T of 4.5 GHz. A fully integrated 900 MHz power amplifier is implemented with the technology. At an input power of 7 dBm with V_{DD}=5 V and a quiescent bias voltage of 3 V, the output power was approximately 23 dBm, and the IPA provides a power gain of 16 dB and a PAE of 49%.

Simulation studies by different European groups have also shown the benefits of using SOI technology for the integration of discrete power RF-LDMOS transistor [4] addressed to base station applications. The breakdown performance can be significantly improved by the use of appropriate field plate configuration [5] in a Thin-SOI LDMOS transistor with deep doped drift region. In these sense, there are on-going attempts to transfer very successful Bulk-Si LDMOS [6] technology to SOI-substrates.

Recently, a research effort has been focused to the application of super-junction concept to SOI power LDMOS transistors. The better trade-off between on-state resistnace and voltage capability obtained via the implementation of opposite doped columns in the drift region opens a new range of application of Silicon-based LDMOS transistors [7].

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
No significant European contribution as of today **Comments:** Overall rather small activity in the field both in Europe and worldwide	Several European industrial players (Philips, ST Microelectronics) have established RF-LDMOS on bulk, and have the competence to transfer to SOI-LDMOS.	Small industrial and academic activity in Europe.

Conclusions and recommendations

It will be difficult to compete with commercial bulk LDMOS with SOI-LDMOS, unless the performance of the SOI-LDMOS is very much improved. A more realistic opportunity for SOI is to demonstrate RF-power LDMOS integrated with CMOS, which would enable smarter power amplifier modules, both for handset and base station applications.

EUROSOI State of the Art Report

Chapter 3. Devices and fabrication technology
Section 3.4. Optical SOI technology
Subsection 3.4.1. SOI waveguides

Date of Issue: May – 2009	**Partner: Tyndall**

Abstract

Silicon-on-Insulator waveguides have been fabricated using deep UV Lithography and by soft UV-nanoimprint lithography.

Introduction

A consequence of the higher lateral index contrast is that the waveguides become more sensitive to scattering at roughness on the core–cladding interface [1]. Therefore, high-quality, high-resolution fabrication tools are required for these waveguides. For research purposes, waveguides components are traditionally fabricated using e-beam lithography. While this is a very accurate technique, it is a serial writing process, making it slow and unsuitable for mass fabrication.

Alternatively, deep ultraviolet (UV) lithography, the technology used for advanced complementary metal–oxide–semiconductor (CMOS) fabrication, offers both the required resolution and the throughput needed for commercial applications. It has been shown that advanced CMOS technology, and more specificly, deep UV lithography, is capable of fabricating nanophotonic structures. However, technology development for 248, 193, and recently 157 nm is driven by the CMOS industry, and processes are therefore not always suited for waveguides structures. The need to fabricate all structures in a single lithographic step can introduce a considerable mismatch between the different types of components, as the dose-to-target for holes, lines, and other structures can vary. In addition, the dense nature of photonic crystals gives rise to optical proximity effects that are difficult to model. Test structures have been fabricated to experimentally measure optical proximity effects and the necessary corrections to apply on the mask [2]. The deep etching, through both the silicon and the oxide layer, causes a large amount of sidewall roughness. Roughness reduction techniques are needed.

This process has made nanophotonic waveguides of very high quality. For the photonic wires, this translates directly into low propagation losses, as low as 0.24 dB/mm for single-mode wires of 500-nm width. Photonic-crystal waveguides are still considerably more lossy than photonic wires, but 7.5 dB/mm loss in a W1 photonic-crystal waveguide has also been shown [2].
Lower propagation losses have demonstrated, below 4dB/cm for strip waveguides (200nm height and 500nm width) of comparable size around 1.55mm [3,4] . For multi-mode waveguides on SOI, the lowest attenuation 2dB/cm was measured from 7 μm wide and 200nm height waveguides, and the loss increased significantly at widths smaller than 5 μm [5]. Rib waveguides exhibit a lower light confinement by comparison with strip guides. The propagation optical losses in a rib waveguide (1μm wide, 380nm height) are obtained for a value of 0.4 ± 0.3dB/cm at 1.31 mm [6].
Recently, SOI photonic crystals slabs have been fabricated by soft UV-nanoimprint lithography over large areas with sub 100nm feature sizes down to a depth between

100 and 200nm. The nanoimpritning step needed a tri-layer stamp. The results were successfully simulated. Although no loss figures were reported.

On the other hand, photonic sensors have attracted great attention because of their immunity to electromagnetic interference, good compactness and robustness and high compatibility with fibre networks, but also due to the shorter response time and higher sensitivity and stability possible, compared to MEMS/MOEMS devices. Using integrated photonic technologies, it is possible to fabricate very compact, high performing and low-cost chemical and biochemical sensors
The reasons of this great interest in SOI-based integrated optics are related to the possibility to realize waveguides exhibiting low loss (less than 1dB/cm) and high index contrast, the low cost of silicon and wide production infrastructure available for silicon based integrated device fabrication. SOI technological platform has been demonstrated as very attractive in the realization of highly compact integrated optical structures, such as micro-ring and micro-racetrack resonators, Bragg gratings, and Fabry-Perot microcavities.

A silicon nanometer guiding structure, usually referred to as a slot waveguide, is attracting considerable attention. In optical slot waveguides, e.g. fabricated in SOI technology by either e-beam or deep-UV lithography, the electric field discontinuity at the interface between high index contrast materials enables high optical confinement inside a nanometer-scale area (gap region) of low index material (e.g. air, silicon oxide, aqueous solutions, silicon nanocrystals, thermo-optic or electrooptic polymers). This guiding structure can be realized nearing two silicon wires having nanometer dimensions, as in the Figure.

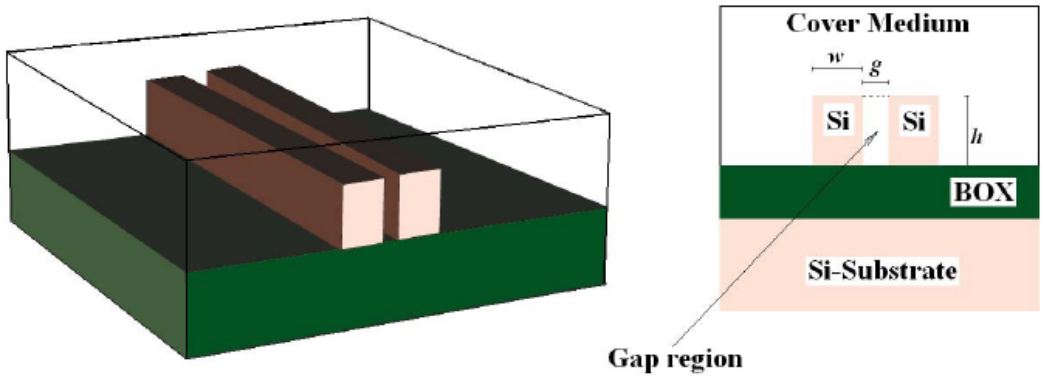

Figure *Slot waveguide typical structure (BOX: Buried Silicon Oxide).*

In the last three years, a great variety of optical devices have been proposed and realized using SOI slot waveguides [8]: micro-ring resonators, disk resonators, optical micro-switches and modulators, nano-mechanical photonic sensors, electrically pumped light emitting devices, directional couplers, all-optical logic gates, multimode interference beam splitters, wavelength demultiplexers, polarization rotators and one dimensional photonic crystals.

The slot guiding structure effective index is very sensitive to changes in the cover medium refractive index. Adopting as cover medium an aqueous solution, whose refractive index depends on the concentration of the analyte of interest (glucose or ethanol, for example), we could observe a waveguide effective index shift due to analyte concentration changes. By monitoring the slot guiding structure effective index in an appropriate integrated architecture (e.g. Mach-Zehnder interferometer, ring resonator, Bragg grating, directional coupler, and so on), it is possible to fabricate

highly sensitive and miniaturized integrated optical chemical sensors [9,10].

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
Leadership: IMEC Contributors: CEA, VTT, Technical University of Denmark COM, CNRS-LPN **Comments:** Main USA competitor is IBM	Compatibility with the CMOS fabrication process. Possibility of using low cost non-traditional lithography is increasing. Potential commercial applications as optical chemical sensing.	Strong demands on fabrication accuracy. Cost. More research in the fast growing field of optical sensing is mandatory.

Conclusions and recommendations

SOI technology has become a major platform for photonic integrated circuits. Several European projects has a particularly interest in waveguide devices. The field is characterized by a strong competition around the world. Cost-reduction strategies are in progress to make this concept development viable. Developments are needed for the optimization of single UV-lithographic step. The EU-Integrated Project "Emerin Nanopatterning methods (NaPa)" is developing alternative nanofabrication methods at wafer scale suitable for photonic crystal components.

Very recently, optical manipulation of nanoparticles and DNA molecules has been

successfully demonstrated in silicon slot waveguides [Yang]. Consequently, the use of slot waveguides in lab-on-achip micro-systems is becoming more and more attractive.

EUROSOI State of the Art Report

Chapter 3. Devices and fabrication technology
Section 3.4. Optical SOI technology
Subsection 3.4.2. SOI based photonic bandgap structures

Date of Issue: May – 2009	**Partner: University College Cork, Tyndall.**

Abstract

We summarise the state of the art on SOI photonic bandgap structures.

Introduction

Photonic crystals (PhC) are attracting attention because of the existence of interesting properties such as photonic bandgap (PBG), i.e. the range of frequencies at which optical propagation is prohibited in any direction and defect mode, i.e. by introducing some defects in PhC, allowed modes appear in photonic bandgaps which are localized within the small volume around the defect. Various types of line defect waveguides can be formed in the PhC's by changing the radius of rods/holes or by removing them completely. These waveguides support true guided modes in the frequency range lying in PBG of photonic crystal. These guided modes are horizontally confined by PBG of the photonic crystal and vertically by total internal reflection because of high index contrast between the slab and the cladding. For symmetric structures in vertical direction, like air-bridge structures, light can be strictly classified into transverse electric (TE) and transverse magnetic (TM) modes or even and odd modes. In such structures PBG for TE mode or even mode can be used selectively. However for asymmetrical structures, like SOI structures, the modes cannot be classified selectively [1].

A frequently used material for realizing such PhC slabs is silicon-on-insulator (SOI) substrates having silicon layer between silicon-dioxide (SiO2) cladding on one side and air cladding on other side. Various PhC components like waveguides, directional couplers, polarizers and polarization splitters have already been realized [2–4] using photonic crystal architecture on SOI substrates. DBWD's are the key components for transmitter receiver devices in bidirectional communication in local area optical networks. 1.31/1.55 lm duplex demultiplexers are also used in fiber-to-home (FTTH) transmission systems and in coarse wavelength division multiplexing (CWDM) systems [5].

Structures with solid support are more realistic than those designs based on air-bridge structures with air cladding on both sides, i.e. the PhC structures are freely suspended in air and hence are mechanically unstable from practical perspectiva. To overcome this instability, SOI based PhC DBWD are designed and developed. In these structures, mechanical robustness is improved by existence of supporting dielectric material under the slab [6].

SOI based PBG structures combine index-guiding in vertical direction with 2D PCs in the plane. Several effects can be used for applications: the PBG can be used for waveguiding, filtering or localising light, while particular dispersion properties allow birefringence, superprism, negative refraction or light extraction effects [7]. These

properties are used for the fabrication of integrated optical waveguides [8], light sources, multiplexers [9] or routers. One can imagine using this technology for an optical clock distribution in advanced CMOS circuits. Furthermore, exploitation of slow light phenomena has potential for realising all-optical switching or all-optical storage. SNOM experiments showed a reduction of the group velocity to approx. c/1000 in a W3 PhC waveguide [10], and active control of the group velocity by localised heating of a PhC waveguide by an integrated micro-heater was demonstrated [11].

A strong point of this technology is the compatibility with CMOS technology and fabrication tools, while a major weakness is the poor light emission properties of silicon-based materials at the moment. Another problem is presented by the important out-of-plane diffraction losses in these structures, but waveguiding losses as low as 2.17 dB/mm were reported [12,13].

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European Contribution on the Field	Current Situation	
European Groups: Leadership IMEC, CEA, COM (Denmark), Max-Planck-Institut Halle **Comments:** Important number of research groups in Europe in this field. International leadership shared with Japan and the USA.	**Strong Points**	**Weaknesses**
	Potentially important for optical interconnect at inter-chip level in CMOS platforms. Compatibility with CMOS technology.	1) Cost of high resolution by top-down methods. 2) Strong demand on the technology for critical dimensions and roughness control.

Conclusions and recommendations

This field of research has emerged recently from the combination of SOI with the new field of photonic crystals, which in 1996 showed its promise at optical wavelengths. Due to the availability of fabrication methods, using existing tools from the microelectronics industry, the field is characterised by a strong competition existing throughout the world where only those with the state of the art in Si nanofabrication working in the optimum mode have a chance to make progress.

EUROSOI State of the Art Report

Chapter 3. Devices and fabrication technology
Section 3.4. Optical SOI technology
Subsection 3.4.3. Hybrid SOI-organic optical structures

Date of Issue: June – 09	**Partner: Tyndall National Institute.**

Abstract

We summarise the state of the art in the area of integrating organic and inorganic materials on SOI platforms, specifically the self-assembly of organic 3D photonic crystals on patterned SOI substrates and related hybrid structures, comprising 2D and 3D photonic crystals architectures.

Introduction

Hybrid optical solutions integrating biophotonic materials with silicon-on-insulator (SOI) Photonic crystals (PCs) allows to enhance the functionality and efficiency of processors scalable to the nanometer regime. Photonic crystals (PCs) present unique optical confinement properties that provide means for reducing photonic device dimensions to keep pace with the persistent miniaturization of integrated circuit components [1]–[3]. Certain biological materials exhibit nonlinearities ideal for exploitation in PC devices.
Active photonic band gap tuning may be explored by subjecting SOI/DNA PC waveguides to electromagnetic radiation, including focused laser incidence [4]. Other soft materials can be considered, especially those exhibiting optically-induced refractive index changes. The soft material deposition method must be optimized for reproducibility, possibly through the use of traditional microfabrication techniques such as evaporation or sputtering.

In hybrid SOI optical structures, the main objective lies in the fusion between silicon-based 2D and 3D photonic structures, i.e. in an on-chip architecture where the coupling and further processing of light from the 3D structures are assisted by the 2D structures, while maintaining compactness and robustness of the components. Here the 2D structures can be, for example, optical waveguides or 2D patterned photonic crystal devices, while the 3D structures are optical cavities of self-assembled opal photonic crystals. In this respect, a novel concept of growth of organic 3D photonic crystals of opal structure on patterned SOI wafers, in basic structures of hexagonal or square shapes has been developed [5,6]. The self-assembled crystals show high homogeneity, and by choosing the medium of the crystals as PMMA, the hybrid structures are well suited as templates for inversion.
One challenge for the future is the patterning of these organic structures by means of electron beam lithography to form cavities and resonators, in which important progress has been reported [7]. Point defects [8] and planar defect layers [9] within 3D photonic crystals have been theoretically proposed and progress towards the realisation of 2D defect layers has been reported [10].
For the inscription of all these defects, self-assembled crystals of high quality are a necessity, both on flat and patterned substrates. Experiments have been performed on patterned wafers with different lateral hydrophilic and hydrophobic characteristics. Opals grown inside the patterns of SOI wafers with features etched down to the BOX layer and with smooth, but otherwise untreated, silicon sidewalls result in the highest

crystalline quality [11].

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Leadership Tyndall: sedimentation of colloids on patterned SOI. VTT: fabrication of suitable SOI wafers. Univ. Mainz: fabrication of electron-beam sensitive colloids.	The processing is scalable up to wafer size level. Colloids can be functionalised for applications other than optical ones.	The technology is just at an early stage. Process compatibility and accompanying simulation work on the integration of components need further development

Conclusions and recommendations

A novel approach that enables incorporation of organic functionalised photonic crystals onto SOI platforms, thus enhancing the prospects of SOI-based nano-photonics, has been demonstrated. Efforts are needed to prove it a viable an scalable technology fully compatible with SOI device fabrication processes. There are several prospects if functionalised colloids can be used for bio-electronic applications.

CHAPTER IV

Devices. Physics.

EUROSOI State of the Art Report

Chapter 4. Devices. Physics.
Section 4.1. Classical SOI MOSFET
Subsections
- **4.1.1. Partially-depleted SOI transistors**
- **4.1.2. Fully-depleted SOI transistors**
- **4.1.3. Ultra-thin SOI MOSFET**
- **4.1.4. Accumulation Mode MOSFETs**

Date of Issue:	**Partner: IME TUW**

Abstract

Partially-depleted (PD) and fully-depleted (FD) SOI MOSFETs are being consolidated as promising alternatives to bulk-CMOS due to their reduced junction capacitance and higher drive current. Especially FD-SOI transistors overcome some of the shortcomings of PD-SOI devices, such as floating-body effects. Compared to double-gate SOI transistors, they are also easier to manufacture.

Introduction

CMOS SOI processes differ from bulk CMOS by the use of an SOI substrate. SOI devices are integrated into a thin silicon layer stacked above a buried insulator, and separated from neighbouring devices by shallow trench isolation. Because each source or drain junction is surrounded by insulators, the junction capacitance is largely reduced as compared to bulk CMOS transistors. Additional oxide isolation considerably diminishes the leakage current as compared with junction isolation. Furthermore, due to the higher saturation current and overshoot effects, SOI devices allow shorter gate delay times than bulk CMOS devices at lower power consumption [1]. Depending on the thickness of the silicon film, fully-depleted (FD), the thinner, and partially-depleted (PD), the thicker, SOI transistors can be distinguished.

4.1.1. Partially-depleted SOI transistors

Partially-depleted SOI devices suffer from floating-body effects, where the potential of the non-depleted silicon body is changed by impact ionization, direct gate tunnelling processes, leading to the so-called kink effect. Special care must be taken if these devices are simulated with standard transport models [2]. Also, the charge on the floating body gives rise to a memory effect which has to be accounted for by circuit designers [3]. A further problem for both FD- and PD-SOI devices arises due to the lower heat conductivity of the insulator, as compared to silicon, which makes SOI transistors more vulnerable to self-heating effects. Body-to-body leakage in stacked devices needs to be further investigated [4]. For thin silicon layers gate-to-body tunnelling arises which may even be beneficial for particular applications [5]. Floating body effect should not be considered as a negative issue of PD transistors: high-performance electronics can take advantage of history effects in the body of the transistors to enhance processor speed by current overshoot in the transistors.

4.1.2. Fully-depleted SOI transistors

Fully-depleted SOI transistors overcome the floating body issues. However, threshold voltage control via channel and polysilicon doping is no more possible in this case, so that undoped channels and metal gate must be employed [6]. Furthermore,

geometrical confinement in the thin silicon layers leads to the formation of subbands in the channel, which calls for novel modelling approaches.

4.1.3. Ultra-thin SOI MOSFET

Ultra-thin body SOI MOSFETs with layer thicknesses in the range of 3.5nm to 4.5nm have been demonstrated [7]. With decreasing thickness of the SOI layer, the electron and hole mobility also decreases compared to bulk CMOS. For SOI layer thicknesses thinner than 4 nm, slight (even atomic-level) thickness fluctuations have a significant impact on the threshold voltage, gate-channel capacitance, and carrier mobility.

4.1.4. Accumulation Mode MOSFETs

Thin-body SOI can operate in accumulation mode [7]. Similar to thin-body SOI FETs in volume inversion mode, the current in accumulation is flowing across the whole Si body, which is beneficial to increase the mobility, reduce the low-frequency noise, reduce the short-channel effects as compared to FDSOI MOSFETs, increase the threshold voltage and avoid effects due to depletion of poly-Si gates.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Basic physics of classical SOI devices mostly represents text-book common knowledge, with contributions from all the groups from all over the world. **Comments:** Although the physics of classical PD, FD, and thin-film SOI devices is well understood, deeper understanding of physical models is required for advanced SOI MOSFET application and novel devices particularly when dealing with ultrathin body devices.	Physical principles driving operation of classical SOI FETs are well understood.	Some leading companies are still adverse to adoption of SOI technology.

Conclusions and recommendations

Fully-depleted SOI devices with ultra-thin (<10nm) silicon layers offer increased performance as compared to bulk CMOS, while overcoming some of the main shortcomings of partially-depleted SOI devices. It is therefore a more promising technique as compared to double- or triple-gate SOI devices which still face major manufacturing technological challenges.

EUROSOI State of the Art Report

Chapter 4. Devices. Physics.
Section 4.2. High Voltage and Power Devices
Subsection 4.2.1. High-Voltage devices

Date of Issue:	**Partner: UGR**

Abstract

Record-setting sRds-on have been reached in thin-film SOI MOSFET by double-RESURF effect. Dielectric isolation allows co-integration of low-voltage logic and up to 1200V switches.

Introduction

The most important aspect for integrated power semiconductors of a given breakdown voltage BVds is a low on-resistance per utilized surface, sRon. In bulk silicon, this value is typically 30 Ω-mm2, due to limitations in electric fields in silicon, impact ionization, and reserve for process spread. Improvements has been reported for nel materials novel materials [2] (GaAs and SiC for their higher critical fields due to larger band-gaps) and novel device architectures [3] (CoolMos™, at the expense of 7 or 9 additional epitaxial and lithography steps). However Philips process permits the use of standard silicon processing equipment with a minimun of masking and processing steps. Additionally, by the use of full dielectric isolation, multiple power devices can be implemented, as required in half – or full – bridge circuit topologies.

Process

The process EZ-HV™ [4] allows implementation of both high-voltage devices such as DMOS, JFET, IGBTs as well as low-voltage control circuitry in 13 masks with double metalization. If needed, 3 additional masks permit utilization of an established 5V CMOS library. Starting material is 1um Silicon-on-insulator (SOI) on top of a 3um buried oxide, with lateral isolation by LOCOS steps. Further options in this modular process are high-side logic (digital circuitry at biases up to positive supply to control and drive power devices) and complementary, p-chanel power components, polycide, and high-temperature compatibility [5].

IGBTs

IGBT and lateral IGBT on SOI need to be further exploited on SOI. LIGBToptimization highlight a superior current capability of LIGBT with the equivalent power MOS. Behavior during temperature reverse bias need to be further investigated [8].

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European Contribution on the Field	**Current Situation**	
European Groups: Leadership: Philips Research USA, Significant Contributor: Philips SC The Netherlands	**Strong Points**	**Weaknesses**
	Lower Rds-on, therefore smaller chip area	Cost, power dissipation, energy efficiency

Conclusions and recommendations

Significant density improvements for power-integrated circuits have been demonstrated for Silicon-on-Insulator. Aditional advantages, such as full dielectric isolation and multiple, independent drains make this process highly suitable for full integration of novel power conversion circuits, such as SMPS, boost-/buck-converters, battery management controllers, and different discharge ballasts.

EUROSOI State of the Art Report

Chapter 4. Devices. Physics.
Section 4.2. High Voltage and Power Devices
Subsection 4.2.2. Power Devices

Date of Issue:	**Partner: CNM-CSIC**

Abstract

Power integrated circuits for 120V, 10A (peak) applications have been realized in thin-film SOI.

Introduction

The first commercial competitive SOI power devices were made in thick-SOI technology [1], [2], which is still competitive for high power automotive [3] applications RF circuitry for base station applications has also been integrated on thick-SOI substrates [4] due to the inherent reduced parasitic capacitances and the high current capability similar to that corresponding to Bulk counterparts.

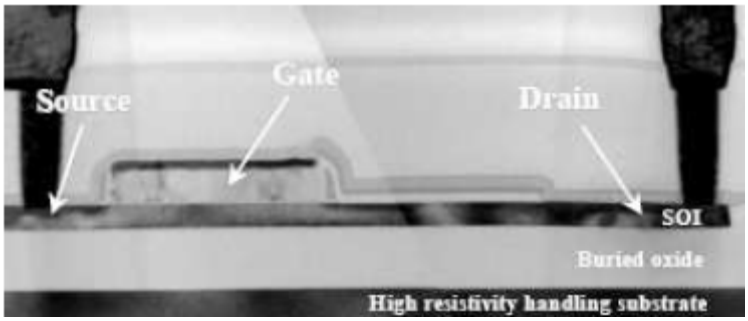
Most of the recent power LDMOS developments are addressed to ultra-thin SOI technologies.

The self-heating effects are accentuated by the submicron nature of the active Silicon layer, thus decreasing the thermal reliability [5]. The small parasitic capacitances due to the coupled effect of ultra-thin active Silicon layer and the buried oxide [6] make this technology appropriated for RF power applications. In addition, an improvement of the passive on-chip inductor's performance with frequency has been proven on SOI [7]. In spite of the SOI advantages, several power LDMOS limitations have to be solved in ultra-thin SOI technology:

- The current capability limitation arising from the substantial reduction of the active Silicon area.
- Voltage capability enhancement through the RESURF principle
- Good body contact not attained with the subsequent increase of the parasitic bipolar transistor's base resistance and the risk of premature breakdown [8].
- The enormous thermal resistance and the self-heating effect [9] which degrades the electrical performances and device reliability (hot spots).

The voltage capability of conventional ultra-thin SOI power LDMOS transistors depends on many geometrical and technological parameters and the device optimisation has to be done according to the final application (RF, automotive, etc.). In thick and thin SOI technologies the voltage capability is proportional to the active Silicon layer (T_{si}). On the contrary, in ultra-thin SOI substrates the vertical impact ionisation is reduced and the voltage capability increases with T_{si} since the avalanche occurs at higher electric fields than the theoretical limit. Therefore a thick enough buried oxide has to be used to sustain the applied drain voltage (80 V need 0.4 μm BOX). Several techniques for controlling the electric field distribution in the drift region doping are used to improve the SOI power LDMOS performances:

- Variation of Lateral Doping via implantation [10]
- Double diffused drift regions [11]
- Source/Drain Field plates [12]

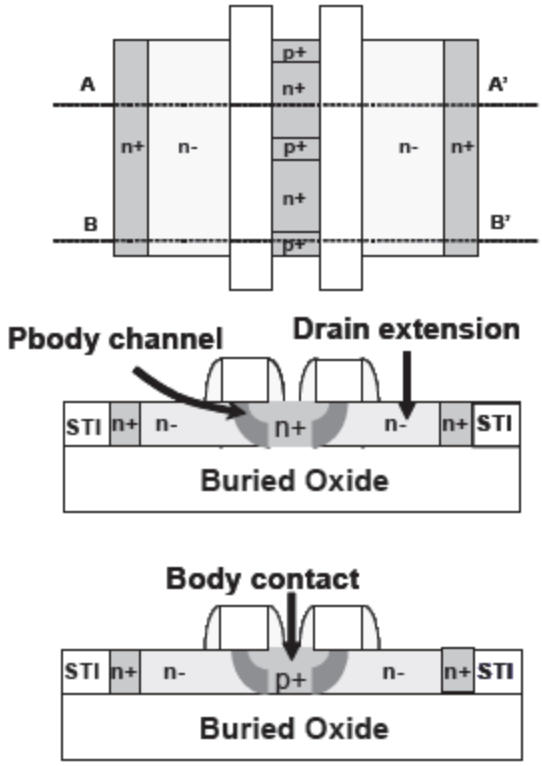


HV LDMOS on SOI

Although the use of ultra-thin SOI technologies is the most promising approach for the future power devices on SOI, other technological possibilities to improve the performance of conventional SOI power devices have been successfully developed but they have not yet been transferred to commercial production due to the process complexity increase and the difficulties for the combination with basic SOI-CMOS circuits. The most relevant technologies are:

- The use of SIPOS layers on top of the drift region was investigated for increasing the voltage capability at the cost of reduced speed [13].
- The Partial-SOI technology based on the patterning of the buried oxide to leave a window beneath the drain of the LDMOSFET which is completely filled with Silicon [14]. Therefore, the voltage is supported across the depletion layer of the device/substrate junction and the heat generated in the active Silicon layer can be more efficiently removed through the backside heat sink. However, this technology is complex and expensive.
- The use of different buried insulator layer with better thermal efficiency in order to decrease the self-heating effects in the active Silicon layer [15]. The combination of SiO_2 and Si_3N_4 is the best option for power devices.

RF power amplifiers is a field dominated by III-V FETs or HBTs but feasibility of RF power MOSFETs fabricated on low-resistivity Si-bulk substrate has been extensively reported in literature [16]. However high resistivity SOI substrate with resistivity in the 1kOhm.cm range is needed for co-integration of the RF-switch [17] and the RF-PA into the RF front-end of a cellular phone. The feasibility of HV-MOSFETs in a 130nm and 65nm thin SOI technologies have been Demonstrated [18].This was achieved by shrinking the electrical length and the gate to drain capacitance. Nevertheless, the gate length cannot be too much reduced and the gate oxide must be kept thick enough for reliability concerns. Body contacts have been used to suppress the kink effect and allow a breakdown voltage *>15V*.



Top view and cross-sections of a HV-MOSFET on thin SOI substrate [19]

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
CNM-CSIC (Barcelona), Philips SC **Comments:** Reliability aspects due to thermal cycling had to be worked out.	Mature Bulk power LDMOS technology and good know-how on SOI power LDMOS device architecture and SOI process technology for feasible future integration in all the available SOI substrates. Integration of RF power amplifiers is feasible with SOI technologies.	Very few research groups in Europe dedicated to power SOI. Current capability limitation and excessive temperature increase.

Conclusions and recommendations

- Renewed European research effort dedicated to power devices for new SOI substrates has to be done.
- The success of future Ambient Intelligence technologies is directly attached to the improvement of power switches on SOI

EUROSOI State of the Art Report

Chapter 4. Devices. Physics.
Section 4.3. RF Devices
Subsection 4.3.1. SOI CMOS RF transistors

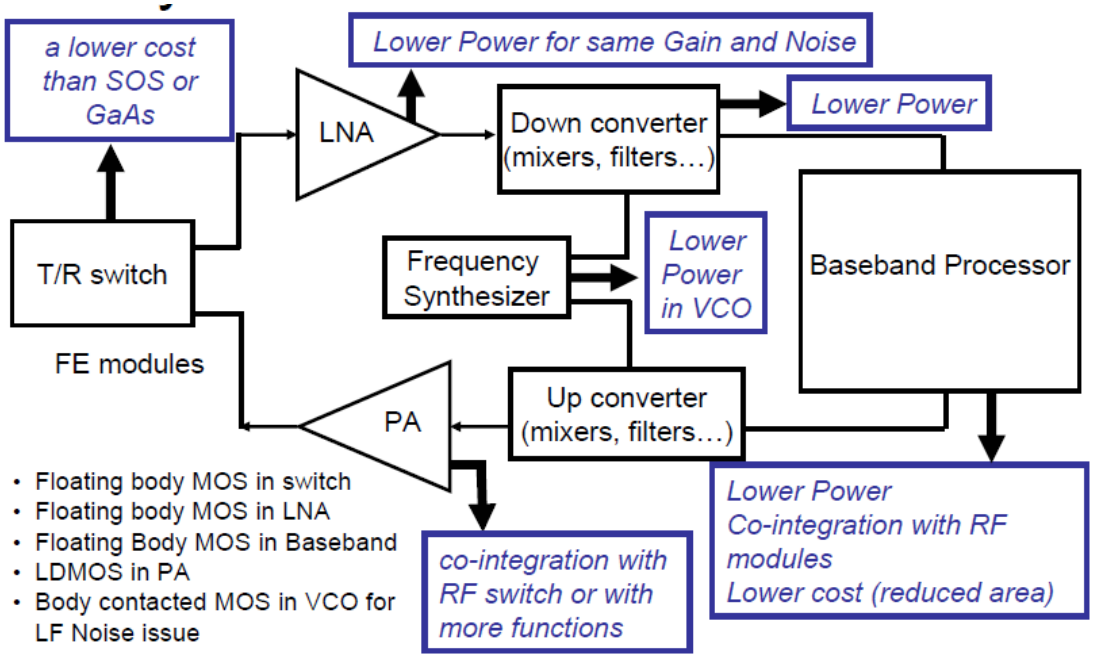
Date of Issue:	**Partner: UGR**

Abstract

This section presents the state-of-the-art SOI CMOS RF transistors.

Introduction

CMOS technology has proven its RF/MMIC capabilities by demonstration of integrated key building blocks from 1GHz to tens of GHz [1-2].



RF communication system integration

However, integration of high quality factor passive RF components and reduction of substrate coupling are difficult on bulk silicon and need special processing and design techniques. SOI CMOS technology is a promising candidate for RF applications due to its lower parasitic capacitance, higher transconductance, smaller short channel effects, reduced substrate coupling, process compatibility and full dielectric isolation for better passive components[3-4]. Due to better scaling capability and lower parasitics, SOI MOSFETs can achieve higher cutoff frequency and lower noise figure, with demonstrated f_t as 243GHz f_t and noise figure less than 0.5dB below 10GHz [5]. Compared with bulk devices, SOI MOSFET shows higher cutoff frequency f_t and higher maximum oscillation frequency f_{max}, as well as lower noise figure (NF_{min}). To further enhance f_{max} which is important for low noise and power applications, T-shape

gate and silicide gate, as well as process optimization of extension region and design optimization of finger number, finger width and folded structure with sharing S/D for multi-finger RF MOSFET are proposed [6-8].

Partially depleted MOSFETs for RF applications.
PD SOI technology now is relatively mature. Yet for RF applications, the inherent floating body effect in terms of kink effect and parasitic bipolar effect may cause intrinsic gain reduction due to the output conductance decreasing, 1/f noise overshoot and linearity degradation due to output conductance nonlinearity and thus the abnormal transconductance distortion[9], [10]. For SOI MOSFET with short channel length and thin gate oxide, linear kink effect (LKE) and thus similar noise overshoot can be observed at high gate voltage and low drain voltage. The overshoot 1/f noise can be up-converted to high frequency and may lead to the higher phase noise of the circuits, such as oscillators. Although body contact technique can be adopted for kink effect alleviation, the additional body resistance may still cause dynamic floating body and increase the high frequency noise level [11]. Specific circuit topology design is another effective way to alleviate noise overshoot problem.

Thin film fully depleted MOSFETs for RF applications.
Thin film fully depleted SOI technology is more promising for future RF circuits due to the reduced body effect, reduced kink effect and nearly ideal gm/Id. Yet the front-back gate coupling effect may cause different 1/f noise behavior. It has been found that for short channel SOI devices, due to the LKE, back interface accumulated device can has higher 1/f noise [12]. On the other hand, AC kink effect is observed in FD SOI device due to the AC hole current as a dominant discharging current flowing through the source-body junction at high frequency [13], which may also cause noise overshoot. It competes with the diode leakage current. Proper channel design can be utilized to suppress the related influence. Other concerns of FD SOI devices include thin film thickness fluctuation and buried oxide impact on the matching behavior and leakage current. Better solutions are still being found [14]. Scaling is the effective way for high performance devices, as well as SoC integration. However, the conventional digital scaling can induce reduction of output resistance and gain. Thin gate dielectric may degrade the noise and matching behavior. Reduced supply voltage may result in small voltage swing and shift of the working point. So low threshold voltage device is expected while maintain reasonable leakage, which leads to a great challenge to device and circuit design. Novel devices with better RF scaling capability are still expected. Maybe double gate device is a better candidate for the low voltage RF circuits due to higher transconductance and higher gain. But it seems still to have matching and design margin problem. This needs further deep investigation for future RF technology.

Substrate coupling in SOI CMOS technology.
CMOS technology has demonstrated capabilities for RF/MMIC applications even to tens of Giga Hertz, the next goal is to integrate delicate RF front-end with the large scale “noisy” digital circuits on the same die. Substrate coupling is one of the obstacles for fully system integration. Experimental results show that the spectrum of substrate noise concentrated below 1 GHz, rather than extended to several GHz range when the clock frequency was high enough [15-16]. Random logic gate activity of the digital circuit generates intense substrate noise from DC to 500 MHz. Thus the low frequency substrate noise is dominant in substrate coupling. To suppress such substrate noise, SOI unique structure has inherent superiority to bulk silicon [17]. However, due to the SOI technology cost and market requirement, the above-mentioned efforts for practical fully integration with SOI technology is still insufficiently taken. So far no fully integration of RF and digital circuits in SOI technology is reported. On the other hand, substrate noise is also an issue for fully integrated RF circuits. When the power

amplifier and VCO are integrated on the same chip, the large signal from power amplifier will inject into substrate and push and pull the operating frequency of VCO. For this substrate noise, both SOI buried layer and deep N well are almost “transparent”. For bulk CMOS technology, this is very difficult to tackle except careful layout. However, SOI CMOS technology can resort to high resistivity substrate to alleviate this problem.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
CEA-LETI (Grenoble) STMicroelectronics (Crolles, France)	• Incorporate RF capabilities with microprocessor. • Better RF passive compo-nents • Reduced substrate losses • Better isolation	• Uncertainty around take-up from industry • Cost

Conclusions and recommendations

From the point view of technology, SOI have many advantages over conventional CMOS. However, the wireless communication market is benefit driven, so the higher cost of SOI wafers is the biggest obstacle for mass production of SOI RF circuits. Compared with SOI technology, bulk CMOS technology has much more design productivity gaps to be filled for RF and SoC integration. But presently it seems that the expenses for the gap filling efforts are acceptable in comparison with the cost of SOI wafer. SOI is the solution for today Applications (3-10GHz range), and the most promising solution for emerging Applications at higher frequencies
(60 GHz WLAN…etc) .Yet for future development of higher frequency circuits, SOI technology may exhibit more and more distinct advantages over bulk technology.

EUROSOI State of the Art Report

Chapter 4. Devices. Physics.
Section 4.3. RF Devices
Subsection 4.3.2. SOI bipolar transistors

Date of Issue: Nov - 2005	**Partner: LIVUNI**

Abstract

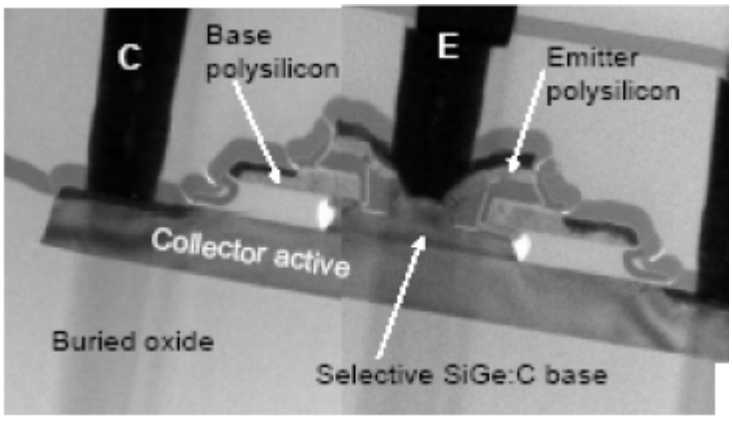
This section presents the state-of-the-art SOI bipolar transistors in vertical and lateral design, particularly focusing on SOI SiGe HBT technology.

Introduction

This section lists the main contributors and the state-of-the-art results concerning heterojunction bipolar transistors (HBTs) on SOI in both vertical and lateral design. European groups contribution is highlighted.

SiGe HBTs on SOI

SiGe HBT on SOI technology (§-§) allows the complete dielectric isolation of the device. This approach reduces parasitic capacitance to substrate, leakage currents, and device size. The SOI substrate eliminates parasitic substrate transistors and latch-up and has the ability to reduce crosstalk §, particularly when combined with buried groundplanes §. These benefits make SiGe HBTs on SOI attractive for mixed signal RF applications.



Bipolar technology on thin SOI, C Raynaud CEA-LETI

Hitachi § has developed SOI/HRS SEG SiGe HBT/CMOS technology, which aims at producing active and passive components for wireless communication systems and optical-fibre-link systems. The SOI is based on a high-resistivity substrate (SOI/HRS). High performance HBTs, CMOS devices, poly-Si resistors, varactors, MIM (Metal-Insulator-Metal) capacitors, and high-Q octagonal spiral inductors were fabricated on a 200-mm SOI wafer using the technology that combines 0.2- μm self-aligned SEG SiGe HBTs with CMOS transistors. SiGe HBTs with shallow-trench isolations (STIs) and deep-trench isolations (DTIs) and Ti-salicide electrodes exhibited high-frequency and high-speed capabilities with an f_{max} of 180 GHz and an ECL-gate delay of 6.7 ps, along with good controllability, reliability, and high yield.

NEC has reported §60 GHz cuttoff frequency super self-aligned selectively grown SiGe-base (SSSB) bipolar technology, which was developed for application in 20-Gb/s optical transmitter IC's. The SSSB transistors with a BPSG (boron-phosphosilicate glass) filled trench were fabricated on a bonded SOI substrate. The transistor region is isolated so that it is completely separated from the neighbouring transistors and from the supporting substrate by dielectric films. An AlSiCu/TiN/Ti silicide electrode structure was used for ensuring the IC's reliability at a higher current density operation. A bond-and-etchback SOI substrate, which consists of a 1.5- μm thick SOI layer and a 0.5- μm thick buried oxide layer, was used. Ion-implantation of arsenic atoms and thermal diffusion were carried out to form a buried sub-collector. A collector epitaxial layer was grown using a conventional LPCVD (Low Pressure CVD) epitaxial technique. The SiGe intrinsic base layer was formed using the self-aligned SEG technology, with a trapezoidal profile for Ge. An emitter 0.4 μm wide was used to reduce the parasitic capacitances and base resistance. SiGe bipolar IC's for an optical transmitter, such as a selector, a multiplier, and a D-type flip-flop, were made using this technology and confirmed its applicability to high-frequency operation.

At IBM the concept of fully-depleted-collector has been used to produce polysilicon-emitter SiGe-base vertical bipolar transistor on SOI§. The transistor operates on the principle that the collector region is fully depleted so that the charge carriers travel laterally towards the collector reach-through and contact after traversing the intrinsic base layer. The SOI silicon layer thickness is comparable to that used in SOI CMOS, and no sub-collector layer or deep trench isolation are required. The transistor is demonstrated in a polysilicon-emitter SiGe-base npn implementation on SOI with a 140-nm silicon layer. This SOI device has the advantage of a higher base-collector breakdown voltage (4.2V) to cut-off frequency (60 GHz) trade-off and facilitates higher voltage applications not attainable by non-SOI bipolar transistors. Projected f_T for a scaled 100 nm device on 55 nm SOI is found to approach 200 GHz §. The results also suggest the possibility of integrating high-performance vertical bipolar transistor and SOI CMOS on the same chip.

A UK consortium comprising the Universities of Liverpool, Queen's Belfast, Southampton, Surrey, and the Imperial College (with industrial partners) is conducting research into SOI HBT technology § and has come up with a number of novel solutions. The bonded wafer technology has been developed to allow incorporation of buried silicide layers both above § and below § the buried oxide. The upper silicide layer produces a low collector resistance and the layer below the oxide has been shown to reduce drastically the coupling of noise from device to substrate. A 20 dB reduction in crosstalk was realized with this technology§. The collector currents of SiGe transistor are enhanced by a factor of 31 over that of a Si transistor §. The self-heating problem of HBTs has been addressed by the incorporation of thermal vias. Thermal via variants incorporating oxide, nitride, and undoped poly-Si have been investigated.
Bonded SOI wafers for this work comprise of a 1 μm buried oxide layer with the surface Si layer thinned to a nominal thickness of 1.5 μm. Deep, poly-Si filled trenches provide isolation through to the buried oxide layer. The patterned SOI layer is used to provide the heavily doped buried collector as well as the crystalline seed layer for subsequent epitaxial layer growth of the silicon collector and SiGe base layers. The transistor layers are grown using SEG for the Si collector, followed in the same growth step by non-selective epitaxial growth (NSEG) for the SiGe base (nominally 12% Ge) and the n-Si emitter cap§. The advantages of this approach are that the basic transistor structure is grown in a single epitaxy step and the growth interface is kept away from the transistor active regions. Note that fully optimized HBT BiCMOS would

require thinner buried oxide to obviate short channel effects (SCE) for the CMOS parts. The ability to realize a buried ground plane provides a major advantage in suppressing SCE associated with drain fringing fields for decananometer MOS transistors. The main additional advantage for the SOI HBT technology discussed here is the EMC (Electromagnetic Compatibility) screening offered by the buried silicide ground plane, which can be integrated with the buried oxide.

Silicide SOI HBT concept

Collector resistance is a key issue in SiGe HBTs on SOI, and buried silicide layers have been proposed § as a solution to this problem for a variety of device applications. Key features of the technology are the inclusion of a buried silicide layer above the buried oxide layer for reduction of collector resistance, and a buried silicide groundplane (GP) below the buried oxide layer for crosstalk suppression §. The n+ buried layer is needed in the SSOI process to prevent the formation of a Schottky contact between the buried silicide and the silicon collector. The technology also features complete dielectric isolation of the transistor island using a combination of deep trench isolation and the buried oxide layer. There are three process options for the SOI collector structure §: (i) the SOI collector with an n+ buried layer (SOI) §, (ii) the Silicide SOI collector with a buried silicide layer (SSOI), and (iii) the SSOI collector combined with a buried silicide groundplane (GPSSOI).

In the silicide SOI process it is advantageous to have a thermal oxide as the buried oxide layer. Resistivities as low as 50 μΩcm were achieved for the buried silicide layer for a bond anneal of 120 minutes at 1000°C §. These results indicate that the buried tungsten silicide layer does not have a serious impact on junction leakage. Moreover, it has been found recently § that the silicon layer and the buried dielectric in the SOI structure are not compromised by the inclusion of the buried silicide, which establishes the GPSOI substrate as a leading contender for crosstalk suppression in future generations of mixed signal circuits on SOI substrates.

SiGeC HBT on a thin film SOI (STMicroelectronics and Bordeaux University, France)

A compact self-aligned SOI SiGeC HBT structure has been developed by STMicroelectronics and Bordeaux University, France. The device uses the self-aligned selective epitaxy emitter/base module. The SOI substrates feature a 160 nm silicon layer on top of a 400 nm buried oxide (BOX). In this design, a short distance is obtained between the collector contact regions and the centre of the emitter window (L_C), which limits performance degradation due to collector transit time or series resistance effects. No base contact is placed between emitter and collector contacts to minimize L_C. The base is contacted in a different plane, and a cellular layout (C_BE^BC) is employed to avoid excessive access base resistance. The fabrication of the device requires the addition of only four masking steps to the 0.13μm SOI CMOS process. The f_TxBV_{CEO} products above 200GHz·V are obtained along with remarkable HF performance (f_T/f_{max}=102GHz/154GHz). Even larger values of f_TxBV_{CEO} product are expected to result from an optimization of the SiGeC base profile towards a reduced current gain. This is the first demonstration that very high speed SiGeC HBTs can be fabricated on thin film SOI substrates.

Lateral SOI bipolar transistors

The progress in SOI technology and the advent of deep sub-micron lithography have contributed to the resurgence of interest in lateral bipolar transistors (LBTs). SOI technology is readily adapted for use in LBTs due to its capabilities to overcome the main difficulties namely, (i) definition of a lateral thin base, (ii) definition of a fully aligned base contact, and (iii) device isolation. The formation of a thin base can be achieved by spacer techniques, dopant diffusion, and novel angled ion implantation.

The-state-of-the-art lateral bipolar transistors on thin film SOI are fabricated by

Toshiba based on the spacer technique. With a small emitter size of 0.12x3.0 μm^2, a low base resistance of 270 Ω due to a novel Co silicided base electrode, and low base-collector parasitic capacitances of 1.4 fF due to SOI material, the device achieved the f_T=12 GHz and highest f_{max} of 67 GHz among the lateral SOI bipolar transistors. The emitter, intrinsic base, and collector region are laterally formed in thin-film SOI. The key point of the proposed technology is a base formation that has two notable features: (i) the silicided p+ polysilicon base electrode in order to reduce base resistance; (ii) very short single crystalline link base region that is formed in the side surface of base electrode in order to connect the intrinsic base and the external base electrode.

CMOS-compatible LBTs on SOI has been recently reported by the University of Toronto (Canada) with Asahi Kasei Microsystems (Japan). This technology requires polysilicon side-wall-spacer (PSWS) structure, and only five lithography masks to realize high-performance LBTs. Notably, the external base width is not limited by photolithography, and a minimum width of 0.1 μm is achieved. This novel PSWS design greatly reduces parasitic capacitance that translates into higher frequency performance. The experimental f_T/f_{max} of the high-speed device are 17/28 GHz (second highest), and, for the high-voltage device, the measured f_T/f_{max} of 12/30 GHz and BV_{CEO} of over 25 V produces a Johnsons product well above 300 GHz·V. This low cost bipolar structure is suitable for SOI-CMOS integration, and an ideal BiCMOS process for future RF SoC (system-on-chip) application.

The highest collector breakdown voltage for a Schottky collector bipolar transistor (SCBT) has been demonstrated by the Indian Institute of. The structure has a low doped base at the collector side and a high doped base at the emitter side, and also an extended buried oxide below the Schottky metal-base region. This design allows significant improvement in collector breakdown voltage, which is about 12 times higher when compared with the conventional thin film lateral SCBT on SOI. The improvement in breakdown voltage is due to the spreading of the electric field away from the Schottky collector metal-base interface into the depleted low doped base and due to the suppression of vertical breakdown at the Schottky metal-buried oxide interface by the extended buried oxide. The proposed structure is expected to have wide applications in the design of high voltage, high speed SOI SCBTs for the new generation analogue circuits.

Lateral SOI SiGe HBT (Southampton University)

§One of the problems of applying SiGe technology to lateral bipolar transistors is finding a suitable method to incorporate germanium into the base. The epitaxial lateral overgrowth (ELO) and confined lateral selective epitaxial growth (CLSEG) are two possible techniques. CLSEG has been successfully applied by the University of Southampton § using cavities built into SOI substrates. LPCVD has resulted in lateral growth of up to 1 μm with good selectivity and epitaxial quality. This technique allows very thin lateral SiGe layers to be formed, enabling the fabrication of lateral heterojunction devices. The simulation results have shown that the lateral SOI SiGe HBT can achieve a maximum f_T of 22 GHz at 34 μA, and an f_{max} of 14 GHz. Maximum current gain was found to be 95. Simulation (the University of Waterloo, Canada and Southampton University, UK) §§have showed that with a germanium concentration of 10% and an overall base width of 100 nm, the lateral SiGe HBT could have a peak f_T of 33 GHz and a peak f_{max} of 160 GHz. Furthermore, simple extrapolation to smaller lithographies and SiGe HBT technologies with higher intrinsic f_T's reveals that a lateral SiGe HBT discussed in § has the potential to exhibit an f_{max} in the neighbourhood of 500 GHz using 0.1 μm lithography at significantly lower bias currents compared to vertical SiGe HBT technology. These devices would represent a new class of ultralow power high-frequency silicon-based transistors.

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European Contribution on the Field	Current Situation	
European Groups: Significant Contributor: UK consortium Leadership: Queen's University Belfast, UK Significant Contributor: Southampton University, UK STMicroelectronics and Bordeaux University, France **Comments:** Novel concepts have been introduced, such as SSOI and CLSEG (UK). Bonded SOI SiGe HBT established (UK). SOI SiGeC HBT fabricated (France).	**Strong Points** ■ Collaborative projects on bonded SOI SiGe HBT ■ SSOI process established ■ CLSEG process established (lateral SOI SiGe HBT) ■ SOI SiGeC HBT	**Weaknesses** ■ Lack of continuity ■ Uncertainty around take-up from industry

Conclusions and recommendations

There is core expertise and competence distributed across a number of universities with an established platform technology to realise SOI-HBT, including the incorporation of buried silicide. Some novel solutions to issues such as buried ground planes for crosstalk, mitigation of self-heating with thermal vias, have been demonstrated. Some of the solutions are relatively expensive but the work is ready for exploitation if niche, value-added applications can be identified.

EUROSOI State of the Art Report

Chapter 4. Devices. Physics.
Section 4.4. SOI MEMS.
Subsection 4.4.1 MEMS processes

Date of Issue: Oct - 2005	**Partner: X-FAB Semiconductor Foundries / LETI**

Abstract

This report shows the state of the art of the MEMs activities in Europe. European teams are highlighted.

X-FAB is a pure play foundry for mixed signal CMOS/BiCMOS technologies. Beside the CMOS/BiCMOS technologies X-FAB offers also MEMS processes. One of these MEMS processes is a SOI wafer based surface micro machining technology.

Introduction

During the last 20 years, we have observed a continuous increase of the number of industrial companies coming to research labs to develop smaller and cheaper products. This has been the case for accelerometers, pressure sensors, force sensors, gyrometers, fingerprint sensors, microswitches, ink jet print heads or magnetic recording heads. Thanks to the mixing between non standard and specific techniques such as anisotropic etching and multi wafer assembly (like wafer bonding), a lot of mechanical structures have been proposed. The merits of this material are numerous: large physical effects for detection (piezoresistivity, photoelectric effect, Hall effect, …), single crystalline material for high mechanical quality structures, well known technology for lower cost and large research effort for future development. The use of SOI wafers is likely the best way to overcome the remaining issue. Among the main advantages, we can note: the microelectronic technology compatibility, batch process for anisotropic chemical etching, mechanical quality of the single crystalline material, silicon superficial layer to realize either the transducer (strain gauges), or the surface microstructure and sacrificial layer electrically insulating and chemically selective. The top silicon layer thickness can be easily adjusted (by epitaxy for example), depending on the application (strain gauges or surface micromachined structures). The use of SOI can also significantly reduce the junction leakage current that strongly limits the efficiency of the sensor for temperature above 120°C.
Most of the MEMs activities on SOI are pursued at XFAB ([1]), Tronics Microsystems, EPFL, CSEM, Colibrys and LETI ([2-6]).

X-FAB started the development of first bulk micro machined MEMS processes for pressure sensors in 1995. In the last years a lot of X-FAB standard technologies and customer specific processes were installed in the production line, which is prepared for high volume applications. X-FAB is able to integrate CMOS and MEMS technologies on one chip. The monolithic integration is already realized for relative and absolute pressure sensors. One of the X-FAB standard technologies is a thick-SOI-wafer based surface micro machining technology for inertial sensors. The sensor elements are variable capacities, which are formed by anisotropic and isotropic plasma Silicon etch processes. The free movable and sensitive sensor elements will be hermitic capped

on wafer level by a cap wafer. This allows the use of standard plastic packages by the assembly process of the Silicon device. The technology has the potential for the integration with X-FAB CMOS technologies.
Recently, LETI and FREESCALE jointly developed a new technology that combines high aspect ratio SOI surface micromachining with polysilicon packaging and a new nitride anchor process with robust release etch manufacturing margin.
Regarding research activities, only one European project is dedicated to MEMs (to our knowledge): MIMOSA project, leaded by ST. This project (started in 2004) has a complete workpackage focussed on an SOI platform for embedded MEMs. This project involves the main actors in MEMs in Europe, and initiates the research in the field of NEMs devices where LETI is the main contributor (with thin SOI substrates).

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
X-FAB is partner in several international projects, which are funded by the EU LETI: Significant contributor EPFL: Significant contributor CSEM: Significant contributor Colibrys: Significant contributor Tronics: Significant contributor	■ Leading edge technology ■ A lot of research labs involved	No international standards regarding long term reliability

Conclusions and recommendations

A lot of research labs are involved in MEMs activities on SOI, with some interactions between some of them (for example: LETI and CSEM, with Tronics). It would be very useful to have a european project focussed on NEMSs devices.

X-FAB's SOI technologies for MEMS applications were developed for high volume applications in the automotive, industrial, aerospace and medical industries. First level of design kit is available.

EUROSOI State of the Art Report

Chapter 4. Devices. Physics.
Section 4.4. SOI MEMS.
Subsection 4.4.2 Ultra-thin SOI nano-accelerometers.

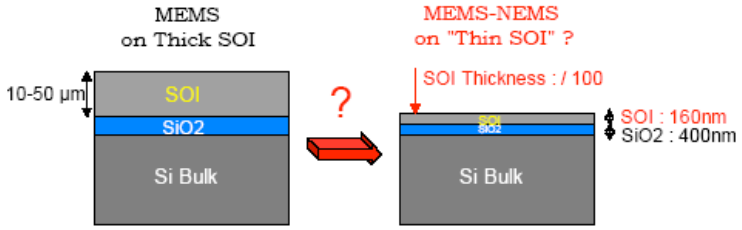
Date of Issue: Dec - 2005	**Partner: CEA-LETI and ST Microelectronics (Crolles)**

Abstract

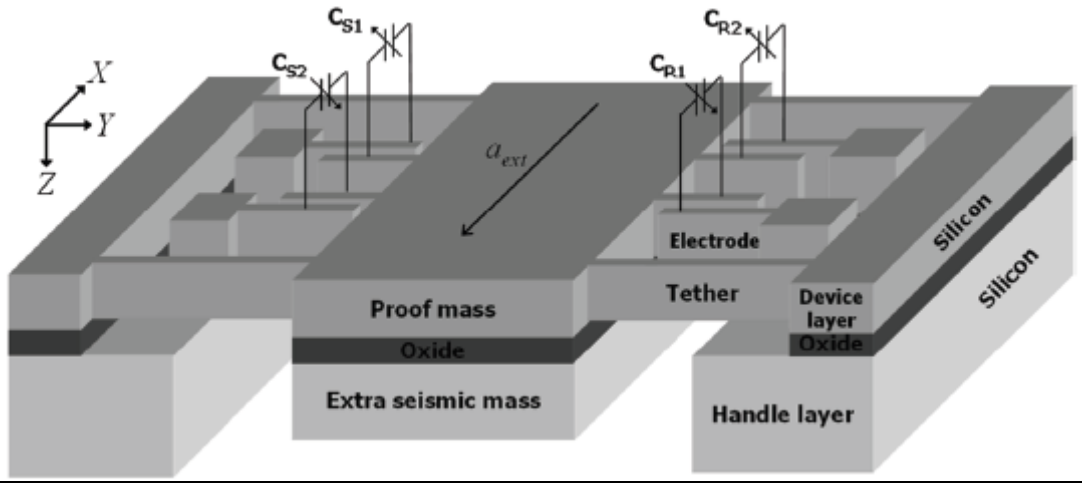
Feasibility demonstration of thin SOI MEMS accelerometers is demonstrated in the framework of MIMOSA project.

Introduction

Nowadays, MEMS accelerometers are usually fabricated with surface micro-machining on thick SOI wafers (SOI thickness : a few µm - 50 µm). With “thin SOI” wafers, the SOI layer thickness is 160 nm, which means that the thickness has been divided by a factor 100 (Figure below). In addition the oxide layer is also very thin (400nm):



In order to carry out the feasibility demonstration, the work has been focused in the first step on basic MEMS structures (cantilever beams, clamped beams, combs…) and on accelerometers using a well-known detection principle: capacitive detection. Because this preliminary work is only a feasibility demonstration, a first choice has been to address 10G and 50G full scale ranges and 100Hz bandwidth. In the future, other acceleration ranges will benefit of the developments made for 10G and 50G accelerometers. Two configurations of capacitive accelerometers have been studied: in-plane and out-of-plane capacitive accelerometers.



Schematic diagram of an SOI accelerometer with added seismic mass

To conclude on the technological point of view, results obtained during technology evaluation show that the fabrication of "thin SOI" MEMS is feasible. This fabrication requires hybrid technology (e-beam + DUV photolithographies) for In-plane configuration and also FH-vapor release technique. The figure presented below shows that the mechanical structures necessary for N-MEMS devices, in particular for "thin SOI" accelerometers, can be fabricated. As a consequence, we can consider that the feasibility demonstration is obtained. The results presented here show that the technological feasibility of first "thin SOI" accelerometers is demonstrated. This conclusion is based on the work carried out in modelling-design and technology evaluation. 50G and 10G accelerometers with In-plane and Out-of –plane configurations have been designed by taking into account specificities due to "thin SOI" approach and some non traditional phenomenon occurring in the nm scale. In addition, the technology evaluation and the fabrication of elementary N-MEMS structures have shown that the use of hybrid lithography (E-beam + DUV) and FH-release technique enables the fabrication of the elementary structures necessary for the fabrication of "thin SOI" accelerometers. Based on the results obtained, the fabrication of first "thin SOI" accelerometers is on progress: the masks (200mm facilities + hybrid lithography) and the process flow are ready. In addition, other complementary works are on progress: characterization, definition of thin film packaging and requirements for electronic. Next objectives are the fabrication and characterisation of 1st generation thin SOI accelerometers, based on results obtained in and development of an experimental set-up adapted to the characterisation of thin SOI accelerometers.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
ST–Microelectronics (Crolles, France) EPFL CEA-LETI EU-MIMOSA project.	Compatibility with the CMOS fabrication process, and standard optical lithography.	Cost. High loss.

Conclusions and recommendations

Feseability of MEMs (resonators, accelerometers) based on thin SOI films has been demonstrated. Co-integration of MEMs technology and transistor processing at the same time has been demonstrated.

EUROSOI State of the Art Report

Chapter 4. Devices. Physics.
Section 4.4. SOI MEMS.
Subsection 4.4.3 Bulk-mode SOI MEM resonators.

Date of Issue: Dec - 2005	**Partner: EPFL and ST Microelectronics (Crolles)**

Abstract

We summarize here the state of the lastest developments on SOI MEM resonators.

Introduction

Latest developments in the field of RF devices and systems show a constant trend towards the miniaturization & integration of the reference oscillator. A large part of the efforts are focusing on silicon or Silicon-On-Insulator (SOI) micro-electro-mechanical (MEM) resonators which promise to be a viable alternative to stable but bulky quartz crystals, due to their compactness, design flexibility and potential CMOS co-integration. A particular focus has been set on bulk-mode MEM resonators, using length-extensional modes [1]. Frequencies of more than 1GHz and very high quality factors are demonstrated, as well as low air-sensitivity of the quality factor.

SOI CMOS MEM resonator

A very simple, CMOS compatible fabrication sequence using only one mask is used to obtain SOI MEM resonators with 1μm-wide transduction gaps [2]. Both the resonator and the electrodes are structured in mono-crystalline silicon, resulting in low stress of the final released device, and thus avoiding unwanted structure bending. Electrical measurements of the fabricated resonators show quality factors in vacuum as high as 18,000 at 80 V biasing voltage and RF power of -10 dBm.

However, in order to avoid the use of such large DC bias voltages as well as to reduce the motional resistance in the range of few kΩ, nano-scale transduction gaps (<200nm) are essential. It is also important to obtain thick resonators, in order to lower the phase noise, so high aspect-ratio gaps are needed. For this purpose, a new technological process has been developed [3], which employs only standard optical lithography with 1μm resolution and IC-compatible processing steps.

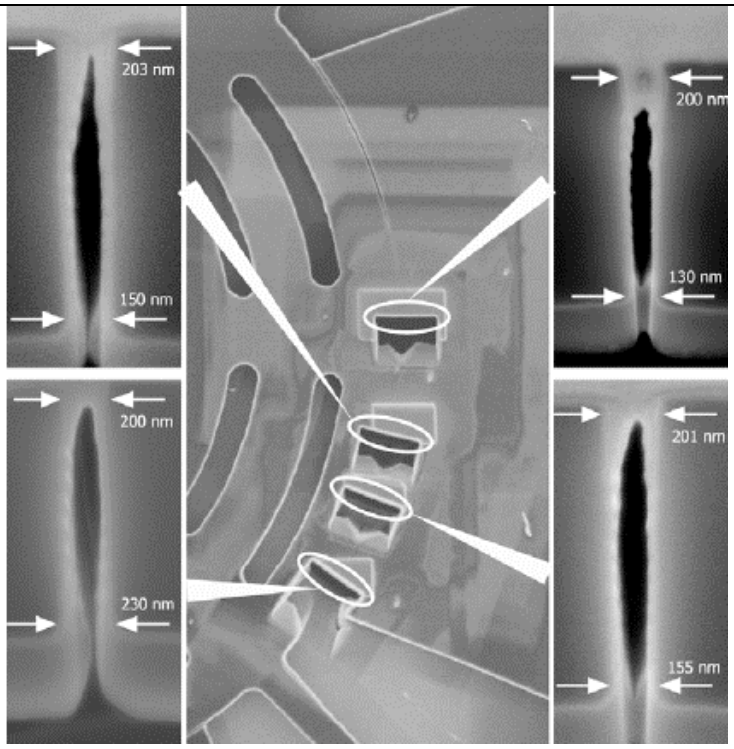

Fig. 1. Bulk-mode MEM Resonator with 200nm transduction gaps

Figure 1 shows the SEM picture of a bulk-mode MEM Resonator. Operation frequency is 31MHz with Q>20.000.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
ST–Microelectronics (Crolles, France) EPFL EU-MIMOSA project.	Compatibility with the CMOS fabrication process, and standard optical lithography.	Cost. High loss.

Conclusions and recommendations

Feseability of MEMs (resonators, accelerometers) based on thin SOI films has been demonstrated in the framework of MIMOSA project. Key role re power saving and new functionality.

EUROSOI State of the Art Report

Chapter 4. Devices and Physics
Section 4.5. Optical SOI waveguides
Subsection 4.5.1 GAA MOS capacitor light modulators

Date of Issue: Feb-2010	**Partner: EPFL and ST Microelectronics (Crolles)**

Abstract

We summarize here the state-of-the-art of Gate-All-Around MOS capacitor light modulators, based on plasma dispersion in silicon.

Introduction

Silicon on insulator has proven to be an excellent technology for on-chip light guiding due to the high index contrast between silicon and the cladding (air or oxide), which makes very tight bends possible. This opens up new opportunities for the fabrication of integrated on-chip signaling systems, compatible with CMOS electronics. One of the key-components for an optical signaling scheme is a light modulator. We have proposed and validated the concept of a silicon light phase modulator based on a Gate-All-Around MOS capacitive structure. Such a device combines the high efficiency of a pin-diode approach with the speed advantage of capacitive operation. The limitation of this concept is mostly in terms of greater optical losses, and therefore this approach requires the use of a resonant structure for intensity modulation rather than a Mach-Zehnder implementation. Figure 1 shows a possible schematic architecture of an on-chip optical clock distribution based on silicon nanowires and GAA light phase modulator. In figure 2 a detailed view of the GAA capacitor for light phase modulation is shown.

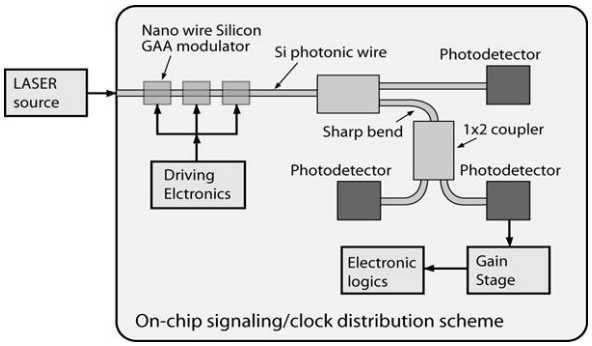

Fig. 1: Schematic of on-chip optical clock distribution vision, using a GAA MOS capacitive light modulator.

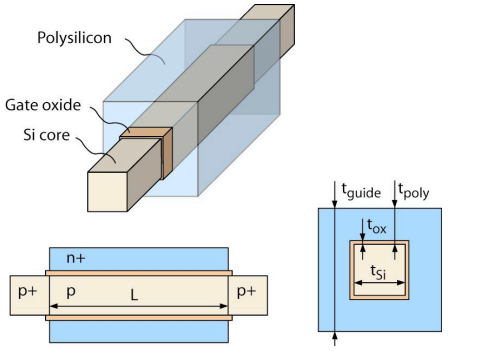

Fig. 2: Schematic of the GAA modulator. It consists of a silicon core surrounded by a thin gate oxide and the poly gate, light propagates in the entire structure

Simulation of device performance:
Extensive 2D and 3D simulation have been carried out on a GAA MOS light modulator structure [3,4]. We find that there is an optimum dimension of the silicon core with respect to efficiency, and that the good overlap between the optical mode and the spatial location of the modulation results in modulation depths comparable to pin-diodes.
High speed operation necessitates short (μm-long) devices with a fairly high level of gate doping. The latter results in a large optical loss and hence resonator-based

structures are to be preferred relative to single pass modulators. The total modulation required will be determined by the quality of the resonant cavity, and the total length can be composed of a series connection of several shorter devices to increase speed.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
ST–Microelectronics (Crolles, France) EPFL (US Patent 2007/0298551 A1)	Compatibility with the CMOS proccess. Capable of simultaneously achieving high speed and high modulation efficiency.	Strong demands on fabrication accuracy. Cost. High loss.

Conclusions and recommendations

The concept of a GAA MOS capacitive light modulator based on plasma dispersion in silicon is validated by 2D and 3D simulations. The excellent overlap between the optical mode confined to the nanowire waveguide and the position of the phase modulation region (inversion/accumulation layer) results in high modulation efficiency combined with high speed.

EUROSOI State of the Art Report

Chapter 4. Devices and Physics
Section 4.5. Optical SOI waveguides
Subsection 4.5.2 SOI Photonic Integrated Circuits (PICs)

Date of Issue: Feb-2010	**Partner: Tyndall**

Abstract

We summarize the state of the art on SOI refractive photonic integrated circuits (PICs)

Introduction

In Silicon circuits, high refractive-index-contrast waveguides with a cross-section of the order of the wavelength squared are used to make passive or active devices. The core of the waveguide is Silicon while the cladding is either a dielectric (such as silica) or air. The waveguide can be a conventional waveguide based on guiding by total internal reflection or a photonic crystal waveguide based on guiding by Bragg diffraction.

Passive devices using waveguides:
Recently, IBM has performed an investigation of the transmission properties of SOI-type PhC W1 waveguides as a function of the hole radius, slab thickness, and crystal length for both TE and TM polarizations. They demonstrate that in order to maximize the bandwidth of low-loss waveguiding the hole radius must be significantly reduced. While the photonic band gap considerably narrows, the bandwidth of low-loss propagation in PhC waveguides is increased up to 125 nm with losses as low as 8±2 dB/cm [1].
Exploitation of slow light phenomena has potential for applications ranging from all-optical storage to all-optical switching [2]. IBM experimentally demonstrated over 300-fold reduction of the group velocity on a silicon chip via an ultra-compact photonic integrated circuit using low loss silicon photonic crystal waveguides that can support an optical mode with a sub-micrometer cross-section [3].
Much research is in progress to improve light coupling efficiency between optical fibres and silicon waveguides. The large mismatch between the common optical fiber dimension and that of the high-index-contrast waveguide makes it difficult to couple light in and out of the chip. A number of techniques have been utilized for this purpose, including prism couplers, grating couplers, tapered fibers and micro-lens mode transformers. None of these approaches offer the combination of high coupling efficiency, wavelength independence, manufacturability and the robustness demanded by the need for low-cost high-volume fabrication for the telecommunications industry. A two-dimensional taper has been fabricated in rib silicon-on-insulator waveguides to couple light from high-numerical-aperture fibers with a coupling loss of 2 dB [4,5].
The first polarization splitter that uses geometrical birefringence control of high-index optical waveguides on SOI platform has been demonstrated. An SOI rib waveguide becomes birefringent as its size is reduced. This idea is used to design and fabricate a directional coupler polarization splitter based on geometrical birefringence [6].

Active devices using waveguides:
The active functions – light emission, modulation, switching and detection - can be

based on the properties of Silicon itself or on the properties of a special cladding material.
The difficulty of modulating light using silicon structures arises from the weak dependence of the refractive index and absorption coefficient on the free-carrier concentration. Liu et al have recently demonstrated a high-speed silicon optical modulator based on a MOS (metal–oxide–semiconductor) configuration; this modulator was the first high-speed optical active device on silicon, with a modulation bandwidth exceeding 1 GHz [7].
A weakness point is the leak of integrated silicon-based efficient light source, but progress has been made. Si p–i–n diodes for light emitters and detectors with optical waveguides have been integrated on silicon-on-insulator (SOI) substrates and photo-detection from the light emitter has been investigated [8].

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Leadership: IMEC Contributors: CEA,VTT, Technical Danish University of Technology COM **Comments:** Main USA competitor is IBM	Compatibility with the CMOS fabrication process	Strong demands on fabrication accuracy. Cost.

Conclusions and recommendations

SOI technology has become an important platform for photonic integrated circuits. The compatibility with CMOS standard technology is an added value to the development of More-than-Moore strategies based on System-on-Chip (SoC). The field is characterized by a strong competition around the world. Cost-reduction strategies are in progress to make this concept development viable

EUROSOI State of the Art Report

Chapter 4. Devices and Physics
Section 4.6. 3-Dimensional Integration

Date of Issue: Feb-2010	**Partner: LETI, UGR**

Abstract

3-D integration reduces the interconnect complexity and delay of 2-D, which are widely avowed as the barriers to the continued performance gain in the future technology generations. The ability of 3D to provide simultaneous power and performance benefits will play a crucial role in extending the silicon roadmap for a few more generations.

Introduction

Many industry observers have questioned the economic viability of the next wafer diameter increase (450 mm), and suggested that a different source of increasing wafer fab productivity should be sought. These suggestions usually involve novel substrates and new circuit approaches. Novel substrates are thought of as large area, low cost, probably non-crystalline materials used as strata for single-crystal silicon. New circuit approaches include 3-D circuits and multi-valued logic, consistent with SOI wafers, or perhaps, radical approaches to 3-D circuitry. The widespread implementation of any of these alternatives to expand and/or replace silicon would be a major task for the industry, requiring an entire hierarchy of paradigms to be discarded and replaced with new ones. 3-D technology promises higher integration density and lower interconnection complexity and delay. At present, however, not much work on circuit applications has been done due to lack of insight into 3-D circuit architecture and performance. One of the purposes of realizing 3-D integration is to reduce the interconnect complexity and delay of 2-D, which are widely avowed as the barriers to the continued performance gain in the future technology generations. 3-D structures effectively reduce the number of long delay nets, significantly reduce the number of repeaters, and dramatically improve the circuit performance. With 3-D integration, circuits can be clocked at frequencies much higher (double, even triple) than with 2-D. However, the impacts of vertical wires on chip area and interconnect delay can be limiting factors on the vertical integration of device layers; and that 3-D integration offers limited relief of power consumption.

Key challenges:

- Precise alignment of full wafers (≤1 μm accuracy).
- Thin adhesive-layer bonding at low temperature (≤400°C).
- Precision thinning and leveling of top wafer (~1 μm thick).
- Inter-wafer connection by high-aspect-ratio (>5:1) vias.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Infineon, Germany LETI. STMicroelectronics, France	higher integration density and lower interconnection complexity and delay.	Not much work in Europe. Implementing new manufacturing technologies usually results in a decrease in productivity, at least in the early stages of implementation. Impacts of vertical wires on chip area and interconnect delay can be limiting factors on the vertical integration of device layers.

Conclusions and recommendations

- 3-D circuits and multi-valued logic, and radical approaches to 3-D circuitry consistent with SOI wafers mean a huge challenge for the designers.
- The success of this approach could produce a reduction of the total cost, increasing the silicon yield.
- Few European groups are working on this area. More efforts should be dedicated to explore the possibilities of 3D integration.

EUROSOI State of the Art Report

Chapter 4. Devices. Physics.
Section 4.7. Novel Devices
Subsection 4.7.1. Multigate Devices

Date of Issue: Feb-2010	**Partner: UGR**

Abstract

The SOI technology allows a high degree of flexibility in the fabrication processes and the final structure to be obtained. The main advantage is the introduction of multigate devices which enhance the electrostatic control needed to avoid SCEs

Introduction

State-of-the-Art devices in mass production are approaching to the performance limit of traditional MOSFET as the critical dimensions are shrunk. Multi-gate devices based on SOI technology, are one of the best candidates to become a standard solution to overcome the problems arising from such aggressive scaling (SCEs). Moreover, the flexibility of SOI wafers and processes allows the use of different channel materials and substrate orientations to enhance the performance of CMOS circuits. Under the Multi-gate concept there is a wide variety of different devices from planar DGSOI and FinFETs to GAA [1] (Fig. 1).

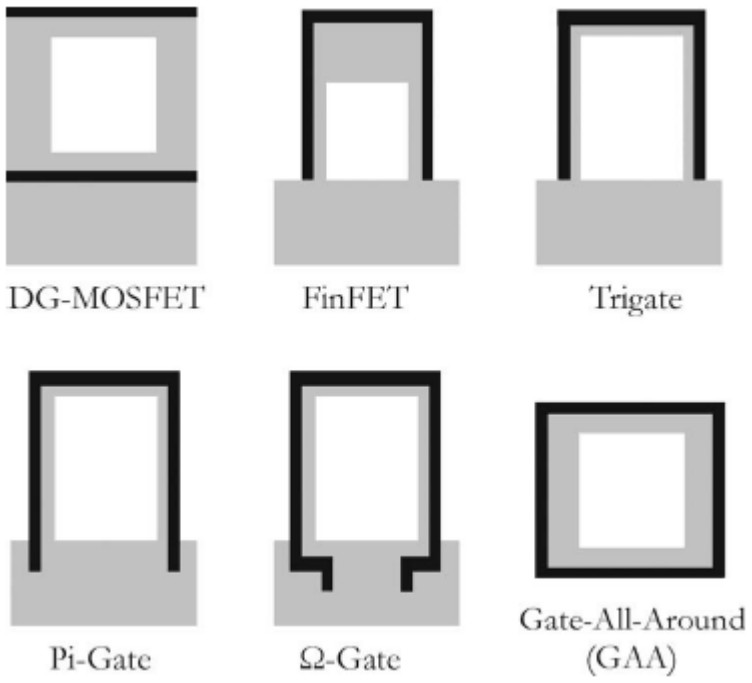

Fig. 1. Multi-gate configurations.

The MuGFETs not only increase the electrostatic control necessary to reduce SCEs, the existence of more than one gate also increase the inversion charge for a given bias and, therefore there is an increase in the current. This is mainly due to the contribution of each gate to the creation of an inversion channel in the corresponding silicon-insulator interface [2]. As the critical dimensions of the devices are reduced, corner effects and inter-channel coupling effects become of special importance. In particular, when a strong interchannel coupling is present, the charge is distributed along the whole channel and no only near the interfaces. In such conditions volume inversion appears and an improvement of the mobility may be observed [3]. Evenmore, the SOI technology allows the use of stacked devices with a common gate in an array-like configuration to obtain 3D multiwired devices [4].

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
EURSOI+ Consortium and main European groups on SOI. Main European Companies are doing efforts on the development of MuGFETs	Great efforts and long tradition on both theoretical and experimental studies of MuGFETs in the European community	It is necessary to assets the standard devices to be used for commercial applications

Conclusions and recommendations

The MuGFETs are expected to be the standard solution to implement the technological nodes in a medium time term.

EUROSOI State of the Art Report

Chapter 4. Devices. Physics.
Section 4.7. Novel Devices
Subsection 4.7.2. Resonant Tunnelling Diodes

Date of Issue: Feb-2010	**Partner: WUT, UGR**

Abstract

The SOI technology with its possibility of fabricating the double gate MOS system with an ultrathin semiconductor layer between two ultrathin oxide layers can be a platform for development of silicon nanoelectronics based on the resonant tunnelling devices: diodes and transistors.

Introduction

The double gate (DG) SOI technology, due to its capabilities of fabricating double barrier quantum system consisting of ultrathin silicon layer closed between two ultrathin SiO2 layers, is privileged to play a role of a technological platform for nanoelectronics based in operation on the resonant tunneling phenomenon. The structure of the resonant tunneling diode (RTD) is schematically shown in Fig. 1.

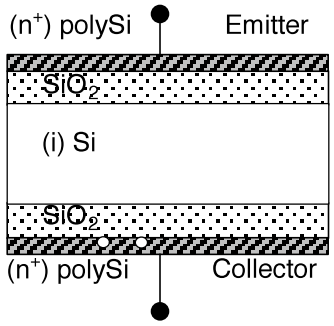

Fig.1. The schematic view of the DG SOI resonant tunneling diode.

If the silicon layer thickness is in the range of a few nanometers, the $SiO_2/Si/SiO_2$ system constitutes a potential well, in which energy of electrons for their motion perpendicular to the interfaces is significantly quantized, as illustrated in Fig. 2. As there are two possible values of the electron effective mass: the longitudinal mass m_l and the transverse mass m_t, there area two ladders of energy levels: E_{eL} and E_{eT}. The same corresponds to holes confined in the valence band of the silicon layer; in the approximate view shown in Fig. 2, there are the heavy hole levels E_{hH} and the light hole levels E_{hL}. As the energy structure of the silicon valence band is much more compound than for the silicon conduction band, its approximation by two parabolic subbands may be not adequate to describe the hole tunnel currents in the accurate way.

If the two SiO_2 layers are ultrathin, i.e., their thickness is in the range of a few

nanometers, electrons in one gate electrode (emitter) can effectively tunnel to the second one (collector). The probability of tunneling through the $SiO_2/Si/SiO_2$ double barrier system is greatly enhanced for energy levels coincident with the quantum well levels and this mode of tunneling is called the resonant tunnneling. If the two gate electrodes are biased independently, the net current of tunneling between them can exhibit ranges of the negative differential resistance, when the subsequent resonant tunnelling levels drop below the edge of the conduction band in the emitter. The resonant tunnelling diode can exhibit several current peaks which mean that the resonant tunnelling based circuits can offer multistability.

The research on the Si/SiO_2 heterojunction based resonant tunneling diodes was initiated by Texas Instruments [1,2]. The first experimental observations of the negative differential resistance in the resonant tunneling diode based on the SOI system have been reported by Shizuoka University group [3, 4]. The devices were fabricated with the use of bonded SOI wafers with 3-7 nm buried oxide and the Si layer of about 2 nm final thickness. The n^+ substrate served as the emitter while the aluminum electrode on the 2 nm thin front oxide played a role of the collector. The reported current peaks were weak and observed at low temperatures, although the group claims on the website that they achieve RTD structures exhibiting negative differential resistance (NDR) even at room temperature. Much more effort must be devoted to fabricate DG SOI RTDs with *I-V* characteristics having NDR ranges of the considerable peak-to-valley current ratio. This goal can be achieved more effectively if experimental work is assisted by theoretical simulations.

Theoretical considerations of resonant tunneling current in the double gate SOI system have been presented in [5-8]. As a result, theoretical models have been worked out which are based on a selfconsistent solution of the double gate SOI system with including energy quantization in both the conduction and the valence band. The resonant tunneling is considered for both electrons and holes. However, different assumptions of the modeling need experimental verification, which has not been done due to the lack of experimental structures. This seems to be a main barrier for further progress of the research. Some European microelectronics industry centers have at their disposal technology enabling fabrication of DG MOS devices with ultrathin silicon and ultrathin silicon dioxide layers, what is required for fabrication of the silicon RTDs. However, up to date, there have been no public releases on their activity in this area.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Warsaw University of Technology, Poland Swiss Federal Institute of Technology, Technical University of Vienna, Austria Fraunhofer Institute of Integrated Systems and Device Technology, Germany Chalmers, Göteborg, Sweden VTT Technologies, Finland	European university teams are advanced in modeling the physics of the double gate MOS structures with ultrathin silicon and silicon dioxide layers. European microelectronics industry centres possess technology enabling fabrication of DG MOS structures with ultrathin silicon and silicon dioxide layers.	Still few experimental works on resonant tunnelling in the double gate SOI structures.

Conclusions and recommendations

DGSOI technology can be a starting point for the development of silicon nanoelectronics based on resonant tunnelling devices. The SoA in this topic is still on early stages and only simulation results are available and therefore, and experimental effort is needed to asses the theory.

EUROSOI State of the Art Report

Chapter 4. Devices. Physics.
Section 4.7. Novel Devices
Subsection 4.7.3. SB-MOSFETs

Date of Issue: Feb-2010	**Partner: UGR**

Abstract

Schottky barrier SOI MOSFETs (SB MOSFETs) are presented as a possible solution to reduce the source and drain serial resistances in next generations' ultra short devices.

Introduction

As the devices are scaled down the serial resistance arising from source and drain regions becomes in an important limiting factor to the device performance. Up to now, the standard solution consists in an increase of the doping density in source/drain areas. However, with today's concentrations close to 10^{20} cm^{-3}, the limit of an effective activation of the dopants is almost reached. It is necessary to find new solution to increase the conductivity of source/drain contacts to reduce the serial resistance [1].

The ideal solution might be to substitute the silicon in source and drain regions by a metal. The main efforts are focused on the development of SOI and Ge based devices. Among the main advantages of using Schottky contacts to implement source and drain contacts it can be highlighted the reduction of serial resistance, the adjustment of the source to channel barrier by choosing an adequate workfunction, abrupt junction profiles and the possibility of single material for both n and p devices. However, from a technological point of view, SB-MOSFETs present important challenges due to the difficulty to create the metal areas. The main technique to obtain metal contacts is the dopant segregation [2], in this way a silicide contact (e.g. PtSi) is obtained. Therefore, an important effort is still needed to obtain reliable devices to be included in standard CMOS fabrication flow.

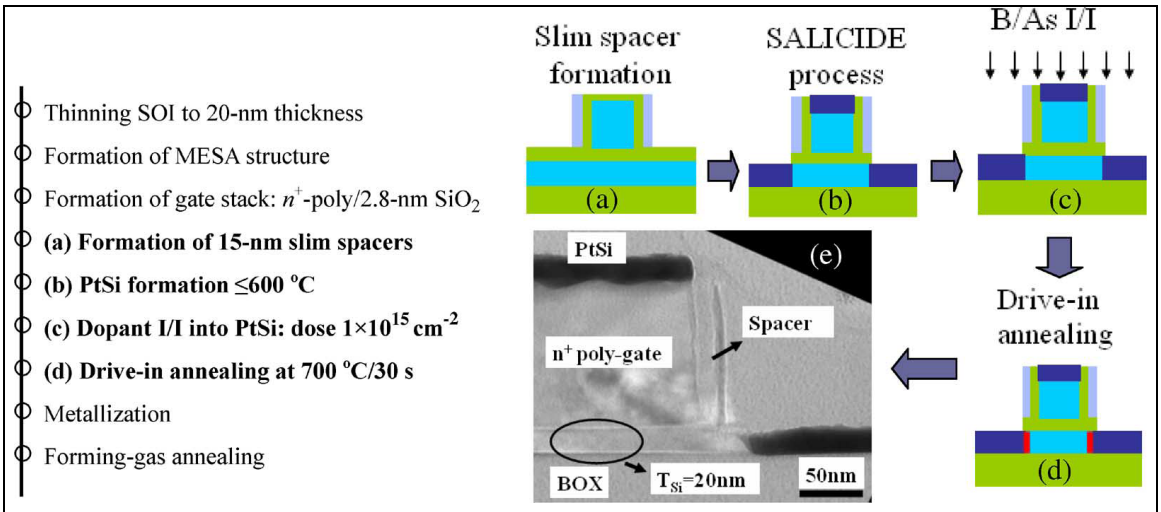

Fig. 1. Process flow for a low-temperature SADS process developed for the SB-MOSFET featuring PtSi-based SB S/D. The TEM cross section of the central part of a fabricated device is also shown

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Jülich, University of Warwick, CNRS **Comments:** Great efforts in this field are also taking place in Japan	Low parasitic resistance, no need of shallow implants, one metal for both p and n devices	The technology is not still mature for production. Important improvements are still necessary

Conclusions and recommendations

SB-MOSFETs are promising candidates to extend the roadmap, whoever an important effort is still needed from both theoretical and experimental point of view to develop devices and circuits.

EUROSOI State of the Art Report

Chapter 4. Devices. Physics.
Section 4.7. Novel Devices
Subsection 4.7.4. Junction-less SOI MOSFET

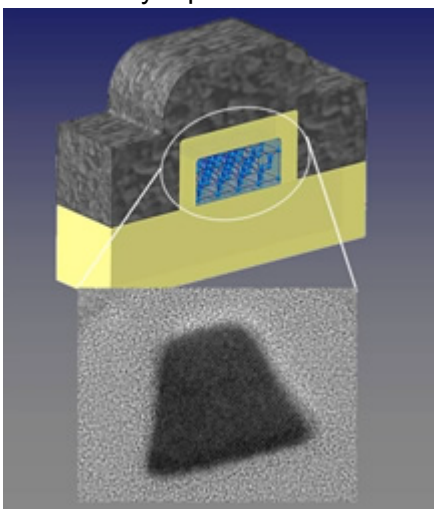
Date of Issue: Feb-2010	**Partner: UGR - Tyndall**

Abstract

Junction-less devices are proposed to be an alternative to junction control in aggressively scaled SOI devices.

Introduction

Current technologies require fabrication processes that are both complex and costly. All existing transistors are based on junctions. Controlling the junction allows the current in the device to be turned on and off and it is the precise fabrication of this junction that determines the characteristics and quality of the transistor. Tyndall National Institute's ground breaking junction-less transistor doesn't require a junction. In these devices (somehow recent evolution of the accumulation mode transistor) the current flows in a very thin silicon wire and the flow of current if perfectly controlled by a 'wedding ring' structure that electrically squeezes the silicon wire [1].



Junction-less transistor from Tyndall National Institute

References

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Tyndall	European university teams are advanced in SOI modeling. European microelectronics industry centres are able to fabricate the needed structures.	An extended characterization study is still needed
Conclusions and recommendations Junction-less SOI MOSFETs are presented as a possible solution to overcome the problems arisen in junction areas as the channel length is reduced		

EUROSOI State of the Art Report

Chapter 4. Devices. Physics
Section 4.8. Operation at high temperatures of SOI devices
Subsection 4.8.1. High-Temperature Subthreshold Slope in SOI MOSFETs

Date of Issue: Nov - 2005	**Partner: ISP**

Abstract

Using numerical simulation and it comparison with experimental data it is shown that at high temperatures (above 150^0C) in the subthreshold (weak inversion) region of SOI MOSFETs the approach, based on the depletion approximation and a charge-sheet model, is no valid.

Introduction

The conventional bulk silicon CMOS circuits can operate only at moderate temperatures (up to 150 - 200^0C). At higher temperatures bulk silicon CMOS devices usually fail because of increased junction leakage, thermally induced latch-up, threshold voltage shifts, etc. Because of the high temperature advantages of SOI MOSFETs the range of SOI CMOS operation has been extended up to 300^0C. In connection with it, there is need to reconsider the validity for high temperatures of some approximations commonly used in deriving the MOSFET parameters. In this work, we revise the validity of a classical expression for the subthreshold swing and analyze the physics that is responsible for the temperature degradation of the subthreshold slope in both thick- and thin-film SOI MOSFETs.

Main results

Reasons for violating of a classical expression at the high-temperature

The commonly used description of the subthreshold characteristics of both bulk and SOI MOSFETs is based on the depletion approximation and a charge-sheet model. In this work, using numerical simulation, it is shown that at high temperatures (above 150^0C) in the subthreshold (weak inversion) region this approach is no longer valid. The first reason lies in the fact that the rise in free carrier charge densities with temperature results in an increased effective substrate capacitance as compared to that determined from the depletion approximation. This is illustrated by Fig.1, which shows the different charge density components as a function of the surface potential at T=300^0C in a bulk or partially-depleted SOI MOSFET (Fig1a) and in a fully-depleted SOI MOSFET. As can be seen from Fig.1, at T=300^0C in a weak inversion region ($\phi_F \leq \varphi_{sf} \leq 2\phi_F$), the total charge density Q_{tot} (shown by solid line) is not entirely determined by the depleted charge Q_{dep} (shown by dashed line) because of the noticeable contribution from the free carriers. This means that the total surface differential capacitance is higher than the depletion capacitance in both thick- and thin-film SOI devices resulting in an additional increase in the subthreshold swing compared to that expected from the classical expression.

Another correction must be introduced into the classical expression to account for the inversion layer broadening caused by lowering the surface electric field in a weak inversion region with temperature. The corrected expression for the high-temperature

inverse subthreshold slope factor can be written as: $S = \frac{nkT}{q} \cdot \ln(10) \cdot \left(1 + \frac{C_{stot}}{C_o}\right)$, where n is a correction factor, which takes into account the effect of lowering of the surface electric field with temperature, C_{stot} is the total surface differential capacitance, which includes the contribution from the free carriers and is higher than the depletion capacitance. For the same doping and the same temperatures n is higher in a SOI device with depleted back interface than in a bulk device because of the lower surface electric field. The thicker is the buried oxide, the higher is the correction factor n. Ignoring the above factors would introduce large errors in predicting the subthreshold characteristics in both thick-film and thin-film SOI devices.

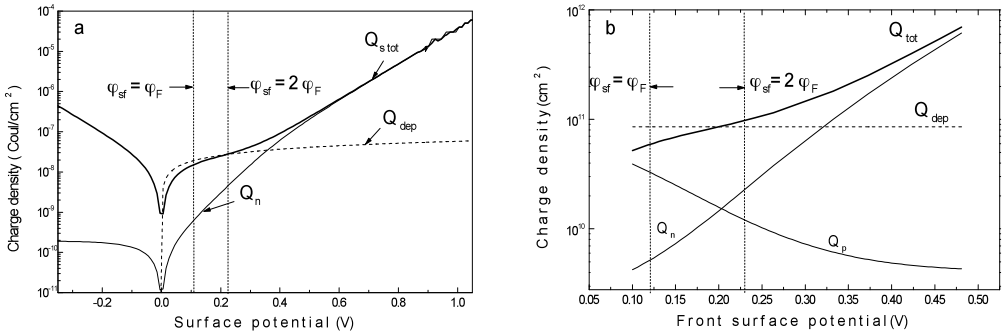

Fig1. The surface charge density components calculated for T=300^{0}C as a function of the surface potential: (a) in a bulk or partially-depleted SOI device with N_A=10^{16} cm^{-3} and in a thin-film SOI device with depleted back interface (N_A=10^{16} cm^{-3}, d_{Si}=85 nm, d_{of}=30 nm, d_{ob}=400 nm, V_{gb}=0).

Experimental Results

The measurements were performed on the 20 μm-long n-channel enhancement mode SOI MOSFETs fabricated on the UNIBOND wafers. The Si film thickness was 85 nm, the front- and back-gate oxide thicknesses were 30 nm and 400 nm, respectively. Fig.2 shows the experimental temperature dependencies of the subthreshold swing measured on the devices made on doped and intentionally undoped Si films having doping concentration of 3x10^{16} and 10^{15} cm^{-3}. It can be seen that the experimental subthreshold swing fits well the linear temperature dependence expected from the classical model only at T≤150^{0}C and rapidly rises with further increase in temperature, in spite of the fact that by the conventional definition both devices remain fully depleted up to 300^{0}C. The subthreshold swing obtained by numerical simulation agrees well with experimental data in the whole temperature range being studied.

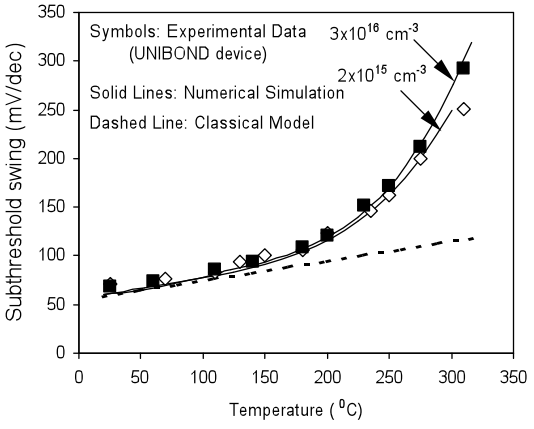

Fig.2. The temperature dependence of the inverse subthreshold slope in a bulk or thick film SOI device for various doping concentrations calculated using the classical expression (dashed lines), with applying the corrections for the increase in C_s due to free carriers (dotted lines) and for lowering the surface electric field (solid lines).

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European Contribution on the Field	Current Situation	
European Groups: UCL, Tyndall, ISP	**Strong Points**	**Weaknesses**
	Main physical processes responsible for high-temperature behaviour of SOI MOSFETs are now clear	C_∞-continuous model for high temperature operated AM SOI pMOSFETs is not now developed, that results in difficulties in calculation of analog integrated circuits

Conclusions and recommendations

It is demonstrated that: (a) the rise in free carrier charge densities with temperature results in an increased effective substrate capacitance as compared to that determined from the depletion approximation; (b) a correction to account for the inversion layer broadening, caused by lowering the surface electric field in a weak inversion region with temperature, must be introduced into the classical expression for the subthreshold slope.

EUROSOI State of the Art Report

Chapter 4. Devices. Physics
Section 4.8. Operation at high temperatures of SOI devices
Subsection 4.8.2. High-Temperature Off-State Current in SOI MOSFETs

Date of Issue: Nov - 2005	**Partner: ISP**

Abstract

The off-state leakage currents in long-channel SOI MOSFETs are investigated by simulation and measurements in the range 20-300^{0}C. The general trends of high-temperature off-currents are interpreted in terms of the diffusion mechanism, which becomes dominant as temperature increases. The potential and carrier distributions in a SOI film for various temperatures, device parameters and applied voltages are analyzed to understand the behavior of the off-state diffusion current. The silicon film thinning and substrate biasing effects are considered. Both single- and double-gate operation cases are analyzed

Introduction

One of the principal high-temperature advantages of SOI CMOS devices over bulk Si devices is much lower leakage current at elevated temperatures due to smaller source-drain junction areas and due to elimination of large well-to-substrate diffusion leakage. In this work the detailed investigation of the high-temperature off-state currents in SOI MOSFETs has been performed using simulations and measurements. The main trends of high-temperature off-state leakage current are analyzed in terms of the diffusion mechanism.

Main results

Off-state leakage current components

In general case, the off-state leakage current in a SOI MOSFET consists of two components, namely: the generation current in the reverse-biased drain junction (I_{gen}) and diffusion current from undepleted body film (I_{diff}). As a rough approximation, the generation current can be given by:

$$I_{gen} = q \cdot d_{Si} \cdot W \cdot \frac{n_i}{\tau_g} \cdot \left\{ \sqrt{\frac{2 \cdot \varepsilon_s \cdot k \cdot T}{q^2 \cdot N_A}} \left[\sqrt{\ln\left(\frac{N_A}{n_i}\right) + \frac{q \cdot V_D}{k \cdot T}} - \sqrt{\ln\left(\frac{N_A}{n_i}\right)} \right] \right\}, \quad (1)$$

where d_{Si} is the Si film thickness, W is the device width, n_i is the intrinsic carrier concentration, τ_g is the minority carrier generation lifetime, V_D is the drain voltage, the other symbols have their usual meaning. Diffusion current for enhancement-mode (EM) devices can be expressed as:

$$I_{diff} = q \cdot W \cdot \sqrt{\frac{D_n}{\tau_{rn}}} \cdot \left(1 - e^{-\frac{q \cdot V_D}{kT}}\right) \cdot \int_0^{d_{Si}} \frac{n_i^2}{N_A} \cdot e^{\frac{q \cdot \varphi(x,T)}{kT}} dx, \quad (2)$$

and for accumulation mode (AM) devices as:

$$I_{diff} = q \cdot W \cdot \sqrt{\frac{D_p}{\tau_{rp}}} \cdot \left(1 - e^{\frac{q \cdot V_D}{kT}}\right) \cdot \int_0^{d_{Si}} N_A \cdot e^{\frac{-q \cdot \varphi(x,T)}{kT}} dx \quad (3)$$

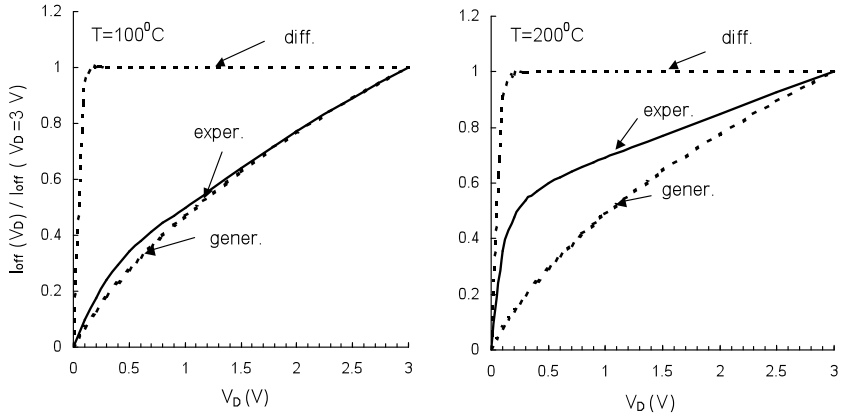
with D_n , D_p the diffusion constants, τ_{rn} ,τ_{rp} recombination lifetime for electrons and holes, respectively; $\varphi(x,T)$ represents the potential distribution across the film thickness in undepleted body film. In AM SOI MOSFETs one should also take into account generation in the depleted Si film under the gate.

As follows from (2) and (3), in general case of non-zero gate voltages and non-zero flat-band voltages, the total carrier density responsible for the off-state diffusion current cannot be expressed by a commonly used approximation $(n_i^2/N_A) \cdot d_{Si}$, but is determined by the potential distribution $\varphi(x,T)$ at proper conditions. Below is shown that at temperatures above 150-200^{0}C (depending on the Si film thickness and drain voltage) the off-state current is caused by the diffusion mechanism. Therefore, the main trends of the high-temperature off-current in SOI MOSFETs should be explained by the carrier concentration distribution in the Si film, which depends on the device parameters and applied voltages.

Identification of generation and diffusion components

Generation and diffusion of the off-state leakage current components can be identified using the temperature and drain voltage dependencies of the off current. Identification of the off-state current components from drain voltage dependence is based on the fact that that the diffusion current tends to saturate with V_D for $V_D > kT/q$ following the law $I_{diff} = I_0\left(1 - \exp\left(qV_D / kT\right)\right)$, whereas the generation current increases with V_D as the drain generation layer width (see(1)).

Fig.1 illustrates the change of the dominant mechanism of off-state current in the ZMR device with temperature. As can be seen from Fig.1(a), at temperature of 100^0 C, the off-state leakage current in the ZMR device is predominantly due to generation the depleted drain region, while at T=300^{0}C it is entirely determined by diffusion mechanism.



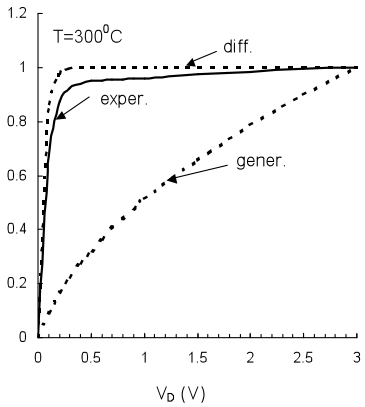


Fig.1. The experimental (solid line) drain-voltage dependence of the off-state current (normalized to its value at V_D=3 V) measured in the ZMR SOI MOSFET at different temperatures showing the change in the dominant mechanism of the leakage current with temperature. Simulated diffusion and generation components are shown by dashed lines (d_{Si} =0.15 mm, d_{of} =0.08 mm, d_{ob} =1.0 mm, V_{gf} = -5 V, V_{gb}=0 V).

Fig.2 shows the $I_{off}(V_D)$-dependence measured at two different temperatures (130^{0}C and 310^{0}C) in an EM and AM SOI MOSFETs fabricated on UNIBOND SOI substrates, which clearly illustrates the change of the mechanism of leakage current with temperature in both types of the devices. The fact that at temperature of 310^{0}C I_{off} tends to saturate when V_D>0.2 V indicates that the diffusion mechanism becomes prevailing.

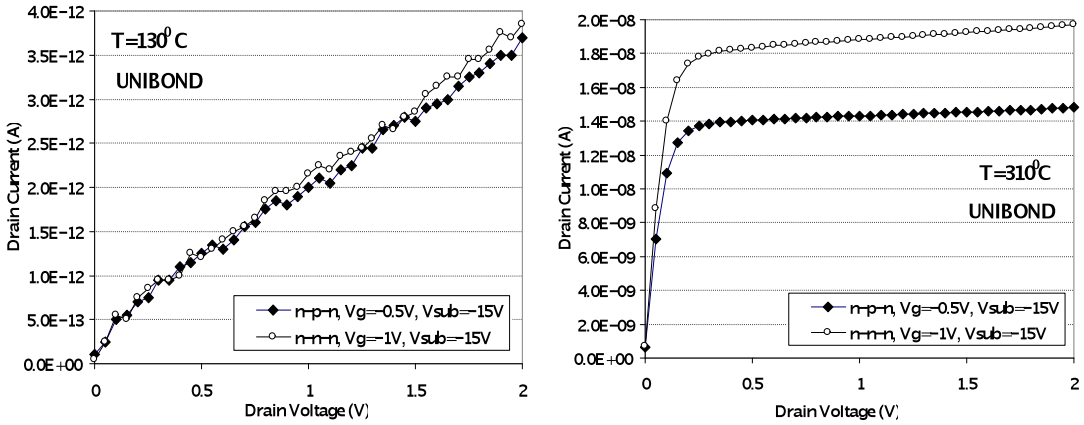


Fig.2. The drain voltage dependence of the off-state current in the long channel enhancement-mode and accumulation-mode UNIBOND SOI MOSFETs measured at temperature of 130^{0}C and 310^{0}C, showing the change in the dominant mechanism of the leakage current with temperature (d_{Si} =0.08 mm, d_{of} =0.03 mm, d_{ob} =0.38 mm, W/L=60/8).

Experimental results presented above clearly indicate that at sufficiently high temperatures (above 100-200^{0}C depending on the film thickness and applied drain voltage) the off-state current in a SOI MOSFET is entirely caused by the diffusion mechanism. The thicker silicon film, the lower temperature at which diffusion mechanism becomes prevailing. Therefore, the main trends of the high-temperature off-current in SOI MOSFETs can be derived from the analysis of the potential and carrier concentration distributions under off-state conditions.

The silicon film thickness effect

Fig.3 shows the minority carrier concentration distributions in the SOI films with various film thickness calculated for the n-channel EM device biased in the off-direction

at T=300^{0}C. Fig.3(a) and 3(b) illustrate the single- and double-gate control cases, respectively. The dashed line shows the minority carrier concentration in quasi-neutral Si with the same doping. It is evident that the carrier concentration distribution in a SOI film is nonuniform across the film thickness and depends strongly on the film thickness. An average minority carrier concentration at given conditions is essentially lower than that in quasi-neutral silicon n_i^2/N_A. The thinner is the Si film, the lower is an average minority carrier concentration. As a result, the total off-state minority carrier density obtained by integrating over the film thickness, which is responsible for the off-state diffusion current, and thus the high-temperature off-state current and on-to-off current ratio should exhibit a strong non-linear dependence on the Si film thickness, as shown in Fig.4. The measurements performed on the ZMR SOI devices with various film thicknesses support the above conclusion (Fig.5).

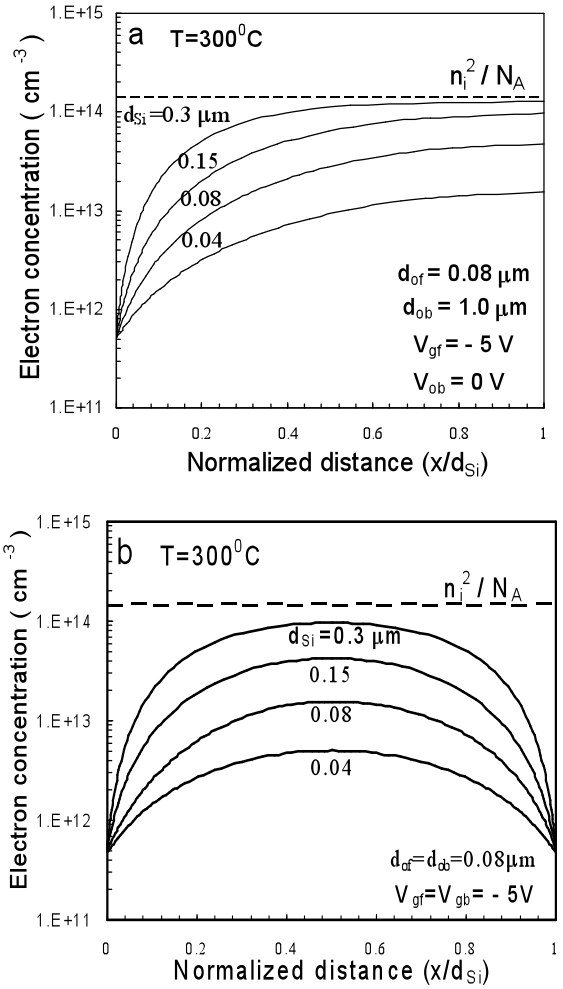


Fig.3. The minority carrier concentration distributions in the Si films with various film thickness in the n-EM SOI MOSFET strongly biased in the off-direction in single-gate (a) and double-gate (b) regimes at T=300^{0}C. (N_A=1x10^{16} cm^{-3}).

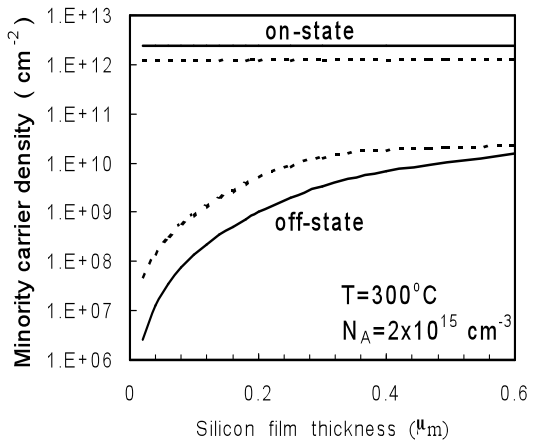


Fig.4. The total on- and off-minority carrier densities vs. the film thickness in double-gate (solid line) and single-gate (dashed line) regimes.

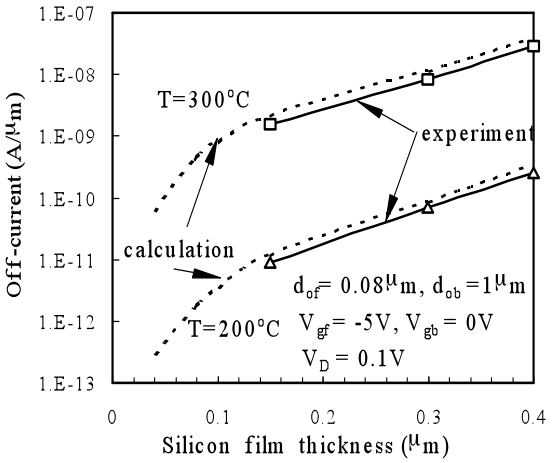


Fig.5. The experimental (solid line) and calculated from the diffusion model (dashed line) high-temperature off-state current in ZMR SOI MOSFETs as a function of the film thickness

Advantages of the double-gate regime

Fig.4 clearly demonstrates the high-temperature advantages of double-gate regime (in addition to the second channel in the on-state). In contrast to the on-state, in which the drain current flows predominantly in the surface channels and thus is essentially independent on the film thickness, the off-state diffusion current results from the middle part of the Si film, where minority carrier concentration is extremely sensitive to the film thickness (Fig.2). Thus for given Si film parameters, the minimum achievable off-current and maximum on-to-off current ratio should be in the double-gate regime. As is evident from Fig.4, an improvement in on-to-off current ratio due to the double-gate regime is expected to be 2n (a factor of 2 is due to the second channel in the on-state, and a factor of n, which depends on the film thickness and doping, is due to a lowering of the off-state diffusion current).

The channel length dependence

From the predominance of the diffusion mechanism at high temperatures it follows that in the devices with channel length less than the diffusion length ($L<L_{diff}$) the high temperature off-current (per unit device width) should increase with decreasing of the channel length due to bipolar effect, roughly as $1/L$. This was supported by two-

dimensional MEDICI simulation.

Another interesting conclusion, which follows from the predominance of the diffusion mechanism , is that in relatively short-channel devices (in which $L<L_{diff}$), the diffusion current and thus the high-temperature off-state current should not depend on the diffusion length or carrier lifetime. This makes predictable the high-temperature characteristics without knowledge of these parameters, which depend on the material quality.

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European Contribution on the Field	Current Situation	
European Groups: UCL, ISP, Tyndall	**Strong Points** Main physical processes responsible for high-tempera-ture behaviour of SOI MOSFETs are now clear	**Weaknesses** C_∞-continuous mo-del for high tempe-rature operated AM SOI pMOSFETs is not now developed, that results in diffi-culties in calculation of analog integrated circuits

Conclusions and recommendations

It is demonstrated that at high temperatures (above 100-200^0 C depending on the Si film thickness and drain voltage) off-state current in SOI MOSFETs is due to the diffusion mechanism. A diffusion model for the high-temperature off-state current in SOI MOSFETs, which is based on the analysis of the potential and carrier concentration distributions in the Si film, has been developed. This model predicts a strong nonlinear dependence of the high-temperature off-state current on the Si film thickness. A strong decrease in the high-temperature off-state current and improvement in on-to-off current ratio is expected to be for thin films and double-gate regime due. The proposed diffusion model allows one to explain all trends of the high-temperature off-state current behavior in EM SOI MOSFETs (namely, temperature and silicon film thickness dependencies, channel length and drain voltage dependencies, back-gate biasing

effect).

At sufficiently high temperatures and low drain voltages, the similar behavior of the off-state current is expected to be in EM and AM SOI MOSFETs.

The high-temperature off-state characteristics of relatively short-channel ($L<L_{diff}$) devices appear to be predictable without knowledge of the carrier lifetime or diffusion length.

CHAPTER V

Simulation and modeling

EUROSOI State of the Art Report

Chapter 5. Simulation and modeling
Section 5.1. Process and technology simulation

Date of Issue: April – 2009	**Partner: University of Granada**

Abstract

The state of the art of SOI process and technology simulation is linked to the more general simulation tools used in conventional standard CMOS processes and technology. In this respect, apart from the initial substrate of SOI wafers used to fabricate both FD or PD SOI devices the processes involved in the fabrication are similar to non-SOI devices.

We list and describe here few of the most well known simulators used in the industry as well as the processes, and the models used to reproduced them.

Introduction

The history of commercial process simulators began with the development of the Stanford University Process Modeling (SUPREM) program. Building upon this beginning with improved models SUPREM II and SUPREM III were developed. Technology Modeling Associates, Inc. (TMA) which was formed in 1979 was the first company to commercialize SUPREM III. Later Silvaco also commercialized SUPREM and named the product ATHENA. TMA commercialized SUPREM-IV (2D version) and called it TSUPREM4. In 1992, Integrated Systems Engineering (ISE) came out with the 1D process simulator TESIM and the 2D process simulator DIOS. At about the same time development of a new 3D process and device simulator began at TMA and after TMA was acquired by Avanti, the product was released in 1998 as Taurus. Around 1994 a first version of the Florida Object Oriented Process Simulator (FLOOPS) was completed. FLOOPS was later commercialized by ISE in 2002. One other process simulator PROPHET was created around 1994 at Bell labs which later became Agere, but has not been sold commercially. In 2002 Synopsys acquired Avant!, corp. and in 2004 Synopsys acquired ISE. Synopsys released a new process simulator combining the best features of Taurus, TSUPREM4, into the FLOOPS platform and it was called Sentaurus Process. SILVACO Procucts are ATHENA for 2D Process simulation, ATLAS for 2D Device Simulation, Victory Process /device for 3D Simulation. Besides these simulators, there are numerous other university and commercial simulators such as PROMIS, PREDICT, PROSIM, ICECREAM, DADOS, TITAN, MicroTec, DOPDEES, ALAMODE.

The state of the art of SOI process and technology simulation is linked to the more general simulation tools used in conventional standard CMOS processes and technology. In this respect, apart from the initial substrate of SOI wafers used to fabricate both FD or PD SOI devices the processes involved in the fabrication are similar to non-SOI devices. Therefore this section described the features of state of the art process simulators.

Suppliers of Modeling and Simulation capability are mainly universities and research institutes funded by government and/or projects. TCAD vendors play an important role in the development of those capabilities, and are in most cases the interfaces between

R&D and the end customer in industry, customizing the R&D results into commercially supported simulation tools. Simulation efforts in semiconductor industry mainly focus around the adaptation and application of the simulation capabilities to the development and optimization of technologies, devices and ICs. In this respect is important to highlight the main features of commercial simulators since they are the tools which are being used in the industry and correspondingly they represent for the industrial community the state of the art of process and technology simulation.

We will not include all the simulators that can be found in the market right now, however we consider few of the most significant to try to figure out what are the main characteristics included in current process and technology TCAD tools. The information provided here was taken from the vendors web sites.

Current characteristics of semiconductor process simulators
The fabrication of devices is simulated by dealing with a set of processes that reproduce the real chemical processes and give us an idea of the geometrical structures obtained and its features in terms of dopant and layers of different materials distributions in 3, 2 or 1 dimensions. Most of the tools are coupled with device simulators to simulate the electrical and thermal behavior of the devices which are obtained as a result of the processes performed on the initial wafer. The results of the device simulator help to obtain the parameters of the models which are needed in circuit simulators. In this respect, different fabrication processes are reflected in parameters such as for example the frequency of a ring-oscillator or the cut-off frequency of a transistor**,** making the set of simulators a powerful tool in the development process.

After a simulation it can be predicted the 1D, 2D, or 3D geometry and the impurity profiles generated by a fabrication process. It can also be investigated the effect of variations in the fabrication processes and it can be analyzed the mechanical stresses developing in your device during processing. With current tools complete process flows can be simulated, including implantation, deposition, etch, diffusion and oxidation of 3D structures. Specific 3D process effects, such as LOCOS and STI corners, can also be studied. To do so, efficient automatic mesh generators are used to facilitate the simulation. Finite elements algorithms among others are developed to deal with 1D-2D-3D geometries and efficient moving-boundary simulations.

Some tools also include interfaces to insert new equations in the model. This provides an easy and flexible way to define new physical models and partial differential equations. Areas of particular importance include impurity and defect diffusion, electromigration, silicon oxide growth, etc. It is possible to simulate all common materials and impurities, plus user-defined materials, impurities and reactions.

Among the simulation features are:
Simulation of arbitrarily shaped 1D, 2D and 3D structures with complete process simulation including deposition, etch ion implantation, oxidation, silicidation, and diffusion. Advanced adaptive mesh generation which provides optimal grids using a minimum number of mesh points. Dynamic memory allocation - the size of the simulated problem is limited only by the capacity of the computer. Large selection of fast, direct and iterative linear solvers.

Among the models are:

Implantation:
- Dual Pearson, Pearson and Gaussian analytic models.
- Energy range 0.5 KeV to 10 MeV.
- Energy, dose, tilt, and rotation-dependent channeling.
- Depth-dependent lateral standard deviation, separate for random scattering and channel backscattering model extends the profiles under the masks beyond the limitations of the conventional analytic models.
- Shadowing effects due to wafer tilt and rotation.
- Easy integration of the users' implant moment data into the hierarchical implant data tab.
- Implant damage/amorphization model. Physically based Monte Carlo model includes channeling, amorphization, temperature dependence, damage self-annealing, substrate orientation and tilt/rotation effects. Choice of models for multilayer targets.

Diffusion:
- High-concentration effects (diffusivity enhancement and precipitation).
- Impurity interaction with point defects.
- TED, OED, and ORD effects.
- Impurity interaction via Fermi level, point defects and electric field.
- Generation, diffusion and recombination of point defects.
- Dopant-assisted recombination of point defects.
- Saturation of dopant/defect pair concentrations.
- Interstitial clustering (formation and dissolution of {311} defects).
- Interface dopant pile-up (dose-loss) during low- temperature transient diffusion.
- Dopant diffusion through polysilicon with dependence on grain size and boundary.
- Dislocation loops.

Oxidation:
- Visco-elastic model.
- Robust boundary movement by level set method.
- Parallel oxidation by multiple oxidizing species.
- Initial logarithmic oxidation kinetics in dry oxygen.
- Surface orientation dependence for complex 2D and 3D structures.

Deposition and Etching:
- Robust boundary movement by level set method.
- Conformal deposition.
- Dry etching for polygonal masks in 3D.
- Wet etching.
- Planarizing etching (CMP).
- Concentration-dependent oxidation rates.
- Thin-oxide enhancement. Gas partial pressures calculated from flow rates.
- User-defined ambient.
- Effect of HCl on oxidation rates.

Silicidation:
- Deposition and growth of titanium and tungsten silicides.
- User-defined models for other silicides.

Other models:

Deposition and etching. Conformal deposition. Epitaxial growth, with impurity diffusion. Dry etching with masked undercutting and angled sidewalls. Isotropic etching. Etching of arbitrary regions. Exposure and development of photoresist.

COMMERCIAL TOOLS

A state of the art document would be incomplete if the most important TCAD tools were not described**,** since they are a reference in the industry and in the R&D community. That is why, some of them are described below. We do not aim at describing them in full**,** but just to drive the reader attention to their existence and some of the features that the vendors highlight in their web sites. They share the most of the features we have listed above and they should be evaluated in the context of the companion tools provided by the vendor. It is important to stress that all of them include the possibility of simulating SOI devices since the differences with respect to the conventional devices are marginal.

1.- SILVACO: ATHENA Process Simulation Software (http://www.silvaco.com**)**

ATHENA framework integrates several process simulation modules within a user-friendly environment provided by Silvaco TCAD interactive tools. ATHENA has evolved from a world-renowned Stanford University simulator SUPREM-IV, with many new capabilities developed in collaboration with dozens of academic and industrial partners. ATHENA provides a convenient platform for simulating processes used in semiconductor industry: ion implantation, diffusion, oxidation, physical etching and deposition, lithography, stress formation and silicidation.

Key features: • Fast and accurate simulation of all critical fabrication steps used in CMOS, bipolar, SiGe/SiGeC, SiC, SOI, III-V, optoelectronic, MEMS, and power device technologies.
• Accurately predicts multi-layer topology, dopant distributions, and stresses in various device structures.
• Advanced simulation environment allows:

- easy creation and modification of process flow input decks including automatic control of layout mask sequences
- automatic and user-defined mesh generation and control
- interactive plotting of 2D structures and distributions as well as 1D cross-sections
- run-time extraction of important process and device parameters
- optimization of process flow and calibration of model parameters

• Focused TCAD support team of Ph.D. physicists continuously developing models for new semiconductor technology advances.
• Replaces costly wafer experiments with simulations to enable shorter technology development cycles and higher yields.

Components

SSuprem4 – 2D Core Process Simulator
SSuprem4 is a 2D process simulator that is widely used in the semiconductor industry for design, analysis and optimization of various fabrication technologies. SSuprem4 accurately simulates all major process steps in modern technology by using a wide range of physical models for diffusion, ion implantation, oxidation, etching, deposition, silicidation, epitaxy and stress formation.

MC Implant – Advanced Monte Carlo Implantation Simulator
MC Implant is a generic ion implantation simulator, which models ion stopping, defect generation, and ion implantation distributions in amorphous and crystalline materials. Extensive comparisons with measured profiles have shown that MC Implant is highly accurate and predictive. The simulator can be used for a variety of ion/material combinations, arbitrary geometries, different substrate orientations, implant doses, energies and angles.

Elite – Advanced Physical Etching and Deposition Simulator
Elite is an advanced 2D topography simulator for modeling physical etching, deposition, reflow and CMP planarization processes for modern semiconductor technologies. Within the ATHENA framework, Elite provides seamless bi-directional integration with SSuprem4 and Optolith process simulators and contains an additional MC Deposit/Etch module, which provides several Monte Carlo based atomistic etching and deposition models.

MC Deposit/Etch – 2D Monte Carlo Deposition and Etch Module
MC Deposit/Etch is an advanced topology simulation module seamlessly interfaced with Elite, through the ATHENA framework. The module includes several Monte Carlo based models for the simulation of etch and deposit processes which use fluxes of atomic particles.

Optolith – 2D Optical Lithography Simulator
Optolith is a powerful non-planar 2D lithography simulator that models all aspects of modern deep sub-micron lithography: imaging, exposure, photoresist bake, development and reflow. Optolith provides a fast and accurate alternative to experimental evaluation of mask printability and process control. Optolith simulates both projection imaging and proximity printing with a large mask-to-resist gap.

More details can be found elsewhere:
http://www.silvaco.com/products/process_simulation/athena_datasheet_b.html

2.- SILVACO: VICTORY PROCESS. Full Physical 3D Process Simulator

VICTORY PROCESS is an open architecture process simulator. VICTORY PROCESS includes a complete set of advanced models for etch, deposition, implantation, diffusion and oxidation. Company proprietary models and public domain research models can be easily integrated into VICTORY PROCESS through its open architecture making it suitable for both commercial and academic applications. VICTORY PROCESS replaces costly wafer experiments with simulations to deliver shorter process development cycles.

1. **Key Features:**

- Accurately predicts 3D topology, 3D dopant distribution and 3D stress profiles
- Automatic meshing and Adaptive Mesh Refinement of tetrahedral and hierarchical Cartesian meshes
- Input file syntax is compatible with ATHENA simulation decks
- Capable of simulating a wide range of technologies from semiconductor fabrication to surface mounted MEMS and hard coatings for media and tribological applications
- Open architecture allows easy introduction and modification of customer specific physical models

- Sophisticated, multi-particle and multi-threaded ballistic flux models for physical deposition and etching with substrate material redeposition
- Viscous oxidation model and fast implantation and diffusion models
- High stability due to novel approach to the moving boundary problem
- Fast 3D structure prototyping capability enables the in-depth physical analysis of specific processing issues
- Links seamlessly to state-of-the-art 3D device simulators

More details can be found elsewhere:
http://www.silvaco.com/products/vwf/athena/victory/victory_datasheet.html

3.- PROMIS. 2D Process simulator (http://www.iue.tuwien.ac.at/4.8.0.HTML)
PROMIS (PROcess Modeling In Semiconductors) is a two-dimensional simulation program for ion implantation and diffusion processes. Built-in models exist for coupled point defect-dopant diffusion and various high-concentration effects.
Main features:
• PROMIS has a user interface which allows easy implementation of a large class of elliptic and parabolic systems of nonlinear, coupled partial differential equations (PDEs) with fairly general boundary conditions. Therefore, PROMIS is also well suited as a tool for the development and prototyping of new physical models.
• The PDE solver employs finite differences for space discretization and the Backward Euler method for time discretization. PROMIS generates an adaptive grid and has an automatic time step control.
• Ion implantation in PROMIS can be treated both by an analytical model taking into account depth dependent lateral moments, and by a Monte Carlo model allowing the simulation of ion implantation in fairly arbitrary structures such as trenches and multi-layer structures.

4.- SYNOPSYS. Taurus-Workbench (http://www.synopsys.com)

Synopsys has four process simulation tools: Sentaurus Process; Taurus TSUPREM-4; Sentaurus Lithography; and Sentaurus Topography.

Sentaurus Process
Sentaurus Process is an advanced 1D, 2D and 3D process simulator for developing and optimizing silicon semiconductor process technologies. It is a new-generation process simulator for addressing the challenges found in current and future process technologies. Equipped with a set of advanced process models, which include default parameters calibrated with data from equipment vendors, Sentaurus Process provides a predictive framework for simulating a broad range of technologies from nanoscale CMOS to large-scale high-voltage power devices. Sentaurus Process is part of a comprehensive suite of core TCAD products for multi-dimensional process, device, and system simulations, embedded into a powerful user interface.
Characteristics:
- Fast prototyping, development, and optimization of a broad range of technologies with comprehensive physics-based process modeling capabilities.
- Enhance device performance by optimization of thermal and mechanical stress in process structures with stress history.
- Provides insights into advanced physical phenomena through self-consistent multi-dimensional modeling capabilities.

Taurus TSUPREM-4

Taurus TSUPREM-4 is an advanced 1D and 2D process simulator for developing semiconductor process technologies and optimizing their performance. With a comprehensive set of advanced process models, Taurus TSUPREM-4 simulates the process steps used for fabricating semiconductor devices, reducing the need for costly experiments using silicon. In addition, Taurus TSUPREM-4 has extensive stress modeling capabilities, allowing optimization of stress to increase device performance.

Characteristics:

- Develop cost effective, leading-edge CMOS, bipolar, and power device manufacturing processes.
- Predict 1D and 2D device structure characteristics by accurately simulating ion implantation, diffusion, oxidation, silicidation, epitaxy, etching and deposition processing, reducing experimental runs and technology development time.
- Analyze stress history in all layers as a result of thermal oxidation, silicidation, thermal mismatch, etching, deposition and stress relaxation.
- Study impurity diffusion, including oxidation-enhanced diffusion (OED), transient-enhanced diffusion (TED), interstitial clustering, dopant activation and dose loss.

Sentaurus Lithography

Sentaurus Lithography represents computational lithography within TCAD Sentaurus, the physics-oriented technology simulation product family. The simulator covers a wide range of applications in optical, immersion, extreme ultraviolet (EUV) and electron beam (e-beam) lithography, allowing predictive modeling and thorough analysis of fundamental effects. The integration of Sentaurus Lithography with Sentaurus Topography allows seamless modeling of complex technologies such as double patterning. The interfaces of Sentaurus Lithography to Synopsys applications in the area of design and mask synthesis accelerate the generation of OPC models, minimizing process variability.

Sentaurus Topography

Sentaurus Topography is an advanced simulator for physical modeling of topography-modifying process steps such as deposition, etching, spin-on-glass, reflow and chemical-mechanical polishing. It supports complex process structures of multiple layers with different material properties, using advanced physical models and numeric algorithms. Sentaurus Topography is also ideal for predicting the topography of back-end processes by simulating the complex steps used to build the interconnect layers.

Process development engineers can use Sentaurus Topography to optimize existing processes and to develop new process flows. In manufacturing, Sentaurus Topography is a key tool to study the effects of misalignment and process variation to improve process capability and yield.

In addition, the interface between Sentaurus Topography and Sentaurus Process allows users to combine front-end thermal and topography simulations in one environment. Sentaurus Topography is fully integrated into Sentaurus Workbench, a state-of-the-art TCAD framework and visualization tool.

Characteristics

- Simulates profile evolutions of deposition and etching processes, including APCVD, LPCVD, PECVD, HDP CVD, wet etch, reactive ion etch (RIE), ion milling and sputter etch.
- Emulates reflow, spin-on-glass and chemical-mechanical polishing.
- Simulates etching characteristics under different reactor conditions leading to sidewall bowing, etchback planarization and RIE lag effects.
- Investigates impact of sidewall angle and deposition conditions on trench or contact filling and void formation.

- Characterizes plasma discharge and sheath transport mechanisms including plasma (ions and neutral) angle and energy distribution at wafer surface

5.- DADOS: An Atomistic KMC Simulator for advanced Silicon processing (http://www.ele.uva.es/~simulacion/)

Atomistic process modeling, a kinetic Monte Carlo simulation technique, has the interest of being both conceptually simple and extremely powerful. Instead of reaction equations it is based on the definition of the interactions between individual atoms and defects. Those interactions can be derived either directly from molecular dynamics or first principles calculations, or from experiments. The limit to its use is set by the size dimensions it can handle, but the level of performance achieved by even PC's, together with the design of efficient simulation schemes, has revealed it as a good candidate for building the next generation of process simulators, as an extension of existing continuum modeling codes into the deep submicron size regime.

Why atomistic KMC Process Simulators?

Compared to standard Continuum Process Simulators, the advantages of atomistic KMC Process Simulators are:

- Direct relation to microscopic data (from ab-initio or from experiments)
- Multiple mechanisms are included simultaneously with no simulation-time cost
- No convergence problems (there are no equations)
- Intrinsically three-dimensional.
- Specially efficient when dimensions shrink
- Highly non-equilibrium conditions are not an issue.
- Discrete character of dopants (local inhomogeneities).
- No topology problems with moving boundaries.
- Capture cross sections of extended defects directly given by the geometry.
- Intuitive view of the microstructure (easy comparison to TEM micrographs).

DADOS (**D**iffusion of **A**tomistic **D**efects **O**bject-oriented **S**imulator) is the atomistic KMC Process Simulator developed by Martin Jaraiz and coworkers at the Department of Electronics of the University of Valladolid. It is suitable for the simulation of front-end processes in advanced, deep-submicron Silicon-based technologies. DADOS can be used either as a research or a TCAD tool.
For TCAD use, DADOS is commercialized by Synopsys Inc., CA, as a core element of the Sentaurus Process simulator. For research purposes, DADOS is used as the engine of UVAS (University of Valladolid Atomistic Simulator), a simulation environment (running under MS-Windows) that controls DADOS and allows the extraction of simulation results.

References

Key Groups in the WORLD

[1] Silvaco International is a leading provider of electronic design automation (EDA) software for analog and mixed-signal integrated circuit design. Santa Clara (CA, USA)
[2] Synopsys, Inc. Corporate Headquarters 700 East Middlefield Road Mountain View, (CA, USA)
[3] Professor Dutton's TCAD group. Department of Electrical Engineering 161 Packard Building, 350 Serra Mall Stanford, (CA, USA)
[4] Professor Mark Law. Department of Electrical and Computer Engineering 535, NEB, University of Florida (USA)
[5] Professor Martín Jaraiz at the University of Valladolid, Spain.

European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Technische Universität Wien, (Austria) ETH Zurich, (Switzerland) University of Valladolid (Spain)	Knowledge related to almost all the processes involved in the fabrication of devices. Attempts to build tools. Experimental and fabrication facilities to develop model and to tune simulators.	Not coordination. Efforts extremely scattered. Lack of reliable and complete tools. Specific models for key SOI process steps.

Conclusions and recommendations

There are research groups in Europe related to process simulations, however the reliable tools available for the industry come from very few companies or research groups at universities. The efforts in this field seem to be scattered all along Europe and not coordinated at all. Therefore, a European coordination of the know-how, and most important the possibility to build a tool complete and reliable enough to be used by industrial partners in the developments efforts would be very desirable.

EUROSOI State of the Art Report

Chapter 5. Devices. Simulation and Modeling
Section 5.2 Device Simulation
Subsection 5.2.1. Introduction

Date of Issue: Aug – 2009	**Partner: University of Granada**

Abstract

Device modeling is used for scaling studies and technology optimization; therefore, the ability to correctly represent today's performance and predict tomorrow's limitations is paramount.

Introduction

Device simulation is used to predict the behavior of SOI devices. The flexibility of SOI technology has permitted much new geometries rather than classical MOSFET (e.g. FINFET, GAA) or the possibility to implement concepts never used before on Si (e.g. Velocity Modulation, optical waveguides).In this view, new device structures can be checked and compared by simulation in order to select the most advantageous configuration. This is particularly useful at the early stage of technology development, where the measured devices are still affected by the poor quality of the SOI material, and a large amount of interface states and recombination centers strongly reduce the device performances. Each effect related with the introduction of new device structure and/or channel material can be studied in a separate way in order to give advice to technology development.

In the simulation tools, the device under study is represented by a physical model that leads to a set of equations (usually in a continuous space) solved using different techniques or numerical methods.

Basically, two main set of solvers can be found. The commercial tools are focused on industrial applications. They permit to perform simulations using a friendly interface and well established physical models, usually calibrated in order to reproduce the characteristics of conventional Bulk MOSFETs. These tools are usually unable to correctly describe the physical effects taking place in advanced devices such as FD SOI and SOI with non conventional channels (strain channel, orientation other than (100), etc). To tackle these issues, research solvers are developed at universities and R&D departments to study new geometries and new effects, and are based on more accurate physical models.

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EUROSOI State of the Art Report

Chapter 5. Device Simulation and Modeling
Section 5.2. Device Simulation
Subsection 5.2.2. Device models and model approximations

Date of Issue: April – 2009	**Partner: University of Granada**

Abstract

Device modeling refers to a suite of models and methods describing carrier transport, potential and field distribution in different materials. Several modeling approaches, physical approximations and numerical techniques can be used depending on the problem under study and the required level of detail. We here review the most common of the approaches with special emphasis to recent developments concerning SOI devices.

Introduction

Device modeling refers in general to a suite of models and methodologies to describe carrier transport, potential and field distribution in materials. In general terms two problems must be solved in a consistent way: The electrostatic problem, that is the spatial distribution of charges and potentials in the device; the transport problem, that is the way carriers move in the given potential profile. For each of these problems, different levels of complexity can be found.

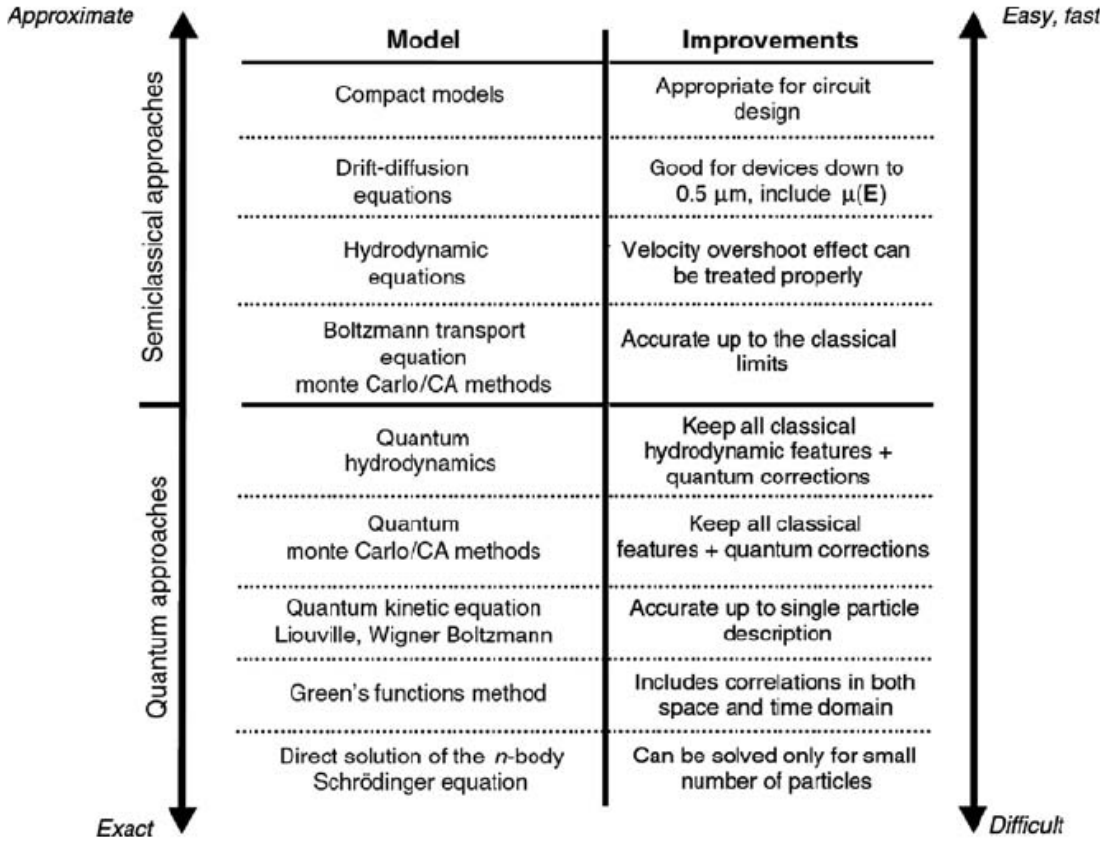
As for the transport, we go from the simple Drift Diffusion model to more complex and CPU intensive Hydrodynamic and Energy Balance models based on the momenta of the Boltzmann Transport Equations (BTE). The complex carrier transport physics of ultra short devices, especially on SOI substrates, mandates at times the usage of Monte Carlo codes, which stochastically solve the Boltzmann Transport Equation in an exact way. Simplified analytical solutions of the BTE can sometimes provide useful hints for interpreting the results of detailed numerical simulations.

As for the electrostatic problem, the Poisson equation has obviously to be solved. The small feature sizes of state of the art devices demand the usage of Schrödinger solvers that account for quantum effects on the spatial charge distribution. This latter point is especially relevant for Ultra Thin Body SOI transistors, where size-induced quantization can influence substantially the electrostatic behavior of the device. Quantization is also well known to influence the scattering mechanisms of the carriers in the inversion layer, and therefore has implications also on the transport properties.

Most model implementations at the research level can handle only 1D or 2D geometries; commercial tools are often 3D in real space but available transport and quantization models are limited to few choices based on the momenta of the BTE.
The choice of the appropriate model depends on the problem, the device architecture and the level of details required and it is therefore left to the user. Some of the combinations most widely used are:

- Poisson + Drift-Diffusion [all commercial tools]
- Poisson + Hydrodynamic (Moments of the BTE) [all commercial tools]
- Poisson + Monte Carlo [1, 2]
- Poisson + Schrödinger + Monte Carlo [3]

- NEGF (Non Equilibrium Green Functions) [4]
- Fully Ballistic transport (2D Poisson + 2D Schrödinger) [5]
- Partial ballistic (2D Poisson + 1D Schrödinger for each section)
- Deterministic Solution of BTE [6]



Hierarchy of transport approaches used in the description of electronic transport in semiconductors [7, 8]

Device modeling is used for scaling studies and technology optimization; therefore, the ability to correctly represent today's performance and predict tomorrow's limitations is paramount. The flexibility of SOI technology has permitted much new geometries rather than classical MOSFET (e.g. FINFET, GAA) or the possibility of implementing concepts never used before on Si (e.g. Velocity Modulation). Thus, simulation tools should be able to handle specific SOI requirements:

- Fully Depleted and Partially Depleted channels
- Floating body effects
- Single, Double, Triple Gate and Gate all around architecture
- Self heating effects
- Defects and charges at the Si-Insulator interface
- Size induced quantization in the vertical direction (and consequent splitting between 2-fold and 4-fold subbands in 100 silicon)

In addition, since the SOI MOSFET is nowadays the most scalable device concepts, physical effects relevant in ultra short devices can be exacerbated in SOI devices. Among these:

- Tunneling and Transport in the thin gate dielectrics
- Source/Drain tunneling
- High k dielectric non-ideality

Numerical methods refer to the different strategies and mathematical methods carry out to face the problem to solve. Discretization, including mesh design, and resolution methods are its two main aims. Specific numerical problems can stem as a result of the model approach and approximations used.

Most of the device model equations are written in a continuous space (e.g. Poisson's equation) therefore, derivatives and integral have to be approximate by discrete and accurate enough expressions which allow us to write the equations as a function of the grid points. Uniform mesh results in huge amount of grid points to obtain accurate results or good convergence, leading to unacceptable execution times even for 2D simulations (not only for 3D). Non-uniform meshes and adaptative grids change the number of points depending on the variation of some magnitudes in a local sense including more grid points in sensitive areas (e.g. interfaces) reducing the final matrix dimension and the convergence time comparing to uniform meshes. With these methods, matrix become non-symmetric, thus symmetrization algorithms are applied allowing the use of fast solvers. Adaptative grid method uses interpolation algorithms to obtain the value of the magnitudes in the new mesh points. Meshing algorithms must guarantee that discretization errors caused by the removal or by the movement of mesh nodes do not negatively affect the simulation results: Especially for applications in sensitivity analysis it must be guaranteed that changes of the results are due to physical reasons and not critically affected by changes of the meshes used in the different simulations.

Concerning solving methods, iterative methods such as SOR (Successive Over Relaxation) or Newton-like schemes are widely used. Direct methods (or pseudo-direct methods) speed up linear solvers when sparse matrix theory can be applied due to the fast inversion matrix algorithms. Conjugate Gradient for definite positive symmetric matrix and Biconjugate Gradient for general matrix both of them using preconditioner for linear systems of equations and Arnoldi decomposition for eigen-values problems are some of the standard methods.

The self consistent solution of the Schrödinger and Poisson equations poses specific stability problems because of the non-local nature of the coupling between potential and charge in a quantized system [9].
Finally, statistical solutions of the BTE with the Monte Carlo method also pose specific problems related to the stability of the self-consistent loop with the Poisson equation and the estimation of the statistical convergence of the results. Recent developments in the modeling of the convergence properties of MC-Poisson loops allowed to define helpful criteria to steer the choice of simulation parameters for stable solutions [10, 11, 12]. Moreover, "real" random number generators are also very important for general stochastic methods (e.g. Monte Carlo) implementation.

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Key Groups in the World:

University of Florida, Gainesville, Florida, USA
Arizona State University, Tempe, Arizona, USA
IBM Watson Research Center, USA
University of Illinois at Urbana Champaign, Illinois, USA
Purdey University, West Lafayette, Indiana, USA

European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
Integrated Systems Laboratory, Zurich (Switzerland) Technische Universität Wien (Austria) (SC) University of Glasgow (UK) (SC) University of Granada (Spain) (SC) University of Udine (Italy) (SC) University of Salamanca (Spain) University of Pisa (Italy) University of Bologna (Italy)	-Well established models for electron transport in thick and thin layers -Standard tools full compatible for conventional concept devices	-Specific SOI features have to be completely included -Ultra thin layer transport and high-k materials models under development

Conclusions and recommendations

Device models and numerical methods have been developed to perform scaling studies and technology optimization. Specific simulation tools have to be developed to take into account SOI characteristics and phenomena, especially in the ultra thin body case.

EUROSOI State of the Art Report

Chapter 5. Devices. Simulation and Modeling.
Section 5.2. Device Simulation
Subsection 5.2.3. Capabilities of Commercial Simulation Tools

Date of Issue: May – 2009	**Partner: University of Granada**

Abstract

Commercial tools are focused on industrial applications. They permit to perform simulations using a friendly interface and well established physical models obtaining reasonably accurate results in a computing time short enough to use the tool during the product develop process. However, these tools usually lack the capability to correctly model non-conventional structures (GAA, finFET, FD SOI) and the strong non-equilibrium transport effects taking place in decananometric devices.

Introduction

In the following we describe the main features of some commercial tools for device simulation. It must be remarked that these tools were originally developed for the study of conventional Bulk MOSFETS, and that the capability to simulate SOI devices has been added in a second time. In particular, models to describe the mobility reduction in thin film SOI devices are typically not included in these commercial simulators. Quantum effects are being incorporated in new versions. Carrier transport is based on the drift-diffusion or energy-balance models, and they are unable to correctly describe non-equilibrium transport in decananometric channels.

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- **1.- SILVACO: ATLAS Device Simulation Software** (http://www.silvaco.com)
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ATLAS enables device technology engineers to simulate the electrical, optical, and thermal behavior of semiconductor devices. ATLAS provides a physics-based, easy to use, modular, and extensible platform to analyze DC, AC, and time domain responses for all semiconductor based technologies in 2 and 3 dimensions.

Key Features

• Accurately characterize physics-based devices in 2D or 3D for electrical, optical, and thermal performance without costly split-lot experiments.
• Solve yield and process variation problems for optimal combination of speed, power, density, breakdown, leakage, luminosity, or reliability.
• Fully integrated with ATHENA process simulation software, comprehensive visualization package, extensive database of examples, and simple device entry.
• Choose from the largest selection of silicon, III-V, II-VI, IV-IV, or polymer/organic technologies including CMOS, bipolar, high voltage power device, VCSEL, TFT, optoelectronic, LASER, LED, CCD, sensor, fuse, NVM, ferro-electric, SOI, Fin-FET, HEMT, and HBT.
• Connect TCAD to Tapeout with direct import of ATLAS results into UTMOST for SPICE parameter extraction.

2D Device Simulation Modules

S-Pisces – 2D SILICON DEVICE SIMULATOR
S-Pisces is an advanced 2D device simulator for silicon based technologies that incorporates both drift-diffusion and energy balance transport equations. A large selection of physical models are available which include surface/bulk mobility, recombination, impact ionization and tunneling models. Typical applications include MOS, bipolar, and BiCMOS technologies. The capabilities of all the physical models have been extended to deep submicron devices, SOI devices, and non-volatile memory structures.

Blaze – 2D DEVICE SIMULATOR FOR ADVANCED MATERIALS
Blaze simulates devices fabricated using advanced materials. It includes a library of binary, ternary and quaternary semiconductors. Blaze has built-in models for graded and abrupt heterojunctions, and simulates binary structures such as MESFETS, HEMT's and HBT's.

MC Device – 2D MONTE CARLO DEVICE SIMULATOR
MC Device simulates the behavior of relaxed and strained silicon devices including non-equilibrium and ballistic effects in 2D. MC Device is part of the ATLAS Device Simulation Framework and is fully integrated with Interactive Tools.

Giga – 2D NON-ISOTHERMAL DEVICE SIMULATOR
Giga combined with the S-Pisces or Blaze device simulators allows simulation of self heating effects. Models in Giga include heat generation, heat flow, lattice heating, heat sinks, and effects of local temperature on physical constants. Thermal and electrical physical effects are coupled through self-consistent calculations. Giga is a fully integrated component of the ATLAS device simulation framework.

Luminous – 2D OPTOELECTRIC DEVICE SIMULATOR
Luminous is an advanced device simulator specially designed to model light absorption and photogeneration in non-planar semiconductor devices. Exact solutions for general optical sources are obtained using geometric ray tracing. This feature enables Luminous to account for arbitrary topologies, internal and external reflections and refractions, polarization dependencies and dispersion. Luminous also allows optical transfer matrix method analysis for coherence effects in layered devices. The beam propagation method may be used to simulate coherence effects and diffraction.

LED – 2D LIGHT EMIITING DIODE SIMULATOR
LED is a module used for simulation and analysis of light emitting diodes. LED is integrated in the ATLAS framework with the BLAZE simulator and allows simulation of electrical, optical and thermal behavior of light emitting diodes.

Organic Solar – ORGANIC SOLAR CELL AND PHOTODETECTOR SIMULATOR
The Organic Solar module enables ATLAS to simulate the electrical and optical properties of organic solar cell devices, photodetectors and image sensors. Organic Solar is integrated into the ATLAS framework and allows the steady-state, transient and AC simulation of the electrical and optical behavior of photovoltaic organic devices. The exciton densities, diffusion, generation/recombination and dissociation characteristics can all be simulated.

MixedMode – CIRCUIT SIMULATION FOR ADVANCED 2D DEVICES
MixedMode is a circuit simulator that includes physically-based devices in addition to compact analytical models. Physically-based devices are used when accurate

compact models do not exist, or when devices that play a critical role must be simulated with very high accuracy. The physically-based devices may be simulated using any combination of ATLAS 2D modules. The physically-based devices are placed along side a circuit description that conforms to SPICE netlist format.

Laser – SEMICONDUCTOR LASER DIODE SIMULATOR
Laser is the world's first commercially available simulator for semiconductor laser diodes. Laser works in conjunction with Blaze in the ATLAS framework to provide numerical solutions for the electrical behavior (DC and transient responses) and optical behavior of edge emitting Fabry-Perot type lasers diodes.

Quantum – 2D SIMULATION MODELS FOR QUANTUM MECHANICAL EFFECTS
Quantum provides a set of models for simulation of various effects of quantum confinement and quantum transport of carriers in semiconductor devices. A self consistent Schrodinger – Poisson solver allows calculation of bound state energies and associated carrier wave functions self consistently with electrostatic potential. Schrodinger solvers can be combined with Non-equilibrium Green's Function (NEGF) Approach in order to model ballistic quantum transport in 2D or cylindrical devices with strong transverse confinement. Quantum also includes models for the quantum mechanical corrections to drift-diffusion and hydrodynamic equations.

3D Device Simulation Modules

Device3D – 3D DEVICE SIMULATOR
Device3D is a 3D device simulator for silicon and other material based technologies. The DC, AC and time domain characteristics of a wide variety of silicon, III-V, II-VI and IV-IV devices can be analyzed. Device3D accurately characterizes physics-based devices for electrical, optical, and thermal performance without costly split-lot experiments. Device3D solves yield and process variation problems for optimal combination of speed, power, density, breakdown, leakage, luminosity and reliability.

Thermal3D – THERMAL PACKAGING SIMULATOR
Thermal3D is a general heatflow simulation module that predicts heatflow from any power generating devices (not limited to semiconductor devices), typically through a substrate and into the package and/or heatsink via the bonding medium. Operating temperatures for packaged and heat sinked devices or systems can be predicted for the design and optimization phase or for general system analysis.

Giga3D – 3D NON-ISOTHERMAL DEVICE SIMULATOR
The Giga3D module extends Device3D by incorporating the effects of self-heating into a device simulation. It includes models for heat sources, heat sinks, heat capacity and thermal conduction. Physical and model parameters become dependent on the local lattice temperature where appropriate, allowing the self-consistent coupling between the semiconductor device equations and the lattice temperature.

Luminous3D – 3D OPTOELECTRIC DEVICE SIMULATOR
Luminous3D is an advanced simulator specially designed for analysis of optical response of non-planar semiconductor devices in three dimensions.

Quantum3D – 3D SIMULATION MODELS FOR QUANTUM MECHANCIAL EFFECTS
Quantum3D provides a set of models for simulation of various effects of quantum confinement and quantum transport of carriers in semiconductor devices. A self consistent Schrodinger – Poisson solver allows calculation of bound state energies

and associated carrier wave function self consistently with electrostatic potential. Schrodinger solvers can be combined with Non-equilibrium Green's Function (NEGF) Approach in order to model ballistic quantum transport in 3D devices with strong transverse confinement.

2.- SYNOPSYS: (http://www.synopsys.com)

Device simulation tools simulate the electrical characteristics of semiconductor devices, as a response to external electrical, thermal or optical boundary conditions imposed on the structure. The input device structure typically comes from process simulation steps using tools like Sentaurus Process or Taurus TSUPREM-4 or through CAD operations and process emulation steps with the aid of tools like Sentaurus Structure Editor. Synopsys offers two device simulation tools – Taurus Medici and Sentaurus Device. Taurus Medici is a 2D device simulation tool and Sentaurus Device is a 2D and 3D device simulation tool with the best features incorporated from Taurus Medici and ISE device simulator Dessis.

Sentaurus Device: An advanced multidimensional (1D/2D/3D) device simulator
Overview: Sentaurus Device is an advanced multidimensional device simulator capable of simulating electrical, thermal, and optical characteristics of silicon-based and compound semiconductor devices. Sentaurus Device is a new-generation device simulator for designing and optimizing current and future semiconductor devices.
Features: Sentaurus Device is a general purpose device simulation tool which offers simulation capability in the following broad categories:
• Conventional and Deep Submicron CMOS Technologies: Sentaurus Device can simulate all silicon and strained silicon technologies including Silicon Germanium (SiGe) pockets or other external stress sources. Advanced numerical capabilities can capture hot carrier effects, non-local and quantum effects for advanced applications. Sentaurus Device's 3D simulation capability can simulate narrow width effects in deep submicron devices, parasitic channel effect in shallow trench isolation and floating body effect in SOI structures.
• Compound Semiconductor Technologies: Sentaurus Device can simulate advanced quantization models including rigorous Schrödinger solution and complex tunneling mechanisms for transport of carriers in heterostructure devices like HEMTs and HBTs made from, but not limited to, GaAs, InP, GaN, SiGe, SiC, AlGaAs, InGaAs, AlGaN and InGaN.
• Optoelectronic Devices: Sentaurus Device has the capability to simulate the optoelectronic characteristics of semiconductor devices like CMOS image sensors, solar cells, and lasers. Options within Sentaurus Device also allow for rigorous solution of the Maxwell's wave equation using FDTD methods.
• Power Electronic Devices: Sentaurus Device is the most flexible and advanced platform for simulating electrical and thermal effects in a wide range of power devices such as IGBT, power MOS, LDMOS, thyristors, and high-frequency high-power devices made from wide band-gap material like GaN and SiC.
• Monte Carlo Device Simulation: Sentaurus Device offers a rigorous solution of Boltzmann's equation using robust and computationally efficient full band ensemble Monte Carlo methods for very small gate length devices.
• Memory Devices: With advanced carrier tunneling models for gate leakage and trapping de-trapping models, Sentaurus Device can simulate any floating gate device like SONOS and flash memory devices including devices using high-K dielectric.
• Radiation Effects: The impact of radiation on semiconductor device operations can be studied with Sentaurus Device. Both single event effects, which include single

event upset (SEU) and single event transient (SET), and total ionization dose (TID) effects can be simulated.
• Novel Semiconductor Technologies: Advanced physics and the ability to add user-defined models in Sentaurus Device allow for investigation of novel structures made from new material.

Taurus Medici: A 2D device simulator
Taurus Medici is a 2D device simulator that models the electrical, thermal and optical characteristics of semiconductor devices. A wide variety of devices including MOSFETs, BJTs, HBTs, power devices, IGBTs, HEMTs, CCDs and photodetectors can be modeled. Taurus Medici can be used to design and optimize devices to meet performance goals, thereby reducing the need for costly experiments.
With the continued scaling of CMOS devices, device design and optimization become more difficult. Previously unimportant phenomena, such as direct tunneling, can now dominate device performance and design criteria. The vast array of advanced transport and quantum models available in Taurus Medici allow users to perform accurate simulations of deeply scaled devices.
Characteristics:
• Analyze electrical, thermal and optical characteristics of devices through simulation without having to manufacture the actual device.
• Determine static and transient terminal currents and voltages under all operating conditions of interest.
• Understand internal device operations through potential, electric field, carrier, current density and recombination and generation rate distributions.
• Investigate breakdown and failure mechanisms, such as leakage paths and hot-carrier effects.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Integrated Systems Laboratory, Zurich (Switzerland)	-Well established models. -Friendly Human-Machine interface. -Fast convergence codes. - Quantum effects for SOI included in most cases	-Poor control on model definition -Lack of specific models for FD thin-film SOI, especially with regard to mobility and transport. -Transport models not accurate for sub-100nm channels (full solution of the BTE is required).

Conclusions and recommendations

Commercial simulation tools are designed mainly for developing purposes in an industrial environment. With optimized accurate/time consuming rates, commercial simulators are useful for studies based on well established models and geometries.
The use of 3D simulators allow the extension to non conventional geometries.
The simulation of channel materials differents to silicon are under development and should be further pursued. Specific models for ultra thin body SOI transport should be implemented.

EUROSOI State of the Art Report

Chapter 5. Devices. Simulation and Modeling
Section 5.2 Device Simulation
Subsection 5.2.4. Research Level Simulators

Date of Issue: Feb – 2010	**Partner: UDINE, UGR, USAL**

Abstract

Research simulation tools are used at universities and R&D departments to study new geometries, new effects and more accurate physical models with no restrictions on the computation time. Models and tools have been developed to deal with the modeling issues related to SOI structure and non-conventional materials (ballistic transport, high-k gate insulators, strained channels, etc.).

In this section we will describe some of the research tools developed by European and non-European groups.

Introduction

Commercial simulators provide numerically strong and optimized tools with a friendly interface, however, sometimes are not flexible enough for researching purposes in the sense of new geometrical configurations or full custom models. In particular, commercial tools are almost exclusively based on the Drift-Diffusion and Hydrodynamic models that are not accurate enough to describe non-equilibrium transport in nanoscale devices. To this purpose, Monte-Carlo tools, providing the full solution of the Boltzmann-Transport-Equation (BTE) are required. However, in most industrial environments, Monte Carlo simulations are not popular, due to the computing time, that delays the development of the technological process. Therefore some of the new features in simulation can be found on research simulators developed both in industry labs and universities.

Main limits of drift-diffusion tools:
Drift-diffusion simulators show a widespread use for the study of MOSFET devices in general and SOI transistors in particular. Starting from a macroscopic approach several restrictive hypotheses about the thermal equilibrium of carriers are considered and non-local effects are neglected. In this way, extremely efficient (from the computational point of view) simulators can be developed. However, when dealing with the investigation of ultra-short SOI transistors, some problems are to be solved: hot carrier effects and non-stationary phenomena must be incorporated in some way as corrections to the primary model if physically sound simulators are desired.
In particular, most of the commercial device simulators can be included in this category. These commercially available device simulation tools can be of help to gain the basic understanding of device electrostatics and to promote the development of simple in-house models by acting as a reference, together with experimental measurements, to confirm in a first step the reliability of the model developed. However, they present some important limitations: in addition to the already commented problems of drift-diffusion models (that in many cases are solved by using complex solutions in some critical areas, as in the case of MINIMOS, that implements a Monte Carlo module replacing occasionally the drift-diffusion kernel), they are still strongly parameter dependent (fundamentally by the adequate selection of mobility

models), it is not easy to analyze specific effects or detailed transport phenomena and their reliability is mainly limited to the static behavior (although nowadays many of them provide also the dynamic behavior and a strong effort is being devoted to the implementation of noise modules). Options such as the windowed Monte Carlo are rarely used and therefore not brought to the same degree of maturity of in house developed pure Monte Carlo codes. Their reliability is therefore somewhat limited.

A more elaborated approach is the hydrodynamic model. As the drift-diffusion model, it is also macroscopic and deterministic, but significantly more complex. Its main feature is that it incorporates the dependence of some key parameters of the model on the average carrier energy, also taking into account a more elaborate subset of the momentum equations derived from Bolztmann transport equation. The result is a model with a higher computer cost and in principle much more efficient for the investigation of small-size transistors. Moreover, some additional features of SOI devices such as carrier and lattice heating effects can be readily incorporated through the solution of carrier energy balance equations and lattice heat equation, as in the case of the commercially available device simulator Taurus-Medici^{TM}. However, the expansion of the Boltzmann transport equation in a set of momenta equations requires the definition of closure conditions that are often semi-empirical. As the number of momenta is increased (as recently proposed with the so called six-moment approach) these conditions become increasingly questionable, and certainly not well understood in terms of the underlying physics. It has already been proved, and recently further demonstrated, that many unphysical effect with huge impact on the computed solution can be obtained by using energy balance and/or Hydrodynamic models.

Another problem of these approaches is the inclusion of quantization. Several models have been proposed to correct the electrostatic potential, but they are usually unable to reproduce the quantization effects present in FD SOI devices, that requires the solution of the Schrödinger equation. The impact of quantization on the transport properties in the framework of the momenta based expansion of the BTE is an essentially unaddressed problem in the electron device modeling community.

Concerning Drift-Diffusion and Hydro-Dynamic modeling approaches, we remark the following works made by European groups:

- Infineon Technol. (Munich, Germany) have investigated, using a drift-diffusion model, several parameters as gate length, Si body thickness, etc. in FD SOI with gate length between 25 and 50 nm [1].
- Vienna Tech Univ. (Austria), investigated anomalous output characteristics provided by hydrodynamic and drift diffusion simulations [2, 3].
- Research groups from the CNRS (Marseille, France) and the Dept. Silicon Technol., CEA (Grenoble, France), have investigated unphysical phenomena occurring in hydrodynamic simulation of realistic PD SOI MOSFET [4].
- In the Swiss Fed. Inst. Technol. (Zurich, Switzerland) they analyze quantum mechanical effects for a DG SOI MOSFET and compare to the result obtained using a 1D Schrödinger-Poisson solver [5].

Simulation of noise and RF performances:

One additional drawback of hydrodynamic and drift-diffusion tools is that they do not provide the instantaneous distribution of carrier velocity or current at terminals including fluctuations due to random carrier motion, thus not being adequate for the direct study of noise. An indirect solution is frequently considered, namely the Shockley's Impedance Field Method: through the consideration of local noise sources provided by physical descriptions of diffusive noise or by Monte Carlo simulations, it is possible to obtain excellent results as compared to experimental measurements. However, though providing a strong physical background about the different regions contributing to

noise, the primary noise sources are not incorporated in a natural way, as previously mentioned, so highest-level research simulation tools are required to properly account for the complexity of noise behavior in downsized SOI transistors.

The Monte Carlo method is based on a microscopic description of the movement of carriers inside the device. In this way, it is possible to solve instantaneously the Boltzmann equation, thus avoiding the problems of the models previously mentioned. Moreover, it provides the distribution functions of all relevant quantities, such as velocity or energy of carriers, and it is able to supply the energy dependence of some parameters required by the hydrodynamic approach. Important phenomena occurring in submicrometric devices are incorporated in a natural way, such as hot carrier effects or non-stationary transport. The Monte Carlo approach is inherently very modular in terms of scattering mechanisms that can be incorporated in the models, so that new physics can be quite easily added to the simulation. Another important advantage provided by the Monte Carlo method is that it reproduces in a natural way the random features of transport, thus allowing to study noise phenomena and providing noise sources without making any assumption about their physical origin: no pre-existing knowledge about the nature of noise in a particular material or device is required (as it happens in the Shockley's Impedance Field Method). The promising noise performance of SOI transistors in the RF domain adds to the reasons for their success and the use of noise-level simulators (together with an accurate development of compact models) becomes mandatory. Dealing with Monte Carlo simulation tools, some different possibilities exist, such as single particle and ensemble simulators or the most complex one, the Monte Carlo device simulator in 1D, 2D or 3D. Monte Carlo simulation of SOI devices represent nowadays a very active field where several European research groups occupy positions of unprecedented excellence. Issues addressed by these grous include, without being limited to, mobility characteristics, electronic transport features in Double Gate transistors, scalability of the ultra thin body SOI concept or the properties of strained thin Silicon films.

Device ensemble simulators can be viewed as global modeling tools, since they provide not only the static current-voltage characteristics and average internal quantities, but also the main dynamic and noise parameters of interest. The calculation of dynamic parameters is usually performed through the Fourier analysis of the transient response of current when voltage steps are applied at terminals. Noise sources are provided through the spectral analysis of instantaneous gate and drain current fluctuations in common source configuration. Combining noise sources and admittance parameters, the main intrinsic noise parameters and extrinsic circuital figures of merit (NF_{min}, R_n, etc.) are determined. With this background, the basis for the global study of devices is set up; however, the special features of advanced SOI devices require some special features that we are going to comment now.

Some activities in Europe in the field of noise simulation are reported in the following:
-The Electronics Group of the Univ. Salamanca (Spain) has developed a 2D ensemble Monte Carlo simulator for the study of n-type and p-type SOI devices. In particular, works regarding the comparison of the high-frequency behavior of bulk and FD SOI MOSFETs, as well as the experimental investigation of FD transistors, have been achieved, treating also the investigation of the noise performance of the transistors in the RF domain [6, 7].
- In the Tech. Univ. Ilmenau (Germany) a semiclassical ensemble Monte Carlo simulator has been employed to analyze excessive noise in ultra-scaled DG MOSFETs, though not considering channel quantization [8]
- The group at the TU Braunschweig (Germany) has devoted many efforts to the study of noise in scaled devices using Monte-Carlo and Hydrodynamic tools. A review of their work can be found in [9] and references therein.

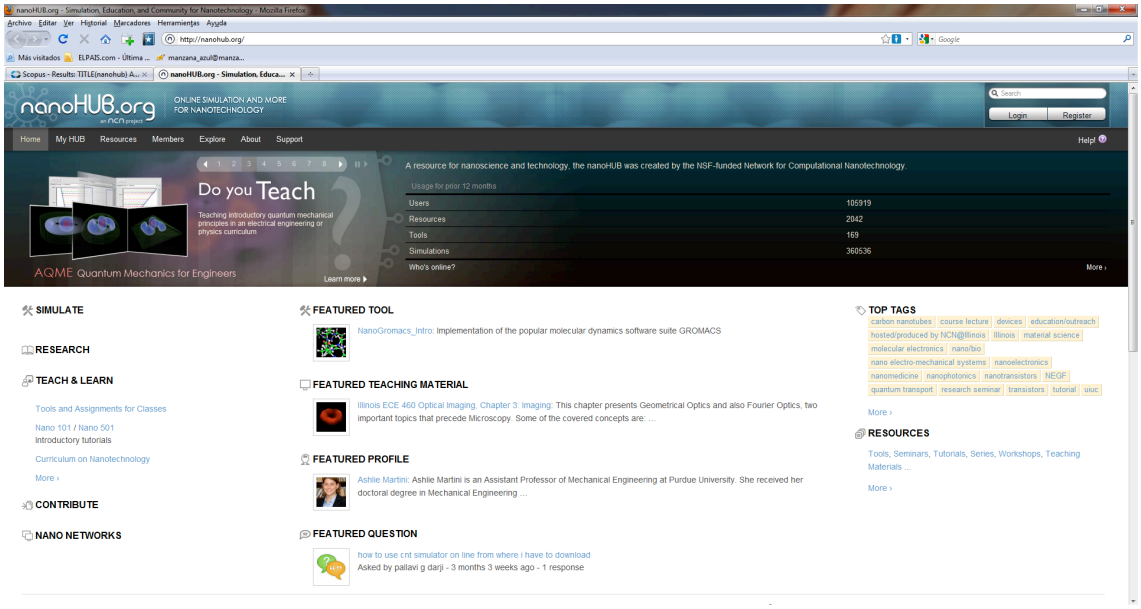
Modeling issues in decananometric MOSFETs:
Electronic transport simulation in ultimate devices requires a full many-body quantum mechanical description going beyond the usual ground state descriptions of solids used in ab initio calculations of the electronic states. Clearly, a full many particle description of transport including the real number of particles in both the device, its contact to the external environment, and the external environment itself, is beyond the ability of any computational platform in the foreseeable future. Hence, successive levels of approximation that sacrifice information about the system and the exact nature of transport are necessary in any sort of realistic description of transport.

For the specific case of simulating the carrier transport and drain current of deca-nanometric MOSFETs, the most relevant modeling ingredients necessary for an accurate simulation have not been completely understood yet.
Difficulties arise from several factors: the need to account for the strong quantum mechanical effects induced by vertical confinement in the conduction film; the unknown transport regime (ballistic or scattering limited); the unknown importance of new scattering mechanisms not present in bulk MOSFETs (e.g., related to SO phonons, film thickness fluctuations); the unknown importance of interference and quantum transport effects in the lateral direction; the possible tunneling through the source barrier and wave-function penetration in the dielectric layer; etc. All these unknowns, stimulated the research community to pursue a variety of modeling approaches.
Experimental results [10] recently confirmed in [11] demonstrated that a degradation of mobility occurs in ultra thin (UT) silicon films with thickness below approximately 10nm and that a small but unambiguous increase of mobility at low inversion charge density is observed in double gate operation with respect to single gate operation of UTB SOI devices. Moreover, a reduction of mobility has been observed when the SiO2 layer is thinned below approximately 2nm [12,13]. A viable approach to tackle the problem is to calculate the scattering rates for the quantized 2D electron gas in the inversion layer and then compute zero-lateral-field mobility using either the momentum relaxation time approximation (MRT) [14,15] or the Monte-Carlo method [17,18].
A difficult task is the extension of these tools, developed to study the low-field mobility, to 2D device simulation tools able to simulate the drain current of advanced MOSFETs such as nanowires.
In theory, also these tools should be based on the scattering rates for the quantized 2D electron gas in the inversion layer. This requires the development of Multi-subband Monte-Carlo tools [19,20], or the implementation of quantum corrections in semi-classical Monte-Carlo simulation. Such tools are extremely promising also in view of the possibility to emulate ballistic transport by simply switching off the scattering in different parts of the channel. Quantum mechanical tunnelling through the source barrier can also be included in ways similar to what has been done in the past for carrier injection through the gte dielectric. Moreover, by changing the band structure and scattering rate description the same simulation machinery can in principle address also devices with channels made of different materials. One problem with this latter approach is that the commonly used classical solution to model surface roughness scattering, i.e the combination of diffusive and reflective scattering, is no longer valid when dealing with quantized channels [21].

Overview of some Research simulation codes: Several researching groups have developed their owns codes, some of them are commented below.

Nanohub (Purdue University) http://www.nanohub.org

Nanohub is a resource for nanoscience and technology, the nanoHUB was created by the NSF-funded Network for Computational Nanotechnology [22,23].
The simulation tools and resources available at nanoHUB.org offer significant opportunities for both research and education in computational nanoelectronics. Users can run simulations on existing powerful computational tools rather than developing yet another niche simulator. The worldwide visibility of nanoHUB provides tool authors with an unparalleled venue for publishing their tools. The educational resources of nanoHUB are one of the most important aspects of the project, according to user surveys. New collections of tools into unified curricula have found a receptive audience in many university classrooms. The underlying cyberinfrastructure of nanoHUB has been packaged as a generic software platform called HUBzero. The Rappture toolkit, which generates simulation GUIs, is part of HUBzero.

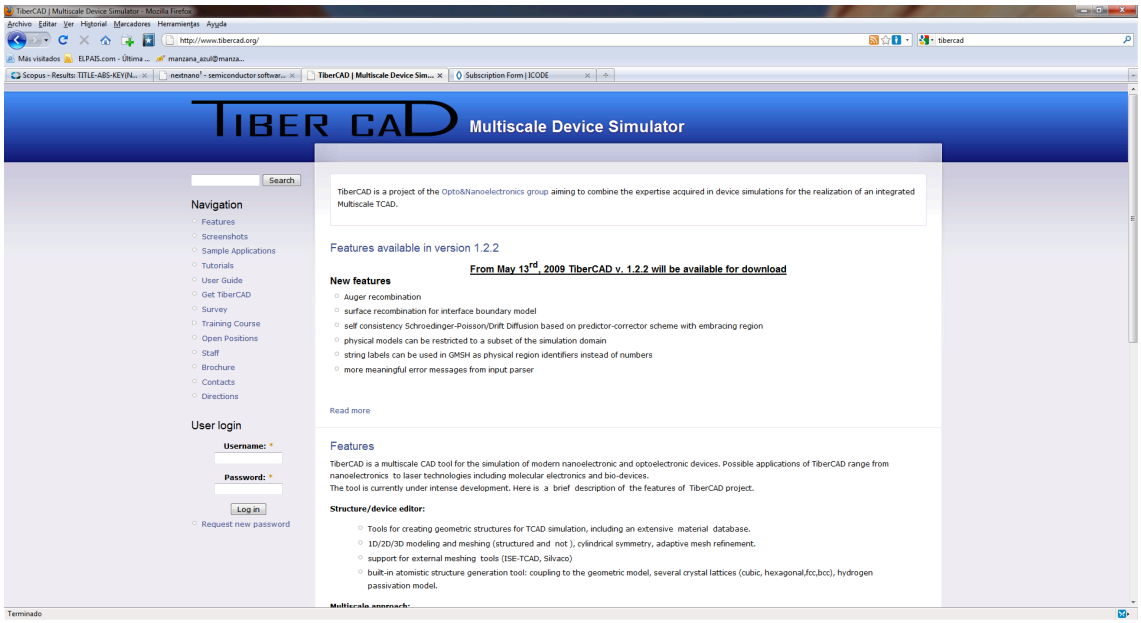


Nextnano http://www.nextnano.de
Nextnano is a semiconductor nanodevice simulation tool that has been developed for predicting and understanding a wide range of electronic and optical properties of semiconductor nanostructures [24,25]. The underlying idea is to provide a robust and generic framework for modeling device applications in the field of nanosized semiconductor heterostructures. The simulator deals with realistic geometries and almost any relevant combination of materials in one, two, and three spatial dimensions. It focuses on an accurate and reliable treatment of quantum mechanical effects and provides a self-consistent solution of the Schrodinger, Poisson, and current equations. Exchange-correlation effects are taken into account in terms of the local density scheme. The electronic structure is represented within the single-band or multiband kp envelope function approximation, including strain. The code is not intended to be a black box tool. It requires a good understanding of quantum mechanics. The input language provides a number of tools that simplify setting up device geometry or running repetitive tasks.
Examples that demonstrate the wide range of possible applications for this software in the fields of solid-state quantum computation, nanoelectronics, and optoelectronics, are the following, 1) The realization of a qubit based on coupled quantum wires in a magnetic field, 2) carrier transport in two different nano-MOSFET devices, and 3) a quantum cascade laser.

TiberCAD http://www.tibercad.org
TiberCAD is a multiscale tool for the simulation of modern electronic and optoelectronic devices. Applications of TiberCAD range from nanoelectronic to laser technologies including molecular electronics and bio-devices. The tool is under intense development. TiberCAD has been developed by the Nano & Optoelectronics group of the University of Rome "Tor Vergata" [26,27].

TiberCAD Characteristics:
• Tools for creating geometric structures for TCAD simulation, including an extensive material database.
• 1D/2D/3D modeling and meshing (structured and not), cylindrical symmetry, adaptive mesh refinement.
• Support for external meshing tools (ISE-TCAD, Silvaco)
• Built-in atomistic structure generation tool: coupling to the geometric model, several crystal lattices (cubic, hexagonal,fcc,bcc), hydrogen passivation model.
• Quantum, classical, atomistic and continuous descriptions can be used in different regions of a device/nanostructure within the same simulation; analysys and optimization may be performed at all the relevant scale lengths, possibly including self-consistent behavior.

TiberCAD Applications:
• Electronic device analysis (HEMT, MOSFET, HBT etc.)
• Nanoelectronic devices (Nano-MOSFET, CNTFET, nanowire etc.)
• Molecular and organic electronic devices (OTFT, OLED, OPV)
• Optoelectronic devices (LASER, LED, photo detectors)
• Solar cells (silicon based, CdTe, CIGS, DSSC, organic)
• Nanostructures



Minimos 6.1 (Technische Universität Wien) http://www.iue.tuwien.ac.at
MINIMOS is a software tool for the numerical simulation of field-effect transistors such as silicon bulk and SOI MOSFETs, and gallium arsenide MESFETs. The fundamental semiconductor equations, consisting of Poisson's equation and two carrier continuity equations, are solved numerically in two- and three-dimensional domains. Finite differences are employed for space discretization, and the Backward Euler method for

time discretization. MINIMOS generates an adaptive grid and has an automatic time step control [28].

Features of MINIMOS 6 include transient analysis, dynamic trap-rate equations for both interface and bulk traps, a band-to-band tunneling model, and a self-consistent Monte Carlo module which replaces the drift-diffusion model in critical device areas.

PISCES-2ET (Stanford University) http://www-tcad.stanford.edu

PISCES-2ET device simulation program is developed based on the IIB version of Stanford's well-established PISCES code and a carrier energy transport (ET) model proposed by Prof. R. W. Dutton's research group at Stanford. Its simulation capability for device electrical characteristics has been expanded from silicon and GaAs to cover major compound materials commonly used in high-speed heterostructures and optoelectronic devices.

Major new capabilities in PISCES 2ET include: Energy transport model to provide information for carrier temperatures, simulate thermal diffusion in the substrate to include the effect of lattice temperature variation, extensive surface mobility models for MOSFET simulation including Lombardi's model, capability of simulating heterostructure devices including HBTs and HFETs.

University of Granada (Spain)

Different numerical tools have been developed at UGR:

A one-electron Monte Carlo simulator has been developed to calculate the electron mobility in inversion layers. Electron quantization of the electrons in the inversion layer has been taken into account by self-consistently solving the Poisson and Schrödinger equations. Phonon, coulomb and surface-roughness scattering have been considered to accurately reproduce experimental results. This simulator allows the study of different phenomena such as: Remote coulomb scattering [29] and remote surface roughness [30].

Furthermore, the simulator is prepared to analyze transport properties in other materials different to silicon such as: GaAs, SiC, strained-Si.

An EMC simulator has been used to solve the BTE self consistently with Poisson's equation. Quantum effects are included via the multivalley version of the so called Effective Conduction Band Edge (ECBE) [31]. A new version of the ECBE has been developed to include the effects of confinement directions in each valley via the effective mass tensor. The whole code is a 2D real-space and 3D k-space where time is also considered as an independent variable to perform transient simulations. Self consistency is kept updating the electrostatic potential and the quantum-corrected potential every 0.1 ps using the actual electron concentration given by Monte Carlo. The code has so far been used to study different effects. More details can be found elsewhere [32,33].

A Multi-Subband EMC simulator has been also developed to include quantum effects by solving the 1D Schroedinger equation self-consistently with the BTE ans Poisson's equations in each considered slice of the device under study. This tool allows a more precise description of the subband structure which is mandatory for the study of ultrathin body devices. More detaiks can be obtained in [34].

University of Paris XI (Orsay, France)

The tools developed by the University of Paris is a Monte-Carlo simulator for free-electrons. The code has been used to study the effect of scattering in double-gate devices [35] and the behavior of basic CMOS/SOI inverter calculating the propagation delays for step and ramp inputs. Recently, quantum corrections similar to the ones in [36] have been implemented and applied to the analysis of DG SOI MOSFETs [37].

University of Pisa (Italy)
The tool developed at the University of PISA (Italy) is based on the solution of the Schrödinger equation in the different sections of a device. The sections are linked together by assuming either ballistic or drift-diffusion transport, describing the two limiting cases of carrier transport (no scattering / strong scattering). An empirical mobility model is considered for carrier transport in the different subbands and valleys. Recently the group leaded by Prof. Iannaconne has been focused on new channel materials such as carbon nanotubes (CNTs) and graphene nanoribbons [37,38].

University of Salamanca (Spain)
USAL has developed an ensemble MC simulator which incorporates both hole and electron transport. The simulator is self-consistently coupled to a Poisson solver, and considers two dimensions in the real space and three dimensions in the momentum space. Quantum corrections to the potential [29], Coulomb screening, degeneracy and a diffusive model for surface scattering are considered in the simulation. From a basic transport point of view, information about statistics of scattering mechanisms into the channel and the corresponding distribution functions can be achieved. In this way, the transition from diffusive to ballistic transport can be ready evaluated as well as the effects on the effective mobility in these regimes.
The code is optimized to obtain the noise sources (whose primary physical origin is naturally included) as well as the high-frequency performance. For this sake, additional algorithms have been developed, which allow determining important high frequency dynamic parameters (like those of the small-signal equivalent circuit) that combined with the noise sources allows determining the usual circuital noise figures of merit (NF_{min}, R_n, G_{opt}, etc). This methodology has shown particularly useful applicability for the analysis of experimental SOI devices [40,41].

University of Udine (Italy)
Three different tools has been developed by Univ. of Udine to study the transport in decananometric devices:
1) Tool for mobility calculation based on MRT. Basic MRT theory is only applicable to elastic or isotropic scattering mechanisms, while surface optical phonon scattering is anisotropic and inelastic. An extension of the MRT technique has thus been developed, where the MRTs of the different sub-bands are calculated solving the system of equations that for each total energy links the MRTs of the different sub-bands coupled by the inter-sub-band transitions [14,15]. In this way, acoustic and optical phonon scattering, ionized impurity and surface charge scattering, remote coulomb scattering (RCS), surface optical phonon and silicon thickness fluctuation scatterings are included in the calculations. The program reads quantized energy levels and wave-functions from a S-P solver in the effective mass approximation.
2) Full-Band Monte-Carlo with quantum corrections. It is a self-consistent EMC transport simulator for a free electron gas. The code implements quantum mechanical corrections to the electrostatics and scattering rates in order to account for the strong vertical quantization effects taking place in modern MOSFETs. Electrostatic effects are treated according to the effective potential approach [42,43]. The implemented scattering mechanisms are: acoustic and optical phonons, ionized impurity, and surface roughness scattering. Additional features are the calculation of the substrate and gate currents and an oxide transport model.
3) Two-dimensional Multi-subband Monte-Carlo [19]. This code is a self-consistent EMC transport simulator for the quantized electron gas (2D in k-space, 2D in real space) in the inversion layer of modern MOSFETs. Presently the code solves self-consistently the BTE of the 2D electron gas in one vertical slice of a MOSFET device

(bulk, SOI, DG). The collision term includes all the scattering rates that are considered to be the most relevant for modern bulk and SOI MOSFETs.

MOCA, University of Illinois at Urbana Champaign, Illinois, USA
It is a Full-band Monte-Carlo tool with quantum corrections based on the solution of the Schrödinger equation. The different valleys are corrected in a different way, mimicking the effect of subband splitting. Scattering of the free-electron gas has been adapted to the modeling of the inversion layer. Details are given in [44].

We would like to remark that the above list of the research simulation tools is not exhaustive of all the research work carried out by the scientific community in the development of device simulators for advanced device architectures.

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Key Groups in the World:

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Arizona State University, Tempe, Arizona, USA
IBM Watson Research Center, USA
University of Illinois at Urbana Champaign, Illinois, USA

Purdey University, West Lafayette, Indiana, USA

European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
University of Bologna (Italy) University of Pisa (Italy) University of Udine (Italy) University of Paris XI (France) University of Glasgow (UK) University of Granada (Spain) University of Salamanca (Spain) Technische Universität Wien (Austria) TU Braunschweig (Germany)	- Full custom physical models - New ultra thin layer transport models. - New SOI material capabilities.	- Experimental data on basic transport properties is still very limited. - Some computational approaches are time consuming. - Not always friendly Human-Machine interface

Conclusions and recommendations

Research simulation tools are designed to study new effects and concepts on today and future devices. Flexible models and accurate numerical methods are necessary for pre-device development simulations.

Open issues that need to be addressed are:

- Ballistic transport is still an open issue where different approaches have been applied. However, the lack of experimental results does not allow a proper test for the numerical and theoretical models. Ballistic transistors will be the subject of primary attention in the next few years. Taking into account that the mean free path in Silicon is few nanometers (typically between 20 and 30 nm), most of devices fulfilling the ITRS predictions should present quasi-ballistic transport features. Adequate treatment of quantum tunneling is mandatory in this case to obtain a reliable modeling of these transistors.

- The treatment of quantum mechanics in the devices is a major challenge when dealing with ultra-thin FD SOI's and DG devices, where transversal channel quantization can be of great importance. In the field of compact modeling and Monte Carlo simulators, important efforts have been already developed. The use of multisubband approaches have demonstrated higher accuracy the physical description of the problem.

- Commercial simulators and ensemble device simulator still lack of an adequate and completely physical treatment of quantum effects. Quantum corrections to the potential show a widespread use today, but they should not be considered as the final solution to the problem, in particular when dealing with second-order quantities.

- Ensemble Monte Carlo simulation of Partially-Depleted SOI transistors is still an open field. In this case, a bipolar simulation is required in order to take into account the contribution of the substrate (majority carriers) to the high-frequency performance of the transistor. To our best knowledge, up to date there are no works referring to this subject in the Monte Carlo literature. The

importance of this kind of transistors requires urgently performing Monte Carlo studies (additional to the preliminary works already elaborated) that may help to understand and optimize this family of SOI devices.

- Surface scattering may play a major role in ultra-thin SOI films. Although the treatment of surface scattering in Monte Carlo simulation has been the subject of many works, in the case of EMC simulations, a unified algorithm for the treatment of surface scattering is desired in order to deal with devices fabricated in ultra-thin layers. The commonly used classical solution (combination of diffusive and reflective scattering for particles hitting the Si-SiO_2 interface) is no longer valid when dealing with quantized channels.

CHAPTER VI

Reliability of SOI devices and circuits

EUROSOI State of the Art Report

Chapter 6. Reliability of SOI devices and circuits
Sections 6.1, 6.2, 6.3, 6.4, 6.5, 6.6, 6.7

Date of Issue: Dec – 2009	**Partner: UGR, Philips SC**

Abstract

Here we briefly review different issues concerning the reliability of SOI wafer, devices and circuits.

Introduction

This section intends to list and update the main issues concerning the reliability of SOI devices and circuits. Limitations will be reviewed for each process, calling for further improvements in some areas.

6.1.- Wafer Level Reliability

For any SOI CMOS process, the quality of SOI wafers must be the same than bulk silicon wafers. For advanced generations, ultra-thin gate oxide (<2nm) is grown on silicon film where a very low defect rate must be achieved. The same yield is currently achieved at manufacturing level. Whatever the process used for elaborating the SOI wafers, it must guarantee the highest crystalline quality with the lowest defect density. A special attention has to be paid to the BOX where any defect could result in a leakage path to the underneath substrate. A defect below the body will suppress its floating nature, changing the electrical behaviour of the transistor, which may lead to an operation failure in the critical paths of the chips. For single gate FD devices, a tight control of potential trapped charges in the BOX is necessary to avoid any Vt fluctuation, as Vt depends on the flat-band voltage at the silicon film/BOX interface. For future FD devices, the BOX thickness is expected to be reduced to further improve the short-channel effect control and attenuate the self-heating effect [1,2]. Reliability of the buried oxide will then become a major issue, depending on the process used for fabricating the SOI wafer.

The density of generation/recombination traps arising from defects and contaminations [3] in the silicon film must also be maintained as low as possible. A high density of these traps will increase the body/source-drain junction leakage current and then modify the floating body potential, resulting in a Vt variation and fluctuation of the parasitic bipolar transistor gain. Additionally, the change in carrier lifetime due to trap variation will influence the history effect, making a wider variation in the modelling of digital circuits necessary.

The wafer level reliability evaluation comprised of off-state degradation mode, bias-temperature stress (BTS), channel hot carrier (CHC) and gate oxide time dependent dielectric breakdown (TDDB). Off-state stress mode is performed at high temperature (140 ºC) and applying elevated drain bias with the gate and source at zero bias. Bias-temperature stress is also performed at high temperature, except the drain to source bias was set to zero and the gate biased in strong inversion. Channel hot carrier stress is performed in the on-state (gate to source bias greater than the threshold voltage) mode at various temperatures. The conventional constant voltage TDDB method is used to evaluate the gate oxide lifetime.

Historically, SOI unique defects, such as silicon dislocations and HF defects, have precluded SOI to be introduced into mainstream semiconductor technology. These defects are responsible for gate oxide yield and reliability. However, in today's state of the art SOI material, these defects have been minimized to acceptable levels.
In today's semiconductor fabrication process, plasma induced charging effects [4] are becoming more important. However, it has been shown that SOI is less susceptible to charging damage. Damage occurs during plasma processing when current flows through the gate oxide into the substrate (bulk devices). In SOI, the buried oxide prevents this current flow into the substrate, thus, resulting in less damage. However, plasma damage can occur in SOI when differential charging develops between nodes due to electron shading. This behaviour is observed and can be modelled. SOI unique defects represent a negligible portion of the fail distribution. The impact of fundamental device (MOSFET) reliability mechanisms is essentially equivalent to bulk silicon. Furthermore, SOI unique defects, which lead to time dependent failure, have been minimized to acceptable levels.

6.1.1.- Gate-oxide quality – TDDB

The reliability of a gate dielectric stressed with a high electric field is evaluated by Time Dependent Dielectric Breakdown (TDDB). This breakdown is typically influenced by lattice defects and impurities discussed above. To obtain a clear breakdown behaviour, test structures need to be designed with small gate area, so the total gate leakage is relatively small. Besides soft breakdown that challenges ultra-thin dielectric testing, Random Telegraph Signal (RTS) noise is more common in SOI, especially with small-area Floating Body (FB) test structures. Since the T-gate is a special structure in SOI, we need to assess its reliability. The results imply that the addition of a T-gate shortens gate dielectric lifetime. This is because part of the gate dielectric is biased in accumulation and thus has shorter lifetime.

For high-k oxides TDDB characterization is in a starting phase. A discussion is going on in the literature on the occurrence of progressive breakdown in these materials [3].

6.1.2.- Hot-carrier degradation

SOI devices suffer from hot-carrier effects as the device geometries are aggressively scaled down. Carriers may be trapped in the gate oxide or at the spacer edge, modifying the physical parameters of the devices (Vt, mobility) through an aging mechanism. The worst case bias conditions for aging SOI devices are generally different from bulk because of the floating body. An additional mechanism takes place, corresponding to the charge trapping and interface state generation in the gate oxide silicon interface and the buried oxide (BOX) silicon interface. The latter is more significant for fully depleted devices. PD devices are generally not affected by the back interface trapping due to the decoupling between front and back interfaces. On the contrary, Vt of FD devices are modified by the back interface trapping due to the coupling between front and back interfaces. The strength of the coupling is characterized by the ratio of gate oxide to BOX thickness (T_{ox} / T_{BOX}). When a thin buried oxide is used, the coupling is stronger and Vt depends on both interfaces. FD FinFET, double and triple gate devices correspond to a strong coupling case.
Control of the leakage current at the edge of the transistor limited by the lateral isolation (LOCOS, STI) is a critical issue when developing an SOI CMOS process. Lack of control at the edge will result in an increase of the leakage current. A deep statistical analysis of the leakage current must be performed to check the quality of the lateral isolation.

It is seen that the I_{dsat} of a typical FB NMOS / PMOS is shifted and it follows power-time laws with different exponents, suggesting a single carrier injection in PMOS and

hole + electron injection in NMOS. Besides DC-HCI, AC-HCI is an alternative way of characterizing hot carrier reliability. It is done with ring oscillators (RO), which correlates directly with the actual product. A comparison of bulk vs. SOI AC-HCI lifetime does not show significant differences. During AC-HCI stress, SOI transistors have limited self-heating, and as a result, their behaviour is similar to that of bulk. To understand the correlation between DC and AC degradation, it has been compared these two hot carrier injection HCI degradations. DC-HCI was found to have a larger voltage scaling factor, a result that can also be explained by self-heating.

It has been demonstrated that the hot-carrier reliability of the bulk CMOS devices can be improved with the passivation of the interface traps by deuterium instead of hydrogen. The deuterated device exhibits less degradation than the hydrogenated device after stress, indicating the reduction of hot-carrier degradation with deuterium incorporation at the gate oxide and silicon interface [4].
The deuterated devices always exhibit less interface trap generation than the hydrogenated ones. The improved interface stability in the deuterated SOI devices can also be attributed to Si-D bonds that are much more resistant than Si-H against the bombardment by channel hot electrons.

The relation between hot-carrier effects and silicon film thickness does not seem to have come to a consensus in the literature. For SOI p-MOSFETs with raised source and drain, it has recently been found that hot carrier induced device degradation in nanoscale devices increases with decreased film thickness [5].

The magnitude of device reliability improvement decreases as the current density increases, suggesting the important role of the vibrational heating mechanism in interface degradation of deep submicron SOI devices. This point deserves a deeper study.

6.1.3.- Negative and Positive Bias Temperature Instability (NBTI and PBTI))
A PMOS with a surface channel and a P poly gate is subject to NBTI degradation. NBTI is manifested as an increase in threshold voltage (Vt) and a decrease in drive current (Idsat) during the operation in the inversion mode at a bias that limits the gate tunneling below the Fowler–Nordheim (F–N) regime at elevated temperature. This effect becomes increasingly prominent as CMOS technology scales down, given that a thinner gate dielectric is more prone to the influence of interface states. The mechanism of NBTI degradation, though not completely understood yet, is widely believed to relate to hole-assisted Si-H bond dissociation in $Si_3{\equiv}SiAH$ through an electrochemical reaction that produces interface states ($Si_3{\equiv}Si$) and positive fixed charges ($O_3{\equiv}Si+$). NBTI degradation is very sensitive to the gate dielectric fabrication process and may be employed as a process monitor by a fab. This failure mechanism may seriously affect the semiconductor reliability, competing with HCI. For 130 nm technology, product-level reliability measurements show that F_{max} degradation can no longer be accounted for by HCI alone. It appears that NBTI plays a significant role in the overall reliability of a microprocessor. Although SOI technology possesses some unique reliability features, FB SOI technology exhibits NBTI degradation very similar to that of bulk technology [6].
The Vt shift of BT devices has been compared subjected to the NBTI stress at 2.6 V and 100ºC to that of FB devices. About 14% more degradation is observed in the Body Tied (BT) devices. To verify that the extra degradation is indeed associated with the body tie, it has been considered the body-tie terminal floated (BTf) in some BT devices and stress them at the same condition. It was obtained similar results to those of the FB devices. This unique body-tied effect on NBTI reveals that both hole population and oxide field control NBTI degradation.

In designing circuit elements like SRAM cells, a serious issue has been discussed on how to design for time dependent device variations. Regardless of whether an SRAM cell stores 0 or 1, if the cell is not accessed frequently, one of the PMOS pull-up transistors could be in NBTI stress for a prolonged period of time and erode read/write stability of the cell. In order to allow simple and direct estimate of actual usage of an IC, a new class of technique known as “silicon odometers” have been proposed. One suggestion for such a recording method is to measure quiescent leakage current, Iddq to establish on-the-fly-dependent degradation due to NBTI [6].

For high-k gate oxides it has been found recently that incorporation of rare earth metals into HfSiO/TiO stacks reduces the positive bias temperature stress (PBTI) [7].

6.2.- Electro – Static Discharge (ESD)

ESD susceptibility of SOI technology is a major reliability issue. In bulk technologies good protection levels have been demonstrated by using NMOS/CMOS output buffers. However, most protection schemes developed for bulk may not be compatible with SOI structures. For example the use of thick-field oxide devices becomes impractical on SOI wafers.

The SOI human body model (HBM) protection levels drop to almost 50% of the bulk technology protection levels for MOSFET protection scheme. Most of the ESD failures are attributed to thermal runaway, which can explain the reduction in the protection levels due to the self-heating problem associated with the SOI. The protection elements that can be used for the ESD protection of SOI circuits are mainly diodes and transistors. Diodes are always considered the easiest and the simplest way to protect against an ESD event due to their low turn-on voltage and low capacitance. MOSFET transistors can also be used for ESD protection in the grounded gate configuration. However, during snapback operation uniform triggering is not usually guaranteed and current can crowd in a portion of the width causing partial damage to the transistor. There are some solutions that have been introduced to solve the problem either by blocking the salicide on the junction, thus increasing the resistance and, therefore, pushing the current away from the surface to achieve uniform triggering, or by external triggering of the gate or the substrate, or both. These solutions, though successful, might increase the input capacitance and leakage or complicate the protection circuit design and consume more area.

So a diode protection seems more attractive for ESD protection of SOI circuits. In this respect, the lateral diode is the best way to create a uniform diode in the SOI technology and it has been used for ESD because of its high current capability, low capacitive loading, and its simplicity to design. There are several ways to build the lateral diode, but the most compatible one with the CMOS process is the poly-bounded lateral diode.

ESD has a specific importance as one of the problems to be solved for FinFETs. The extremely small floating fin body regions, which carry the current, are thermally detached from the substrate by the buried oxide. This may be of concern in MOS operation but even more so during ESD. However, the initially extremely low ESD values of FinFETs have been strongly improved by overall process maturity and added process features. The ESD levels of FinFETs now seem scalable up to the levels compliant with full IC design constrains [8].

6.3.- Latch-Up

SOI ICs are completely immune to classic four-layer p–n–p–n single-event latch-up. However, floating body effects make SOI ICs susceptible to single-event snapback (single transistor latch). The sensitive volume for charge collection in SOI technologies

is much smaller than for bulk-silicon devices potentially making SOI devices much harder to single-event upset (SEU). However, bipolar amplification caused by floating body effects can significantly reduce the SEU hardness of SOI devices. Body ties are used to reduce floating body effects and improve SEU hardness. By using body ties to reduce bipolar amplification, much higher dose rate upset levels can be achieved for SOI devices than for bulk-silicon devices since the sensitive volume for dose rate effects is typically two orders of magnitude lower for SOI devices than for bulk-silicon devices [9].

6.4.- Electro-migration

This chapter will cover several aspects related to metallization which effect the reliability of SOI-based products. Some of them are improved compared to conventional processing, such as junction spiking, others are more sensitive, like thermal-gradient induced migration and thermo-mechanical fatigue.

6.4.1. Junction spiking

Generally not a topic with silicidation anymore. Especially fully depleted SOI work with contact doping regions (S/D implantations) spanning the whole SOI film thickness which further alleviates any concerns about spiking due to electromigration at metallurgical junctions.

6.4.2 Wiring

High-performance circuits and especially power electronics in SOI experience more local heating due to the low thermal conductance of silicon dioxide (two orders of magnitude lower than silicon). These higher temperatures and especially the increased thermal gradients will worsen metal migration by adding substantial thermal migration in addition to the current-induced electromigration.

6.4.3 Thermal fatigue

The lower thermal mass of thin SOI films allows switching devices to heat and cool much more rapidly with varying load. This has effects on electrical parameters on the device, but also mechanical effects are induced. The strain induced by repetitive heating and disparate thermal expansion coefficient can give rise to failures typically in the brittle dielectric.

6.4.4 New Materials

New materials such as copper for metallization and low-k dielectrics for the interconnections are necessary to improve the device performance and keep on shrinking their dimensions. Obviously this will mean some difficult challenges that have to be faced. From the reliability point of view we can highlight the next ones:

- Stress migration of Cu vias and lines as well as the electromigration performance.
- Thermal-mechanical stability of the interfaces between metals, barriers and interlevel dielectrics and resulting line-to-line leakage.
- Time Dependent Dielectric Breakdown (TDDB) of the Cu/low-κ system.
- Reliability impact of lower thermal conductivity of low-κ dielectric.
- Reliability issues due to the porous nature of the low-κ dielectrics and moisture.
- Impact of metal-ion drift and/or diffusion on gate dielectric reliability.

For high-k gate dielectrics only a small volume of results have been published so far concerning SOI devices. In a recent paper, NBTI was studied for p-multichannel on SOI which demonstrated a lower V_T degradation for this kind of structures than for p-FD SOI planar devices [10].

6.5.- Radiation Effects

SOI technology has long been explored for radiation-hardened space and military applications. The advantages of SOI technology arise from the fact that the active devices are built on top of an insulating layer. This results in considerably less p–n junction area and parasitic capacitance, making SOI devices superior to bulk-silicon devices for high-performance/low-power applications [11].
Unfortunately, the insulating layer also introduces an additional source for radiation-induced charge trapping. Positive charge trapping in the buried oxide can invert the back-channel interface of partially depleted n-channel transistors, forming a conductive channel between the source and drain. This can lead to large increases in leakage current in partially depleted transistor ICs. Because charge trapped in the buried oxide of fully depleted transistors is directly coupled to the top-gate transistor, positive charge trapping in fully depleted transistors will cause a decrease in threshold voltage of the top-gate transistor.
The total dose response of SOI devices is more complex than for bulk-silicon devices due to the buried oxide [12]. Process techniques that reduce the net amount of radiation-induced positive charge trapped in the buried oxide and device design techniques that mitigate the effects of trapped charge in the buried oxide have been developed to harden SOI devices to bulk-silicon device levels. One such device design technique for partially depleted devices, the Body Under Source Field Effect Transistor (BUSFET), utilizes a shallow source eliminating the back-channel conducting path between the source and drain. Inherent to the BUSFET is also an improved body tie. For fully depleted devices, process techniques that reduce the amount of charge trapping in the buried oxide must be used. The worst case bias for charge trapping in the buried oxide for partially depleted transistors has been shown to be the OFF or TG bias configuration. The worst case bias for trapping in field oxides is the ON bias configuration. Thus, the worst case biases for buried and field oxides are different and this can lead to complications in hardness assurance testing [13].
The facts that SOI devices are dielectrically isolated, have reduced collection volume, and reduced p–n junction area as compared to bulk devices make it possible to manufacture SOI devices with significantly better single-event upset (SEU) and dose rate radiation response. Although SOI ICs are immune to classical latch-up, they are prone to single-event snapback caused by bipolar amplification. As excess electrons are injected into the body region and drift toward the source, the concentration of electrons can be increased by impact ionisation leading to a runaway condition, i.e., snapback. Snapback limits the practical widths of SOI transistors; however, for BUSFET ICs, very long gate-width transistors can be fabricated. The sensitive volume for dose rate effects is typically two orders of magnitude lower for SOI devices than for bulk-silicon devices. Because of this, SOI ICs can be fabricated that function without upset in much higher dose rate environments than bulk silicon ICs. However, just like for single-event effects, bipolar amplification can significantly reduce the dose-rate hardness of SOI ICs unless body ties are used. The bipolar gain is less for fully depleted devices than partially depleted devices. The bipolar gain does not appear to be strongly affected by circuit dimensions, and future downscaling of devices may not significantly increase the effects of bipolar amplification.

For FinFETs, a threshold voltage shift of less than 10 mV mV has been reported at a radiation dose of 6 Mrad(SiO_2). For higher doses the usual mobility degradation cased by interface trapgeneration was observed [14]. For high-energy neutron irradiation on MuGFETs, extreme sensitivity was demonstrated recently after 1Mrad irradiation [15].

6.6.- Mechanical effects: Strain, thermal cycling

Managing internal mechanical stress is a key point to ensure high performance and high reliability in advanced CMOS technologies. Stress can be generated in MOSFET devices at many technological process steps, as they generally imply different process temperature as well as materials with different mechanical properties, thermal

coefficient mismatch, and so on. As CMOS devices continue to scale down, these effects become more and more important. Former studies have demonstrated that mechanical stress can affect work-function, band-gap, effective mass, and carrier mobility as well as junction leakage. In the case of heterostructures as SiGe devices, stress is used to improve performance. However, the effects of mechanical stress can also reduce the device's performances, and become mainly detrimental: For the back-end part of the process, stress voiding and mechanical weakness of low-k materials are of prime importance. For the front-end part of the process, shallow trench isolation (STI) is, today, the major source of stress in MOSFET channels. Stress can also, in the worst case, affect yield through dislocations. It can also induce design dependent nMOS and pMOS drivability. While piezo-resistivity has been deeply studied in bulk silicon for sensors from both theoretical and practical viewpoints, few works have been performed on advanced deep sub-micrometer CMOS technologies. Stress is difficult to measure locally and is also difficult to simulate, since there is a critical lack of data for many thin-film materials used in technological processes. To optimise the future devices, it is therefore crucial to evaluate the effects of mechanical stress on short channel transistors characteristics.

The STI process can induce significant mechanical stress in devices. A compressive stress develops due to the trench oxidation, difference in thermal expansion coefficient between Si and SiO_2 and visco-elastic effects during thermal anneals. Electrical parameters (i.e., mobility, threshold voltage, etc.) are modified through piezo-resistive effect. A decrease of nMOS current and an increase of pMOS current are observed with increasing compressive stress [1].

An important result is that the higher stress effects observed on pMOS compared to nMOS for SOI devices are not due to piezo-resistive coefficient differences but rather to different internal stress. Among the possible causes of this difference are STI sidewall oxidation, silicide stress, different doping amorphisation and recrystallisation effects.

Using a four-point bending method, it was possible to extract valuable information on piezo-resistance and on stress effects for advanced 0.13μm bulk and SOI technologies. Stress profile induced by STI has been extracted leading to a better understanding of the differences between bulk and SOI technologies, as well as between nMOS and pMOS devices. Higher pMOS drain current shifts are usually observed relatively to nMOS and are due to the difference of technology process leading to different stress. A convincing hypothesis for this difference is stress relaxation in the case of nMOS due to amorphisation and recrystallisation. Such methodology and data can have many further applications in the field of simulation calibration and of electrical analysis of parameters dependence with stress. A deeper study of the stress effects would help to understand, minimize or optimise internal stress effects induced during the process.

In addition, the lower thermal mass of SOI transistors and their higher thermal insulation from the surrounding by low-k dielectric, lateral and vertical oxide isolation leads to larger and faster thermal cycles on a very local scale. Some studies [5] have shown, that such stresses in operation leads to novel failure mechanisms, such as thermal gradient migration of metals and thermal fatigue of intermetal dielectrics.
The thin active silicon used in SOI has much lower thermal capacity than its equivalent in bulk. The surrounding dielectric has often two orders of magnitude lower thermal conductivity than silicon, giving rise to much more localized hot spots and thermal gradients. The different materials used in SOI, and their mismatch in thermal expansion coefficients, give rise to mechanical strain. In best case such strain will change device parameters (mobility enhancement or degradation, etc). In the worst

case they can lead to thermal fatigue as discussed in chapter 6.4.3.

6.7.- Application-specific tests

6.7.1. High-voltage and power products

A careful selection of acceleration factors is necessary, as some effects can be recovered even by a low-temperature annealing. Philips made good experiences with voltage-, temperature-, and frequency acceleration, but some control experiments at low temperature (retention of gettered hot carriers in oxides) and low frequency (more extreme temperature excursions during operation) are important. Heat generation is one of the important reliability issues for power devices. Methods for hot-spot detection and heat diffusion in SOI based circuits have been reported [17, 18].

6.7.2. Sensors, Actuators

Many micro-mechanical devices suffer from stiction and unpredictable degradation of gliding surfaces. Life-testing should cover a representative fraction of the device lifetime, but no reasonable acceleration models have been established this far.

6.7.3. Packaging

Finally in the packaging of the chips there are some issues to be taken into account. It is important to consider the ability of bumps to withstand thermal and mechanical stresses while providing sufficient current carrying capability and also the possibility that solder joints fracture at 1st and 2nd level interconnects.

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European Contribution on the Field	Current Situation	
European Groups	**Strong Points**	**Weaknesses**
• Rene Rongen, PHILIPS – Gerstweg 2, NL-6534 AE Nijmegen – The Netherlands • Jean-Luc Pelloie SOISIC – 15 rue des Martyrs 38054 Grenoble Cedex 9 - France • SOITEC http://www.soitec.com • LETI-CEA http://www-leti.cea.fr • Thorsten Schroeter, XFAB - Haarbergstr.67, D-99097 Erfurt - Germany • Volker Dudek – ATMEL http://www.atmel.com	- Power-integrated circuits have been successfully protected. - Long experience and knowledge in the fabrication of SOI wafers and circuits.	- Little established knowledge on MEMs, sensors and actuators. - Few European groups are leading the field of reliability of SOI devices and circuits.

Conclusions and recommendations

As a recommendation, we would like to mention that not only a lot of experimental work has to be done in the reliability field but also the development of numerical tools would help to understand and improve the reliability performance of the SOI circuits and devices. We mention some points to be consider as future work:

- Simulation tools for concurrent optimisation of circuit performance and reliability.
- Tools to simulate electromigration, thermal-mechanical stress and process induced charging.
- Software for soft error detection and correction at chip and system level, including random logic faults.
- Degradation issues for high-k/metal-gate stacks

Europe should consider seriously the reliability of devices and circuits as a critical subject to keep on the SOI development. Different issues such as gate oxide quality, hot carrier degradation or mechanical effects could prevent the continuous performance development. To avoid this possibility it is necessary to increase investments and combine efforts between different research institutions coordinated at a European level. Close collaboration with industry for feedback and statistical evidence is crucial. Work on the natural capability of standard FinFETs to withstand

the radiation effects should be encouraged.

CHAPTER VII

Physics. Advanced Device Concepts

EUROSOI State of the Art Report

Chapter 7. Physics. Advanced Device Concepts
Section 7.1. Transport enhanced FETs

Date of Issue: Nov – 09	**Partner: Tyndall**

Abstract

We describe here the advantages, disadvantages, and major challenges of the transport enhanced FETs, providing the key references from the literature.

Introduction

It is has long been known that that tensile stress applied along the channel length in silicon improves electron mobility, and compressive stress improved hole mobility [1].

Strain is introduced in CMOS devices to increase carrier mobility. In bulk devices, compressive strain (which increases hole mobility) can be obtained by introducing Ge atoms in the source and drain, and tensile stress (which increases electron mobility) can be obtained by depositing a contact etch-stop layer (CESL). Substrate strain can also be generated when a thin Si layer is grown on SiGe. The Si lattice takes on the larger lattice constant of SiGe and produces biaxial tensile strain. Biaxial tensile strain has been demonstrated to improve NMOS performance and with large enough strain, can improve PMOS performance. However the IC industry has not adopted the substrate strain for manufacturing largely due to the quality of the substrates because misfit defects, threading dislocations result in unacceptably high leakage currents.

IBM and AMD have devised a new way of straining silicon, called "Dual Stress Liners" or DSL. The technique will ideally eliminate much of the complexity involved with strained silicon, such as the use of epitaxy of SiGe layers. DSL improves transistor performance in its chips by 24 percent, without affecting fabrication yield.

Intel uses a form of strained silicon with similar characteristics in its 90-nanometer chips and 65-nanometer chips. The use of strain improves performance of transistors by 30 percent, according to Intel. The unique strained PMOS transistor structure features an epitaxially grown strained SiGe film embedded in the source drain regions. Dramatic performance enhancement relative to unstrained devices are reported. These transistors have gate length of 45nm and 50nm for NMOS and PMOS respectively, 1.2nm physical gate oxide and Ni salicide. World record PMOS drive currents of 700μA/μm (high V_T) and 800μA/μm (low V_T) at 1.2V are demonstrated. NMOS devices exercise a highly tensile silicon nitride capping layer to induce tensile strain in the NMOS channel region. High NMOS drive currents of 1.26mA/μm (high VT) and 1.45mA/μm (low VT) at 1.2V are reported. The technology is mature and is being ramped into high volume manufacturing to fabricate next generation Pentium® and Intel® Centrino™ processor families [2].

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European Contribution on the Field	Current Situation	
European Groups: STM, UGR, Udine	**Strong Points**	**Weaknesses**
Comments: The first group has a leading technology to produce transport enhanced FETs. UGR and Udine have a strong experience on theoretical studies on the impact of strain on carrier mobility in the operation of SOI devices.	* Higher I_{on}/I_{off} compared to bulk * High mobility is achieved without change in device architecture	* Process compatibility and thermal budget * Operating temperature

Conclusions and recommendations

Transport enhanced FETs offer a very practical solution for improving circuit performance in high-performance CMOS without changing device architecture. We recommend to do intensive research at short term, especially on the fabrication issues. An important effort must be done also in compact modelling.

EUROSOI State of the Art Report

Chapter 7. Physics. Advanced Device Concepts
Section 7.1. Transport enhanced FETs
Subsection 7.1.1. Strained Si, Ge, SiGe, SiGeC, SON or other semiconductor on SOI

Date of Issue: Nov – 2009	**Partner: Tyndall**

Abstract

In order to enhance the driving current capability of MOSFET devices, alternative channel materials can be used. In this section we describe the main physical effects related to alternative materials such as strained Si, Ge and SiGe and their influence on the carrier mobility and drain current.
We will emphasize the modelling issues related to the simulation of such materials.

Introduction

Strained silicon directly on an insulator (sSOI) can help to reduce problems by eliminating the SiGe layer below the strained silicon [1]. Strained sSOI silicon layers have been used for multi-gate MOSFETs. Since the channel conduction is on the sidewall of the fin, the bi-axial stress of sSi produces tensile stress in σ_{xx} direction, compressive stress in σ_{zz} direction and tensile stress in σ_{yy} direction. For narrow fins, σ_{yy} direction is expected to relax, while σ_{xx} and σ_{yy} stress are intact. Experimental data indicates (110)/<110> electron mobility is improved by 60% [2] and (100)/<100> electron mobility is improved by 30%. The stress from sSOI is additive to tensile nitride liner and metal gate described in several papers [3,4,5]. Up to 40% drive current improvements has been observed when sSOI, tensile nitride liner and gate electrode are used. The tensile stress in σ_{xx} degrades the (110)/<110> PMOS performance, but increases (100)/<100> hole mobility.

Conventionally, sSOI is fabricated by wafer bonding and layer transfer of strain Si. Although this technique has successfully been used to produce SOI substrates, its fabrication cost is a concern for commercial applications. Some of the key process/substrate elements in fabricating such sSOI include (i) a device wafer that contains epitaxially grown thick graded buffer layers (GBL) of SiGe with strain-Si on top. (ii) deposition of an oxide layer on (i), (iii) bonding of the device wafer with a handle wafer (bulk-Si), and (iv) layer transfer of strain-Si/oxide stack onto the handle wafer.

300 mm sSOI wafers designed to enable a wide range of high-speed, low-power IC applications are commercially available from SOITEC, Bernin, France. They have an electron mobility factor of up to 80% built into the substrate, and are manufactured using the company's Smart Cut process. The wafers exhibit strain uniformity of 1.5 GPa with homogeneity of ±7% across the entire wafer. The recorded strain corresponds to a silicon lattice deformation of almost 1%. Wafer strain is maintained at temperatures of up to 1100°C.

Germanium is coming back as an interesting semiconductor material in various fields like high performance CMOS microelectronics, optical devices (photodetector, multijunction solar cells, laser, etc.). Concerning nanoelectronics, GeOI should enable

the design of advanced MOS transistors working in the partially or fully depleted regimes or multi gates non planar transistor. It is seen as a substrate of choice for the 32nm technology node and beyond. A paper focuses on the first 200 mm GeOI substrates made from epitaxial wafers using the Smart Cut™ technology and associated results [6]. The pure Ge epilayers grown on Si(001) are in a definite tensile-strain configuration, with a threading dislocation density for as-grown layers of the order of $6x10^6$ cm^{-2}, which is the state-of-the-art for the growth protocol adopted. Detailed characterizations of final GeOI structures realized using the Smart Cut™ technology are presented as well (final roughness, defectivity evaluation, thickness measurement). The GeOI substrates have also been characterized from an electrical point of view.

Results on formation of thin film GeOI structures by the Smart-Cut technology are presented in a paper. [7] Thin single crystal layers of Ge have been successfully transferred, via oxide bonding layer onto standard Si substrates with diameters ranging from 100 to 200 mm. Compared to SOI manufacturing, the development of GeOI requires adaptation to the available germanium material, since the strating material can be either bulk Ge or an epitaxial layer. Some results are presented for GeOI formation according to the different technological options. Germanium splitting kinetics is discussed and compared to already published results. To show good quality of the GeOI structures, detailed characterization has been done by TEM cross sections for defect densities, intrefaces abruptness and layers homogeneities evaluation. AFM was used for surface roughness measurements. These results help define procedures that are required to achieve large diameter high quality GeOI structures.

SiGe-on-insulator material was fabricated by wafer bonding and hydrogen-induced layer transfer techniques. The transferred SiGe layer is strain relaxed and has a Ge content ranging from 15% to 25%. High-quality strained Si layers were grown on the SiGe-on-insulator substrates by the UHV/chemical vapor deposition process at 550 °C. An electron mobility of 40 000 cm^2/V s in a modulation-doped Si/SiGe heterostructure was achieved at 30 K on a SiGe-on-insulator substrate [8]

High performance CMOS operation of fully depleted (FD) and partially depleted (PD) strained-SOI MOSFETs on a thin-film-SGOI substrate with high Ge content (25%) fabricated by the combination of SIMOX and ITOX technologies, without using the usual thick SiGe buffer layers has been demonstrated. High electron (85%) and hole (50%) mobility enhancement of strained-SOI MOSFETs against the universal carrier mobility is measured. It is demonstrated, as a result, that the gate delay time of strained-SOI CMOS is improved by about 70%, compared to that of control-SOI CMOS. Moreover, we also discuss both the strained-Si thickness and the effective field dependent difference between electron and hole mobility enhancement factors of strained-SOI CMOS [9]

It has been shown by simulation that electron mobility and velocity overshoot are greater when strained inversion layers are grown on SiGe-On-insulator substrates (strained Si/SiGe-OI) than when unstrained silicon-on-insulator (SOI) devices are employed. In addition, mobility in these strained inversion layers is only slightly degraded compared with strained bulk Si/SiGe inversion layers, due to the phonon scattering increase produced by greater carrier confinement. Poisson and Schroedinger equations have been self-consistently solved to evaluate the carrier distribution in this structure. A Monte Carlo simulator is used to solve the Boltzmann transport equation. Electron mobility in these devices is compared to that in SOI inversion layers and in bulk Si/SiGe inversion layers. The effect of the germanium

mole fraction x, the strained-silicon layer thickness, T_{Si}, and the total width of semiconductor (Si+SiGe) slab sandwiched between the two oxide layers, T_w were carefully analyzed. A strong dependence of the electron mobility on T_{Si} was observed, due to the increase in the phonon scattering rate as the silicon layer thickness is reduced, a consequence of the greater confinement of the carriers. This effect is less important as the germanium mole fraction, x, is reduced, and as the value of T_{Si} increases. For T_{Si}>20 nm, mobility does not depend on T_{Si}, and maximum mobility values are obtained [10]. Monte Carlo simulations show that electron mobility is greater when strained-silicon inversion layers are grown on SiGe-on-insulator substrates than when unstrained-silicon-on-insulator devices are employed (as experimentally observed). However, the electron mobility in strained-Si/SiGe-on-insulator inversion layers is strongly dependent on the strained-silicon layer thickness, T_{Si}, due to an increase of the phonon scattering, which partially counteracts the increase in the mobility achieved by the strain. This effect is less important as the germanium mole fraction, *x*, is reduced, and as the value of T_{Si} increases [11].

The effective hole mobility in pMOSFET devices utilizing SiGe(C) channels on ultrathin SOI substrates was investigated in a recent publication.[12] Mobility enhancement with more than 60% was obtained using both SiGe and SiGeC channels. The SCE were well controlled at L = 0.1 μm, and OFF-state currents were excellent for all transistors including the SiGeC devices. For future generations of ultrascaled devices, where issues such as (SCEs), temperature budget, dopant diffusion, and mobility will be extremely critical, these results point out the potential of applying SiGe or SiGeC channels on ultrathin SOI substrates. The starting material for the device fabrication was p-type (100) SOI UNIBOND (360-nm Si on 400-nm SiO2) or SIMOX (190-nm Si on 150-nm SiO_2) wafers. The top Si layer was thinned by successive dry oxidation and wet HF etching aiming at a thickness of 15 or 25 nm. An epitaxial stack of (8 nm) $Si_{0.72}Ge_{0.28}$(C0.002) and (4 nm) Si was deposited by reduced pressure chemical vapor deposition (RPCVD) on the wafers with 15-nm Si. A key issue in the realization of high-mobility strained materials is highquality substrates in combination with an optimized epitaxial process [18]. This is especially important for C incorporation where C has a tendency to locate at nonsubstitutional sites. The preepitaxy wafer treatment consists of a standard *ex situ* cleaning in combination with an *in situ* (900 ◦C) hydrogen annealing. It should also be noted here that in order to maintain an ultrathin-body (UTB) structure, no Si buffer layer was deposited prior to the SiGe(C) growth. This is otherwise normally performed to decrease the defect density in the strained layer. After Mesa isolation, a 3-nm gate oxide was thermally.

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Key Groups in the WORLD:

Toshiba, Japan
University of Tokyo, Japan
IBM, U.S.
National University of Taiwan
National University of Singapore
University of Texas , Austin (TX), U.S.
University of Illinois at Urbana-Champaign, Urbana (IL), U.S.
University of Stanford (CA), U.S.

European Contribution on the Field	**Current Situation**	
European Groups: ST Microelectronics (Crolles, France):	**Strong Points**	**Weaknesses**

fabrication of sSi devices University of Warwick (UK): fabrication of sSi devices University of Stuttgart (Germany): fabrication of sSi devices Forschungszentrum Jülich (Germany): fabrication of sSi devices KTH, Royal Institute of technology (Sweden): fabrication of sSi devices IMEP (Grenoble, France): device characterization University of Granada (Spain): device simulation and modelling University of Udine (Italy): device simulation and modelling TU Braunschweig (Germany): device simulation and modelling	-Fabrication facilities -Advanced modelling tools for Si that can be easily extended to sSi and Ge channels.	-The origin of the mobility improvement in sSi has not been fully clarified yet. -Lack of reliable experimental data for: Ion improvements in sSi an Ge channel, universal mobility of Ge inversion layers -Tools for pMOSFETs are at a preliminary stage.

Conclusions and recommendations

Devices with alternative channel materials have been successfully fabricated all around the world.
The electron mobility improvement relate to strained Si channels has been measured by many groups and physical models to explain it have been proposed.
Modeling the hole mobility improvement in sSi pMOSFETs is a much more difficult task and requires the development of ad-hoc simulation tools.
No universal mobility data has been obtained for Ge channels yet. However, a clear improvement in pMOSFET mobility has been observed. Tools for Ge MOSFET simulation are currently under development.
The improvement in the ON current of nano-scale MOSFETs associated to the use of high channel material need to be assessed in a more quantitative way.
In general, in this field the main role is played by Asian and U.S. companies and Research Labs. The efforts in Europe should be coordinate in order to reduce the gap with Asian and U.S. groups.

EUROSOI State of the Art Report

Chapter 7. Physics. Advanced Device Concepts
Section 7.2. Metal gates

Date of Issue: Jan – 2009	**Partner: Tyndall**

Abstract

Metal gates are invoked in the ITRS as a technology performance booster necessary to pursue downscaling of CMOS technology. However, many challenges are associated with the fabrication process since the metal work function should be tuned to optimize the threshold voltage of n- and p-MOS transistors.

Introduction

A detailed analysis of the use of metal gates in SOI and MuGFETs has been published in a book chapter by W. Xiong. [1]. For high-performance CMOS, where low threshold voltages are desired, a two-workfunction metal gate system is required. For n-channel FETs, the workfunction needs to be ~200mV below the midgap of the silicon. For p-channel devices, the workfunction needs to be ~200mV above the midgap of silicon. In low-power CMOS, a single midgap metal gate system can be used to obtain a symmetrical threshold voltage for n-channel and p-channel devices at approximately ±350mV.

The use of a metal gate eliminates the poly depletion problem found in devices wih a polysilicon gate. It increases carrier mobility by reducing the transverse electrical field at a given gate overdrive. Metal gate and high-k dielectrics are key scaling enablers for all MOS technologies. Integrating metal gate electrodes into the MOSFET front-end processes is difficult. One of the main reasons is most metals are not compatible with high-temperature (>1000ºC) processing.

Some metal nitrides are stable at very high temperatures. Examples are TiN, TiSiN, TaN and TaCN. The workfunctions of these metals after high-temperature annealing are typically between 4.4eV to 4.7eV, depending on: 1) the layer thickness, 2) alloy composition, 3) crystal orientation and 4) on the gate dielectric material. Metal nitrides are not suitable gate materials for planar CMOS, but they do have the right workfunction for low-power, multi-gate CMOS applications, and have thus been used to fabricate multi-gate MOSFETs [2]. The digital circuit performance of MuGFET made with TiN and TiSiN has been demonstrated to exceed the planar technology with similar gate length.

The integration of metal nitride with multi-gate devices is straightforward. A thin layer of metal nitride is deposited either by Atomic Layer Deposition (ALD) or by Chemical Vapor Deposition (CVD). ALD and CVD give conformal step coverage of the fin sidewalls, which is important for high aspect ratio fins. The metal layer is then covered with a thick polysilicon capping layer for gate patterning. The polysilicon capping layer serves as a planarization medium and reduces gate resistance after silicidation.

For high-performance CMOS applications, gate stacks with workfunctions at +/-200mV away from the silicon midgap are sufficient to set the threshold voltages, but

this requires integrating two or more workfunction metal gate systems onto the same chip, one for N-channel transistors and one for P-channel devices.

Several integration schemes have been proposed to produce gates with tunable workfunction materials: Fully Silicide (FUSI) metal gate, metal layer inter-diffusion, the use of multiple metal thicknesses, and nitrogen-implanted molybdenum (Mo) gates.

The use of Fully Silicided (FUSI) metal gate on multi-gate device was first reported in [3]. FUSI metal gates are formed through a silicidation process after the dopant activation anneal, which avoids the problem of compatibility issues of the metal gate with front-end thermal cycles. The front-end process, up to the gate silicide formation step, is the same as for a standard polysilicon gate device. After source and drain activation and silicidation, a layer of filling dielectric material is deposited and polished until the gate is reached. Then, a thick layer of metal (usually Ni or Co) is deposited on top of the gate. After proper thermal anneal, the gate is completely silicided all the way to the gate dielectric. Any unreacted metal is then stripped off using a wet process. The FUSI gate used in a multi-gate MOSFET fabrication process is similar to that used for planar devices. Due to the differential gate poly thickness caused by the fin topography, however, the deposited Ni needs to be thick enough to form a silicide layer all the way to the buried oxide. It is important to control the formation a uniform silicide phase throughout the gate and keeping the Ni from diffusing though the gate dielectric.

The most commonly used silicides, NiSi and $CoSi_2$, have workfunctions near midgap. In order to adjust the workfunction, a high concentration of dopant is implanted into the polysilicon prior to the gate silicide formation. The effect of dopants on the final effective workfunction of FUSI gate depends on the type of gate dielectric used: on a nitrided gate oxide, boron- and aluminum-doped FUSI have been reported to increase the workfunction up to 4.9eV, while phosphorus, arsenic and antimony can reduce the workfunction down to 4.2eV [4, 5].

The origin of such effective workfunction changes with pre-doped poly silicon is a dopant segregation effect that occurs during silicide formation. Doping atoms have much smaller solid solubility in NiSi than in polysilicon. As Ni consumes Si to form NiSi, dopants in the polysilicon start to segregate out and are pushed toward the gate dielectric interface. When the silicon in the gate is completely consumed and transformed in NiSi, an extremely high concentration of dopant is formed at the interface between the silicide and the gate dielectric, which alters the effective workfunction of the gate stack.

The “dopant segregation” effect is less pronounced on high-k dielectrics. Boron doping has little impact on the workfunction due to Fermi level pinning. The use of nickel-rich silicides can help to reduce the Fermi level pinning. A workfunction of 4.85eV was achieved with Ni_2Si [6]. Extremely high concentrations of Ytterbium in NiSi was used to move the workfunction up to 4.22eV [7]. Unfortunately, the simultaneous integration of multi-phase Ni silicides on the same chip is by no means an easy task.

The effective workfunction (EWF) of TiN and TiSiN has been found to change with the thickness of the layer [8]. Up to 250mV workfunction shift were observed when TiN thickness was increased from 3nm to 20nm. The workfunction saturates at mid band gap for TiN layers thicker than 20nm. TiSiN has a workfunction that varies from 4.44eV to 4.83eV when the layer thickness is increased from 2.5nm to 20nm [9, 10]. Similarly, the workfunction of TiSiN saturates at 20nm. The origin of the workfunction

shift with TiN and TiSiN thickness is the effective nitrogen content in the metal. The top portion of the TiN is oxidized and becomes nitrogen deficient. For thin TiN layers, a relatively Ti-rich TiN is formed, which yields a lower workfunction value.

The effective workfunction of molybdenum (Mo) varies with the nitrogen content in the metal [11]. Molybdenum is a good candidate for gate material because its high melting temperature (2623ºC) makes it compatible with CMOS processing. In addition, it has a low resistivity. The workfunction of Mo is 4.9eV. Nitrogen implant can reduce the Mo effective workfunction to 4.5eV. The amount of workfunction shift is a function of the implanted nitrogen dose and the thermal anneal done after the implant. Low nitrogen implant energy should be used to avoid penetration of nitrogen ions in the gate dielectric.

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(2004)

European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Comments: The research focused on metal gates is mainly covered by experimental groups. In this topic Europe is well behind USA and Asia. However, the ITRS established the need to use metallic gates for the next technological nodes. This means a considerable lack of knowledge in this area that could also be very important in the design of nonvolatile memories.	• No poly depletion effects, no boron penetration, very low resistance and suppressed remote charge scattering.	• Integration of two or more workfunction metal gate systems onto the same chip is a challenging task. • More experimental and theoretical work has to be done to comprehend the metal gate technology.

Conclusions and recommendations

It seems clear that the use of metal gates will be mandatory to overcome poly-Si drawbacks. Much experimental work should be done in this topic since different questions remain unsolved (e.g.: Metal gate still suffer from the inadequate tuning of the workfunctions for threshold voltage (V_{TH}) definition of both n- and p-MOS).

EUROSOI State of the Art Report

Chapter 7. Physics. Advanced Device Concepts
Section 7.3. Ultrathin body SOI FETs

Date of Issue: Nov – 09	**Partner: UAB**

Abstract

We describe here the advantages, disadvantages, and major challenges of ultrathin body SOI FETs, providing the key references from the literature.

Introduction

To reduce short-channel effects such as DIBL (drain-induced barrier lowering) in SOI MOSFETs one has to reduce the silicon film thickness to 20 nm or below. Extremely thin SOI devices are often referred to as "ultrathin SOI" (UT SOI) or "ultrathin body" (UTB SOI) devices. Several effects related to the modification of the band structure do appear when such thin films are used. Classical theory predicts that the threshold voltage decreases in a fully depleted SOI MOSFET when silicon film thickness is decreased, assuming the doping concentration N_a is held constant.This is due to the reduction of depletion charge qN_at_{si} in when the film thickness is deceased. When the film thickness is below 10 nm, however, the depletion charge is very small and can usually be neglected. On the other hand, two non-classical contributions to threshold voltage have to be taken into account. The first contribution comes from the fact that the concentration of inversion carriers needs to be bigger that what classical theory predicts in order to reach threshold. Thus the potential Φ in the thin silicon film is larger than the classical $2\Phi_F$. The second contribution arises from the splitting of the conduction band into subbands: the mimimum energy of the subbands (and thus the minimum energy in the conduction band) increases when the film thickness is decreased, which increases the gate voltage needed to reach any particular inversion carrier concentration. This also causes the threshold voltage to increase. This quantum phenomenon was first reported in 1993 by Omura *et al.* [14] and has since been confirmed and measured by several research groups.

In the particular case of a double-gate device, and neglecting any potential variation in the silicon film ($\Phi=0$), the Schrödinger equation can be used to find the minimum energy of the first conduction subband. The solution is:

$$E_n = \frac{\pi^2 \hbar^2 n^2}{2 m^* t_{si}^2} \qquad (n=1,2,3,\ldots)$$

The energy of the lowest subband is found by letting $n=1$:

$$E = E_{co} + \frac{\pi^2 \hbar^2}{2 m^* t_{si}^2}$$

where E_{co} is the classical, "three-dimensional" minimum energy of the conduction band. The threshold voltage of a single-gate device can be derived from the basic capacitance relationship:

$$C_{inv} = C_{ox} + C_{depl}$$

In a lightly doped (ideally undoped), fully depleted device, the depletion capacitance can be neglected, such that:

$$C_{inv} = C_{ox}$$

Under the same conditions, and in subthreshold operation, the inversion charge and capacitance in a double-gate device are given by:

$$Q_{inv} = -q\, n_i\, t_{si}\, e^{\left(\frac{q\Phi}{kT}\right)} \text{ and } C_{inv} = -\frac{1}{2}\frac{dQ_{inv}}{d\Phi} = -\frac{1}{2}\frac{q}{kT}Q_{inv}$$

where Φ is the potential in the channel and the coefficient 1/2 is due to the double gate. Using these relationships we can write:

$$Q_{inv} = -2\, C_{ox}\frac{kT}{q}$$

Using these expressions, the potential Φ can be found. Adding the workfunction difference between the gate and the silicon film, Φ_{MS}, and the increase of bandgap (1.25) to the channel potential, we find the threshold voltage: [1]

$$V_{TH} = \Phi_{MS} + \frac{kT}{q}\ln\left(\frac{2\, C_{ox}\, k\, T}{q^2\, n_i\, t_{si}}\right) + \frac{\pi^2\, \hbar^2}{2\, q\, m^*\, t_{si}^2}$$

The first term of the latter equation is the workfunction difference between the gate and the silicon film. The second term of the equation represents the potential Φ in the channel. It is inversely proportional to the silicon film thickness t_{si}. In very thin films, Φ can be significantly larger than $2\Phi_F$, and as a result, the inversion carrier concentration at threshold can be much larger in a thin-film device than in a thicker one [2].

This increase of threshold voltage is not correctly predicted by classical simulators since it does not involve the Schrödinger equation. The third term in the expression of V_{TH} is related to the variation of the minimum energy in the conduction band with silicon film thickness, which can only be predicted through quantum-mechanical calculations.

An increase of short-channel effects is predicted for very thin silicon films (<10 nm) because of the increase of bandgap energy and the decrease of effective density of states in the conduction band due to 2D quantization [3, 4].

Several factors influence mobility in thin SOI films. Surface roughness scattering plays a role in very thin films, and so does scattering by interface charges.[5, 6] Both scattering mechanisms become important in extremely thin (a few nanometers) films where electrons are tightly squeezed between two Si-SiO_2 interfaces. The most interesting behavior, however, is that of the phonon-limited low-field mobility. When the silicon thickness is reduced below 20 nm the energy bands split into subbands and the electrons are redistributed in these several subbands. Electrons in the lower subband have a lower mass, and therefore, a higher mobility than the other subbands.

When the film thickness becomes smaller than 15 nm the mobility slightly increases in the subbands and then plummets as the film thickness is further reduced. The slight increase is due to a reduction of the effective mass of the confined electrons when film thickness is decreased, while the plummeting is caused by an increase of scattering rate due to the overlap of the electron wavefunctions in the different subbands and Coulomb scattering due to charged centers at the Si-SiO_2 interfaces [7]. The latter scattering rate is inversely proportional to the silicon film thickness. When the film thickness is decreased below 20nm the total mobility, taking into account all

subbands, increases slightly below 15nm. Then, as the film thickness is further reduced below 5nm, the population of the higher energy subbands decreases abruptly to the profit of the lowest-energy subband (n=1). Since this subband exhibits the highest mobility the overall macroscopic mobility increases and it can reach a value 10% larger than bulk mobility. Finally, as the thickness is reduced below 3nm, the mobility drops sharply [8] because all the electrons are confined within a very limited space and inter- and intra-subband scattering rates become very high [9, 10, 11, 12].

Midgap gate materials are very attractive for fully depleted single- and multiple-gate SOI MOSFETs where short-channel effects are controlled by the use of ultrathin silicon films rather than by high channel doping concentrations. They are not useful in partially depleted devices where strong short-channel effects appear unless high channel doping concentrations are used [13].

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<table>
<tr><th>European Contribution on the Field</th><th colspan="2">Current Situation</th></tr>
<tr><td rowspan="2">European Groups: LETI, UGR, URV

Comments: LETI have activities in both the fabrication and modelling of ultra-thin body SOI FETs. UGR have activities in physical modelling of these devices. URV have activities in compact modelling of these devices.</td><td>Strong Points</td><td>Weaknesses</td></tr>
<tr><td>• Improved subthreshold slope.
• Low junction capacitance.
• Bulk compatible or no significant change in design with respect to bulk.</td><td>• Very thin silicon required with low defect density.
• Difficult to adjust threshold voltage.</td></tr>
<tr><td colspan="3">Conclusions and recommendations

Ultra-thin body SOI FETs offer a promising way to improve CMOS performances beyond classical MOSFET capabilities because the improved electrostatics and low junction capacitance. We recommend to explore intensively several fabrication issues related with the control of the threshold voltage and silicon body thickness and defect density. UT-SOI FETs developed by LETI are very promising candidates for next node technology.</td></tr>
</table>

EUROSOI State of the Art Report

Chapter 7. Physics. Advanced Device Concepts
Section 7.4. Source and drain engineering
Subsection 7.4.1. Metallic S/D junctions
Subsection 7.4.2. Non-overlapping S/D junctions

Date of Issue: Nov – 09	**Partner: Tyndall**

Abstract

The main features of metallic and non-overlapping Source/Drain junctions are described, together with the main advantages of this technology as compared to conventional doped contacts. Key contributors in the field are identified.

Introduction

Lightly doped drain (LDD) and HALO structures are commonly used in bulk CMOS and can readily be adapted to SOI MOSFETs [1, 2, 3, 4]. The real problem facing SOI MOSFETs is the high resistance values of the source and drain. In a MOSFET the source and drain resistance is inversely proportional to the film thickness. This resistance can reach high values in thin-film devices, which jeopardize circuit speed performance. The source and drain resistance can be lowered by several techniques: silicide formation, elevated source and drain, and the use of Schottky junctions.

Formation of a silicide layer on source and drain is a routine operation in bulk silicon processes and it is widely used in SOI processing as well. The most popular silicides are titanium silicide ($TiSi_2$), cobalt silicide ($CoSi_2$) and nickel silicide (NiSi) [5, 6, 7, 8]. However, the metal layers deposited on thin SOI devices to form silicides must be thinner than those used in bulk devices.

An early work from Mitsubishi studied the source and drain sheet resistance in silicided ($TiSi_2$) SOI MOSFETs as a function of the deposited titanium thickness [9, 10]. The silicon film thickness is 100nm. The source and drain sheet resistance can be reduced from 300 Ω/square to 2 Ω/square by sputtering titanium and forming the silicide in a two-step annealing process. The lowest resistance is obtained when a 45nm-thick metal layer is deposited, and the use of thicker titanium layers leads to increased resistance, as well as shorts between the gate, and the source, and drain. More recent results have confirmed that there exists a process window for the thickness of the deposited titanium. For 100 nm-thick devices, the optimal titanium thickness is between 35 to 45 nm. Thinner metal yields a non-continuous silicide layer with high resistivity, and thicker metal layers tend to consume all the silicon in the source and drain regions. Since silicon is the diffusing species in titanium silicide, silicon from the channel region diffuses into the silicide once the entire silicon thickness has been consumed, which leads to the formation of Kirkendall voids underneath the gate edges, resulting in non-functional devices [11].

In addition to the formation of voids in the silicon film, there is another reason to keep the silicide from reaching the buried oxide. The series resistance of a silicided SOI junction abruptly increases when the thickness of the silicide approaches that of the silicon film. This effect is due to a reduction of the contact area once the silicide consumes the silicon layer because the horizontal portion directly underneath the

silicide is no longer available for contact [12]. The effective area through which current can flow is then drastically reduced and the resistance increases. The optimum silicide thickness appears to be approximately 80% of the total silicon film thickness.

Initial publications ruled out full silicidation of source and drain junctions because of the formation of Kirkendall voids. Recent improvements on silicide formation, however, have demonstrated the achievability of full silicidation of thin (12-27 nm) source and drain junctions. It has been shown that the formation of cobalt silicide using a two-step annealing process can be used to create thin, fully silicide junctions with no Kirkendall voids and low leakage current [13, 14]. Contact resistances as low as 4×10^{-8} Ωcm^{-2} and 10^{-7} Ωcm^{-2} have been obtained on N^+ and P^+ junctions, respectively. To obtain the contact resistance in ohms one should multiply those numbers by the area of the junction $A=W\,t_{si}$ [15].

Another way of fabricating thin SOI devices with good source and drain (S&D) resistance consists of using different silicon film thicknesses for the channel and the S&D regions. The use of a thinner silicon film in the channel region provides the desired fully depleted SOI MOSFET features, and the use of thicker silicon for the sources and drains decreases the S&D resistance. This can be achieved in two ways. In a first approach, a thin silicon film is used, and selective epitaxial growth is used to increase the thickness of the S&D regions (elevated source and drain technique) [16, 17, 18, 19, 20, 21, 22]. It is important to note that while it reduces the device resistance, the presence of elevated source and drain structures increases the gate-to-source and gate-to-drain capacitances, such that increased CV/I (intrinsic time delay) characteristics can seriously deteriorate when thick raised extensions and thin liners, separating the gate from the source and drain, are used [23].

A second technique to fabricate thin-body devices with thicker source and drain starts from a silicon film having the thickness desired for source and drain. The channel area is then thinned using a LOCOS-like technique (recessed channel technique) [24, 25, 26, 27, 28]. It is even possible to self-align the recessed region to the polysilicon gate [29].

7.4.1. Metallic S/D junctions

Schottky sources and drains in SOI CMOS provide an alternative to standard S&D engineering [30]. Schottky S&D have a smaller junction RC constant than classical junctions, and, therefore can outperform standard p-n junction S/D MOSFETs. The Schottky barrier formed between the metal or metal silicide should be as low as possible to minimize the contact resistance [31]. Platinum silicide (PtSi) has been used by several groups to form Schottky junctions in p-channel SOI MOSFETs [32, 33], while erbium silicide ($ErSi_{1.7}$) has been used in n-channel devices [34]. Theoretical studies show that the use of Schottky junctions in very short-channel MOSFETs could essentially eliminate most of the S&D resistance, provided that negative or very small positive Schottky barriers are formed [35]. The lowest published Schottky formed on p-type silicon are 0.2-0.22, 0.09 and 0.05eV for platinum silicide, iridium silicide and PtGeSi, respectively [36]. The lowest barriers formed on n-type silicon are 0.27 and 0.06 eV for erbium silicide and platinum/erbium silicide [37]. It is worth noting that Schottky junctions have been used to form the collector of SOI bipolar transistors [38].

7.4.2. Non-overlapping S/D junctions

As sub-50 nm gate length DG MOSFETs have undoped ultra-thin silicon film for enhanced channel mobility, a possible option to control SCEs and achieve low I_{off} is to engineer SDE regions by optimisation of spacer width along with lateral source/drain

doping gradient instead of the conventional method of increasing the channel doping and/or altering the thickness of the silicon film. This concept of “non-overlapped gate-source and gate-drain” extension regions was recently proposed for a sub-20 nm bulk MOSFET [39]. However, in order to maintain I_{off} to an acceptable lower value in bulk MOSFETs, high channel doping and gate overlap may be needed in bulk devices. Therefore, non-overlapped MOS architecture structure seems more promising for ultra-thin single gate (SG) and double gate SOI devices with intrinsic channel. The effects of source/drain doping gradient and spacer width for single and double gate SOI MOSFETs have been analysed by several authors using 2D simulations [40, 41, 42, 43] and for triple and double gate FinFETs using 3D simulations focusing on I_{off} and I_{on} [44, 45].

Gate misalignment is not a critical limiting factor for low voltage operation in gate-underlap double gate (DG) devices. Results show that underlap architecture significantly extends the tolerable limit of gate misalignment in 25nm devices. DG MOSFETs with high degree of gate misalignment and optimal gate-underlap design can perform comparably or even better than self-aligned nonunderlap devices. Results show that spacer-to-straggle (s/σ) ratio, a key design parameter for underlap devices, should be within the range of 2.3–3.0 to accommodate back gate misalignment. These results are very significant as the stringent process control requirements for achieving self-alignment in nanoscale planar DG MOSFETs are considerably relaxed without compromising the performance [46]. Gate-underlap DG devices operated at low current levels are particularly useful for ULV analog/RF applications as both gain and speed of devices can be significantly improved in misaligned structures and stringent process control requirements to achieve a perfect-alignment can be considerably relaxed.

DG/Fin-FET based 6-T SRAM cell with independently addressable gates offers dynamic threshold voltage control to improve trade-offs in SRAM design. The ability to control [47] spacer width and lateral straggle of S/D doping profile through gate-underlap architecture provides an additional degree of freedom, alongside transistor structural parameters. A spacer-to-straggle ratio in range 2-3 is optimal to minimize the possible trade-offs between read stability, write-ability and leakage and attain high SRAM performance that does not degrade with Lg downscaling. Scaling guidelines established between technological and structural parameters suggest that a nearly constant SNM can be maintained over a wide range of spacer and silicon film thickness, without significantly compromising write-ability or leakage current, by selecting spacer-to-silicon film thickness ratio in range 1.5-2 for 22 nm devices [48].

The source and drain contact resistances of accumulation-mode and inversion-mode Multigate FETs are compared in a recent study [49] where the influence of gate-underlap structure is analyzed through simulation and experimental results. In a gate-underlap structure, accumulation-mode devices have a lower source and drain resistance, a higher current drive and a higher transconductance than inversion-mode devices. Furthermore, accumulation-mode devices show less process variability than inversion-mode FETs because the source and drain resistance, and its dependence on back-gate voltage, is much less sensitive to the length of the underlap region. The underlap resistance is expected to become a significant issue in short-channel devices where the channel resistance is lower than in the long-channel devices used in this study.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
IEMN (France), Université Catholique de Louvain (Belgium), University of Salamanca (Spain), Institute of Electron Technology (Poland), ST Microelectronics, NXP Semiconductors.	• Significant top-quality results in the investigation of SB-MOSFETs. • Coordinated efforts between European groups (SODAMOS project).	• High-frequency noise characterization of SB-MOSFETs is necessary. • Need of accurate models to represent the high-frequency dynamic and noise performance of transistors.

Conclusions and recommendations

Metallic S/D junctions are a highly recommendable alternative to avoid the problems associated to elevated parasitic S/D resistances in ultrascaled devices. Europe holds a strong position in the field due to the coordinated effort of several groups. At the present moment this technology is still under development, so still more research at the academic and industrial level is needed in the short and mid terms to make it completely feasible for commercial applications. Strong efforts must be made to determine the possibilities of SB-MOSFETs for analog high-frequency applications.

EUROSOI State of the Art Report

Chapter 7. Physics. Advanced Device Concepts
Section 7.5. Double gate devices

Subsections

Date of Issue: Jan - 2006	**Partner: WUT**

Abstract

This section shortly presents different flavors of the double gate SOI devices and sketches main topics in their physics.

Introduction

The first article on the double-gate MOS (DGMOS) transistor was published by T. Sekigawa and Y. Hayashi 1984.[1] That paper shows that one can obtain significant reduction of short-channel effects by sandwiching a fully depleted SOI device between two gate electrodes connected together. The device was called XMOS because its cross section looks like the Greek letter χ (*Xi*). Using this configuration, a better control of the channel depletion region is obtained than in a "regular" SOI MOSFET, and, in particular, the influence of the drain electric field on the channel is reduced, which reduces short-channel.[2] A more complete modeling that includes Monte-Carlo simulations, was published by Frank, Laux and Fischetti in 1992 in a paper that explores the ultimate scaling of the silicon MOSFET.[3] According to that article, the ultimate silicon device is a double-gate SOI MOSFET with a gate length of 30 nm, an oxide thickness of 3 nm, and a silicon film thickness of 5 to 20 nm. Such a (simulated) device shows no short-channel effects for gate lengths larger than 70 nm, and provides transconductance values up to 2300 mS/mm. The first fabricated double-gate SOI MOSFET was the "fully DEpleted Lean-channel TrAnsistor (DELTA, 1989)",[4] where the device is made in a tall and narrow silicon island called "finger", "leg" or "fin". The FinFET structure is similar to DELTA, except for the presence of a dielectric layer called the "hard mask" on top of the silicon fin [5, 6, 7, 8, 9]. The hard mask is used to prevent the formation of parasitic inversion channels at the top corners of the device.

Other implementations of vertical-channel, double-gate SOI MOSFETs include the "Gate-All-Around device" (GAA), which is a planar MOSFET with the gate electrode wrapped around the channel region [10], the Silicon-On-Nothing (SON) MOSFET [11, 12, 13], and the the Multi-Fin XMOS (MFXMOS) [14]. It is worth noting that the original GAA device was a double-gate device, even though the gate was wrapped around all sides of the channel region, because the silicon island was much wider than thick. Nowadays, most people use the GAA acronym for quadruple-gate or surrounding-gate devices having a width-to-height ratio much closer to unity [15, 16, 17].

The MIGFET (Multiple Independent Gate FET) is a double-gate device in which the two gate electrodes are not connected together and can, therefore, be biased with different

potentials [18, 19]. The main feature of the MIGFET is that the threshold voltage of one of the gates can be modulated by the bias applied to the other gate [20]. This effect is similar to the body effect in FDSOI MOSFETs. An application using MIGFET is signal modulation. A simple square law mixer can be formed using a single MIGFET by applying a small RF signal to one gate and a large low-frequency signal to the other gate. This single-device modulation is possible because the channel is fully depleted and the gates are perfectly symmetrical and aligned. This signal modulation circuit reduces transistor counts and rail-to-rail transistor stack, making it possible to design compact low-power mixers [21].

7.5.1. Ground plane SOI transistor

It can be shown that DIBL is lower in fully depleted SOI devices than in bulk devices [22]. In SOI devices short-channel effects can be further minimized by heavily doping the top of the substrate under the BOX to form ground-plane electrode [23]. In that case, most of the electric field lines from the source and drain terminate on the buried ground plane instead of the channel region. Such an electrode, however, does increase the source and drain capacitance to the substrate and may degrade cross-talk characteristics. It is possible to realize a localized ground-plane electrode that is self-aligned to the gate and does not overlap with source and drain [24].

7.5.2. Volume inversion transistors

Volume inversion was discovered in 1987 by Balestra *et al.* [25] and was first observed in double-gate GAA MOSFETs in 1990 [26]. Volume inversion is a phenomenon that appears in very thin (or narrow) film multigate SOI MOSFETs due to the fact that inversion carriers are not confined near the Si/SiO_2 interface, as predicted by classical device physics, but rather at the center of the film. To correctly predict volume inversion one needs to solve both the Schrödinger and the Poisson equation in a self-consistent manner.

Volume-inversion carriers experience less interface scattering than carriers in a surface inversion layer. As a result an increase of the mobility and transconductance is observed in double-gate devices. Furthermore, the phonon scattering rate is lower in double-gate devices than in single-gate transistors. In thick films there is no interaction between the front and the back channel and there is no volume inversion. The mobility is identical to that in a bulk MOSFET. If the film gets thinner volume inversion appears and the mobility is increased because of reduced $Si\text{-}SiO_2$ interface scattering.

In thicker films the inversion carriers are concentrated near the interfaces, but in thinner films most of the carriers are concentrated near the center of the silicon film, further away from the interface scattering centers, which increases their mobility. In very thin silicon films, however, the inversion carriers in the volume inversion layer do experience surface scattering because of their physical proximity to the interfaces, and mobility drops with any decrease in film thickness [27, 28, 29].

7.5.3. Asymmetrical DGSOI transistor

Simulations indicate that asymmetrical polysilicon gates (*i.e.*: one N^+-type gate and one P^+-type gate) yield devices with higher current drive, lower off current and better short-channel effect control than symmetrical gates (using the same gate material for both gates). This improvement is essentially due to the fact that only one channel is formed in a device with asymmetrical gates and to extended gate to gate electrical coupling and dynamic threshold voltage lowering, which enables low off current and

high on current with low gate capacitance. This beneficial coupling effect is reduced in symmetrical double-gate transistors by the presence of two channels [30, 31].

A report on numerical study on the device performance of an asymmetric poly-silicon gate FinFET and FinFET with TiN metal gate structure can be found in [32]. Numerical simulation revealed that the asymmetric poly-silicon FinFET structure and TiN gate FinFET structures exhibit superior V_T tolerance over the conventional FinFET structure with respect to the variation of fin thickness. For instance, the V_T tolerance of the asymmetric poly-Si FinFET were 0.02 V while TiN gate FinFET exhibited 0.015 V tolerance for the variation of the fin thickness of 5 nm (from 30 to 35 nm) while the conventional FinFET demonstrates 0.12 V fluctuation for the same variation of the fin thickness. Our numerical simulation further revealed that the threshold voltage (V_T) can be controlled within the range of −0.1 to +0.5 V through varying the doping concentration of the asymmetric poly-silicon gate region from 1.0×10^{18} to 1.0×10^{20} cm^{-3}.

Flexibly controllable threshold-voltage (V_{th}) asymmetrical gate-oxide thickness (T_{ox}) four-terminal (4T) FinFETs with HfO_2 [equivalent oxide thickness (EOT) = 1.4nm] for the drive gate and HfO_2 + thick SiO_2 (EOT = 6.4–9.4nm) for the V_{th}-control gate have been successfully fabricated by utilizing ion-bombardment-enhanced etching process. Owing to the slightly thick V_{th}-control gate oxide, the subthreshold slope (S) is significantly improved as compared to the symmetrically thin T_{ox} 4T-FinFETs. As a result, the asymmetric T_{ox} 4T-FinFETs gain higher Ion than that for the symmetrically thin T_{ox} 4T-FinFETs under the same I_{off} conditions [33].

7.5.4. Velocity Modulation Transistors (VMTs)

The current trend in microelectronics is the high end silicon devices and circuits will be processed on wafers with a very thin silicon-on-insulator (SOI) layer. In this project the feasibility to realise a novel, extremely fast silicon transistor based on carrier velocity modulation will be investigated. These SOI velocity modulation transistor (VMT) may have intrinsic and extrinsic operation speed of several hundreds of GHz. The SOI VMT can replace high speed 3-5- transistors, e.g., in telecommunication and automotive radar applications.

Velocity modulation transistors (VMT) are proposed as a way to explode short transit time between two adjacent channels with different transport properties in order to obtain a fast switch. Originally proposed for III–V heterostructures, a Monte Carlo study of silicon-based VMTs is presented in this work showing that surface roughness in double-gate silicon-on-insulator devices can be used as a mobility degradation mechanism to obtain current ratios higher than 30 and therefore feasible devices. Transient simulations have been also carried out obtaining sub-picosecond switch times for 0.1 μm gate length. Switch time limitations are also discussed including both intrinsic and extrinsic factors [34]. The concept of velocity modulation transistor (VMT) explores the perpendicular transit time between two adjacent channels of very different transport properties. The essential requirements for velocity modulation are twofold: (1) To switch the electron gas between two channels without changing the carrier density and (2) to create large enough mobility difference between both interfaces. This device was originally proposed using III–V heterostructures such as n-AlGaAs/GaAs/n-AlGaAs forming two different channels at the heterointerfaces in GaAs. One of the channels was highly doped with compensated donor and acceptor dopants, whereas the other one was kept undoped. In that case the compensated-doped channel formed the low mobility channel and the undoped one the high mobility channel. Several works can be found in the literature based on different heterostructures using the same procedure to obtain differences on the transport

properties. Current ratios obtained for those cases were smaller than 3 while a practical device should present, at least, a ratio of 10. Obviously, it would be very interesting to realize this idea on a silicon-based technology since it could be operated in the ‘‘teraherz gap’’ with applications on health and security equipment. Thanks to the flexibility of silicon-on-insulator (SOI) technology nowadays is possible to create such heterostructures in silicon-based devices. A first performance prediction study of a VMT-like structure in Si was described in which the degradation mechanism for the low mobility channel was again a compensated doping profile. Due to the fact that in this approach, front and back gate lengths were different a high electron density modulation was present (higher than 25%) between the two conduction states leading to a non-proper operation as VMT (again the achieved current ratio was approximately 3). Moreover, very recent experimental studies report that it is possible to move charge from the top interface to the bottom one in DGSOI devices obtaining velocity modulation at room temperature keeping constant the actual inversion charge constant. So that, the aim of this work is to carry out a thorough investigation about the performance of DGSOI transistors operated as VMT at room temperature considering surface roughness instead doping compensation as a degradation mechanism to create a low mobility channel.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Theory: Many teams in Europe are engaged in work on physics and simulation of the double gate SOI devices. Some have leadership in particular areas. Their knowledge and expertise fields are complementary, creating a very strong scientific community. ENSERG, Grenoble, France University of Bologna, Italy University of Udine, Italy University of Pisa, Italy University of Granada, Spain University of Salamanca, Spain Warsaw University of Technology, Poland UCL, Louvain-la-Neuve, Belgium Swiss Federal Institute of Technology, Technical University of Vienna, Austria Fabrication: ST Microelectronics, Crolles, France CEA-LETI, Grenoble, France **Comments:** Simulation of all issues concerning the double gate SOI structures (electrostatics, carrier concentration distribution, transport, current-voltage characteristics) is a subject of collaboration of European research teams in a framework of 6FP NoE SINANO.	European community is very advanced both in theory and fabrication of double gate SOI structures.	Weak collaboration between the university and industry groups.

Conclusions and recommendations

European groups are strong in the field of theory and simulation of the double gate SOI devices as well as there is knowledge and practical experience for implementation of this technology into the industry. However, more collaboration between university and industry researchers is recommended. Explore the possibility to implement III-V device concepts on SOI.

EUROSOI State of the Art Report

Chapter 7. Physics. Advanced Device Concepts
Section 7.6. Multigate devices
Subsections
- **7.6.1. FinFETs**
- **7.6.2. Vertical transistors**
- **7.6.3. Gate-all-around (GAA) and G4-FETs**

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Abstract

We describe here the advantages, disadvantages, and major challenges of the FinFET, vertical transistor, Gate-all-around (GAA) transistor, and G4-FETs providing the key references from the literature.

7.6. Multigate devices

In a continuous effort to increase current drive and better control short-channel effects, silicon-on-insulator MOS transistors have evolved from classical, planar, single-gate devices into three-dimensional devices with a multi-gate structure (double-, triple- or quadruple- gate devices). These multigate FETs are grouped under the acronym “MuGFET”. It is worth noting that, in most cases, the term "double gate" refers to a single gate electrode that is present on two opposite sides of the device. Similarly, the term "triple gate" is used for a single gate electrode that is folded over three sides of the transistor. One remarkable exception is the MIGFET (Multiple Independent Gate FET) where two separate gate electrodes can be biased with different potentials. It is also worth pointing out that one device may have several different names in the literature.

7.6.1. MuGFETs

The first fabricated double-gate with a gate along its sidewalls SOI MOSFET was the "fully DEpleted Lean-channel TrAnsistor (DELTA, 1989)",[1] where the device is made in a tall and narrow silicon island called "finger", "leg" or "fin". The FinFET structure is similar to DELTA, except for the presence of a dielectric layer called the "hard mask" on top of the silicon fin [2, 3, 4, 5, 6]. The hard mask is supposed to prevent the formation of parasitic inversion channels at the top corners of the device.

The triple-gate MOSFET is a thin-film, narrow silicon island with a gate on three of its sides.[7] Implementations include the quantum-wire SOI MOSFET [8, 9] and the tri-gate MOSFET [10, 11].

The Electrostatic Integrity of triple-gate MOSFETs can be improved by extending the sidewall portions of the gate electrode to some depth in the buried oxide and underneath the channel region (Π-gate device [12, 13] and Ω-gate device [14, 15, 16]). From an electrostatic point of view, the Π-gate and Ω-gate MOSFETs have an effective number of gates between three and four. The use of strained silicon, a metal gate and/or high-k dielectric as gate insulator can further enhance the current drive of the device [17, 18, 19, 20].

More recently, planar surrounding-gate devices with square or circular cross sections have reported [21, 22]. Surrounding-gate SOI MOSFETs with a gate length as small as 5 nm and a diameter of 3 nm have shown to be fully functional [23, 24].

The quality of the electrostatic gate control over the channel can be expressed using a simple expression that can be derived from Poisson's equation. [25] It is found that short channel effects are basically non-existent if the effective channel length is five times larger that a value called the "natural length" of the device, and noted λ. The natural length is given by:

$$\lambda \cong \sqrt{\frac{\varepsilon_{si}}{n\varepsilon_{ox}} t_{si} t_{ox}}$$

where t_{si} and t_{ox} are the thickness of the silicon film and the gate dielectric, ε_{si} and ε_{ox} is the permittivity of the silicon and the gate dielectric, respectively, and n is the equivalent number of gates (ENG). The ENG is basically equal to the physical number of sides of the devices covered by a gate and it expresses how efficiently the gate controls the electrostatics in the channel, assuming a square cross section (W_{si}=t_{si}). In a single gate device, n is equal to unity; n=2 in a double-gate device, n=*3* in a trigate configuration, n=4 in a gate-all-around (4 gates device), and $n \approx \pi$ in a pi-gate device. The omega-gate structure is a pi-gate configuration with a larger lateral extension of the gate electrode underneath the channel region. The Ω-gate MOSFET has an effective number of gates larger than a pi-gate, but smaller than a 4-gate device.

Short-channel effects are absent if the effective gate length is larger than 7 to 8 times the natural length, λ. This behavior is common to all gate configurations. Acceptable level of short-channel effects (DIBL<50mV and subthreshold slope <75 mV/decade) are obtained if the effective gate length, L, is smaller than 4λ. Thus, for instance, to have the same short-channel behavior than a gate-all-around device, a single-gate SOI transistor needs to be made in a silicon film that is twice as thin.

To increase the current drive per unit area, multiple surrounding-gate channels can be stacked on top of one another, while sharing common gate, source and drain. Such devices are called the Multi-Bridge Channel MOSFET (MBCFET) [26, 27], the Twin-Silicon-Nanowire MOSFET (TSNWFET) [28], or the Nano-Beam Stacked Channels (GAA) MOSFET [29].

The bulk FinFET is a FinFET made on bulk silicon instead of an SOI wafer. Fins are etched on a bulk silicon wafer and trimmed using an oxidation step. Field oxide is deposited to avoid inversion between the fins. Device with fin width down to 10nm have shown to have good punchthrough immunity down to the sub-20nm gate length regime [30, 31].

A comprehensive simulation study of process variations in bulk FinFETs has been published [32]. Using full 3D TCAD, an evaluation of process parameter space of bulk FinFET is presented from the point of view of DRAM, SRAM and I/O applications. Process and device simulations are performed with varying uniform fin doping, anti-punch implant dose and energy, fin width, fin height and gate oxide thickness. Bulk FinFET architecture with anti-punch implant is introduced beneath the channel region to reduce the punch-through and junction leakage. For 30nm bulk FinFET, anti-punch implant with low energy of 15 to 25 keV and dose of 5.0×10^{13} to 1.0×10^{14} cm^2 is beneficial to effectively suppress the punch-through leakage with reduced GIDL and short channel effects. The simulations show that bulk FinFETs are approximately independent of back bias effect. With identical fin geometry, bulk FinFETs with anti-punch implant show same I_{ON}–I_{OFF} behaviour and approximately same short-channel

effects as SOI FinFETs.

7.6.2. Vertical transistors

The structure that theoretically offers the best possible control of the channel region by the gate, and hence the best possible Electrostatic Integrity is the surrounding-gate MOSFET. The first surrounding-gate MOSFETs were fabricated by wrapping a gate electrode around a vertical silicon pillar. Such devices include the CYNTHIA device (circular-section device) [33, 34] and the pillar surrounding-gate MOSFET (square-section device) [35]. A comparative study of transconductance over drain current as a function of drain current normalized behaviour between Cynthia and Pillar Surround Gate SOI MOSFETs, regarding the same aspect ratio is performed, in order to analyze the potential of Cynthia Surround Gate MOSFET in analog integrated circuits applications. The Cynthia presents better behavior regarding this important merit figure for analog integrated circuits design than Pillar Surround Gate MOSFET, based on 3-D numerical simulations [36].

Analytical models for the electrical characteristics of cylindrical surrounding-gate MOSFETs can be found in the literature [37, 38, 39, 40].

7.6.3. Gate-all-around (GAA) and G^4-FETs

The original "Gate-All-Around device" (GAA) is a planar MOSFET with the gate electrode wrapped around the channel region [41], the Silicon-On-Nothing (SON) MOSFET [42, 43, 44], the Multi-Fin XMOS (MFXMOS) [45], the triangular-wire SOI MOSFET [46] and the Δ-channel SOI MOSFET [47]. It is worth noting that the original GAA device was a double-gate device, even though the gate was wrapped around all sides of the channel region, because the silicon island was much wider than thick. Nowadays, most people use the GAA acronym for quadruple-gate or surrounding-gate devices having a width-to-height ratio much closer to unity [48, 49, 50].

The name "silicon-on-nothing (SON)" does not really apply to a silicon-on-insulator material, but rather to a technique that can be used to fabricate SOI devices [51]. The SON process consists of the following steps. Firstly a strained layer of SiGe and a layer of silicon are epitaxially grown on a silicon wafer. After the epitaxy, conventional CMOS processing steps are carried out up to the formation of source/drain extensions and the formation of gate spacers. Next, trenches are opened in the source/drain areas using anisotropic plasma etching, which accesses the SiGe layer. The SiGe layer is then removed using a highly selective (100:1) plasma etch process. The removal of the SiGe forms an air tunnel that isolates the device from the substrate. This air tunnel gives the SON name to the process. The device is supported by a bridge structure supported at both ends by the field isolation. The air tunnel can then be filled using LPCVD oxide deposition to produce an SOI structure. The process is completed by epitaxial growth of silicon to form sources and drains.

The 4-gate transistor (G^4 FET) has two (top and bottom) MOS gates and two (lateral) JFET gates. It is operated in accumulation mode and has the same structure as an inversion-mode partially depleted SOI MOSFET with two independent body contacts. An earlier device with similar terminal configuration was called the cross-MOS device [52, 53]. In the G^4 FET, these body contacts play the role of source and drain, whereas the former source and drain junctions now act as lateral JFET gates.

The G^4 MOSFET has the standard front and back MOS gates plus the two lateral junctions that control the effective width of the body. The current flows from source to drain. The height and width of the conductive path are modulated by a mix of MOS

and JFET effects. The conductive path can range from from a tiny quantum wire surrounded by depletion regions to a strongly accumulated body, depending on the applied gate voltages. Each gate has the ability of switching the transistor on and off. The independent action of the four gates allows for mixed-signal applications, quantum-wire effects, and quaternary logic schemes [54, 55, 56]. A model for the G^4 FET has been published in the literature [57].

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
LETI, IMEC, UCL, URV, UAB		
Comments:		
- FinFET	* Higher drive current * Improved subthreshold slope * Improved short-channel effect * Relatively easy process integration	* Fin thickness less than the gate length * Fin shape and aspect ratio
The first three cited groups are working on FinFET fabrication issues. URV and UAB work in compact modelling of Fin-FETs.		
- Vertical transistors	* Potential for 3D integration * Lithography independent channel length * Up to 30% gain gain in layout density	* Junction profiling difficult * Process integration difficult * Parasitic capacitance * Single gate length * New device layout
IMEC is working on fabrication of vertical transistors.		
- N-gate FETs	* Higher drive current * Thicker Si body possible	* Limited device width * Corner effect * Sub-lithographic fin thickness required
LETI and UCL are involved in fabrication issues of N-gate FETs. UAB is involved in compact modelling.		

Conclusions and recommendations

- ***FinFETs*** offer a very practical solution for implementating the double-gate structure. We recommend to do intensive research on FinFETs, especially fabrication issues and compact modelling.
- ***The vertical transistor*** offers the best scaling potential. We recommend to focus on process integration and layout design. Compact modelling and physical models are required to explore the capability of the vertical transistor at both the device and circuit levels.

- ***N-gate FETs*** offer a very practical solution for relaxation of the thickness of Si-body. We recommend to explore N-gate FETs, especially fabrication problems, and modelling for projecting the maximum performances.
- Develop circuit design using the independent signals applied to each gate to reduce the transistor count in logic circuits and to enhance the functionality of analog circuits.

EUROSOI State of the Art Report

Chapter 7. Physics. Advanced Device Concepts

Section 7.7. Ballistic Transistors

Date of Issue: Jun – 2009	**Partner: UGR**

Abstract

We describe here the advantages and major challenges of the ballistic MOSFET operation, providing the key references from the literature.

Introduction

A physical model and a computer simulation program for nanoscale ballistic SOI MOSFETs has been developed. The transistor parameters included are the type and level of doping in the source and drain regions, gate length, Si and gate-oxide thicknesses, spacer length, gate-material work function, etc. Transistor performance is characterized in terms of transconductance, subthreshold slope, on- and off-state drain currents, gate–source overlap capacitance, etc. The software enables one to optimize the transistor parameters. On the other hand, the model is simplified in that it neglects the difference in work function between the materials of the gate region and the channel, as well as other materials-related factors [1].

A quasi-ballistic mobility model based on the previous work has been used to simulate two different structures: Fully-Depleted and Double-Gate MOSFETs. Using this approach were analyzed, in a first step, the transport properties by extracting the value of the backscattering coefficient and of the “kT-layer”. In a second step, were simulated CMOS inverters to illustrate the direct relation between the circuit performances and the nature of the transport in the channel. The results show that the switch of DGMOS is more abrupt than that of FDMOS, in both ballistic and quasi-ballistic transport. Moreover, the comparison of thick- and thin-BOX FDMOS structures confirmed that the devices electrostatics (i.e. the short channel effects) has a considerable influence on the small circuit performances in quasi-ballistic transport. Finally, it is noted that this approach will be used for the validation of compact models of ballistic/quasi-ballistic case at both device and circuit level [2].

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<table>
<tr><th>European Contribution on the Field</th><th colspan="2">Current Situation</th></tr>
<tr><td rowspan="2">European Groups:
• University of Udine, Italy
• Institut für Integrierte Systeme, ETH Zürich, Switzerland: These groups are working on Monte Carlo simulation of ballistic transistors.
• UAB, URV, Pisa: These groups are working on compact modelling of ballistic transistors.

Comments:
SHOTs are expected to be a promising transistor structure for future higher-speed CMOS devices.</td><td>Strong Points
Maximum drive current and speed.</td><td>Weaknesses</td></tr>
<tr><td>European groups have developed physically based simulators prepared to analyze the behaviour of devices with effective gate length bellow 25 nm.</td><td>Very difficult to control the sources of scattering.

Lack of experimental data to compare theoretical results.</td></tr>
</table>

Conclusions and recommendations

The ballistic transistor offers the maximum performance; it must be considered at the ultimate scaling limits. It should be explored using rigourous models that account for scattering mechanisms and quantum mechanics. Compact models are needed for exploring the resulting performances at the circuit level.

In order to fully understand this phenomenon, the use of physical models, device simulations and if possible actual fabrication of devices is necessary. Also, the present gap between the results predicted by analytical models and rigorous simulations has to be bridged.

Different channel materials (strained-silicon or germanium) and different channel orientations featuring higher injection velocity and lower scattering are expected to enhance the on-current. Therefore, those topics should thoroughly understood and also included in the numerical simulators.

Moreover, since the ballisticity ratio $BR=I_{ON}/I_{BL}$ is determined by the scattering experienced by the carriers in the channel, accurate scattering models taking into account quantum corrections are necessary to simulate devices with channel lengths below 25nm. The use of high-k dielectrics, metal gates and source/drain contacts should also be considered in a near future.

EUROSOI State of the Art Report

Chapter 7. Physics. Advanced Device Concepts
Section 7.8. High-k materials

Date of Issue: Oct – 2009	**Partner: UAB**

Abstract

We describe the motivation for high-k materials integration in CMOS processes and present challenges.

Introduction

The use of new elements to obtain new desirable properties is a technology booster that has made it possible to extend the life of CMOS and reduce dimensions beyond barriers that were previously considered insurmountable. For instance, the reduction of gate oxide thickness below 1.5nm leads to a gate tunnel current that quickly becomes prohibitively high. Replacing silicon dioxide by a high-k dielectrics such as hafnium oxide (HfO_2), which has a dielectric constant of 22 (*vs.* 3.9 for SiO_2), allows one to increase the thickness of the gate dielectric by a factor 22/3.9=5.5 without reducing the gate capacitance (*i.e.* the current drive of the transistor). The use of new gate dielectrics gave rise to the notion of Equivalent Oxide Thickness, EOT, which is defined by the relationship $EOT = t_d \frac{\varepsilon_{ox}}{\varepsilon_d}$, where t_d is the thickness of the dielectric layer, and ε_{ox} and ε_d are the permittivity of silicon dioxide and the dielectric material, respectively. For example, a 4nm-thick layer of HfO_2 is electrically equivalent to an SiO_2 layer of 0.7nm.

The following observations can be made: the natural length λ (and hence short-channel effects) can be reduced by decreasing the gate oxide thickness, the silicon film thickness and by using a high-k gate dielectric instead of SiO_2. In addition, the natural length is reduced when the number of gates (ENG=Effective Number of Gates) is increased, according to:

$$\lambda = \sqrt{\frac{\varepsilon_{si}}{ENG \times \varepsilon_{ox}} t_{si} t_{ox}}$$

The natural length is typically reduced by using a high-k dielectric with a high value of ε_{ox}. Using multi-gate devices, it is possible to trade a thin gate oxide for thin silicon film/fin thinning since λ is proportional to the product $t_{si} \times t_{ox}$. [1]

High-k dielectric can be combined with metal gate, strained silicon in a MuGFET configuration to obtain “ultimate” performance out of silicon.[2]

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European Contribution on the Field	Current Situation	
	Strong Points	**Weaknesses**
European Groups: IMEC (Leuven) LETI (Grenoble) **Comments:** Multiple research groups in universities are involved in different issues related to high-k gate insulators.	• Provides a path for simultaneously controling the gate leakage current and the short-channel effects.	• Issues with the carrier mobility, stability, reliability, and thermal design.

Conclusions and recommendations

Poly-Si gate electrodes help to reduce gate leakage but pFET gates in high-k stacks show large threshold voltage shift and scalability is questionable due to large poly-Si depletion. Identification of p+ and n+ metals and their integration in a CMOS process are a challenge. It is also needed a thermal analysis of SOI transistors using high-k materials.

Targets: Implementation of high-k gate stacks with metal gates in scaled devices (metal deposition, patterning, integration issues, characterization). Fundamental understanding of future gate stack materials and their impact on the electrical properties and reliability of scaled devices.

CHAPTER VIII

Circuit Design

EUROSOI State of the Art Report	
Chapter 8. Circuit Design **Section Title 8.1 Transistor modelling for circuit simulators**	
Date of Issue: Nov – 2009	**Partner: URV and UGR**

Abstract

The state of the art of SOI circuit simulation is linked to the availability of reliable compact device models in circuit simulators. In this respect, it is important to highlight the main features of commercial simulators since they are the tools which are being used in the industry and correspondingly they represent, for the industrial community, the state of the art of circuit simulation

Introduction

Compact device modeling is used for scaling studies and technology optimization; therefore, the ability to correctly represent today's performance and predict tomorrow's limitations is paramount. The flexibility of SOI technology has permitted much new geometries rather than classical MOSFET (e.g. FinFET, GAA) or the possibility of implement concepts never used before on Si (e.g. Velocity Modulation). In order to link the improvement due to device scaling and to the introduction of new device concept (DG, Trigate, etc) with circuit simulations are needed. For this task, accurate SPICE models for SOI devices are required. These SPICE models may be able to handle specific SOI requirements:

- Fully Depleted and Partially Depleted channels
- Volume inversion in DG MOSFETs
- Short-channel effects
- Possibility of floating body effects
- Single and Multiple Gate structures
- High k dielectric
- Si-Insulator interface
- Detailed quantum effects modeling
- Tunneling through the thin gate oxide
- Ballistic and quasi-ballistic transport in sub-50 nm devices
- Self-heating
- Variability / Mismatch

The main analog circuit simulators are:

ADS	www.agilent.com	AIM-Spice	www.aimspice.com
Antrim-A/MS	www.antrim.com	APLAC	www.aplac.hut.fi
ELDO	www.mentor.com	ICCAP spice	www.agilent.com
Intusoft	www.intusoft.com	HSIM	www.nassda.com
LTspice/SwitcherCAD III	ltspice.linear-tech.com	Star-Hspice	www.avanticorp.com
MacSpice	newton.ex.ac.uk	Micro-CapV	www.spectrum-soft.com
MINIMOS-NT	www.iue.tuwien.ac.at	NanoSpice	www.anawork.com
NG-Spice	ieee.ing.uniroma1.it	PSPICE[+]	www.orcad.com
SABER	www.analogy.com	SANCAD	www.sancad.com
SIMetrix	www.newburytech.co.uk	SmartSpice	www.silvaco.com
SMASH	www.dolphin.fr	Spectre	www.cadence.com

SpectreRF	www.cadence.com	SPICE3	legwww.epfl.ch/ekv/
Spice-Opus	fides.fe.uni-lj.si/spice	Synopsys	www.synopsys.com
TopSPICE	www.penzar.com	TRANZ-TRAN	legwww.epfl.ch/ekv/
T-Spice	www.tanner.com/eda/	WinSpice	www.winspice.com

Description of the main SOI MOSFET models implemented in commercial circuit simulators

STAG SPICE Model: "Southampton Thermal Analogue model"
Developed by: Department of Electronics and Computer Science. Southampton University Microelectronics Centre – U.K.
Availability: Only source C files.
Technical Information:

Features new to STAG version 2.6:

Thermal resistance and capacitance can automatically scale with device area
Up to five thermal time constants can be modelled
Source and drain series resistance can scale with device width
Automatic calculation of body junction capacitances and back gate overlap capacitances
More accurate modelling of body charge for devices operating in saturation
New threshold voltage model - experimentally extracted values can be used directly in STAG

Features in STAG version 2.1:

Partially depleted SOI MOSFET model
Static (DC), transient and small signal (AC) model
Physically based
Fully charge conserving
Surface potential continuous through all regions of operation
Static and dynamic self-heating effects
Externally accessible temperature node to permit implemention of thermal coupling network
Floating body effects modelled physically with symetrical network
Transient and small signal floating body effects
Parasitic bipolar effects in DC, transient and AC
Short channel effects
Thermal and 1/f noise models
Very good convergence
Implemented in SPICE 3f5

UFSOI Model: "SOISPICE is an enhanced version of SPICE2G.6 containing the UFSOI FD and NFD MOSFET models developed at the University of Florida"
Developed by: Professor J. G. Fossum, OI Group. Department of Electrical and Computer Engineering -University of Florida.
Availability: Only source C files.
Technical Information:
The models are charge-based with five terminals, and have a floating-body option. The model for the fully depleted (FD) device properly accounts for the charge coupling between the front and back gates, and includes a two-dimensional analysis of the electrostatic potential in the SOI film and underlying BOX for subthreshold-region operation. The model assumes that the film is strongly FD, except in and near the

accumulation region where it accounts for the majority-carrier charge, and hence dynamic floating-body effects. The non-fully depleted (NFD, which in later releases is evolved to UFPDB) device model properly accounts for DC as well as dynamic floating-body effects defined by capacitive coupling and carrier recombination/generation. Both models include an optional quasi-2D accounting for the (coupled) parasitic BJT (current and charge), which can be driven in the floating-body mode by transient body charging current and/or generation current, including that due to impact ionization which is characterized by a non-local, carrier temperature-dependent model for the ionization rate integrated across the channel(s), (optional) LDD, and drain. The charge modeling has been recently upgraded; all terminal charges (including MOS and bipolar components) and their derivatives are continuous for all bias conditions. Substrate depletion charge under the source and drain regions, which becomes important when the BOX is scaled, is included as components of source, drain, and back-gate charge. Temperature dependence for both models is also implemented, without the need for any additional parameters, as is physics-based noise modeling for AC simulation, which accounts for thermal noise from the channel and parasitic series resistances, shot noise at the source and drain junctions, and flicker noise in the channel. The temperature-dependence modeling is the basis for a self-heating option, which uses special iterate control for the local device temperature node that yields good convergence even for large circuits.

BSIM-SOI 3.2 SPICE Model: “Berkeley Short-Channel IGFET Model”

Developed by: Professor Chenming Hu, BSIM RESEARCH GROUPDepartment of Electrical Engineering and Computer Sciences niversity of California, Berkeley.

Availability: Only source C files.

Technical Information:

Real floating body simulation in both I-V and C-V. The body potential is determined by the balance of all the body current components.

An improved parasitic bipolar current model. This includes enhancements in the various diode leakage components, second order effects (high-level injection and Early effect), diffusion charge equation, and temperature dependence of the diode junction capacitance.

An improved impact-ionization current model. The contribution from BJT current is also modeled by the parameter Fbjtii.

A gate-to-body tunneling current model, which is important to thin-oxide SOI technologies.

Enhancements in the threshold voltage and bulk charge formulation of the high positive body bias regime.

Instance parameters (Pdbcp, Psbcp, Agbcp, Aebcp, Nbc) are provided to model the parasitics of devices with various body-contact and isolation structures.

An external body node (the 6th node) and other improvements are introduced to facilitate the modeling of distributed body-resistance.

Self heating. An external temperature node (the 7th node) is supported to facilitate the simulation of thermal coupling among neighboring devices.

A unique SOI low frequency noise model, including a new excess noise resulting from the floating body effect.

Width dependence of the body effect is modeled by parameters (K1, K1w1, K1w2).

Improved history dependence of the body charges with two new parameters, (Fbody, DLCB).

An instance parameter Vbsusr is provided for users to set the transient initial condition of the body potential.

The new charge-thickness capacitance model introduced in BSIM3v3.2, capMod=3, is included.

LETISOI Model: “LETI SOI Model”

Developed by: Dr. O. Faynot, Laboratoire d´Electronique, de Technologie et d´Instrumentation, CEA-Grenoble.

Availability: Only source C files.

Technical Information:

The LETISOI model has been developed for partially-depleted SOI MOSFETs. Current and charge equations have been derived from a physical basis. The model includes the floating-body effects, self-heating, polysilicon depletion effect, gate oxide tunnelling current, temperature dependence and the bipolar transistor action. The LETISOI model has been extended to RF applications, and, implemented in ADS. It has been validated for channel lengths down to 0.25 μm and frequencies up to 10 GHz.

PHYMOSS Model: “PHYsical MOdel for SOI Simulation SOI Model”

Developed by: Derived from LETISOI SOISIC (Silicon on Insulator Systems and Integrated Circuits) GRENOBLE , France.

It is planned to extend this model to Fully-Depleted devices.

EUROSOI State of the Art Report

Chapter 8. Circuit Design
Section 8.1. Transistor modelling for circuit simulators
Subsection 8.1.1. Partially-depleted

Date of Issue: Nov – 2009	**Partner: URV**

Abstract

The present state-of-the-art on the modeling of partially-depleted (PD) SOI MOSFETs is described.

Introduction

Since PD SOI CMOS technologies are now being used for high-speed low-power applications, there is a need of scalable and accurate models of these devices for circuit simulators.
A few models of PD SOI MOSFETs are already available in commercial circuit simulators: BSIMSOIv3.2, UFSOI, LETISOI, STAG, ST SPICE model, PSP. All these models seem to provide accurate simulated I-V characteristics, with continuous transitions between regimes thanks to the use of interpolation functions. Models that are based on a surface potential formulation (like UFSOI) need less parameters than other models (such as BSIMSOIv3.2). The steady reduction of the device size enhances the relevance of some physical effects that will need to be properly accounted for in the models. Many of these phenomena are related to the two or three-dimensionality of the device and, in order to be adequately considered without, a model based on a full two- or three-dimensional approach will be necessary. Besides, floating-body in PD SOI MOSFETs, can make appear some effects that have not been included in any model so far (gate induced floating body effect, subthreshold swing increase in narrow devices,...).
2.

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European Contribution on the Field	**Current Situation**

European Groups:	Strong Points	Weaknesses
LETI group. Led by Dr. O. Faynot (developed the LETISOI model). Collaboration with SOISIC (Silicon on Insulator Systems and Integrated Circuits) GRENOBLE , France	LETISOI is implemented in commercial simulators. Validated for channel lengths down to 0.13 μm	The model has not been extended to the nanoscale range of channel lengths
University of Southampton. Led by Prof. W. Redman-White (developed STAG model)	STAG is implemented in circuit simulators. It is formulated in terms of surface potentials.	The model has not been extended to the nanoscale range of channel lengths

Conclusions and recommendations

The LETISOI and STAG models were not validated for devices with less than 100 nm of channel length. It seems that there is no European group working on the development of a compact PD SOI MOSFET model for sub-100nm devices. On the contrary, BSIMSOI and UFSOI have been adapted to sub-100nm devices. In particular, UFSOI has shown to provide good accuracy for devices with a 70 nm channel length.

EUROSOI State of the Art Report

Chapter 8. Circuit Design
Section 8.1. Transistor modeling for circuit simulators
Subsection 8.1.2. Fully-depleted

Date of Issue: Oct – 2009	**Partner: URV**

Abstract

The present state-of-the-art on the modeling of fully-depleted (FD) SOI MOSFETs is described.

Introduction

Fully depleted SOI MOSFETs have a better immunity to short channel effects than PD SOI MOSFETs, and therefore, are very promising devices for scaled-down SOI CMOS circuits, in particular for low power applications. However, although several models have been proposed, just a few are available in commercial circuit simulators. A version of the URV/UCL model was implemented in the IsSPICE simulator (from Intusoft), but that version had only been validated down to 1 μm channel length. A version valid down to 0.13 μm channel length is available only in an internal version of ELDO. The models available in most circuit simulators are BSIMSOIv3.2 and UFSOI. BSIMSOIv3.2 includes an option for FD SOI MOSFET with a smooth transition to the partially-depleted behaviour.; one of its main drawbacks is its excessive number of fitting parameters. UFSOI is surface potential based, but, as BSIMSOI, was not validated by comparison with measurements from sub-100 nm devices. As the device size is shrunk down, new phenomena, as in PD SOI MOSFETs, become relevant and need to be included in the model. The two or three dimensionality of these effect affect intrinsic properties of FD SOI MOSFETs, such as the coupling between gates. Recently, the trend towards FD transistors with undoped, ultra thin body and possibly ultra thin buried oxide causes new challenges for compact models, especially with regards to the usual charge sheet approximation, since the conduction channel can take place at any depth in the Si film and since such as in double gate devices, volume inversion might occur. Due to this and differences in interfaces and front/back gate oxides, adapted mobility models are also required.

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
URV group (led by Prof. B. Iñíguez)	FD SOI MOSFET model validated up to L=0.13μm	The last versions of the model are not implemented in any simulators. No self-heating included.
UCL group (led by Prof. D. Flandre)	Currently working with URV group on FD SOI MOSFET modeling. Last model version implemented in the internal version of ELDO. Modeling of FD SOI MOSFETs at high temperature.	No self-heating included. Empirical model for the subthreshold swing dependence on temperature.

Conclusions and recommendations

There are just a few European groups working on the compact modelling of FD SOI MOSFETs. Some work on high temperature modelling has been done at UCL. Very few models are available in commercial versions of circuit simulators and they have not been validated by comparison with experimental results from sub-100 nm devices. Anyway, a new version of UFSOI (UFDG) was shown to provide good agreement with numerical simulations for devices with a 28 nm gate length, although this version is not available in circuit simulators yet. The adequacy of these models with undoped, ultra thin body and possibly ultra thin BOX FD transistors is still questionable.

EUROSOI State of the Art Report

Chapter 8. Circuit Design
Section 8.1. Transistor modeling for circuit simulators
Subsection 8.1.3. Double and Multiple Gate SOI MOSFETs

Date of Issue: Nov – 2009	**Partner: URV**

Abstract

The present state-of-the-art on the modeling of double and multiple gate SOI MOSFET is described.

Introduction

Double and multiple gate MOSFETs seem to be the MOS devices that can be scaled down to the shortest possible channel length, since they are the devices with the highest immunity to short-channel effects. However, very few compact models have been proposed for these devices, and most of them have only been experimentally validated for long-channel undoped devices. Anyway, several models have been successfully checked by comparison with experimental measurements or numerical simulations of multiple-gate SOI devices, even in the nanometer node. Ultimate double and multiple-gate MOSFETs pose new challenges for compact modeling: new multiple gate coupling, volume inversion and accumulation, quantum confinement, ballistic and quasi-ballistic transport.

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
URV group (led by Prof. B. Iñíguez) UAB group (led by J. Suñé)	Continuous model for ultimate GAA in the ballistic regime (with quantum effects included). Explicit continuous model for well tempered cylindrical surrounding gate MOSFETs in the drift-diffusion regime.	Charge control model derived from the 1D Poisson’s equation. Models only valid for undoped devices.
EPFL and InESS groups (led by J. M. Sallese)	Compact continuous model for DG MOSFET. Direct parameter extraction techniques.	Charge control model derived from the 1D Poisson’s equation. Model only valid for undoped devices in the drift-diffusion regime.
LETI group (led by Dr. O. Faynot)	Explicit compact model for asymmetrical Double Gate MOSFET. Charge and capacitance models.	Only valid for long-channel undoped devices. Quantum confinement ignored.
IMEP group (led by Prof. S. Cristoloveanu)	Physical model for the DG MOSFET channel current in the ballistic and quasi-ballistic regime. Self-consistency between the 1D Poisson’s equation and the 1D Schrödinger equation.	Charge control model derived from the 1D Poisson’s equation. Model not valid in the drift-diffusion regime.

L2MP/CNRS Laboratory, Marseille (led by Prof. J. -L. Autran); joint work with STM Francegroup (led by T. Skotnicki)	Analytical subthreshold DG MOSFET model in the ballistic regime. Compact DG MOSFET model in the drift-diffusion regime for doped devices. 2D short-channel effects included. Tunneling of carriers through the source-drain barrier. Quantum confinement included. Drift-diffusion model validated for GAA/SON devices down to *L*=30 nm.	The charge-control model is derived from a quasi-2D (and not strictly 2D) Poisson's equation. Model only valid for very thin films. Several fitting parameters used in the model for the drift-diffusion regime.
University of Pisa (led by Prof. G. Lannaccone)	Continuous model for DG MOSFETs and cylindrical surrounding gate MOSFETs, valid from ballistic to the drift-diffusion regime. DG MOSFET Model validated for FinFETs down to *L*=80 nm.	Charge control model derived from the 1D Poisson's equation.
UniK (Kjeller, Norway) (led by Prof. T. A. Fjeldly)	Fully 2D compact model for DG MOSFET valid for the ballistic regime and the drift-diffusion regime in very short-channel devices (based on conformal mapping). Self-consistency between the 2D Poisson's equation and the 1D Schrödinger equation.	The drift-diffusion transport modeling is only valid for very short-channel devices.

Conclusions and recommendations

European contribution to compact modelling of double and multiple-gate SOI MOSFETs has become very strong in the last years, in the framework of the SINANO Network of Excellence. So far, there are practically no models available in commercial versions of circuit simulators. Anyway, an alfa version of the so-called BSIMDG1.0 can be obtained from the web. On the other hand, the UFDG model, although not yet available in circuit simulators, has been proven to accurately fit the numerically simulated characteristics of FinFETs down to a channel length of 100 nm. Several compact models from European groups have been successfully compared with 2D and 3D numerical simulations and experimental measurements (down to L=80 nm in the case of Pisa group, and down to 30 nm in the case of L2MP group) in the drift-diffusion regime. There is still no specific compact model for FinFET which takes into account the effect of the top gate. One problem to validate models in the ballistic regime is the lack of proper numerical simulators in this regime.

EUROSOI State of the Art Report

Chapter 8. Circuit Design
Section 8.2. Digital Logic
Subsection 8.2.1. High-Speed (Microprocessor, Data Communications)

Date of Issue: April – 2009	**Partner: UCL**

Abstract

SOI for high-speed digital circuit design is briefly reviewed. PD-SOI has been explored from basic blocks up to complete μP. FD has not been fully exploited yet. The EU has not been competitive until now, but the knowledge has been developed and could be effectively exploited. A notable exception is the development of ARM IP cores which have been demonstrated in IBM PD SOI and OKI FD SOI.

Introduction

SOI is faster than Bulk for high-speed logic used in general purpose or dedicated (e.g. networking) microprocessors. A simple migration leads to 20-30% more speed, same power, in both partially (PD) and fully (FD) depleted technologies [1]. FD is the best compromise between leakage and dynamic power, performance, and ease of design, but not exploited adequately. PD, while easier to manufacture, presents design concerns due to the floating body (noise and hazards in dynamic logic, pass-gates and history-dependent timing). Industrial researchers (IBM, Motorola, ST, ARM) and universities (Florida, Columbia, Polito) focused on solving the latter and other SOI issues (e.g. no built-in decoupling capacitance requiring more thin-oxide MOS capacitors, need for special ESD protection, special layout and lvs/drc for body-contacted devices, long simulation for body voltage convergence) with methods and CAD tools [Bern.] [2] [3] [4] [5] [6] [7]. Basic blocks like ALU [8] and register files [9] for μP, mux-demux for networking [10] [11] up to complete microprocessors [12] [13] [14] [15] have been demonstrated and now PD is mature. The body contact has been explored to improve performance (DTMOS and its derivatives) [16]. For example, IBM has ported several generations of the Cell microprocessor for gaming applications on SOI PD process down to 65nm in production [17], and 45nm close to [18]. AMD continues with its high-end products on PD SOI. Both are now delivering foundry access. Below 45nm node, PD SOI suffers from variability issues and limitations on performances, similarly to bulk technology. Only undoped FD SOI and MuG FETs offer a drastic reduction of variability problems [19], which has however not been demonstrated at circuit level up to now.
Open challenges and opportunities are thus still full FD exploitation and demonstrators employing new technologies (3D integration with dual gate [20], finfet [21], etc.). Notably, for data communication using e.g. serial high-speed links (such as SERDES or PCI), no publications have been found in the literature (first to appear in IEEE SOI conference, 2009).

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
• CEA-Leti, France (M. Belleville): Contributor in digital circuit design, methodologies, DTMOS • STMIcroelectronics, France (P. Flatresse): Contributor in libraries design and characterization methods. • Polito, Italy (M. Casu): Contributor in DTMOS for high-speed and libraries characterization methods. • UCL, Belgium (D. Flandre): Very high-speed 64-bit adders [A. Nève et al, "Power-Delay Product Minimization in High-Performance 64-bit Carry-Select Adders", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 12 (2004) 235 – 244.]. SERDES design in PD SOI CMOS. • ARM, Grenoble, IP design methodologies for high-performance PD SOI.	Very strong know-how of SOI technology, devices and basic circuits. Potential exploitation of advanced SOI technologies (90nm, 65nm, 45 nm). ARM leading IP provider	No/few SOI experience on big circuit design (e.g. microprocessors, SoC)

Conclusions and recommendations

There remains a gap in EU w.r.t. USA in high-speed digital circuit design (academia and industry). Nonetheless the know-how is present in EU. It is highly desirable to grow and exploit it in SoC mixed-signal design, where general purpose and dedicated processors are integrated with analog and RF, targeting wireless telecommunications where EU holds an outstanding position. EU researchers should also contribute to demonstrate the performance of advanced and alternative technologies (e.g. double gate, finfet) on basic digital circuits for high-speed applications.
This depends on availability of simulation tools (in particular, models, but not only, efficient SoC design softwares such as optimizer and place & route are available in industry, not in universities) and technologies (regular MPW access). In both cases

organisations such as Europractice or CMP should be motivate to do so, which means strategically funded.
The lack of EU industry strategy on the topic remains the major blocking point. AMD and Intel collaborations and investments in the EU should be targeted.

EUROSOI State of the Art Report

Chapter 8. Circuit Design
Section 8.2. Digital Logic
Subsection 8.2.2. Low-power / Low-voltage.

Date of Issue: April – 2009	**Partner: UCL**

Abstract

Many academic and industrial works have reported the features that make SOI a serious candidate for low-power and high-performance applications. Moreover, the advantages of SOI in comparison with standard bulk CMOS, make low-power low-voltage techniques possible to implement with few penalty on circuits performances.

Introduction

As MOS transistors enter deep-submicron (DSM) sizes, undesirable consequences are being arising. Among those, the short-channel effects and the increase of static power consumption. On the other hand, the increased integration density follows an exponential trend with time [1]. The latter generates an increase by 4 times every 3 years in power consumption. Various techniques have been proposed to reduce the power consumption. They include the optimization at technological and device levels, supply voltage reduction, MTCMOS (Multi-Threshold CMOS) techniques to reduce leakage power [10], the choice of the suitable design style for primitive cells, the architecture optimization, the use of low-power oriented bus architecture where the internal bus voltage swing is reduced in order to save a large portion of power in VLSI systems [2] …etc. At the technological level, SOI was early reported as a serious candidate for low-power and high-performance applications. In 1998, IBM was the first company to use SOI for their servers and workstations [3]. Many companies like Samsung, AMD and Motorola followed the same trend [4, 5]. Recently at UCL, a fully-optimized 64-b carry select adder was implemented in 0.13µm PD SOI CMOS [6]. DTMOS device technique was also investigated and compared with floating body configuration in 0.13µm PD SOI CMOS [11]. On the other hand, in DSM process, static power has more widely to be taken into account. Indeed, with the continuous renewal of the technology generations, the leakage current will become even greater than the dynamic current in the overall power dissipation [7]. The choice of the suitable design style of the basic gates helps the designers to achieve low-leakage power consumption. A comparison of basic gates implemented with different design styles in 3 DSM technologies, was presented in [8]. The results have shown that conventional CMOS logic is more advantageous in terms of leakage power consumption than CPL (Complementary pass-transistor logic) and DPL (double pass-transistor logic) to implement both low order and high order NAND and NOR gates. While the low-power XOR gate proposed in [9] consumes leakage power 50% less than the CPL XOR gate. In [3], it is reported that two designs were implemented in IBM microelectronics for the 0.22µm CMOS generation, for a comparison purpose of bulk-Si and SOI performance at the microprocessor level. Simulation of a wide variety of critical paths had shown that performance gains of 20-35% are obtained when the design is implemented in SOI. This performance gain is due to the lower diffusion capacitance in SOI. As a consequence, a 22% reduction in total chip capacitance can be obtained. Moreover, SOI performance gain is higher as one goes to circuits using stacked devices. Different circuit dividers in both 0.12µm bulk CMOS and 0.12µm SOI CMOS

technologies, were compared in [13] with regard to their power-delay product. The lowest divider energy at an operating frequency higher than 20 GHz was observed on that of 0.12µm SOI technology, thanks to the lower parasitic capacitance offered by SOI technology. This makes both speed performance and power consumption advantageous in circuit divider implemented in the latter. On the other hand, in [14], the authors report that a test circuit containing a complete 40-bit pipeline which can be used in a DSP processor, was implemented in 0.12µm generation of bulk-Si and SOI. It was shown that for the same clock frequency, an active power consumption 2 times lower was measured in SOI as compared with bulk.
More recent studies at gate level confirm once more the SOI advantages over bulk in 0.13µm and 65nm generations [15,16].
Furthermore, a comparison of delay and power dissipation of 2-input NAND gates implemented with both DTMOS and fixed body configurations, was reported in [12]. It was shown that the speed advantage of the DTMOS gate over the fixed body increases as supply voltage is reduced.
Recently, new MTCMOS structures have been designed on SOI [17].
OKI has released ARM microprocessor cores on 0.15µm FD SOI CMOS confirming the above-mentioned benefits, as well as a more than tenfold increase of the resistance to transient radiations.
With scaling, subthreshold design to be discussed in the next section starts to offer performances of relevance for relatively high speed applications with reduced power [18]. However variability problems are enhanced in subthreshold and need attention, with undoped thin body FD SOI as an attractive solution.

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European Contribution on the Field	Current Situation	
European Groups: UCL (D. Flandre): development of MTCMOS flip-flops, latches… CEA/Leti, France (M. Belleville): standard-cell library for FD SOI technology and demonstration of basic digital circuits.	**Strong Points** Expertise is available.	**Weaknesses** Multi-threshold voltages are limited in DSM technologies.

Conclusions and recommendations

Although a lot of studies on basic circuit blocks (gates, adders, ...) show the advantages of SOI over bulk for low-power circuits, there is a lack of demonstrations on complete circuits (low-power microprocessors, ASIC's).

MTCMOS techniques are still difficult to implement in DSM technologies because only 1 or 2 threshold voltage values are available, which is not enough in some digital designs.

EUROSOI State of the Art Report

Chapter 8. Circuit Design
Section 8.2. Digital Logic
Subsection 8.2.3. Ultra Low Voltage

Date of Issue: April – 09	**Partner: ISEP & UCL**

Abstract

Future battery and self-powered portable equipments will require ultra low power consumption. This can be achieved by a strong reduction of supply voltage. SOI technology, with fully and partially depleted devices, is very well suited for ultra-low voltage digital design. Several digital circuits and systems working under 0.5V supply voltage have already been demonstrated.

Introduction

Lowering supply voltage (V_{dd}) is the best approach to reduce the power consumption of CMOS LSIs since the power dissipation is directly proportional to the square of V_{dd}. However, this lowering has to come with a threshold voltage scaling to maintain acceptable performance and is limited by the increase of leakage currents that follows. To compensate this degradation, the solution is to scale down the threshold voltage of the transistor at the expense of leakage current increase. Two main approaches have been proposed to deal with Ultra Low Voltage issues:

1.- "Zero Vt" concept: The goal is to target the maximum energy efficiency at a given ION/IOFF ratio which is usually set to 100. The maximum energy efficiency is obtained when the dynamic power consumption is roughly equal to the static one. In this case circuits can be operated at very low power supply and transistor threshold voltages. Circuits running at VDD = Vt = 200 mV have been demonstrated for CMOS technologies down to 180 nm. To compensate for process and temperature variations, back-biasing is usually used. It has been recently shown that for technologies below 130 nm the body effect of fast-device is by far not sufficient to compensate Lgate variations, responsible of an IOFF increase by a factor of 40 when comparing simulations to measures on a fabricated device. In addition device options targeting Vt = 150mV has shown a pronounced roll-off due to the lack of halo implant. The conclusion is that Ultra Low Vt and reasonable roll-off cannot be achieved simultaneously. The "Zero-Vt" approach is not a viable solution for Sub-130 nm CMOS technologies.

2.- "Standard-Vt" concept: The idea is to use standard technologies and to operate the circuits in the subthreshold/moderate region. This approach is suitable for some niches where performance is not an issue and where Ultra Low Power consumption is the target. Examples of such applications are solar operated devices, wrist watches, pacemakers, hearing aids etc…
Silicon On Insulator technology is a good candidate for Low Power applications, because:

- Good device isolation
- Reduced parasitic capacitances
- Better dynamic device characteristics
- Better Ion/Ioff trade-off

Besides these intrinsic advantages, Ultra Low Voltage Standard-Vt approach shows additional benefits:

- Dynamic power is strongly decreased
- For Vdd=500mV, at Vdd/2 the transistors of an inverter are in weak inversion à Short circuit current becomes a leakage current
- The leakage currents are directly related to the electric field in the device. Reducing Vdd will decrease drastically the electric field and then leakage currents such as I_{GIDL}, I_G, I_{DIBL}… are reducedIn Partially Depleted SOI, a degree of freedom is added when using Dynamic-Threshold transistor (DTMOS). The floating body is directly connected to the gate. The subthreshold slope S is close to the ideal value, the ration Ion/Ioff is excelent and the drivibility of the transistor is improved significantly but at the expenses of dynamic power consumption increase. The selective use of DTMOS may lead to performance improvement.

The two major challenges in this approach are delay penalty compensation and noise immunity control. Some work has been done at ISEP and others groups to deal with these issues as shown in the following references [1-12]
Partially-Depleted (PD) SOI devices may be used to realize ultra-low voltage circuits. An active use of the floating body effect in PD-SOI allowed Seiko to improve the performance of low-voltage and low-power operation to realize an ultra low power IC for wrist-watch application operating with V_{dd}=0.42V [13].Other works rely on the use of body-bias-controlled schemes to improve the performance at ultra-low voltage. In Dynamic-Threshold MOS, Threshold Voltage is dynamically controlled by connecting the body to the gate [14]. Several circuits with 0.5-V_{dd} based on DTMOS have been published [14, 15]. Main drawbacks of DTMOS are the extra layout area and gate capacitance. Moreover, some studies show that for advanced processes, performance of DTMOS are degraded due to increased body resistance and capacitance [16]. Methods to control the body biasing of selected PD-SOI transistors have also been proposed to realize ultra-low voltage circuits with high speed performance and low leakage in standby mode [17, 18].

The main advantages of SOI devices for ultra-low voltage operation are obtained with Fully Depleted (FD) SOI technology. Fully depleted SOI devices can operate at very low-V_{dd} due to their nearly ideal subthreshold slopes that make it possible to reduce the threshold voltage without leakage current increase. Regrouped in a national SOI project, japanese companies and universities (NTT, Sharp, Toshiba, Oki, Nec, Tokyo Institute of Technology) have demonstrated a short-range wireless system self-powered by ambient energy sources [19]. Oki has fabricated low-power LSI IC for a Casio solar watch where the microprocessor blocks (ROM, RAM, CPU, etc…) work at a supply voltage of 0.7V [20]. Flip-Flops, Adders, SRAMs and Processors in FD SOI operating under 0.5V-V_{dd} with ultra-low power consumption have been reported [19, 21, 22, 23]. The back gate bias has been demonstrated by OKI to reduce the corner problem due to process variability [24]. Nevertheless, with standard BOX thickness (>100nm), large bias voltages (5V) are required for efficient process variability mitigation. Ultra-thin BOX is thus a candidate to improve the efficiency of back gate bias [25].

From 2008, there has been a trend (Intel, MIT with TI, T.U. Eindhoven with NXP) at research level to design ultra-low-voltage subthreshold circuits in cutting-edge nanometer technologies (65/45nm) [26][27][28]. Indeed, 65/45nm technologies are interesting as they provide lower dynamic power consumption and allow cramming more devices and thus more functional units on the same core to provide sufficient throughput at ultra-low-voltage (parallel processing). Nevertheless, the increase of

short-channel effects (DIBL, degraded subthreshold slope) and variability raises noise margin issues for logic below 0.25V and implies and increase of the minimum energy level (trade-off between dynamic and static energies) between 90nm and 45nm nodes [29]. In this light, it has been shown at UCL that undoped thin-body FD SOI at 45nm node can provide 60% reduction of the minimum energy level (demonstrated on an 8-bit multiplier) with safe logic operation down to 0.15V [30].

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European Contribution on the Field	Current Situation	
European Groups: • STMicroelectronics/TIMA: ULV design in bulk (not in SOI up to now) • Polito, Italy (M. R. Casu): ULV design in PD-SOI • ISEP, France (A. Amara): modelling, ULV SRAM memory design, ULV Computing • UCL, Belgium (D. Flandre): ultra-low power digital blocks, SRAMs	**Strong Points** Modelling, design Design, process. Strong know-how in SOI technology and circuits design.	**Weaknesses** Lack of experience in large systems design. No advanced FD SOI process available yet in Europe.

Conclusions and recommendations

SOI technology offers many advantages for tomorrow's Ultra-Low-Power driven applications. Some open issues such as noise immunity, delay penalty compensation based on innovative circuits and architectures need to be addressed by the research community in Europe. Our groups, thanks to our close partnerships with LETI laboratory and STMicroelectronics, are ideally positioned to push the research in this direction.
We recommend encouraging new comers in this topic by submitting research proposals for EC funding.
The results obtained in Japan demonstrate the strength of SOI technology for ultra-low voltage digital design. European groups have the required know-how in SOI technology and ultra-low voltage circuits design but up to now, the results that were obtained were not implemented in complex systems. The access to an advanced FD SOI process is a necessary condition to the further development of this field in Europe. The LETI process development and promotion within EUROSOI+ is addressing this issue. The use of an undoped ultra-thin body FD SOI process is indeed a tremendous asset for subthreshold design tackling the variability challenge.

EUROSOI State of the Art Report

Chapter 8. Circuit design
Section 8.3. Memories
Subsection 8.3.1. SRAM

Date of Issue: Dec – 2009	**Partner: Polito**

Abstract

The use of SOI technology for SRAM circuits and its history is briefly reviewed. Milestones designs are referred. Key issues and potential are mentioned. The knowledge in EU for successful design of SOI SRAM is present.

Introduction

SRAM are fundamental for VLSI systems ranging from high-speed microprocessors (e.g. for cache memories) to low-power ASIC. Their fabrication capability has always been a technology test-bench since when SOI was mainly used in rad-hard applications. First SIMOX SRAM date to 80's and early 90's (NTT, 1k in '82, TI 16k-1M in '86-'93, IBM 256k-1M in '91-'93). After having recognized the potential of SOI for high-volume, the pioneering IBM's studies focused on solving PD-SOI floating-body effects [1] (data-dependent bitline capacitance and leakage, history effect in timing circuitry, data-dependent mismatch in sense-amps, parasitic bipolar effect in pass-gates and dynamic gates) and exploiting SOI unique features (reduced bitline capacitance, lower write level due to dynamic Vth, N+/P+ shunt and consequent substrate contacts removal, radiation hardness).
Proper design guidelines have been derived [2] and applied in migrating designs from Bulk to PD-SOI [3,4]. Nowadays, designing PD-SOI SRAM is a mature field: IBM, HP, TI published at the solid-state conference (ISSCC) microprocessors with hundreds kB caches (e.g. [5]), and SRAM blocks up to 8 Mb [13]. FD-SOI SRAM are of extreme interest in the field of rad-hard circuits [6], low power [7], low voltage [8] and in conjunction with microprocessors [9,10] or DSP [11]. Open challenges and opportunities are full FD exploitation and use of new technologies like 3D integration for improved memory density. SRAM cells with ultra-low-static power dissipation have been presented in 0.13 μm PD SOI CMOS [12].

With scaling well below 100nm, variability and leakage have become the major issues for SRAMs, leading to the introduction of alternative architectures around the basic 6T-implementation. In bulk, 8T-SRAM are used by Intel at 45nm node for low-voltage register files with improved SER resilience [14]. For ultra-low-voltage subthreshold operation or ultra-low-leakage applications, several new cell architectures with 8, 10 and even 12 transistors have been proposed to preserve static noise margins [15-18]. At the same time, many SRAM chips and bulk now propose dynamic biasing in order to minimize leakage in stand-by mode [14][17]. In PD SOI, 8T SRAM have been demonstrated by IBM [19], while dynamic cell biasing have also become common [13][20,21].
Nervertheless, as long as low-voltage nanometer technologies are concerned, the main advantage of SOI comes from the robustness of undoped thin-body FD SOI against Vt mismatch. This could be determinant for the adoption of such a technology at 32/22nm generations to enable low-leakage low-voltage operation of ultra-compact 6T SRAM cell [22,23]. Vt-mismatch, and thus SRAM scalability, is greatly improved in

narrow SOI FinFETs, with respect to planar bulk, because of their undoped channel and near-ideal gate control [24-26].

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
• CEA-Leti (M. Belleville) and ARM (J.L Pelloie), France: Contributor in PD and FD SRAM technology and design. • STMicroelectronics, France (P. Flatresse): Contributor in PD-SOI SRAM technology and design.Polito, Italy (M. Casu): Contributor in PD-SOI design and methodologies. • UCL, Belgium (D. Flandre): Contributor in SOI SRAM design for ultra-low-static power. • Glasgow University (A. Asenov): Contributor to FD SOI SRAM analysis (variability)	Very strong know-how of SOI technology, devices and its use implications in SRAM circuits.	Knowledge localized in excellence centers, need for dissemination, lack of industry adoption of new concepts related to lack of specific design tools

Conclusions and recommendations

SRAM circuits are fundamental for VLSI designs because of their large and always growing employment in SoC. It is fundamental to have at disposal memory generators (all views, from layout to HDL) and reliable models for design and simulation. This remains a key point the circuit design research community in the SOI field should pursue so as to facilitate the successful adoption of this technology by the EU industry, since, otherwise, the industry remains reluctant to adopt new SRAM concepts.

EUROSOI State of the Art Report

Chapter 8. Circuit design
Section 8.3. Memories
Subsection 8.3.2. Embedded DRAM

Date of Issue: April –2009	**Partner: UGR**

Abstract

The use of SOI technology for DRAM circuits and its history is briefly reviewed. Milestones designs are referred. Key issues and potential are mentioned. The knowledge in EU for successful design of embedded DRAM is definitely present.

Introduction

The rapid growth in DRAM density is limited by the minimum cell storage capacitance capacitance achievable under the constrains of soft error rate (SER), static and dynamic data retention time and the sense amplifier sensitivity. The major advantages of SOI DRAMs include the superior SER performance and static data retention time characteristics.

Embedded DRAM have long been discussed in SOI but did not penetrate industrial products until recently. Advantages of SOI for DRAM are classical: reduced bit line capacitance, better MOSFET switch properties, reduced p-n junction leakage, enhanced resistance to temperature elevation and transient radiations. The difficulty has been to efficiently integrate in SOI the ultra compact DRAM node capacitor. IBM has recently demonstrated and produced an SOI e-DRAM with a buried capacitor, describing the advantages of buried oxide Insulation to ease the process in comparison to Bulk [1,2].

A completely different alternative is also being promoted by different companies and public institutions (Innovative Silicon [3,4], Toshiba, Samsung [5], IMEP ...) Due to the difficulties for shrinking dimensions in the conventional DRAM capacitor while maintain a minimum capacitance (around 25fF/cell), the solution proposed is to suppress the capacitor storing the charge inside the floating body of an SOI transistor. These cells are commonly named One-Transistor-DRAM (1T-DRAM), Floating-Body-DRAM (FBDRAM) or Zero-Capacitor-DRAM (ZRAM). Claimed benefits are a drastic reduction of the DRAM cell node area ($4F^2$ theoretical vs. $8F^2$- $12F^2$ in conventional DRAM), a subsequent improvement of power and speed performance and a clear simplification of the process. The concept has been ported to many SOI processes, including FD and multiple gate [6].

In addition to EPFL and Innovative Silicon, as the pioneers of the Z-RAM invention, IMEP (Grenoble) and UCL (Belgium) have collaborated on the development of the MSDRAM alternative based on double-gate devices [7,8]. More recently a new concept conceived in collaboration between UGR (Granada) and IMEP (Grenoble) called A-RAM is being carefully investigated. A-RAM has demonstrated better potential scaling than other 1T-DRAM solutions due to its groundbreaking body architecture [9].

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
• UCL, Belgium (D. Flandre) and IMEP, Grenoble (S. Cristoloveanu): Contributor in FD SOI 1T-DRAM developments and innovations. • UGR: Development of propietary A-RAM technology. • EPFL/Innovative Silicon (P. Fazan): Patent and develop 1T-RAM concepts. • IMEC: 1T-RAM on UTB SOI.	Very strong know-how of SOI technology, devices and its use implications in 1T-DRAM or Z-RAM circuits. Industrial leader.	Wider industrial adoption of the concept

Conclusions and recommendations

Embedded DRAM is a key block of modern digital or system-on-chip products. On SOI, e-DRAM is mastered by IBM, whereas EU is the clear industrial and research leader for new 1T-DRAM/Z-RAM concepts. Industrial adoption of these new concepts is under intensive investigation.

EUROSOI State of the Art Report

Chapter 8. Circuit Design
Section 8.4. Analog & RF
Subsection 8.4.1. Analog and RF characterization techniques

Date of Issue: Sept – 2009	**Partner: UCL**

Abstract

Wideband characterization techniques are developed for extracting the electrical behavior of integrated active and passive devices in SOI technology.

Introduction

8.4.1.1 Wide frequency band characterization at room temperature

For high frequency characterization, properly-sized individual transistors with coplanar access pads and calibration (de-embedding) structures are required. Full wideband characterization consists in the following steps:
• DC large-signal I-V curves serve as a starting point for
- wafer-level monitoring of process variations
- selecting “good” devices and adequate bias points for subsequent ac characterization
- benchmarking against other technologies
- investigate large-signal non-linearities
- simulating large-signal circuits
• Measurements from DC to 100 MHz are necessary for in-depth understanding of intrinsic device properties and the subsequent precise and physical modeling and simulation, thanks to the characterization and extraction of the values of all internal time constants linked to floating-body or self-heating effects, generation-recombination and tunneling phenomena, RC couplings, 1/f noise, interface states, etc. [1]-[4].
• Microwave and Millimeter-Wave characterizations constitute powerful characterization tools to assess the dynamic and high frequency noise performances of various SOI transistors [5]-[9].
Figures of merit such current gain and maximum oscillation cut-off frequencies (f_t, f_{max}) can be extracted, and a small signal equivalent circuit (SSEC) is developed. Such SSEC is fundamental if one wants to relate microwave performance to technological or physical parameters [10]-[11].

8.4.1.2 DC to high-frequency characterization from low to high temperature (77-400K)

In order to correctly assess the potential of the technology, a set of DC and RF measurements is required both at room temperature but also over a broad range of temperatures
• Measurements at room temperature (300 K)
Large-signal non-linear I-V characteristics of utter importance for high-speed applications can be extracted at low frequency based on our dedicated IFM methodology and at high frequency based on non-linear vector network analyzer measurements [12]. At the mean time, the development of a full RF large signal model, for which the parameters are extracted from the DC I-V characteristic

(nonlinear drain expression) and accurate SSEC extraction (nonlinear gate charge expression), can be investigated [13]
• Measurements over a broad range of temperatures [77 to 400 K]
- Characterization at temperatures higher than room temperature is necessary to access the exact device performance under actual circuit operating conditions (in a range up to 340 K to 400 K depending on ratings). Temperature variations also allow to enhance certain behaviors or to reveal additional device properties.
- RF Noise Characterization at temperatures lower than the room one is also interesting to investigate down to 77 K (up to 50 GHz) with a two-fold objective; the study of channel noise [14] and the extraction of noise performance (noise figure).

All these techniques have recently been extended to FinFETs [15]-[19], Silicon-on-Nothing MOSFETs [20]-[21], Schottky Barrier MOSFETs [22]-[24], Graded Channel SOI MOS [25], as well as multichannel MOSFETs [26].

4-port VNA is also a quite interesting piece of equipment to deeply analyze the frequency behavior of advanced MOS devices. The body node in PD SOI MOSFETs using VNA multiport measurements has been analyzed over a wide frequency band in [27].

8.4.1.3 State-of-the-art RF Performance of SOI MOSFETs

Since the invention of the bipolar transistor in 1947, the operating frequencies of integrated transistors have been improved every year. In 1958, a cut-off frequency above 1 Giga-Hertz is reached with a germanium bipolar transistor [28]. Since that date, several integrated technologies have been investigated and improved to further increase the operating frequency of transistors. In 1965, a GaAs metal semiconductor field effect transistor (MESFET) appears in the literature [29]. In 1973, a maximum oscillation frequency (fmax) of 100 GHz is measured for a FET [30]. In 1980, a new architecture of field effect transistor with high electron mobility (HEMT) is proposed and fabricated [31]. In 1995, a cutoff frequency fmax higher than 500 GHz is extrapolated for a HEMT [32]. In 2000, the limit of 1 Tera-Hertz is reached with III-V heterostructure bipolar transistor (HBT) [33] and even overpassed by HEMT in 2007 [34].
It is only in 1996, thanks to the successful downscaling of the silicon MOSFET gate, that cutoff frequencies higher than 200 GHz are presented [35]. Since that date, the interest in MOSFETs for low voltage, low power, high integration mixed-mode ICs (digital and analog parts on the same chip) in the field of microwave and millimeterwave applications has been constantly growing. MOSFET is a well-known, well-controlled and mature technology, as well as cost effective, which makes it the key technology for mass production.
Nowadays, thanks to the introduction of mobility booster such as strained silicon channel, cutoff frequencies close to 500 GHz and 350 GHz are achieved, respectively, for n- and p-MOSFETs [36] with the channel length of 30 nm.
Despite the poor carrier mobility of electrons in silicon compared to III-V materials, silicon MOSFET can be considered as a competitive technology for high frequency applications. It is worth to notice that strained channel silicon MOSFETs even overcome the ITRS roadmap values which gives quite good prospects for silicon technology still for certainly more than 15 years from now on.

8.4.1.4 Main limiting factors for MOSFETs RF Performance

Historically, device scaling remains the primary method by which the semiconductor industry has improved productivity and performance. From the 100-nm technology node, CMOS technologies have been facing many grand technological challenges. In

this context, the most critical issue consists in the so-called short-channel effects (SCE). These parasitic effects tend to degrade the subthreshold characteristic, increase the leakage current and lead to a dependence of threshold voltage with respect to the channel length. Those static SCE have been reported theoretically and experimentally in the literature and solutions have been proposed. However, only a few publications have analyzed the limitation or degradation of high frequency characteristics versus the downscaling of the channel length. Considering a classical small-signal equivalent circuit for MOSFET, we can define the cutoff frequencies fc, fT and fmax representing the intrinsic (related to the useful MOSFET effect), the current gain and the available power gain cutoff frequencies, by expressions (1) to (3), respectively.

$$f_c = \frac{g_m}{2\pi C_{gs}} \tag{1}$$

$$f_T \approx \frac{f_c}{\left(1+\frac{C_{gd}}{C_{gs}}\right)+\left(R_s+R_d\right)\left(\frac{C_{gd}}{C_{gs}}\left(g_m+g_d\right)+g_d\right)} \tag{2}$$

$$f_{max} \approx \frac{f_c}{2\cdot\left(1+\frac{C_{gd}}{C_{gs}}\right)\sqrt{g_d\left(R_g+R_s\right)+\frac{1}{2}\frac{C_{gd}}{C_{gs}}\left(R_s\, g_m+\frac{C_{gd}}{C_{gs}}\right)}} \tag{3}$$

with gm, the gate transconductance, gd, the ouput conductance, Cgs, Cgd and Cds, the gate-to-source, gate-to-drain, and drain-to-source capacitances, respectively, Rg, Rd and Rs, the gate, drain and source access resistances, respectively.

The intrinsic cutoff frequency, fc, measures the intrinsic ability of a field effect transistor (FET) to amplify high frequency signals. As reported in [10], the fc values are a factor of 1.5 to 2 higher for HEMTs than for silicon MOSFETs with comparable gate length, and this is mainly explained by the respective dynamic properties of the two types of semiconductors (difference of gm which is directly proportional to the carrier mobility). In order to enhance the carrier mobility in silicon channel and then to improve the current drive and high frequency characteristics of MOSFETs, strained n- and p-MOSFETs have been investigated these last years. Beside the carrier mobility difference between Si and III-V materials, it has been demonstrated that the fmax/fT ratio is lower in the case of Si devices. As explained in [10], besides the well-know degradation of high frequency characteristics due to access resistances (Rg, Rd and Rs), the decrease of the ratios gm/gd and Cgs/Cgd in CMOS technology strongly contributes to the limiting improvement of fT and fmax with the transistor channel length skrinkage. The increase of the output conductance, gd, with the reduction of gate channel length is one of the well-known short channel effects of FET devices. The degradation of the ratio Cgs/Cgd means a loss of channel charge control by the gate and an increase of the direct coupling capacitance between gate (input) and drain (output) terminals. The self-aligned source and drain regions, one of the main advantages of MOSFET structure, are also a reason for the increase of parasitic capacitances between source and gate and more importantly drain and gate. As demonstrated in [10], from extraction results the Cgs/Cgd ratio is equal to 7.8 for the HEMT and only to 1.5-1.6 in the case of a MOSFET with 90-nm gate length.

It is therefore obvious that the optimization of these internal parameters will be crucial in order to further improve cutoff frequencies of ultra deep submicron MOSFETs. The impact of lightly doped drain (LDD) dose and energy implant as well as annealing temperature and time on Cgs/Cgd ratio, gm and gd and then on fmax has been investigated in [37]. The results demonstrate that LDD implant can indeed be considered as an optimization parameter for improving fmax and especially the ratio Gass/NFmin (Gass and NFmin being the associated power gain and the minimum RF

noise figure, respectively), which is the most important figure of merit for low noise microwave applications. However, the optimization window is quite narrow and it seems difficult for a given technological node to get higher Cgs/Cgd and gm/gd ratios than 2 and 6, respectively, for a classical sub-100-nm gate length MOSFET structure. It is the main reason why fmax is almost equal to fT in the case of MOSFETs and not 1.5 to 2 times higher as in the case of HEMTs with similar gate length and characterized by Cgs/Cgd and gm/gd ratios of 8 and 20, respectively.
In order to further improve the microwave performance of deep submicrometer MOSFETs, it seems crucial to keep the parasitic resistances and capacitances as low as possible, and to consider alternative MOS structures for which the Cgs/Cgd and gm/gd ratios (analog SCE) are improved.
Several technological options have been presented in the litterature those last years to push further the digital and analog performance limits of single gate Si MOSFETs such as:
• Move from bulk Si MOSFETs to partially depleted (PD) [37] or fully depleted (FD) [38] SOI MOSFETs to enhance the gate electrostatic control on the channel carriers and thus minimize the SCE. Nowadays, ultra thin body (UTB) MOSFET in SOI technology with a silicon body thickness less that 10 nm has been proposed [39]-[40]. Thanks to the buried oxide layer (BOX) underneath the SOI transistors, their junction capacitances to the Si substrate are drastically reduced;
• Strained MOSFETs have been largely investigated lately to improve the carrier mobility. The mechanical stress in the channel orginates from specific process steps [41] added into the classical CMOS process flow. Nowadays, strained SOI wafers are produced as well for which the top silicon layer is under a certain level of stress [42]-[43];
• Low Schottky barrier contacts [22]-[24], [44]-[45] are foreseen as a very interesting candidate to lower the source/drain contact resistances, to form abrupt junctions (no overlap), and drastically reduce the thermal budget for CMOS process;
• Metal gate allows to get rid of loss of electrostatic gate control related to the polysilicon gate depletion [46]-[47], as well as to reduce the gate sheet resistance;
• Low-k and air gap [48]-[49] should be introduced to reduce fringing capacitances between gate-to-source and gate-to-drain electrodes;
• SOI wafers with thin BOX have been proposed these last years to reduce SCE (for instance, DIBL) but also to lower self-heating issues [39]-[40], [50]-[51];
• High resistivity silicon substrate has demonstrated superior characteristics for the integration of high quality passive elements such as transmission lines [52], inductors [53], etc., as well as for reduction of the crosstalk between circuit blocks integrated on the same silicon chip [54].

In [18], simulation and experimental results indicate that FinFET is a multiple gate structure of interest to reduce digital short channel effects and then assure a lower threshold voltage roll-off, a better subthreshold slope and then higher Ion/Ioff ratio, but the high frequency performance such as the cutoff frequencies as well as RF noise figure are degraded compared to its Single Gate MOSFET counterpart because of the increased fringing capacitance linked to its complex 3-D non-planar architecture. Consequently, a trade-off exists regarding Wfin between high fT and fmax (large Wfin) and good control of SCE (small Wfin).

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European Contribution on the Field	Current Situation	
European Groups: UCL, IEMN, IMEC	**Strong Points**	**Weaknesses**
Comments: A strong analog characterization basis exists in Europe and especially through the European Associated Laboratory – LEMM – between UCL and IEMN.	The developed characterization methods are really unique and are based mainly on a strong and deep collaboration between microelectronics and microwave laboratories.	

Conclusions and recommendations

In order to fully understand the physical behavior of integrated devices, wideband extractions are needed. These characterization methods allow to develop compact models, give insights about the physical phenomena, figure out the impact of some technological parameters on the device performance and therefore improve the fabrication process itself by providing solutions.

EUROSOI State of the Art Report

Chapter 8. Circuit Design
Section 8.4. Analog & RF
Subsection 8.4.2. HR Substrates & Crosstalk Analysis

Date of Issue: Sept – 2009	**Partner: QUB & UCL**

Abstract

The reduction of device dimensions allows operation in the gigahertz region and provides the opportunity for low-cost integration of RF/digital/analog functions on the same chip for system-on-chip (SOC) applications. SOI will be the technology of choice if it meets the performance requirements for RF applications. However, low-resistivity substrates have limited the integration of high-quality passive components.
The use of High Resistivity Silicon (HR-Si) is foreseen as a promising substrate for radio frequency integrated circuits (RFIC) [1] and mixed signal applications [2], but is known to suffer from surface effects and resistivity degradation near the insulating oxide [1,3,4,5]. Different methods have been proposed to get rid of parasitic surface conduction in the substrate of high resistivity Silicon-on-Insulator wafers. One of such methods consists in passivating the HR substrate with a Rapid Thermal Anneal (RTA)-crystallized layer of silicon before the bonding step.
The challenge in using high-resistivity substrates is to do so in a manner that maintains the device characteristics in order to re-use the digital libraries for lower design cost.

Introduction

High Resistivity Silicon (HR Si) (i.e., ρ > 3 kΩ.cm) is foreseen as a promising substrate for radio frequency integrated circuits (RFIC) [1] and mixed signal applications [2], but is known to suffer from surface effects and resistivity degradation near the insulating oxide [1,3,4,5]. Indeed, charges within the oxide attract free carriers near the substrate surface, reducing the effective resistivity (ρ_{eff}) of the wafer and increasing substrate losses. It has been recently shown in [6] that Q_{ox} values as low as $1x10^{10}$/cm² could lower the value of ρ_{eff} by more than one order of magnitude. Parasitic surface conduction can be strongly reduced if the silicon substrate is passivated before oxidation with a trap-rich, highly resistive layer. This has been successfully achieved using Low Pressure Chemical Vapor Deposited (LPCVD) polysilicon (polySi) and amorphous silicon (ρ-Si) in [7] and [8], respectively.
We investigate the possibility of including a passivation layer within the structure of a classical Silicon-on-Insulator (SOI) HR wafer by bonding an oxidized wafer with a passivated HR substrate. In this context, it is known that due to its high roughness value, the surface of LPCVD polySi layers requires the use of Chemico-Mechanical Polishing (CMP) before bonding, which is a critical and expensive step. On the other hand, ρ-Si is thermodynamically unstable throughout the temperature range of standard CMOS processing. Its inclusion inside a SOI wafer would therefore severely limit the application range for that wafer. We therefore propose a new passivation method to overcome these two issues, which consists in the deposition of amorphous silicon deposited at 525°C onto the HR Si substrate followed by a rapid thermal anneal (RTA) during 120s, at 900°C to crystallize and stabilize the amorphous layer. Improvements have been demonstrated compared to the two reported methods in

terms of substrate passivation efficiency, surface roughness and stability over long thermal anneals.

The effective resistivity (ρ_{eff}) of the wafers are extracted from the measurements of CPW lines with a method depicted in [9]. This latter parameter accounts for the wafer inhomogeneities (i.e., oxide covering and space charge effects) and corresponds to the resistivity that a uniform (without oxide and space charge effect) silicon wafer should have in order to sustain identical RF substrate losses. In other words, it is the value of the substrate resistivity that is actually 'seen' by the coplanar device.
It has been demonstrated that substrate passivation is more efficient with crystallized than with amorphous silicon. This is due to the higher density of traps in polysilicon than in amorphous silicon [12]. Moreover, ρ_{eff} is higher in the case of the RTA-crystallized silicon layer, for which the HR substrate can be considered as lossless, than in the case of the as-grown polysilicon layer. This is also associated with trap density variations. Indeed, traps in polysilicon are mainly located at grain boundaries [13], which makes their volume density dependent on the size of the grains: The smaller the grain size the higher the trap concentration. Pictures obtained by Scanning Electron Microscopy (SEM) show that the typical columnar structure of polySi grains is not present in the RTA-crystallized silicon: The latter displays a much higher density of small, round-shape grains. This particular grain morphology is due to the high and fast thermal stress endured by the sample during the RTA.
The thermal stability of the different passivation layers has been also investigated by submitting the wafers to a 4 hour-long thermal anneal at 900°C, in order to mimic the thermal budget of a CMOS process. It indicates that long temperature anneals have a beneficial impact on ρ_{eff} in the case of crystallized silicon layer. In both cases the increase of ρ_{eff} can be explained by the effusion of H^+ ions, which has the effect to un-passivate traps and increase the total trap density in the passivation layer. It was observed that ρ_{eff} is less affected in the case of crystallized silicon layer, suggesting a higher stability and less hydrogen release when the HR substrate is passivated with RTA-crystallized silicon.
To investigate the suitability of the different passivation layers to be included inside a SOI wafer fabrication process, the surface of the passivated wafers was also analyzed with atomic force microscopy (AFM) on 2µm x 2µm squares. The AFM measurements gave access to surface morphological parameters such as mean roughness and maximum height. The rms roughness / maximum height were 0.37nm / 3.14nm, showing that these low values are expected to ease the bonding with an oxidized donor wafer, and, according to literature data [14], bonding without chemical-mechanical polishing (CMP) could also be achieved. As a consequence, this passivation method appears as a suitable technique for the fabrication of substrate-passivated HR SOI wafers with enhanced and stable resistivity (10 kΩ.cm).

MMICs on SOI

With the introduction of SiGe HBTs and the continued scaling of CMOS technology silicon devices can now operate in the gigahertz regime. This provides an opportunity for silicon RF/system on a chip with mixed analogue and digital circuits and thus at reduced costs. To fulfil these aspirations it is necessary to overcome the degradation of quality (Q) factor of inductors, cross-talk and the noise coupling between the inductors, the digital logic circuits and the analogue circuits.

Some researchers have chosen backend processing solutions after the active devices have been formed on the standard low resistivity silicon. The principle here is to space the passive components about 10 µm above the low resistivity silicon so that the electric field, which penetrates the silicon is much reduced. This has been achieved by

depositing thick layers of polymer such as polyimide, BCB or SU-8 photoresist on the silicon wafer before forming the passive structures on top of the polymer. This layer spacing technique could also be used for rf circuits fabricated on SOI substrates.

A variation on the above post processing spacer technology is to form regions of porous silicon or cavities in the low resistivity silicon substrate where the passive components are to be located. For SOI technology these techniques can be applied as porous silicon regions in the handle wafer or silicon on nothing technology. Other post processing approaches were based on converting the low resistivity silicon to high resistivity. This could be achieved either by very high energy proton radiation or by gold diffusion at low temperatures from the backside of the wafer. This technique generally employed an SOI type structure with a silicon nitride barrier layer in the buried oxide to protect the active devices. This approach requires accurate control of the degradation mechanism.

RF circuits on GaAs benefited from the use of semi-insulating substrate material below the active epitaxial layer. This led researchers to consider the high frequency characteristics of high resistivity silicon (HRSi). Employing coplanar waveguide lines and single layer spiral inductors researchers from Motorola (Arizona) showed that silicon with a high resistivity greater than 3kΩ-cm could be used as a microwave substrate. Silicon has a lower band gap than GaAs, which makes it more sensitive to temperature. At 80°C the intrinsic carrier density begins to lower the resistivity of the HRSi. They demonstrated that the losses for CPW lines on HRSi were comparable to the losses of similar CPW lines on GaAs.

Integration of the CPW lines with active devices on HR Si substrates revealed that there was considerable bias leakage current between the centre signal conductor and ground lines. Separating the CPW lines from the HR Si by a dielectric layer of SiO_2 resulted in a considerable increase in attenuation. The increased attenuation was attributed to the induction of mobile charge near the silicon oxide interface due to the fixed charge in the oxide and/or dc bias on the signal line. If the oxide was removed from the silicon surface in the regions between the centred signal conductor and the ground lines then the increase in attenuation was greatly reduced. In the absence of the oxide there was little mobile charge in the silicon surface in these regions. Researchers at Queen's Belfast reasoned that if the charges induced in the silicon under the oxide were trapped so that they could not respond to the microwave signal then they would not contribute to attenuation losses. Thus these researchers deposited a thin layer of undoped polycrystalline silicon on the HR Si surface before depositing the oxide. Undoped polycrystalline silicon has a resistivity of approximately 10^5 Ω-cm. CPW lines on silicon dioxide on polycrystalline coated HR Si substrates have lower losses than when the metal CPW lines are in direct contact with the silicon. To produce similar highly defect silicon surface layers to trap mobile charge other works have used PECVD amorphous silicon or argon implants to amorphize the silicon surface. These are low temperature processes and so can be used in selective areas after active device fabrication.

A disadvantage of using HR Si is that it is not very suitable for the fabrication of active CMOS or HBT devices which require low resistivity silicon. The ideal solution would be to use bonded SOI substrates where the active SOI layer is low resistivitiy silicon and the handle wafer is HR Si. The active devices are fabricated in SOI islands and the passive components are fabricated on areas where the SOI layer has been removed. To ensure that the surface of the HR Si handle below the buried oxide layer remains high resistivity, a polycrystalline silicon layer is deposited on the handle wafer before bonding. Thus these SOI wafers with passivated HR Si handles offer considerable promise for RF ICs. Only IC compatible material is used so there are no contamination

problems, CPW losses are low, inductor quality (Q) factor should be high, cross-talk should be low and the wafers are relatively cheap. The main limitation of these substrates is that they may be only suitable for operating temperatures up to 100°C.

When considering silicon for RF ICs, researchers at Stanford considered the degradation in the inductor quality (Q) factor at high frequencies. They showed that to minimise quality (Q) factor degradation the substrate should either be a pure conductor or a pure dielectric. The HR Si technology outlined above corresponds to the pure dielectric approach. The pure conductor can take the form of a highly conducting ground plane.

RF ICs

The use of SOI substrates provides better device isolation, reduced capacitance, reduced leakage, higher frequency operation and higher packing density. In mixed signal high frequency circuits there can be a significant amount of energy injected into the substrate from the switching digital circuitry. This noise can then be transmitted through the substrate to interfere with the performance of the sensitive analogue circuitry. At lower frequencies the buried oxide isolation of SOI substrates provides some improvement in cross-talk suppression. However, with the improvements in device frequency performance the reactance impedance provided by the oxide decreases and there is no improvement in cross-talk performance at frequencies above 0.5 GHz. Thus some researchers decided to investigate the use of SOI wafers with low resistivity active layers and very high resistivity silicon handles as these were being advocated for mm wave applications. These substrates could be prepared by wafer bonding of HR Si handle wafers to oxidised low resistivity silicon wafers. One such group at Louvain-la-Neuve, Belgium devised a simple test structure for studying the degree of cross-talk for a given structural arrangement. This effectively allows the amount of coupling from a diffused drain to an adjacent capacitor or diode to be measured. They found a significant reduction in cross-talk with the use of HR Si handles of 5 k Ω-cm for frequencies up to 10 GHz. By employing diffused guard rings the cross-talk was further reduced. Other research groups took a different approach to suppressing the cross-talk. In their approach the surface of the silicon handle is kept at a constant potential and any injected energy is shunted away via a highly conducting ground plane. Since the surface potential of the handle is fixed then there are no voltage variation to transmit noise through the substrate and the cross-talk is confined to the SOI layer and the buried oxide layer. SOI wafers with tungsten silicide ground planes (GPSOI) between the buried oxide layer and the handle wafer are produced by Queen`s Belfast. Using similar test structures as the Louvain-la-Neuve group a significant increase in cross-talk suppression was obtained. To further reduce the cross-talk a Faraday cage like structure was fabricated with vertical trenches lined with tungsten silicide. A further reduction in cross-talk was obtained with the main contribution coming from the measuring probes. The technology is aimed at mixed signal ICs where the sensitive analogue circuitry could be enclosed in a Faraday cage to protect it from noise generated by the digital circuitry. Recently researchers at MIT (Massachusetts) have used a Faraday like cage with bulk silicon. In their case the silicon is thinned to 100 microns a through holes are formed by ICP etching. The through holes are coated with a nitride liner before the back of the wafer and the through holes are plated with copper. The plated through holes form the vertical walls of the Faraday cage.

A disadvantage of employing buried ground planes is that if inductors are required they greatly reduce the quality (Q) form factor. In general the quality factor (Q) for an inductor on a silicon substrate is degraded due to energy dissipated in the substrate. Researchers at Stanford University have shown that this substrate loss can be

overcome if the substrate is a pure dielectric or a perfect conductor. The latter can effectively be achieved by the inclusion of a heavily diffused region on the handle surface or a metallic ground plane. The required sheet resistance of the ground plane is a function of the buried oxide thickness, the size of the area being shielded and the frequency of operation. The effective resistance of the ground plane should be considerably less than the reactive impedance provided by the buried oxide. Thus the sheet resistance of the ground plane must decrease as buried oxide layer is reduced and frequency is increased. The conducting ground plane shields the electric field from the silicon substrate. However, the changing magnetic field of the inductor will induce image or eddy currents in the ground plane. These induced currents will circulate in opposite direction to those in the inductor. Thus the mutual coupling reduces the magnetic field and thus the actual inductance.
The above suggests the use of GPSOI substrates with HR Si handles and where the metallic ground plane is removed in areas allocated for inductors. However inductors occupy large areas and it is very difficult to planarise such areas sufficiently well to facilitate wafer bonding. A simple solution to this problem was not to completely remove the ground plane under the inductors but to pattern it into an array of discrete islands. These islands act as reference points during the planarisation process and so the handles can be bonded. If the islands are small enough the image currents cannot flow and so the quality factor (Q) of the inductors is not degraded.

A patterned ground plane could also be used with low resistivity handles if it is patterned with find slots not into islands but in a manner to prevent image currents from flowing. With such fine slots the electric field is grounded and thus prevented from reaching the silicon substrate. If the ground plane resistance is low, then energy loss will be kept to a minimum. The need for patterned ground planes located to under inductor areas means that the substrates have to be custom prepared or regions set aside as connection pad and inductor area.

An alternative is to use post device island patterning processes to provide cross-talk suppression and minimise inductor quality form (Q) degradation. For cross-talk suppression the emitter and receiver nodes are surrounded by diffused guard rings in the handle wafer. These are produced by trenching through the buried oxide layer and then implanting the exposed handle regions to form the guard rings. These diffused guard rings are contacted from the top by the interconnect metallization. The inductor quality factor (Q) is protected by implanting the SOI layer where the inductor is to be located so that it becomes an effective ground shield. The sheet conductivity of the layer must not be too high or eddy currents will flow degrading inductor performance. The SOI ground shield could be patterned so that the electric field could be shielded from the handle without introducing eddy currents.

SOI substrates are recognised as a means of reducing parasitic capacitances, of improving isolation, reducing leakage currents and providing shallow junctions. In considering the merits of low and high resistivity handles other aspects of device/circuit performance needs to be considered. These include transistor transition frequency f_T, linearity and noise figure. The f_T of an MOST is nearly inversely dependent on the gate capacitance and so the f_T of small transistors can be significantly reduced when input pads or inductors are directly connected to the gate.

Modelling of the influence of pad substrate parasitics on transistor f_T shows that the degradation is reduced for high resistivity substrates. However, the use of high resistivity bulk silicon for CMOS requires special processing to avoid latch up problems and cross-talk. The use of SOI with an HR Si handle greatly minimises pad and interconnect parasitics of transistor f_T. Thermal noise sets the lower limit of detectable signal in a receiver front-end. Substrate noise enters via the pads or large

area inductors and is amplified by the transistors. Theoretical studies show that substrate induced thermal noise is minimised for Fully Depleted SOI (FDSOI) transistors on high resistivity handles. While for FDSOI transistors on low resistivity substrates the noise is similar to that for bulk devices. Reduced noise figures for transistors on HR-Si substrates has been experimentally verified. However, if the drain voltage is increased the noise figure for the FD-SOI devices will increase rapidly due to impact ionization-induced shot noise. This low-breakdown voltage for SOI devices must be taken into consideration in circuit design. SOI devices are free from the voltage-dependent drain capacitance, which is a contributor to device non-linearity. However, they have the additional floating body and kink effect, which result in a nonlinear output conductance. Nevertheless the lowest report noise figures at 2.5GHz operation have been achieved from LNA's on high resistivity SOI substrates.
There are no reports of rf circuits having been fabricated on GPSOI nor of any theoretical studies on the effect of the ground plane on noise figure or linearity. SOI substrates with surface passivated HR-Si handles are considered to have considerable potential both for RF and MMICs.

The transfer of partially and fully processed RF circuits on bulk or SOI substrates to non-silicon substrates is another technique that has yielded some success. Philips has developed a glue, which allows them to attach a fully processed wafer to a glass substrate. The silicon substrate is then thinned back by grinding and/or etching. The technique is particularly effective when using SOI wafers as the buried oxide layer is an excellent stop for polishing and etching back of the handle wafer. Low temperature processing of passive components can then be carried out on the glass substrates.

The processed silicon layer is inverted on the glass substrate and the structure has a limited capacity for heat removal. Some researchers are investigating the double transfer of the processed active layer onto substrates such as sapphire. The original surface of the processed active layer is again on top and heat can be removed through the thermally conductive sapphire substrate. In this way the RF-ICs can be produced in a standard IC fabrication plant benefiting from the use of large substrates and reduced production costs. The processing of silicon on sapphire is a specialized process at only a few production facilities and hence a fairly expensive process. The double transfer process has also an application in stacked or 3-D integrated circuits.

Crosstalk

In recent years, rapid progress of integrated circuit technology has enabled the co-integration of analog front-end and digital baseband processing circuits of communication systems onto the same chip. Such mixed-signal systems-on-chip (SoCs) allow more functionality, higher performance, lower power and higher reliability than non-integrated solutions, where at least two chips are needed, one for digital and one for the analog applications. Moreover, thanks to CMOS technology scaling and its associated increasing integration level, SoCs have become the way to achieve cost effectiveness for demanding applications such as home entertainment and graphics, mobile consumer devices, networking and storage equipment.
Such a rising integration level of mixed-signal ICs raises new issues for circuit designers. One of these issues is the substrate noise generated by switching digital circuits, called digital substrate noise (DSN), which may degrade the behaviour of adjacent analog circuits. DSN issues become more and more important with IC evolution as: (i) digital parts get more noisy due to increasing complexity and clock frequencies, (ii) digital and analog parts get closer and (iii) analog parts get more sensitive because of Vdd scaling for power concern issues.
In general, substrate noise can be decomposed in three different mechanisms: noise generation, injection/propagation into the substrate and reception by the analog part.

Improvement in the reduction of any of these three mechanisms, or in all of them, will lead to a reduction of the DSN and in a relaxation of the design requirements. Typically, guard rings and overdesigned structures are adopted to limit the effect of substrate noise, thereby reducing the advantages of the introduction of new technologies. It is thus a major issue for the semiconductor industry to find area-efficient design/technology solutions to reduce the impact of substrate noise in mixed-signal ICs.

This last decade several publications have demonstrated theoretically and experimentally the interest of high resistivity SOI substrate to greatly reduce the crosstalk level between integrated circuits [11]. In [15], the significant dependence of the crosstalk with respect to the applied bias has been highlighted. The crosstalk level is strongly reduced for negative bias and when deep depletion is formed below the BOX, whereas it is enhanced and exhibits higher cutoff frequencies for positive bias and increased inversion below the oxide. On the other hand, the passivated wafer exhibits: (i) no effect of the applied bias due to the presence of the trap-rich polysilicon layer below the BOX [16] and (ii) a perfect 20-dB/dec slope which shows that purely capacitive coupling occurs in the measurable frequency range (i.e., above the noise floor of the VNA). A reduction of crosstalk below 1 GHz is of particular interest for mixed signal applications, since it is known from previous studies that the frequency spectrum of the noise generated by digital logic typically expands to several hundreds of megahertz, corresponding to multiples of the clock signal or circuit internal resonance frequencies.

In [17], we compare experimental DSN characterizations of CMOS circuits lying on SOI and bulk Si substrates. Current injected into the substrate creates substrate voltage fluctuations (substrate noise). It is mainly created by two mechanisms: coupling from the noisy digital power supply circuit and from switching drains.

The DSN for 8 switching inverter trees biased at either 0.8 or 1.2 V and for an input clock frequency of 225 MHz has been measured in the case SOI and Si bulk substrates. DSN for SOI circuit presents a quite different frequency response. At low frequency, SOI and Si bulk present the same kind of response, with the SOI DSN level decreasing faster with increasing frequency. At higher frequency, the SOI DSN presents a kind of “pass-band filter” shape, which is not visible in the case of the bulk circuit. We have shown in our previous work that this second part of the frequency response is due to ringing on supply rail, due to parasitic capacitances and inductances [18]. For the 1.2 V supply voltage, the SOI technology allows an important reduction of DSN up to 1 GHz. At higher frequency, the noise due to ringing on supply rail becomes dominant, and the bulk circuit shows a lower DSN level. This conclusion is in agreement with the results of studies on the supply noise showing that special attention should be paid to supply rail for SOI technology, due to lower intrinsic decoupling capacitances. At lower power supply (0.8 V), as for the bulk, high frequency noise generation decreases. The ringing supply noise tends thus to be negligible. The SOI technology presents then better DSN results than bulk for frequency up to 2 GHz, and similar DSN level for upper frequency.

The decrease of the DSN should be even more pronounced if a passivation layer (trap-rich layer) is introduced underneatch the BOX.

Non-linearities along CPW lines

High-resistivity silicon substrates are promising for RF applications due to their reduced substrate loss and coupling, as presented in the two previous paragraphs, which helps to enable RF cellular transmit switches on SOI using HRS handle wafers [19]-[20]. RF switches have high linearity requirements: for instance, a recent III-V RF switch product specifies less than -45 and -40 dBm for 2nd and 3rd harmonic power (H2 and H3), respectively, at +35 dBm input power [21]. As requirements become even more stringent for advanced multimode phones and 3G standards, it is important

to investigate even small contributions to harmonic distortion (HD).
As explained above, when the CPW line is biased the distribution of potential and free carriers inside the Si substrate changes like in the case of a classical MOS capacitor. The variation of carriers distribution in the Si substrate with the applied bias or large RF signal will thus lead to the existence of non-linear capacitance (C) and conductance (G) associated with the Si substrate. Those variable C and G are at the origin of the harmonics formation inside the Si substrate.
In [22], it has been demonstrated that the harmonic distortion (HD) of Al metal lines on thermally oxidized HRS p-type substrates of different resistivities. The 1 kΩcm substrate presents lower HD than the 20 Ωcm substrate over most of the power sweep. A drastic drop of the HD is observed when the HR Si substrate is passivated with a trap-rich layer (as-deposited amorphous silicon), that is, by at least 50 and 65 dB in H2 and H3, respectively, or to the noise floor. As explained above, thanks to the high density of traps in the polycrystalline silicon or as-deposited amorphous silicon layer located at the Si-SiO2 interface, the surface potential at this interface is nearly fixed, and the external DC bias or large amplitude RF signal applied to the line does not impact the distribution of carriers inside the Si substrate.

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
SOITEC, France Queen's University, UK UCL, Belgium	Characterization methodology which allows fair comparisons between various Silicon and SOI substrates is available. UCL has a complete CMOS process fabrication line. It is flexible and allows fast prototyping.	Commercial SOITEC substrates have an effective resistivity of only about 200 Ωcm. Research susbtrates demonstrated more efficient at material level have not been integrated in larger platforms and with active devices.

Conclusions and recommendations

Characterization methodology for the extraction of the substrate effective resistivity is available for fair comparison purposes. Extremely high resistivity substrates have been built and fully characterized. This new type of SOI substrates is very promising for RF analog applications.

However, the properties of SOI substrates are now well captured in design tools. Notably a crosstalk simulator at circuit level adequate for SOI is still missing. EU competence are strong in this domain but there remains no major EDA tool vendor in EU.

EUROSOI State of the Art Report

Chapter 8. Circuit Design
Section 8.4. Analog & RF
Subsection 8.4.3. RF modeling (small signal, noise)

Date of Issue: Nov – 2009	**Partner: URV**

Abstract

The present state-of-the art on RF SOI MOSFET modeling is described.

Introduction

SOI MOSFETs are excellent candidates to be an alternative to bulk CMOS in RF applications. In fact, their high frequency performances are better than those for bulk CMOS. However, not much work has been done on SOI MOS modeling at high frequencies. Less work has even been done to study the high frequency noise performances. In Europe, the URV/UCL model for FD SOI MOSFETs has been adapted to RF conditions, being successfully checked using the version implemented in the internal version of ELDO. Most of the SOI MOSFET models available in commercial circuit simulators do not include any extension to RF. BSIMSOI includes a module for RF, but it has some limitations (for example, the gate resistance is not included).

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
URV group (led by Prof. B. Iñíguez)	FD SOI MOSFET model validated up to L=0.13 μm and frequencies up to 30 GHz.	Model only valid for FD MOSFET.

UCL group (led by Prof. D. Flandre)	Currently working with URV group on FD SOI MOSFET modeling. The group developed parameter extraction methods in RF.	The only complete available model is only valid for FD MOSFET.
IEMN group (led by F. Danneville)	Working on RF SOI MOSFET noise modelling together with the URV and UCL groups.	No compact model for PD SOI MOSFETs.
LETI group. Led by Dr. O. Faynot (developed the LETISOI model).	LETISOI model for PD SOI MOSFETs adapted to RF. Validated for channel lengths down to 0.13 μm and frequencies up to 10 GHz.	The model has not been extended to the nanoscale range of channel lengths.

Conclusions and recommendations

There are not may European groups working on the compact modelling of SOI MOSFETs in RF. The URV/UCL macro-model for RF FD SOI devices was successfully tested for frequencies up to 40 GHz and channel lengths down to 0.13 μm, but is only available in an internal version of ELDO. IEMN, through a collaboration with those groups, have developed a model for RF noise in FD SOI MOSFETs, which includes the shot noise due to gate tunnelling but is not available in any simulator yet. Much less work has been done in Europe regarding modeling of PD SOI MOSFETs in RF. The LETI group extended their LETISOI model (for PD SOI MOSFETs) to RF and validated it up to 10 GHz.

Philips level 11 model becoming the standard recommended by the model council for deeply scaled MOSFETs should be extended to the analog and RF specificities of SOI devices by promoting a collaboration between Philips and the EU expert groups in the field.

EUROSOI State of the Art Report

Chapter 8. Circuit Design
Section 8.4. Analog & RF
Subsection 8.4.4. Analogue circuits

Date of Issue: April – 2009	**Partner: UCL**

Abstract

SOI technology offers interesting advantages concerning analogue circuits. More particularly four domains of application for analogue circuits can be identified:
1) resistance to radiation, 2) high temperature 3) high-speed 4) low-voltage operation.

Introduction

The advantages of using SOI technology are evident and well demonstrated in the case of rad-hard and high-temperature circuits. The main players in these fields are the following academic institutions: the Université catholique de Louvain (U.C.L.) (FDSOI) [1-3], the Ecole polytechnique fédérale de Lausanne, EPFL, (FDSOI) [4,5], the university of Southampton (PDSOI) [6,7] and the Oak Ridge national laboratory (FDSOS) [8] and the industry partners Honeywell and Cissoid (see chapter 9.2). The circuits are analogue filters, bandgaps, voltage regulators, sigma-delta A/D converters, etc... The use of SOI technologies in order to lower the supply voltages and the power consumption has been reported by the Carleton university in Canada [9], by Dolphin Integration (PDSOI) [10], the LETI (PDSOI) [10,11] and NTT Telecommunications Energy Labs(FDSOI) [12,13] and in these cases, the use of SOI technologies allowed an improvement of the circuit performances. The circuits presented here are sigma-delta A/D converters, GSM baseband signal processing and self-powered short-range wireless system. Another interesting field in SOI analogue circuits is the integration of SOI-specific devices (naturally doped transistors [14], graded-channel MOSFETs [15]) or devices easier to obtain in SOI than in Bulk like DTMOS [11]. Fully mixed-mode systems have also been reported by OKI [16], where the use of SOI technology allowed power savings.
For ultra-low-power or high-temperature targets, a recent breakthrough could be the development of the UCL ULP concepts, in particular, the ULP composite CMOS diode featuring a reverse current lower by 2 to 4 orders of magnitude than standard MOS off current , with similar forward current. This ULP diode can then benefit most power management circuits, like rectifiers [17], voltage multipliers for RFID input power stage [18], etc. The concept has been successfully ported to 150nm FD SOI and 130nm PD SOI CMOS processes [19].

Apart from that, few recent reports of SOI analog circuits can be found [20]. University of Southampton is no more very active.

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European Contribution on the Field	Current Situation	
European Groups: Three European groups are mainly active in this field: UCL, EPFL and LETI. One EU company : CISSOID **Comments:** There are some circuits and the knowledge to build state-of-the-art analogue circuits. There is a critical need for more SOI processes not only targeting high-temperature applications. Industrialisation begins but apart from high temperature, clear targets and specs are missing.	**Strong Points**	**Weaknesses**
	Knowledge on analogue design present in the active groups.	Availability of CMOS SOI processes. Industrial targets.

Conclusions and recommendations

The successful realisations of mixed-mode systems in Japan illustrate the potential of SOI. In Europe, the availability of state-of-the-art CMOS SOI processes will be the key for further development. Although analogue circuit design is a tough and challenging task, it will never drive the markets. So, processes targeting mixed-mode applications, allowing the integration of digital circuitry and embedded memories will make the decision. Analogue design will follow. But again, the main question remains in the access to adequate SOI CMOS processes at commercial or Europractice/CMP-like

levels, beyond the present internal accesses through collaborative projects.

EUROSOI State of the Art Report

Chapter 8. Circuit Design
Section 8.4. Analog & RF
Section 8.4.5. RF Design

Date of Issue: Sept – 2009	**Partner: CISSOID, UCL**

Abstract

SOI is a very promising technology for RF applications. The intrinsic SOI isolation and the possibility to combine advanced SOI processes with high-resistivity substrates (ρ > 1000 Ω.cm) allow great improvements in terms of low-power consumption, passive devices and SoC integration. Recently the demonstrations have been pushed to 60 GHz and beyond.

Introduction

The great potential of SOI for RF applications has been demonstrated by a lot of different works and research team.
Characterization and modeling works have shown the intrinsic RF performance of Fully-depleted devices in terms of linearity and noise [1], high-Q and high-tuning range of varactors [2] thanks to reduced parasitic capacitances. This allowed designing ultra-low-voltage RF Front-ends [3].
Deep-submicron Partially Depleted SOI processes, with or without high-resistivity substrates, allow to go a step ahead in terms of scaling, offering higher Ft/Fmax and noise performances [4, 5, 6]. The lower parasitic capacitances have shown benefits to design high-frequency [7] and wideband [8] VCO's. The best high-frequency divider in terms of (constant power x delay product) [9] and the best CMOS Distributed Amplifier were demonstrated in a 0.13µm PD SOI process. The opportunity to use floating body devices in Low Noise Amplifiers (LNA) has been investigated in [11]. In the last years, ST Microelectronics has particularly demonstrated the adequacy of SOI for 60GHz bandwidth [13-14].
Finally, SOI on high-resistivity [5] or on Sapphire substrates [12] has shown performances comparable to GaAs to build RF switches.

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European Contribution on the Field	**Current Situation**	
European Groups:	**Strong Points**	**Weaknesses**
UCL-CISSOID: RF characterization & modeling, Passive devices optimization, HR substrates, RF building blocks designs IMEP-LETI-ST: RF characterization & modeling, RF Switches, RF building blocks IEMN: Noise Measurements & Modeling STM : RF design at 60GHz	Good background in the SOI RF characterization & modelling. STM technology.	Few RF SOI circuits already demonstrated at industrial production.

Conclusions and recommendations

A good technology background exists in Europe concerning the characterization and the modeling of SOI RF devices. However, few circuits have already been demonstrated except by IBM in USA.
Since beginning of EUROSOI, the situation has much improved with several EU demonstrations thanks to the MEDEA+ T206 project (access to STMicro 0.13µm PD SOI CMOS). However, beyond this project, future is unknown.
STM has pushed technology to 60GHz and real products are still lagging.

CHAPTER IX

End-users and Industrial Applications

EUROSOI State of the Art Report

Chapter 9. End-users and Industrial Applications
Section 9.1. Radiation-hard Products (Aeronautics & Space Applications)

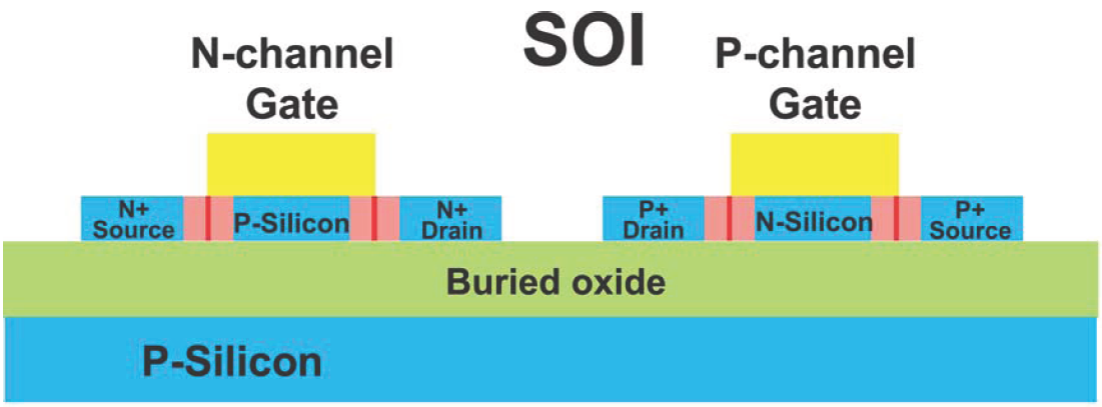
Date of Issue: Sept – 2009	**Partner: CISSOID, UCL**

Abstract

SOI Technology has been used for long in Aeronautic & Space Electronics due to its radiation hardness capability (see section 6.5. on radiation effects). Radiation-hard processes and products have been developed in USA and Europe for these applications.

Introduction

Silicon-on-insulator (SOI) technology has been actively pursued for use in radiation-hardened systems for more than twenty years. More recently, it is quickly becoming a mainstream technology for commercial applications. The cross sections of SOI (top) and bulk-silicon (bottom) n-and p-channel transistors are shown in the Figure.



Cross section of SOI n- and p- channel transistors. Figure taken from Ref [1]

The main feature that has made SOI technology attractive for radiation-hardened and commercial applications is that SOI transistors are built on top of an oxide instead of a silicon substrate [1]. Each SOI transistor inherently includes two transistors: a standard top-gate transistor consisting of the source, drain, and gate oxide, and a back-gate parasitic transistor consisting of the source and drain of the top-gate transistor and the buried oxide. Partially-depleted and fully-depleted transistors are two different kinds of SOI transistors. The top-gate transistor characteristics of a partially-depleted transistor are not directly affected by charge buildup in the buried oxide. For a fully-depleted transistor, the top gate is electrically coupled to the back-gate and radiation-induced charge buildup in the buried oxide will directly affect the top-gate characteristics.

The main interest for SOI for radiation-hard applications is to suppress latch-up and to be less sensitive to Single-Event-Upset (SEU). It is why SOI is mainly used for digital radiation-hard circuits: microprocessors, memories, digital and mixed ASIC, high-

speed or RF functions (PLL, prescalers, …).
The main provider of radiation-hard technologies and circuits is Honeywell [2], who is offering an ASIC service on Partially-Depleted SOI processes from 0.8 down to 0.25µm while developing a 0.15µm SOI process. Honeywell is currently selling 4Mb and 16MB SRAM memories supporting total doses of 1MRad and with SEU of less than 10^{-10} Errors/bit-day as well as standard products (Microprocessor, Analog-to-digital Converter, FPGA, …).
Another player on this market is Peregrine Semiconductor [3] who is offering radiation-hard (300KRad total dose and SEU<1e-10 Errors/bit-day) Radio-Frequency products mainly (PLL, Prescalers, Switches, Mixers, …) based on its 0.5µm Silicon-on-Saphire (SOS) process.
A last and new player in this field is the start-up company American Semiconductor [4] who is offering a foundry service based on 0.18µm SOI process targeting low-power, RF and radiation-hard applications.
In Europe, the "Commissariat à l'Energie Atomique" contributed in the development and characterization of radiation-hard SOI processes [5], the "Université catholique the Louvain-la-Neuve" developed Gate-all-around SOI process and circuits [6], IMEC made a lot of work on the radiation effects on SOI devices [7,8] and the University of Southampton designed SOI radiation-hard SOS circuits [9]. Atmel was offering a SOI-based radiation-hard process called DMILL but this process was stopped. Today, there are no more SOI radiation-hard industrial applications or products in Europe.
However, CEA continued to push SOI research and extended studies to 65nm PD SOI and even FinFETs [10].

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Industrial European position in this field is very weak. Not any European semiconductor company is offering SOI-based processes or products. IMEC: Eddy Simoen group, fabrication and characterization of radiation effects in FinFETs CEA: Veronique Ferlet-Cavrois group, abrication and characterization of radiation effects in FD and PD SOI transistors. **Comments:** This could greatly affect the European Aeronautic and Space industry in case of commercial conflict with USA	High scientific knowledge exists in Universities and Research centers.	No industrial applications in Europe.

Conclusions and recommendations

The EC, in coordination with ESA, could support existing European SOI foundries (X-Fab, STMicroelectronics, Atmel, …) to make their processes compatible with radiation-hard requirements.
A first point could be to characterize the existing SOI processes and circuits designed on these processes under radiations.

EUROSOI State of the Art Report

Chapter 9. End-users and Industrial Applications
Section 9.2. High-temperature Products (Oil & Gas, Aeronautics & Space, Automotive Applications)

Date of Issue: Sept – 2009	**Partner: CISSOID, UCL**

Abstract

SOI is the only technology enabling Integrated Circuits (IC) to work reliably above 150°C. High-temperature electronics are now used in Oil & Gas, Aeronautic & Space Applications and is now targeting the Automotive industry.

Introduction

SOI Technology offers the best performance for the design of high-temperature IC thanks to better temperature stability (Threshold voltage variation, latch-up suppression …) and to a reduction or a suppression of the junction's leakage currents.
To maximize the reliability we need to minimize the number of individually packaged components on a typical data acquisition board, and also minimize the interconnections within a board. Data have shown these areas to be the most unreliable. To meet the smaller overall physical size requirements and reduce the number of actual components, an Application Specific Integrated Circuit (ASIC) can be utilized.

The pioneer in offering SOI processes and products for high-temperature electronics is Honeywell [1] who is selling high-temperature analogue and digital products (Amplifiers, Microcontrollers, Gate Arrays…)
Its SOI technology, coupled with high temperature design techniques, are being used in the Aerospace market today. There are currently several major projects ongoing which are in various stages of development, testing, and demonstration. The reliability testing of components has been ongoing for several years. Data collection of reliability at the component level has indicated the ability to operate within specification for 5 years or more at 225 degrees Centigrade. These results have included thermal cycling, package mechanical testing as well as accelerated temperature and voltage testing. A total of 176,500 device hours of life testing have been completed at temperatures ranging from 250 degrees Centigrade to 300 degrees Centigrade. The life test data is used to project the failure rate and lifetime of the SOI components presented. In addition the use of individual HTMOST components in down hole logging tools have proven reliable up to 300 degrees Centigrade. These systems have demonstrated significant improvements in reliability and lifetime over traditional silicon systems at high temperatures. Lifetimes in excess of 10 years with bottom hole temperatures of 200 degrees Centigrade are now possible.

In Europe, scientific works on high-temperature Fully-Depleted SOI devices and circuits was carried out by the "Université catholique de Louvain-la-Neuve" [2]. High-temperature circuits (power management, sensor interface, EEPROM) were designed by Fraunhofer IMS Duisburg on a semi-industrial 1.6µm Partially-Depleted SOI process [3]. Two EC-funded (FP4 TERMIS and FP5 ATHIS) projects helped to push high-temperature SOI towards industrialization. The first one [4], targeting Space applications, led by the "Ecole Polytechnique de Lausanne" [5], allowed the German

foundry X-Fab [6] to offer now a 1µm Partially Depleted SOI process for high-temperature applications up to 250°C. The second one [7], with CISSOID, the Centro Nacional de Microelectronica [8], Fiat, the "Institut fur Mikroelectronik und Mechatronik" [3], UCL, X-Fab and University of Newcastle is targeting high-temperature SoC for automotive applications.
The European start-up CISSOID, spin-off from UCL, is now offering high-temperature ASIC services [10] and is developing a portfolio of high-temperature standard products IC (Voltage Regulators, XO, ADC, gate drivers…) based on X-Fab process.
C-MAC MicroTechnology and CISSOID have agreed a partnership that will lead to the development of high reliability components, modules and sub systems for high temperature applications operating up to 225°C. The two companies will expand their existing customer relationships in the oil, gas, aerospace, defence, automotive and space industries. This relationship tries to put C-MAC and CISSOID at the forefront of high temperature microelectronic business.
In Germany, Atmel provides 200°C models for its 0.8 µm BCD-on-SOI process [12].
SOI technology is also used by Honeywell, Kulite [13] and First Sensor Technology GmbH [14] to produce high-temperature pressure sensors.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
Four companies are offering SOI processes or products for high-temperature applications: X-Fab, Atmel, CISSOID, First Sensor Tech. **Comments:** SOI for high-temperature is a hot strategic topic but there is not large European administrations investing in like DoD or DoE in USA.	Technologies & expertise are available. One leading start-up in Europe	The industrialization is still emerging and markets remain niche.

Conclusions and recommendations

High-temperature Electronics based on SOI could become strategic for the European industry (Oil & Gas, Aeronautic & Space but also Automotive). The ENIAC platform indeed stresses high temperature operation as one of the key issues for its “More than Moore” and “Heterogeneous integration” roadmaps.
SOI high-temperature electronics bases exist in Europe but the industrialization is still weak and should be improved through R&D projects or supporting companies active in this field.
Again, the problem is to overcome the chicken and egg challenge linked to the development of first low-volume technologies versus the expectations of low-cost components. Ramp-up needs to be sustained.
A second problem lies here in the fact that mature or potential high temperature capable CMOS processes are micron-sized, not nanoscaled and that R&D is such “old-fashioned” but “niche-advanced” technologies is not widely supported in EU project calls although strategic for wide but basic industrial sectors (i.e. not telecom).

EUROSOI State of the Art Report

Chapter 9. End-users and Industrial Applications
Section 9.3. High-speed Products (Microprocessors & Data Communications)

Date of Issue: Sept – 2009	**Partner: CISSOID, UCL**

Abstract

IBM mainframe microprocessors were the first niche for high-performance SOI processes. SOI is now used for general-purpose (PowerPC, 64-bits) and graphics (playstations) microprocessors, pushing SOI towards consumer applications. SOI has captured a significant portion of the pure logic market.

Introduction

The really advent of SOI technology arrived, in 1998, when IBM decided to use it for high-performance mainframe microprocessors [1,2&3]. This demonstrated the maturity of SOI for VLSI. Now, IBM, Freescale and AMD are using SOI for their microprocessor products.
In June 2003, IBM released a low-power PowerPC manufactured in 0.13µm PD SOI [5] and introduced together with Apple the G5 based on the same process [6]. In May 2004, IBM announced the roll-out of a new 64-bit Power5 microprocessor, with 276 millions of transistors in 0.13µm PD SOI on 300mm wafers [5].
Freescale (Motorola) served as SOI foundry for Apple G4 microprocessors and is now selling a family of low-power PowerPC manufactured in 0.13µm PD SOI [7]. In June 2003, Freescale announced the start of the transfer of 90 nm SOI technology to the Crolles Alliance, with ST and Philips [8].
Since the beginning of 2004, AMD produced most of its microprocessors in SOI: all the mobiles, 64-bit and the “Opteron’s” were manufactured in 0.13µm SOI [9]. In April 2004, AMD started the manufacturing of 90nm 64-bit SOI microprocessors in its Dresden Fab in Germany [10]. This strategy is being continued with 45nm PD SOI eventhough AMD fabs have been separated in a new venture called Global Foundries.
Sony PlayStation, Nintendo Wii and Microsoft Xbox graphic microprocessors all rely on IBM SOI Technology [11] and uP cell architecture. Already in 2002, Sony and Toshiba announced a partnership with IBM [12]. This has been confirmed for sub-32 nm CMOS.
Cell, the most advanced multimedia microprocessor ever realized [IEEE Spectrum, January 2006], is fabricated on IBM SOI platform.
Mitsubishi Electric announced in April 2004 a 10Gb Ethernet physical layer single chip transceiver achieving low-power consumption thanks to 100nm gate-length SOI.
European start-up companies are emerging and offering digital design kits (Soisic now part of ARM [13] in France) and very dense embedded memories (Innovative Silicon [14] in Switzerland). These IP’s can address general purpose or dedicated (display) microprocessors applications.

As an example, we can say that ARM announced at the 2009 IEEE SOI Conference, the results from a silicon-on-insulator (SOI) 45nm test chip that demonstrate potential power savings of up to 40 percent over traditional bulk process for manufacturing chips. The test chip was based on an ARM 1176™ processor and enables a direct comparison between SOI and bulk microprocessor implementations. The results confirm SOI technology is a viable alternative to traditional bulk process technology

when designing low-power processors for high-performance consumer devices and mobile applications. ARM and Soitec collaborated to produce a test chip to demonstrate the power savings in a real silicon implementation with a well-known, industry-standard core. The goal was to produce a comparison of 45nm SOI high-performance technology with bulk CMOS 45nm low-power (LP) technology of the same product.

Very recently, at the 2009-IEDM conference in Baltimore [16], IBM researchers indicated that a fully depleted CMOS on extremely thin SOI wafers may be the way to go at the 22nm node. The approach allows reduced SCEs, and supports gate length scaling to 25 nm and beyond. The fully depleted technology involves Soitec, which supplies wafers with a thin silicon layer on top of the buried oxide. The approach depends in part on the recent ability of SOI wafer provider Soitec to deliver SOI wafers with a silicon thickness in the 6 nm range. Most of the 300mm SOI wafers delivered to IBM have an acceptable silicon thickness variation of ±5 Å, although the shipments from Soitec have been in limited quantities thus far.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
No companies developing SOI high-speed products. However, AMD microprocessors are manufactured in Dresden (Germany). IBM had a SOI microprocessor design group in Bobelingen (Germany) now closed. Soisic (France, now ARM) in SOI DK Design and Innovative Silicon (Switzerland) in SOI embedded memories.	SOI microprocessors manufacturing facilities and design centres located in Europe.	No European microprocessor vendor.

Conclusions and recommendations

SOI microprocessors applications are dominated by US Companies, having some activities in Europe. This is probably not the field where Europe has to compete. However, Europe has not to leave advanced SOI technologies to US, Japanese or Asiatic companies because SOI will bring huge benefits for low-power and RF applications where European companies are key players. In this case, the study of embedded microprocessors, as well as memories, is certainly strategic.

EUROSOI State of the Art Report

Chapter 9. End-users and Industrial Applications
Section 9.4. High-voltage Products (Audio, Power Management and Automotive Applications)

Date of Issue: Sept – 2009	**Partner: CISSOID + CNM (CSIC), UCL**

Abstract

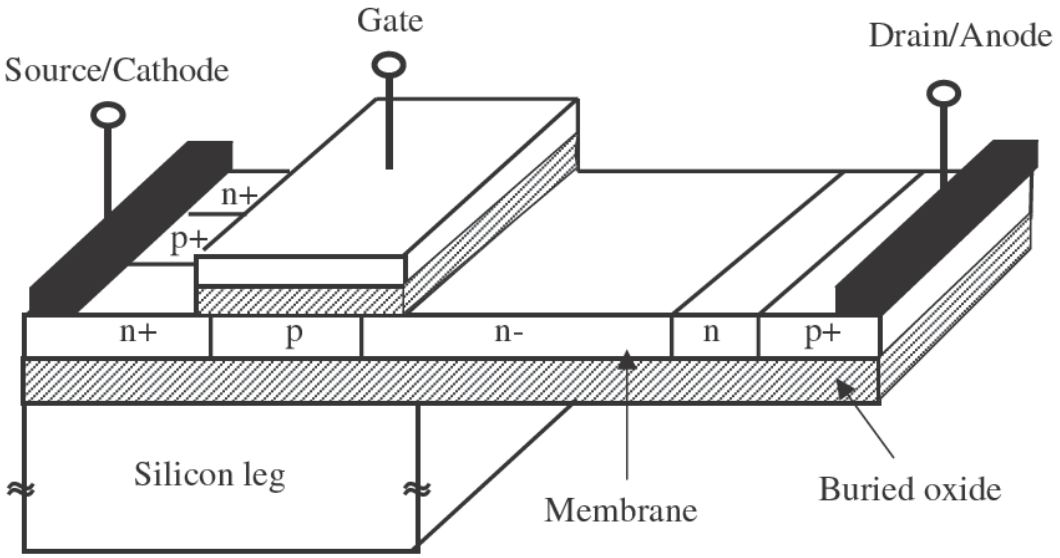
SOI is used in high-voltage applications for its isolation properties. The pioneer in this field was Philips, now NXP, who developed BCD processes on SOI for Audio, Power Management and automotive applications. Now, a lot of companies use it.

Introduction

Thick-film SOI is used by a lot of companies to develop high-voltage process. The pioneer in this field was Philips who developed SOI Bipolar-CMOS-DMOS (BCD) processes based on the RESURF principle [1]. These processes offer high breakdown (up to 800V), lower EMC, latch-up suppression, lower parasitic capacitances and higher packaging densities. They are used to manufacture Audio Power Amplifiers, Automotive IC's, Battery Management, Power Conversion, Lighting Electronics, Display and Line Drivers [2]. Now, a lot of companies have thick-film SOI processes. Philips has a large family of processes with different breakdown voltage (from 70V to 800V) and critical dimensions (from 2µm to 0.4µm) following the application.

However, very recently Philips, has announced the new EZ-HV process based on a layer of silicon only half a micron thick (about 1000 atoms), which is much cheaper to produce than the conventional 10 to 20 micron thick layer used in standard high-voltage silicon-on-insulator processes. The process, which allows ICs to include high-voltage circuits that can handle rectified AC line supply voltages, as well as low-voltage CMOS logic to provide on-chip intelligence, is based on a thin silicon approach to HV-SOI construction that is so novel the company has been awarded a number of patents on it [13]. Until now, such ICs either required the use of a thick layer of silicon to achieve the high breakdown voltage or the use of high-cost substrate materials such as sapphire, both of which made them expensive to produce.
EZ-HV's unique combination of thin silicon and oxide isolation allow them to integrate virtually any type of circuit element onto an IC alongside 650-volt power transistors. The availability of a commercial process for implementing highly integrated cost-effective solutions opens a whole new world of possibilities for design engineers.

Atmel (Germany) proposes a 0.8µm BCD-on-SOI process (>80V), called SMARTIS [3]. X-Fab has a 1µm high-temperature/high-voltage(>100V) thin-film PD and trench-isolation (>500V) SOI processes [4]. Analog Devices (Belfast) is using thick-film SOI for the co-integration of high-voltage and MEMS devices for automotive and optical applications. ST Microelectronics is probably also using thick-film SOI, at least looking on in cooperation with LETI, for high-voltage applications [6]. Infineon is hardly working towards the development of FiNFET transistors.
A start-up company in UK, CamSemi, is developing Lateral IGBT based on SOI [11].



LIGBT Camsemi device. Figure taken from Ref [12]

This technology concept enables high voltage devices to be embedded in a thin silicon/oxide membrane resulting in very significant improvements in breakdown ability and switching speed. The feasibility of realising superjunction structures with breakdown capability in excess of 700V using this technology have been demonstrated.

Thick-film high-voltage high-power SOI technologies seem also very popular in Japan. Toshiba, Fuji Electric, NEC and Mitsubishi Electric developed SOI high-voltage and/or lateral IGBT processes based on SOI technology, i.e. for plasma display panels or automotive applications [7, 8, 9, 10].

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
NXP Semicond. (NL), Atmel (DE), X-Fab (DE), Infineon (DE), CamSemi (UK) **Comments:** Europe has a technology leadership thanks to NXP. However, SOI technologies are not relevant in comparison with the world production.	Good expertise and industrialization in Europe.	Automotive products, power converters and RF applications

Conclusions and recommendations

SOI, mainly for its isolation properties, is appreciated for high-voltage applications. Europe has a strong position in this field.
However, a strong effort has to be addressed to replace as much as possible bulk technology by SOI counterpart in the automotive field, including the power management for the next 42V supply generation. A new market is increasing rapidly in the field of renewable energies.

With high-power diodes and transistors moving to SiC technology for higher temperature, speed or power capabilities, now apperas the need for adequate high voltage drivers. The synergy between SiC and SOI clearly appears with these respects and should be supported. The High temperature electronics network (HITEN) could have helped this, but has no longer been supported by the EC for years.

EUROSOI State of the Art Report

Chapter 9. End-users and Industrial Applications
Section 9.5. Ultra-low-power devices and applications (Watches, …)

Date of Issue: Sept – 2009	**Partner: CISSOID, UCL**

Abstract

SOI has demonstrated a great potential for ultra-low-power ultra-low-voltage applications and was successfully used in watches applications.

Introduction

The first to show the great potential of SOI in Ultra-low-power Ultra-low-voltage products was Seiko Epson who designed a watch IC consuming 30nA at 0.42V in Partially-Depleted (PD) SOI [1].
OKI is fabricating an IC in 0.35µm Fully-Depleted (FD) SOI consuming 150nA at 0.7V for a CASIO solar watch [1,2] and developed a SOI single-chip combing a receiver, a decoder and a real-time-clock (RTC) for Japan's Long-wave Standard Time Code. OKI also successfully used FD-SOI for low-power ARM-based microcontrollers. But OKI was sold this year to Rohm and discontinued research on 0.15µm FD SOI, although 0.2µm remains in production.
In Europe, research groups have shown how to optimize SOI circuits for ultra-low-power applications: UCL has worked on low-power low-voltage analog circuits in FD-SOI [4] and on ultra-low-power design techniques with new SOI-specific circuits [5], the LETI demonstrated a low-voltage 13.56MHz RFID in 0.25µm PD SOI [6]. The Swiss foundry EM-Marin (Swatch Group) announced a 0.5µm Fully-Depleted SOI process capable of 0.5V operation [7]. CISSOID has been offering ultra-low-power ultra-low-voltage circuit design services on SOI [8] but stopped as well as Marin.
In Japan, NTT made a lot of researches on the use of FD-SOI for ultra-low-power applications [9] but has stopped too.

Very recently, LETI has proved how SOI-based planar CMOS meets requirements for low-power, 22nm node devices, offering a practical route to further feature shrink and enabling a significant jump for “green” products [10]. Planar SOI was showed superior to other technologies based on bulk CMOS technology and FinFET architecture. It also shows outstanding performances for ultra-low-power applications requiring 22nm technology. However, the main reason for delaying the research and application of SOI substrates is the high SOI substrate cost which has been demonstrated as a major deterrent for low-cost low power applications [11]. The substrate cost can be partly offset by simplified device isolation and improved circuit density. The cost can be justified if SOI enables more functionality. SOI would be more attractive if high system level integration is needed for low power products.

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European Contribution on the Field	Current Situation	
European Groups: UCL and LETI on ultra-low-power circuit design and and on technology developments. **Comments:** The scientific and design know-how exists in Europe but there is a lack of SOI processes available and a lack of industrialization.	**Strong Points** Good scientific and design know-how.	**Weaknesses** Lack of industrialization. Niche market. Higher SOI substrate cost.

Conclusions and recommendations

The great interest of SOI for ultra-low-power and ultra-low-voltage applications has been demonstrated in Europe and in Japan. Europe has a good scientific and design know-how but there is a lack of low-power SOI processes available and a lack of industrialization in Europe. A low-power SOI process available through a Multi-Project-Wafer (MPW) available in Europe should be of great interest. A high system level integration is needed for low power products to be economically interesting.

EUROSOI State of the Art Report

Chapter 9. End-users and Industrial Applications
Section 9.6. RF & Microwave Products (Wireless Applications)

Date of Issue: Sept – 2009	**Partner: CISSOID, UCL**

Abstract

Although that the great potential of SOI for RF applications has been demonstrated at the research level, only few products are already on the market.

Introduction

As it is shown in the chapter 8.4.5, SOI has a great potential for RF and microwave applications. Allowing to combine low-power digital, high Ft/Fmax & low-noise devices, high-Q inductors and varactors together with a very good isolation between analogue, RF and digital parts, SOI is certainly the best technology for low-power wireless System-on-Chips. However, up to know, only few applications are already on the market. Peregrine Semiconductors [1] is selling a series of high-performances discrete RF components such as Phase-locked Loops (PLL), Mixers or RF Switches made in Silicon-on-Saphire (SOS).
Honeywell is selling RF transceivers, RF switches and Attenuators based on Partially-Depleted SOI on high-resistivity substrates [2].
Skyworks Solutions, announced on 2010 that it has introduced a family of antenna switch modules (ASMs) for 2/3/4G handset and data card platforms using both gallium arsenide (GaAs) as well as silicon on insulator (SOI) technologies [6].

Recently, the great interest of SOI for low-power and RF applications has been demonstrated in Europe in the frame of Research projects, in particular the T206 medea+ project on “SOI for low-power digital and RF” led by ST Microelectronics. In this project, process steps, devices, models and circuits were developed in 0.13µm Partially Depleted SOI [4]. The great interest of high-resistivity SOI for RF applications was demonstrated by UCL (Cross-talk), LETI, CISSOID (Inductors, Varactors and 5GHz VCO [5]) and ST (RF Switches). STM has demonstrated 60GHz designs and is already developing a range of SOI components for communications.
The MEDEA+ consortium targeted very low power, efficient RF applications for mobile communications terminals. The project has already resulted in a commercial product: STMicroelectronics had an antenna switch by the end of 2006 based on SOI technology. Customers are now interested in SOI for the RF part to improve efficiency and its use is being evaluated for new multiband systems.
A MPW access to process would be made available to European research and industry.

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European Contribution on the Field	Current Situation	
European Groups:	**Strong Points**	**Weaknesses**
UCL, LETI, CISSOID and ST Microelectronics	Good scientific and design know-how.	Lack of industrialization.

Conclusions and recommendations

An advanced SOI process for low-power and RF applications could offer breakthroughs for the European wireless industry.
Open existing processes for MPW access and industrialization could happen new ideas and applications to emerge.
Capitalizing on the results and experience already obtained in Medea+ T206 project to address and develop more advanced processes, following both the “more Moore” (next technology nodes) and “more than Moore” (adding process options on existing processes) strategies.