INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

Grant Agreement nº 216373

D4.14. Third motivated list of selected topics for future research on SOI technology. Outcome of the panel discussion held during the 7th EUROSOI Workshop Granada, 17-19 January, 2011

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Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

Table of contents

1.- Introduction.

One of the goals of EUROSOI+ project is the promotion of industrial participation in EUROSOI activities and the coordination of the initiatives so that European Industry successfully faces Roadmap-identified challenges

In the first stage of EUROSOI network (2003-2006), we have carefully studied the situation of SOI technology in Europe, we have identified the current status, where we want to go, and what is the best approach ("road") to follow. Now it is time for taking decisions. SOI community has to face and successfully achieve, in the following years, the challenges identified in the Roadmap.

EUROSOI+ will not duplicate works and actions undertaken in other projects, but will, through a forum linking technologists, scientists, designers and industry:

1. Promote industrial participation in the Network activities, informing industry about relevant progress in SOI technology worldwide and providing a feedback loop for industrial mid and long-term interests to academic and research centres.
2. Organize annual workshops, scientific meetings and discussion panels with industry experts (Tyndall-2008, Chalmers-2009, Grenoble-2010 and Granada-2011)
3. Upgrade the EUROSOI State-of-the-Art Report.
4. Upgrade the European SOI Roadmap: Identify scientific priority areas, and formulate research and development strategies.
5. Promote the interaction between existing SOI projects at national and European level (FP6-IST, FP7-ICT, EUREKA/MEDEA/CATRENE, ENIAC), and facilitate the coordination of their work. Organization of Workshops and scientific meetings.
6. Foster the initiatives to face the challenges already identified in EUROSOI Roadmap, by selecting and creating the research consortium from the best European actors already identified at EUROSOI "Who is Who" guide. Co-ordinate activities at national and European level.
7. Co-ordinate activities with other FP7 instruments: NoEs, IPs, Marie-Curie initiatives.
8. Address and foster initiatives beyond CMOS: take advantage of the SOI knowledge to develop platforms for further technological development in nanotechnology, such as to prepare the transition from microelectronics to nanoelectronics.
9. Propose a list of highly desirable topics of advanced research on SOI by analyzing the future trends in industry and research.

To fulfill this goal, EUROSOI organizes panel discussions with different specialists on SOI technology to identify hot topics in SOI research. These discussion panels are held simultaneously with each EUROSOI workshop. As outcome of these panel discussions, a report with a list of selected topics in SOI research is elaborated.

The seventh Workshop of the Thematic Network on SOI Technology, Devices and Circuits was held on January 17-19, 2011 in Granada, Spain. During this Workshop, the panel discussion, chaired by Prof. Francis Balestra, was held on Tuesday, January 18th. The following experts were invited to participate in the discussions:

1. Dr. Malgorzata Jurczak, IMEC, Belgium
2. Dr. Bruce Doris, IBM, USA
3. Dr. Olivier Faynot, LETI, Grenoble, France
4. Prof. Massimo Fischetti, UT Dallas, USA
5. Prof. Carl Das, IMEC, Belgium
6. Dr. Nobuyuki Sugii, Leap, Japan

Each expert presented his point of view and position on the SOI technology, future applications, and the European situation. The leading thread of this year's debate was "**The contribution of SOI to the brilliant future of Nanoelectronics"**

Each panellist explained its own point of view regarding the selected topic. After the initial positioning, there was a live debate among the panellists and the rest of the audience. This debate was useful to identify the hot topics and concerns of European researchers and how we could contribute to improve the situation.

The details of the Panel are described in the next sections.

2.- Panel discussion participants.

1) Dr. Malgorzata Jurczak − IMEC (Belgium)
Malgorzata Jurczak received the M.Sc. and Ph.D. degrees in electrical engineering from the Warsaw University of Technology (WUT), Warsaw, Poland. In 1991, she was with WUT where, parallel to her work on modeling ofMOS SOI devices for her Ph.D. degree, she worked as Teaching Assistant and Research Scientist in the Institute of Microelectronics and Optoelectronics. In 1994, she was involved in SOI device fabrication project with NMRC, Cork, Ireland, and in 1997, she was with Kyung Hee University, Seoul, Korea, working in reliability of polysilicon TFT. In 1998, she was with CNET, France Telecom, Grenoble, France. She was involved in the development of 0.18 and 0.12 μm CMOS process and alternative approaches for sub-100 nm CMOS (strain Si, vertical transistor, SON). Since 2000, she has been with the Interuniversity Microelectronics Center (IMEC), Leuven, Belgium, where in the years 2000–2003, she was the IMEC coordinator of the IMEC–Philips JDP program on device process integration for 90-nm and 65-nm CMOS, in years 2003–2007, she was the leader of the CMOS Device Implementation Projects Group and the Project Manager of IMEC Industrial Affiliated Program EMERALD on FINFET devices, and in 2008, she became the Program Manager of NVM and Emerging Memories (including RRAM and FBC) programs. She is the holder of 18 European and U.S. patents, and authored and co-authored more than 300 publications. Dr. Jurczak has been a member of scientific committees of IEDM, ESSDERC, VLSI TSA and IEEE SOI conferences and ITRS Roadmap. In 2000, her paper published in IEEE TED, presenting the concept of SON transistor, received the Paul Rappaport Award.

2) Dr. Bruce Doris − IBM (USA)

IBM Research. Biography not available.

3) Dr. Olivier Faynot − LETI, Grenoble (France)
Olivier Faynot received the M.S. and Ph.D. degrees from the Institut National Polytechnique de Grenoble, Grenoble, France, in 1991 and 1995, respectively. His doctoral research was related to the characterization and modeling of deep submicron fully depleted silicon-on-insulator devices fabricated on ultra-thin silicon-implanted oxide wafers. He joined the Commissariat à l'Énergie Atomique/Laboratoire d'Electronique et de Technologie de l'Information (CEA–LETI), Grenoble, in 1995, working on simulation and modeling of deep submicron fully and partially depleted silicon-on-insulator (SOI) devices. His main activity was the development of a dedicated partially depleted SOI SPICE model, which is called LETISOI. From 2000 to 2002, he was involved in the development of a sub-0.1-μm partially depleted SOI technology. From 2003 to 2007, he was leading the development of advanced single- and multiple-gate fully depleted SOI technologies with high-κ and metal gate. From 2008 to 2010, he managed the innovative devices laboratory at CEA–LETI. Since 2011, he is responsible of the Microelectronic Component Section at CEA–LETI. He is the author or coauthor of more than 140 scientific publications on SOI in journals and international conferences. Dr. Faynot has been successively in the

committees of main international conferences such as the International Electron Device Meeting, the symposium on Very Large Scale Integration Technology, the IEEE International SOI conference, and the Solid State Device and Materials Conference since 2001.

4) Pr. Massimo Fischetti − UT Dallas (USA)

Dr. Massimo V. Fischetti received his Ph.D. in physics from the University of California, Santa Barbara, in 1978. From 1979 till 1981 he was a scientist in the physics group of ST-Microelectronics, Italy, conducting experimental work on the hot-electron degradation of silicon dioxide. From 1983 till 2004 he was a research staff member at the IBM T.J. Watson Research Center working on the theory of electron transport in semiconductors and insulators, on Monte Carlo simulation of semiconductor devices and on quantum transport in small structures. Since joining UMass in 2005, Dr. Fischetti has extended his work on the theory of electronic transport in semiconductors, exploring the limits of device scaling and the promises of future technologies. He was elected a fellow of the American Physical Society for his work on the physics of electron transport in solids, and he serves or has served on the editorial boards of several international physics journals

5) Prof. Carl Das − IMEC (Belgium)

Director ASIC Services at IMEC
Director EUROPRACTICE IC Service at IMEC

6) Dr. Nobuyuki Sugii, LEAP (Japan)

Nobuyuki Sugii (M'08) received the B.S., M.S., and Ph.D. degrees in applied chemistry from the University of Tokyo, Tokyo, Japan, in 1986, 1988, and 1995, respectively. In 1988, he joined the Central Research Laboratory, Hitachi Ltd., Tokyo, where he was engaged in the research and development of oxide superconducting materials and devices until 1996 and has been working on the research and development of SiGe materials and complementary metal– oxide–semiconductor devices, including silicon-on-insulator and strained-silicon metal–oxide–semiconductor field-effect transistors, since 1996. From 1991 to 1994, he was a Research Scientist with the Superconductivity Research Laboratory, International Superconductivity Technology Center. Since 2004, he has been also a Visiting Professor with the Tokyo Institute of Technology, Tokyo. Dr. Sugii is a member of the Japan Society of Applied Physics and the IEEE Electron Devices Society. He was a member of the program subcommittees of the Solid State Devices and Materials Conference from 2002 to 2004.

3.- Panel Discussion ideas – The contribution of SOI to the brilliant future of Nanoelectronics?

The panel discussion was organized with the following scheme. The Chair had previously asked the panellists to list key issues in SOI technology. Each panellist introduced his point of view about the main contributions of SOI technology to the Nanoelectronic field in few slides during 5-10 minutes. They explained and documented their feelings from their own experience, by focussing on the following points:

Why SOI for the next generations?

What are the advantages and disadvantages of using SOI?

What applications are prone to use SOI technology?

The comments of each panellist can be summarized as:

Malgorzata Jurczak's answers:

1) Memory technology can benefit from SOI substrates by taking advantage of the area reduction for SRAM and the news 1 transistor DRAM designs.

2) SRAM can be improved due to the reduced variability introduced by the undoped thin film SOI devices.

3) FBRAM based on SOI technology can meet the eDRAM retention specifications.

4) However, memory industry is extremely conservative, still using the DRAM as introduced by Dennard in 1968.

Bruce Doris's answers:

1) Contact and spacer scaling, not only the channel length, is mandatory to fit the pitch.

2) Bulk will not scale for low power applications.

3) SOI substrate cost is becoming a smaller part of total cost. Process cost increases as technology advances, but the costs are similar for both bulk and SOI.

4) ETSOI substrate cost can be potentially justifies by lowering process cost. Therefore, cost is not an issue.

5) Predictions: SOI wafers will have extremely thin and flat Si and BOX layers. SOI wafers may have alternate surface orientations, alternate materials and will be stacked to form 3D chips.

Olivier Faynot's answers:

1) Brilliant future for SOI research due to the wide range of materials + structures to be studied.

2) New fields, such as photonics on SOI, are being opened.

3) Strong competence from FinFET on bulk.

Massimo Fischetti´s answers:

1) Pros: Excellent electrostatic control, Evolutionary lithography and processing, no need for revisiting previous circuits and architecture.

2) Cons: Performance degradation at ultra-short channel lengths. Manufacturing cost, dictated by market, not a technical issue.

Carl Das's answers:

1) There are several questions to be answered before SOI becomes the mainstream technology: Will SOI be competitive to CMOS/3D for the large volume products or will SOI be a technology for a niche market?

2) SoC needs a large portfolio of SC libraries and IP. They are available for bulk technology but not for SOI. This is an important drawback.

Nobuyuki Sugii's answers:

1) In terms of getting more power efficiency, that is, reducing both active and leakage power, inserting the insulating layer is mandatory. New semiconductor materials for channel are awaited.

2) Supersteep subthreshold (mostly SOI-type structure) are needed. Independent DG action focused on adaptive control to maximize power efficiency.

3) ULV (ULP) applications used at the maximum efficiency conditions are sought for the next decade (ULP applications: sensor nodes, implanted medical healthcare, etc.).

4) Cost will be the ultimate factor to take a decision.

4. Conclusions and list of topics

After the initial explanations, there was a long and live debate among the panellists and the audience. Among the different applications where SOI technology could successes, ultra-low power and mobile applications were selected. Mobile Internet and medical applications will create a huge semiconductor business. Memory applications based on SOI technology are not clear at this point, and more research and breakthroughs are necessary. To successfully face these demands, technology will have to provide very low power consumption, high-density memory and computational power. SOI technology provides viable solutions to these challenges thanks to the new substrate materials and device and circuit designs.

However, the main drawbacks are:

1. The lack of a large portfolio of Standard Cell (SC) Libraries and available IP for SOI.
2. The cost still remains as a major drawback compare to traditional bulk MOSFETs.

Both problems become a barrier to broad adoption of SOI.

In summary, SOI technology has demonstrated a significantly superior device and circuit performance and an extraordinary power reduction compared to standard bulk silicon technology. However, the range of commercial applications that currently use SOI substrates is still reduced. New business opportunities are opening and SOI technology should find its way on them. The final success of these new markets depends on two important tasks to be addressed:

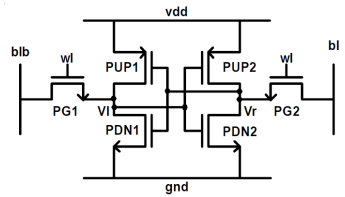
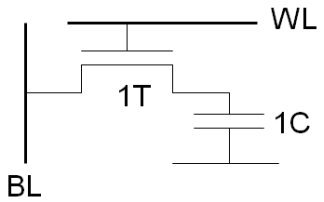
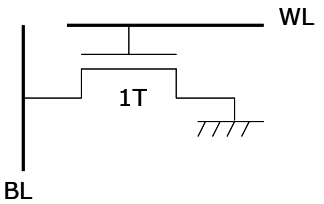
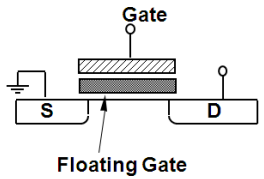
i) Cost reduction compared to currently available technology.

ii) Development of a large portfolio of Standard Cell libraries and IP for SoC.

Appendix. Panelists' presentations.

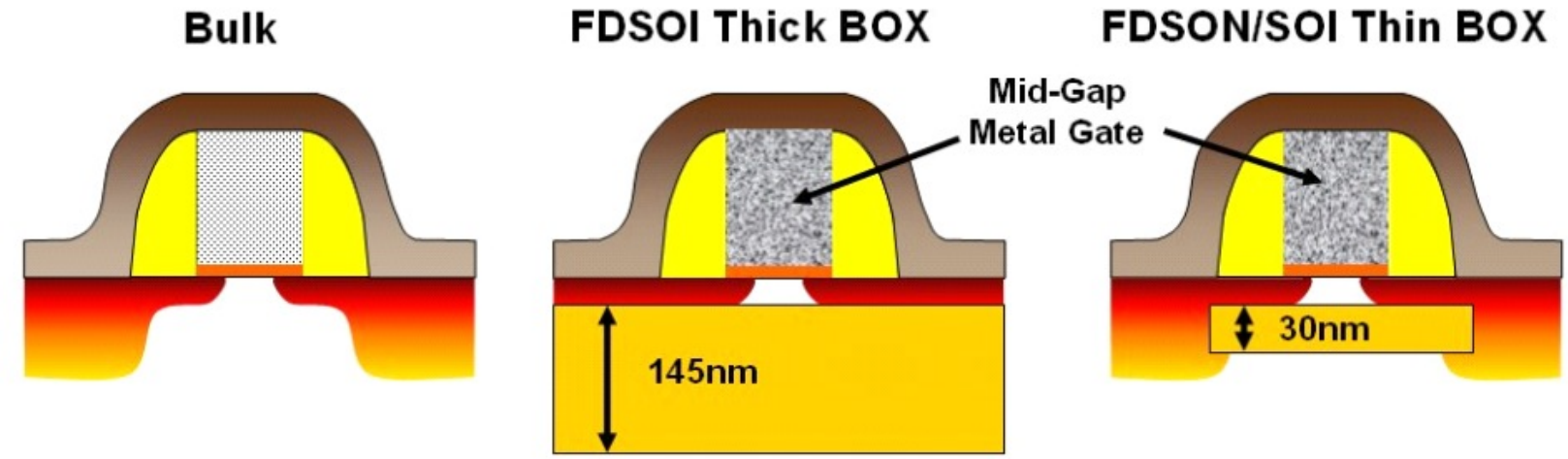
Dr. Malgorzata Jurczak,
IMEC, Belgium

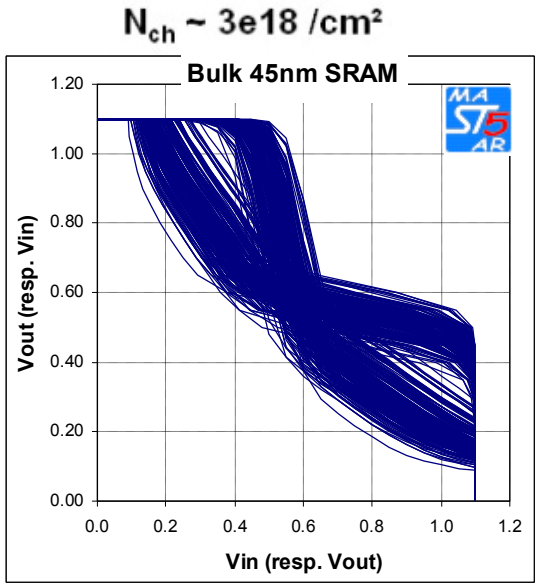
WHICH MEMORY CAN BENEFIT FROM SOI SUBSTRATE?

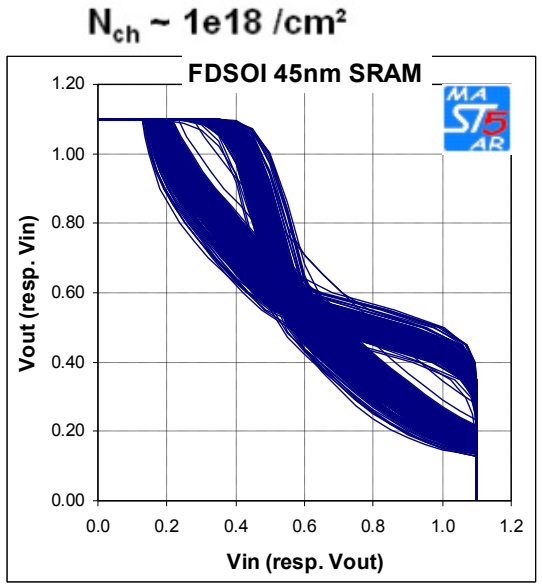
	BULK substrate	SOI substrate
SRAM	 6T	6T but Area benefit: Lg can be reduced as RDF smaller
DRAM	 1T1C	1T1C (embedded applications)  1T with FBC
FLASH	 1T	N/A

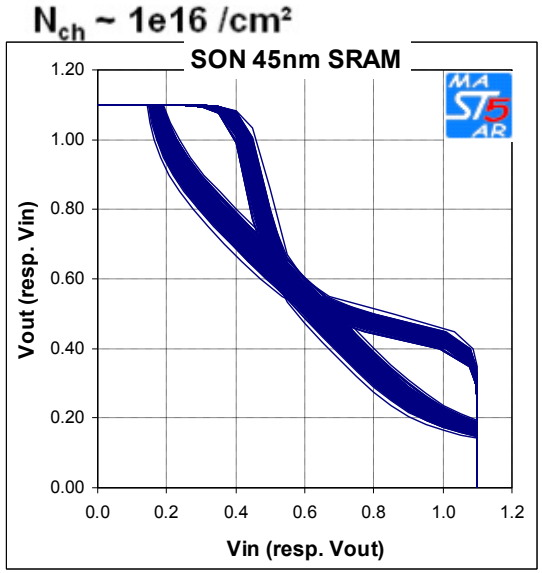
SRAM: IMPROVED VARIABILITY IN UNDOPED THIN FILM SOI DEVICE

$$\sigma V_T \propto N_a^{1/4}$$





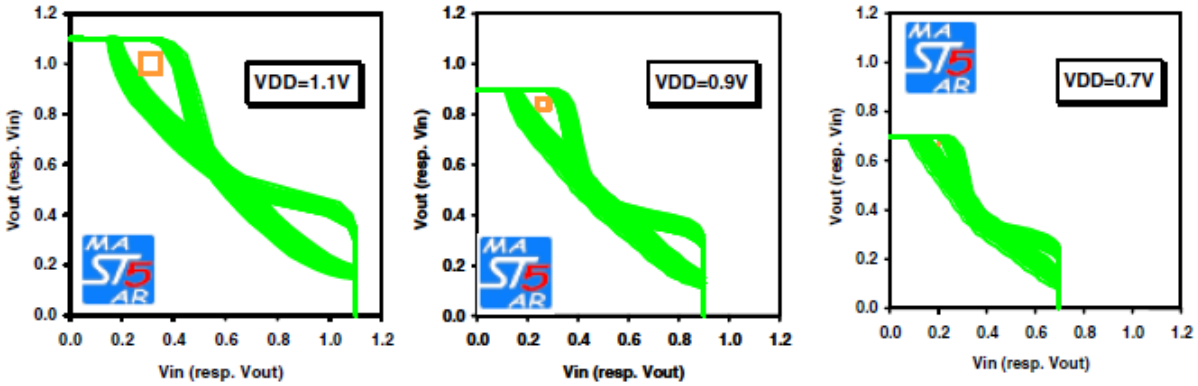




F.Boeuf, VLSI 2007

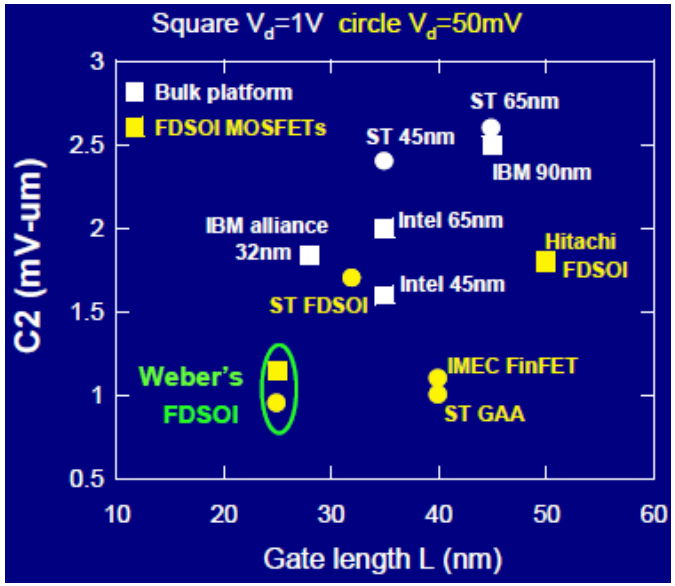
LP SRAM PERFORMANCE

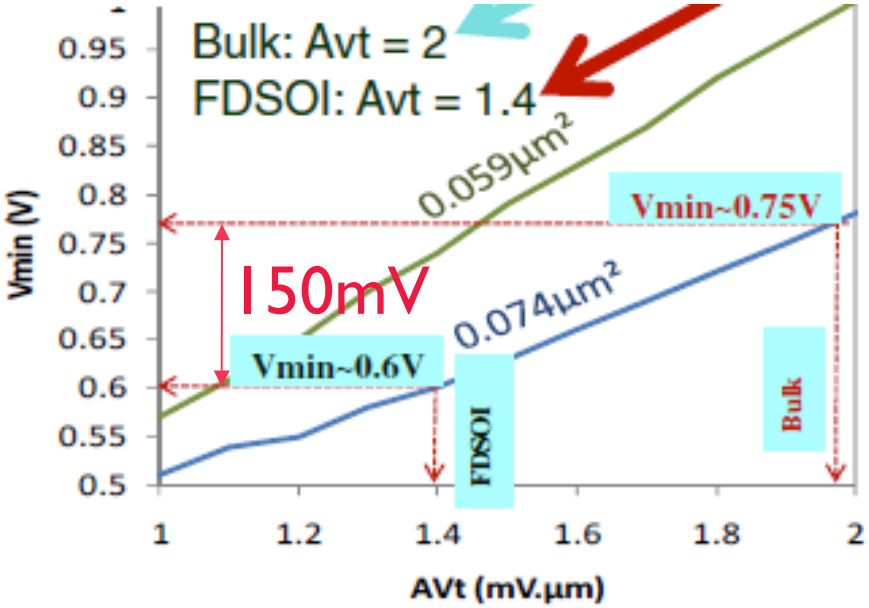
T.Skotnicki, IEDM SC, 2010



SNM degradation with VDD reduction

Weber, LETI, IEDM, 2008





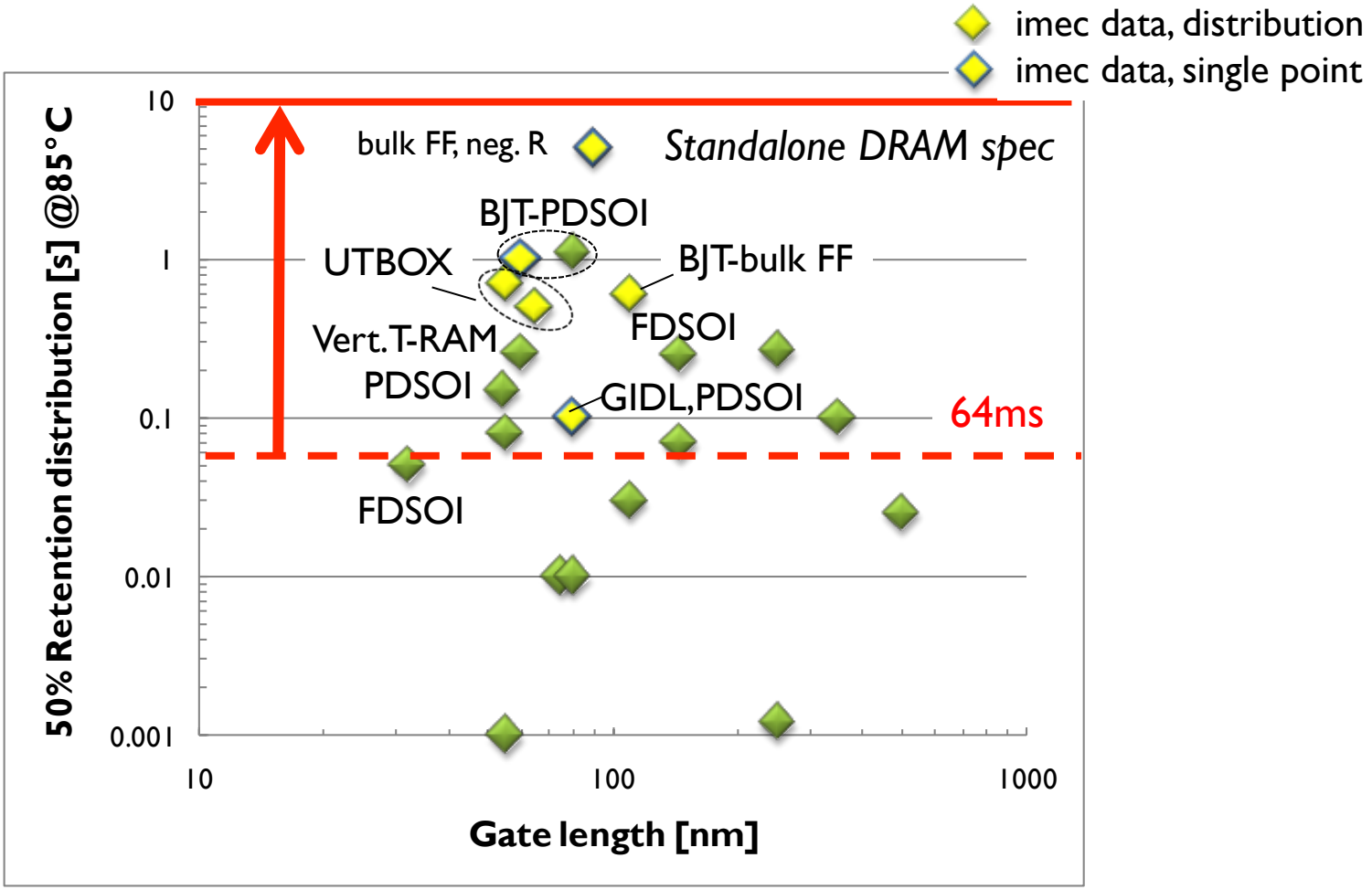
With SOI UTBOX:

- for the same Lg: gain in Vmin
- for the same Vmin – Lg reduction

DRAM TARGET FOR 2X NODE

Specs at 85°C	Standalone applications	Embedded applications
Median retention (50% distribution)	>10s	>10ms
Retention tail distribution	>64ms	>40us
Sense margin	>3μA/cell	>3μA/cell
Endurance	~10^{16} cycles	~10^{16} cycles
WRITE/READ bias	< 2V	< 2V
WRITE speed	< 15ns	<10ns
Device area (footprint)	$4F^2$ <30nm feature size	<$25F^2$ <22nm node

FBRAM BENCHMARKING: RETENTION

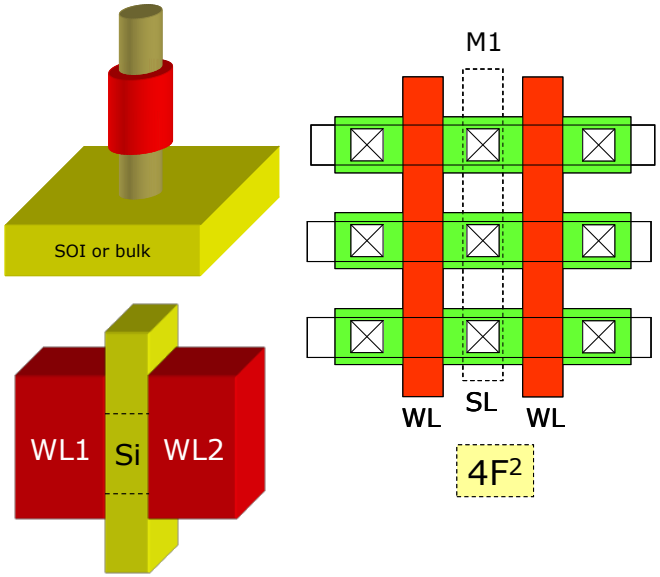


All FBRAMs have much smaller retention (~factor 100) than 1T-1C DRAM
- Much severe constraints on junction leakage to meet DRAM specs
- Or tighter retention specification (wrt to distribution)

FBRAM can meet the eDRAM retention spec (>100µs)

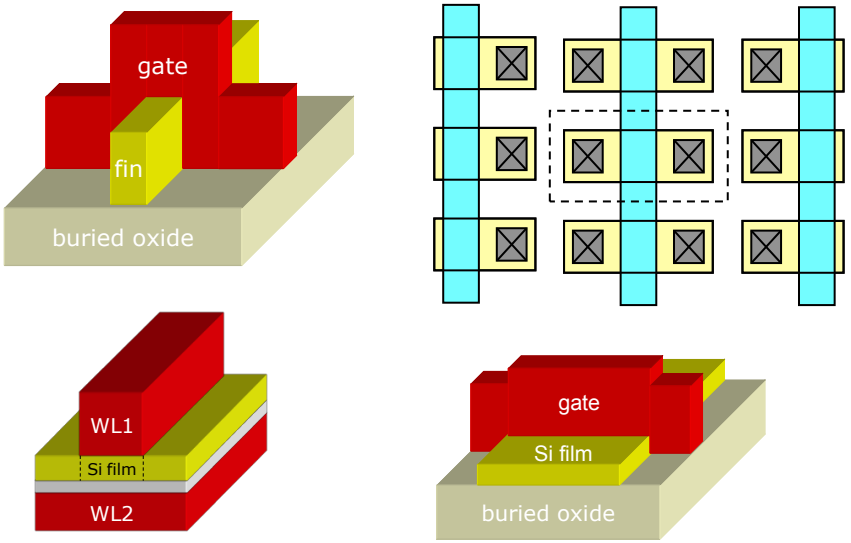
FBC OPPORTUNITIES

Standalone Memory
SOI less



4F^2 footprint
Relaxed Lg for high sense margin

Embedded Memory



Planar transistor compatible with Logic device architecture
Relaxed Lg for high sense margin

Need voltage scaling to address reliability issues
Reduced leakage for better retention
Needs to show enough performance/cost benefit (array+ perifery)

MEMORY INDUSTRY IS VERY CONSERVATIVE

we still use the DRAM as introduced by Dennard in ‘68

We still use the Floating Gate as in Kahng and Sze’s EPROM in ’67

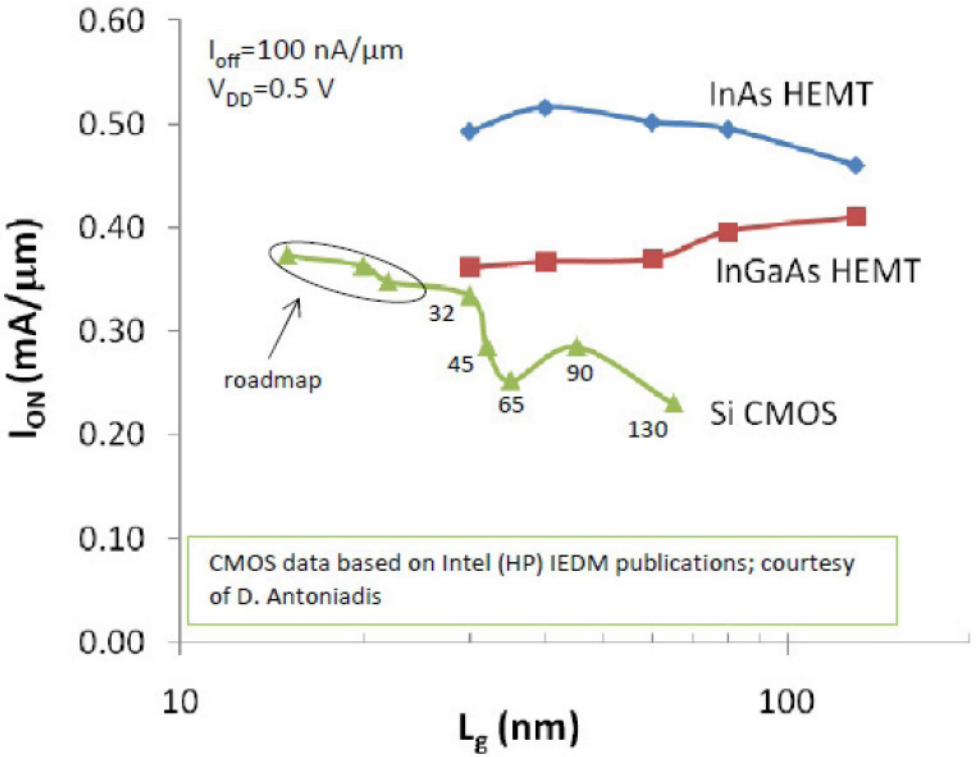
Prof. Massimo Fischetti,
University of Texas at Dallas, USA

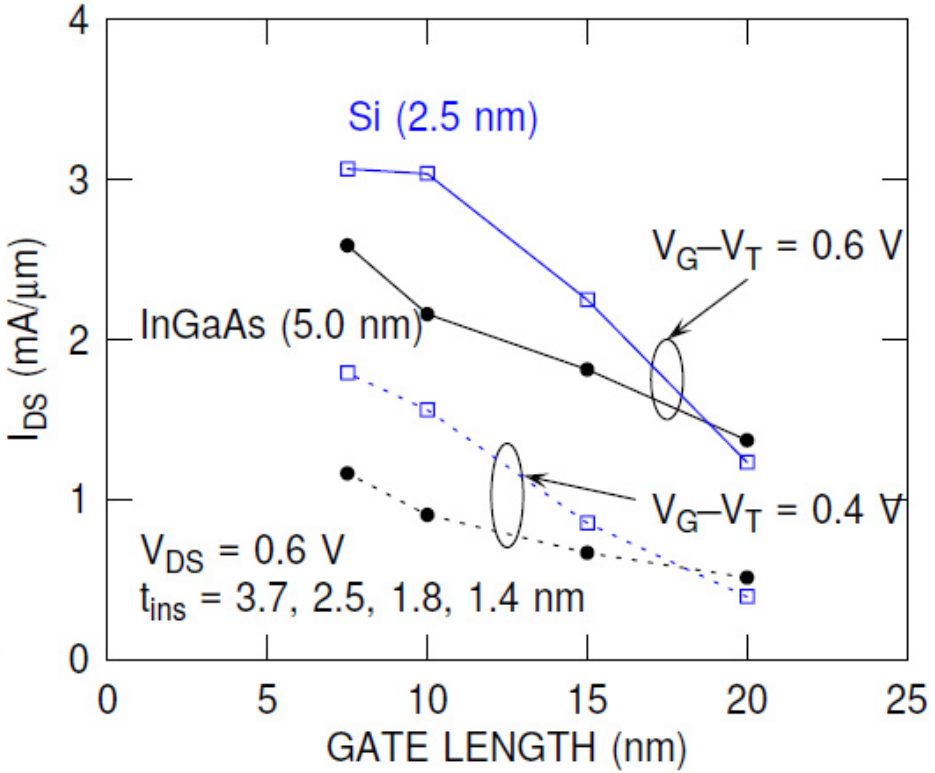
The role of SOI in the future of Nanoelectronics

- **"SOIs" (as "thin/narrow bodies") unavoidable**: **Electrostatics** (the device has to turn off!)
- Why scaling?
  - **Density** (*i.e.*, size → electrostatics & device-design: Clear path to the future)
  - Performance (*i.e.*, channel/insulator materials, size(?), strain engineering(?), etc. :Path less clear)
- SOI towards NWs?
  - Design "evolution" blurred into "revolution" (Who would have guessed 10 years ago?):
    - New materials: Strain/stressors, SiGe, metal gates, high-**κ**
    - Device design: SOI → FDSOI → UTBSOI → ETBSOI→ **FinFETs (?) → NWs (?)**
- Pros:
  - Excellent electrostatic control: Frank-Laux-MVF 1993 work at 30nm on DGFETs limited by lack of imagination.. OK to 5 nm? (quantum issues?)
  - "Evolutionary" litho & processing (*i.e.*, no doubtful self-assembly, growth seeds, and such)
  - No need for revisiting circuit & architecture
- Cons:
  - Performance? (Mobility degradation? V_T control? Device fluctuations?). Not likely to be a show-stopper
  - Manufacturing costs? Likely, but dictated by market (non-technical) issues

Performance outlook

- Predicted as lower-then-expected but still worth the effort
- Bridging the gap between predictions and theoretical expectations



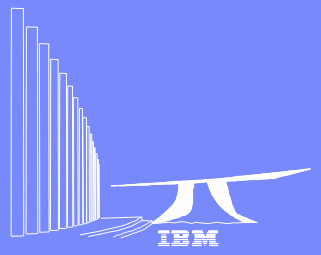


UMass-UCSD-UCSB, IEDM (2007)

Dr. Bruce Doris,
IBM Research, USA

Future of SOI

Bruce B. Doris
IBM Research Division



Possible Technology Roadmap

Node	Device Pitch (nm)	Nominal L (nm)	Year
45	170-180	40-45	2008
32	120-130	30-35	2010
22	80-100	25-30	2012
15	65-75	20-23	2014-15
11	45-55	12-18	2017-18
8	35-45	9-16	
5	25-35	7-12	

Gate must get smaller to fit the pitch.
Contact and spacer scaling are also needed

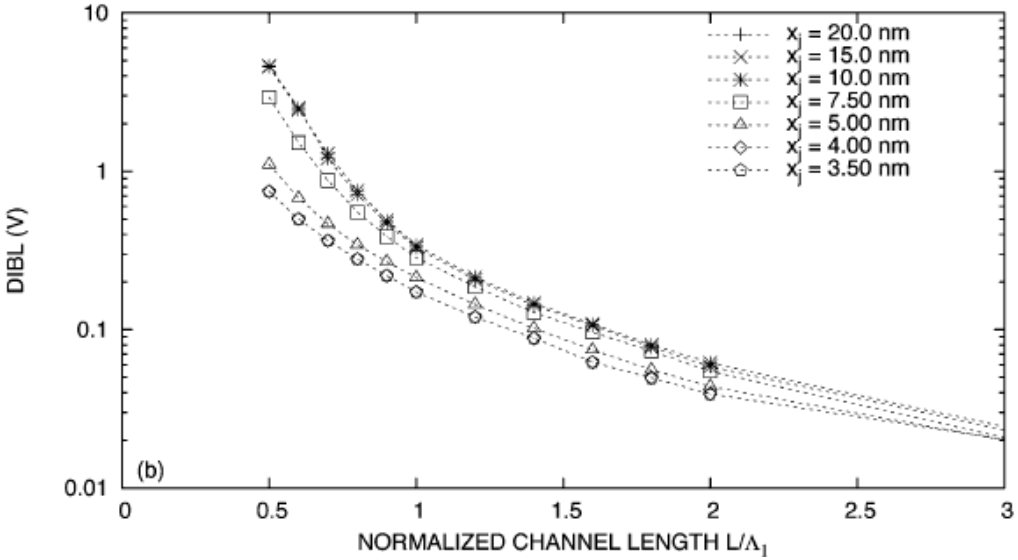
Challenges with Bulk

- Bulk process increasingly complex:
  - STI, Well and S/D patterning and doping
- Well I/I into the adjacent well
  - N-p breakdown
- STI, Well depth scaling
  - Latch-up
- High channel doping – especially for low power
  - GIDL, junction leakage, variability

Bulk will not scale for Low Power applications

Approaches to Scaling L: Junction Depth

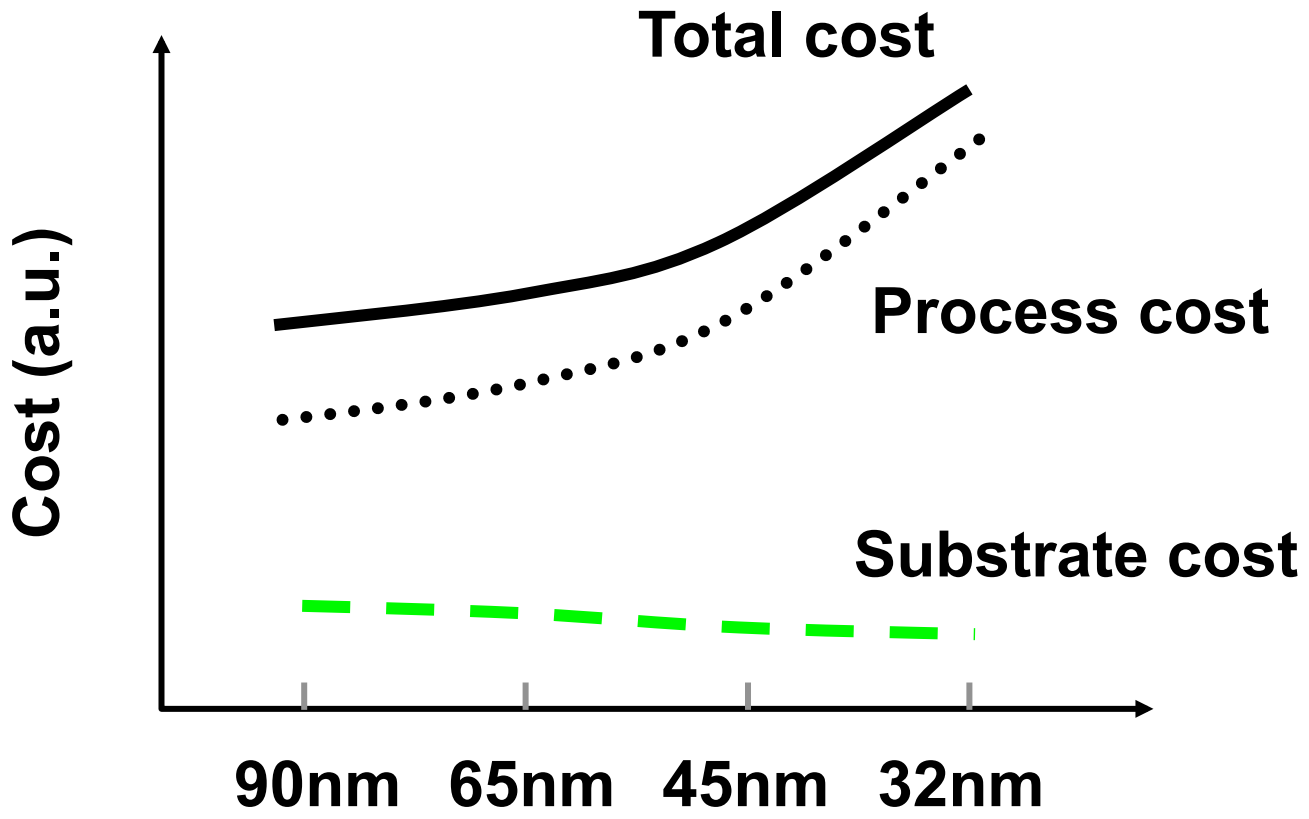
- Junction depth:
  - If S/D junction depths < depletion-layer width, then DIBL is proportional to junction depth
  - Ref: [Sleva/Taur, 05]
    - Λ is scale length ($w+\varepsilon_{Si}/\varepsilon_{ox}t_{ox}$)



- Issues:
  - Increase in S/D resistance (?)

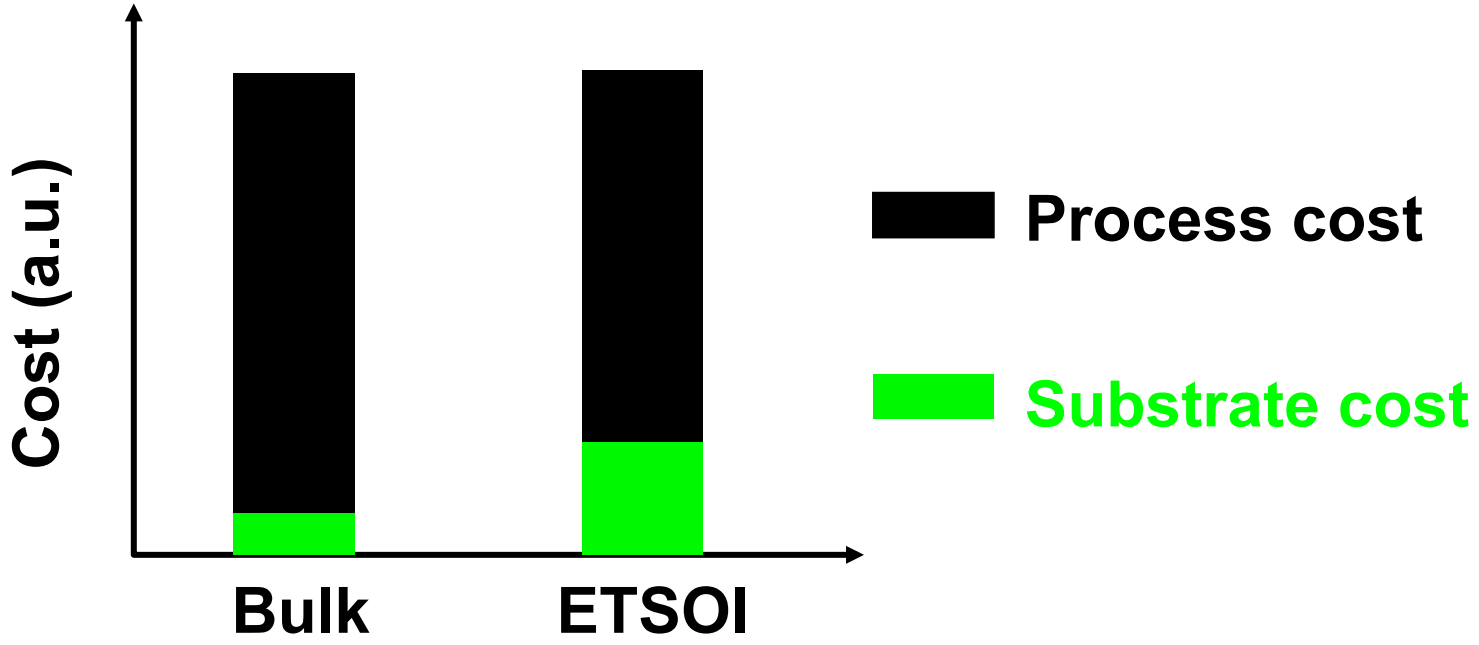
(SiO_2 t = 1.5 nm, depletion w = 10.0 nm, Λ = 13.6 nm)

Process Cost vs. Substrate Cost



- Process cost increases as technology advances.
- Substrate cost is becoming a smaller part of total cost

Low-cost ETSOI Technology

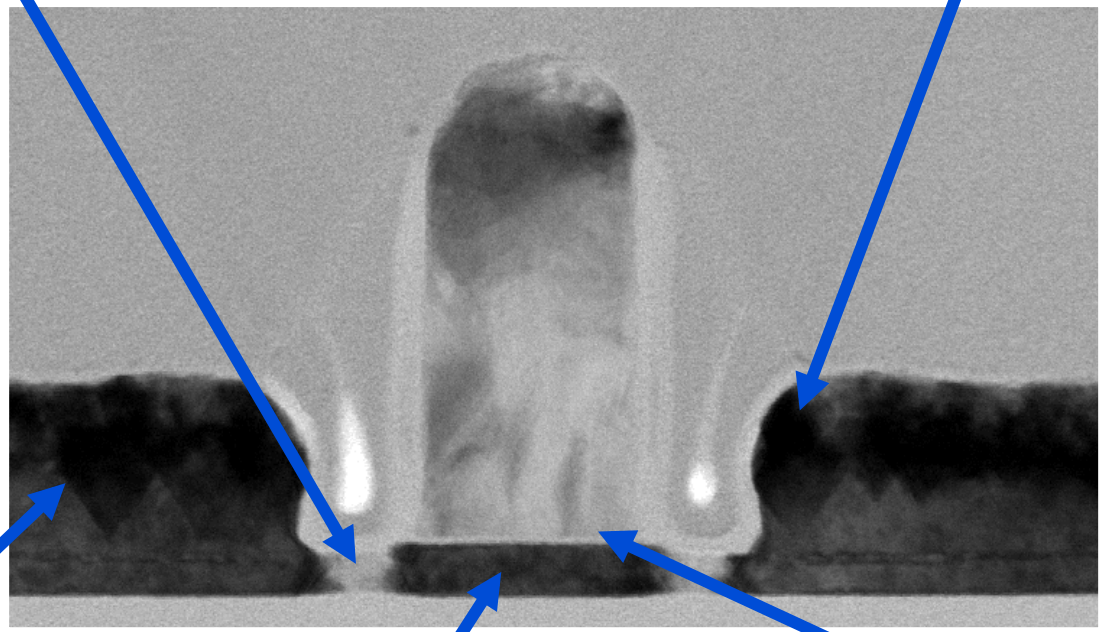


- ETSOI substrate cost can be potentially justified by lowering process cost.
- Cost is not an issue – Bulk must die, ET must provide value add – 60% power savings

ETSOI Issues and Opportunities

Si Consumption, amorphization
- **Process Optimization, USJ**

Parasitic Capacitance
- **Facetted RSD**

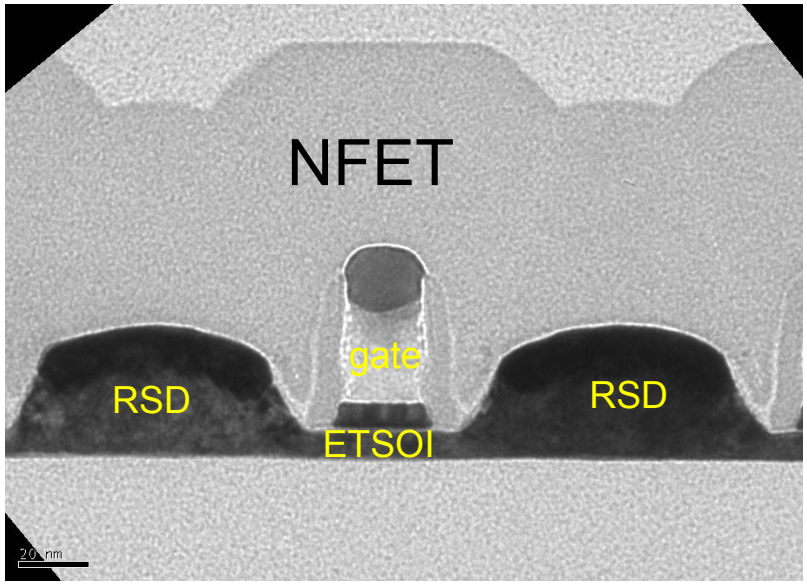


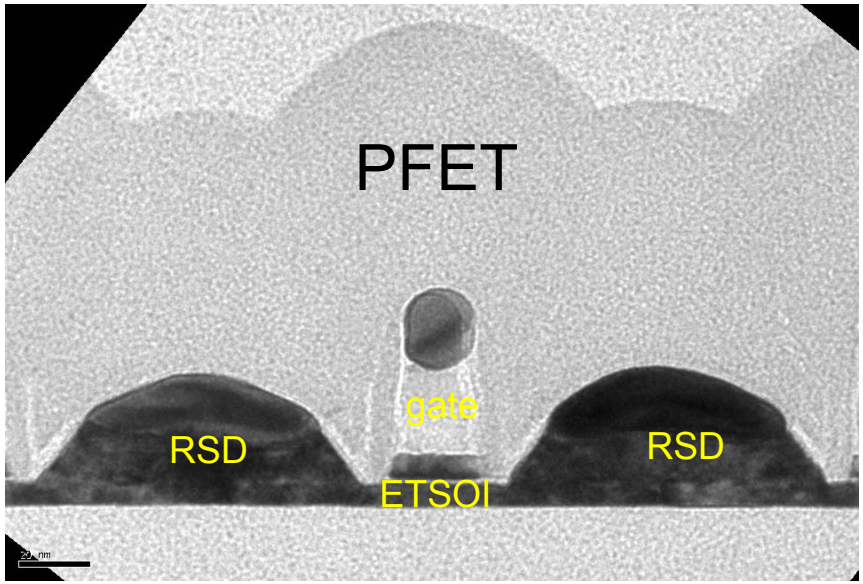
Ext. Resistance
- **RSD**

Vt Variation
- **T_{si} Uniformity**

Vt Adjustment
- **WF Tuning**

ETSOI

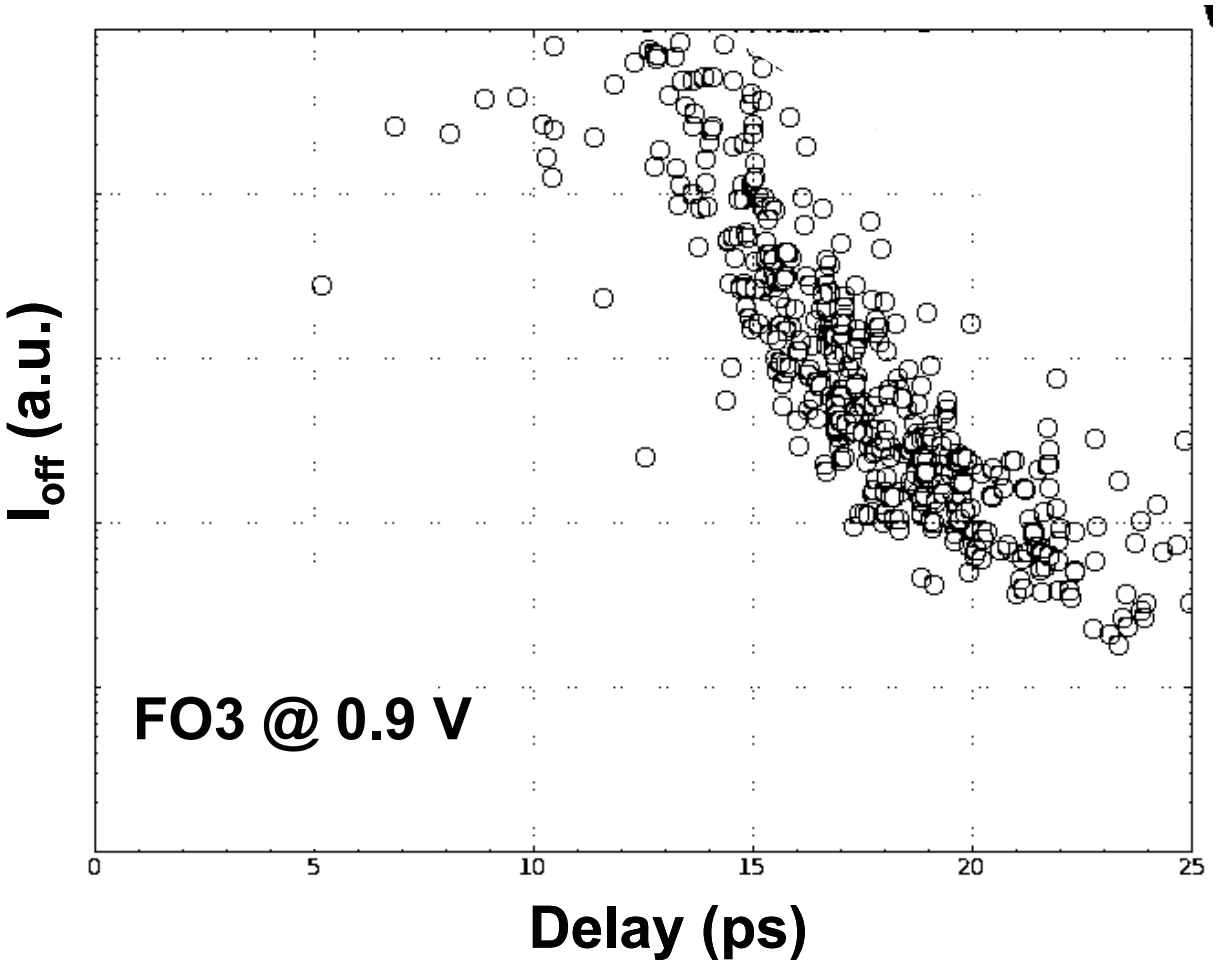




- **Device dimensions**

L_{gate} = 25nm, T_{Si} = 6nm, Total Spacer: 15nm

Ring Oscillator Data at 100nm CPP - 2010



Already 30% faster than 28nm LP

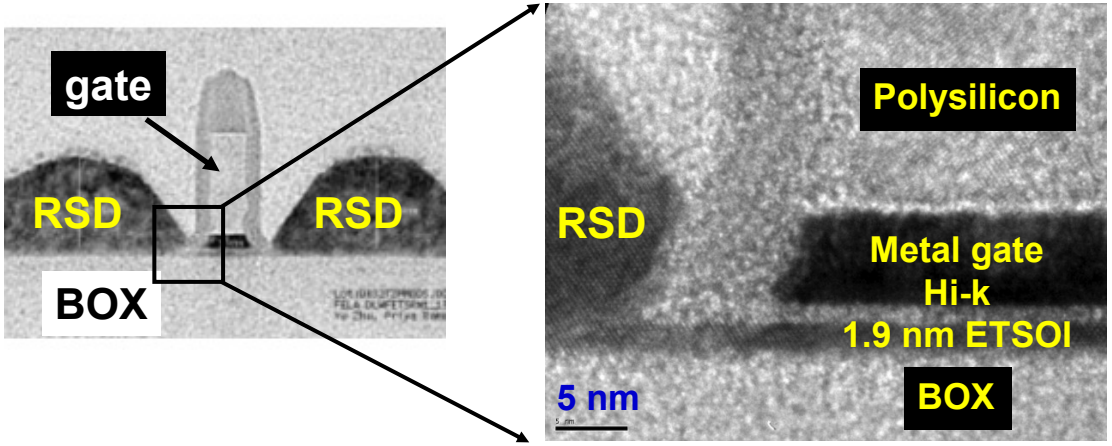
ETSOI scaling

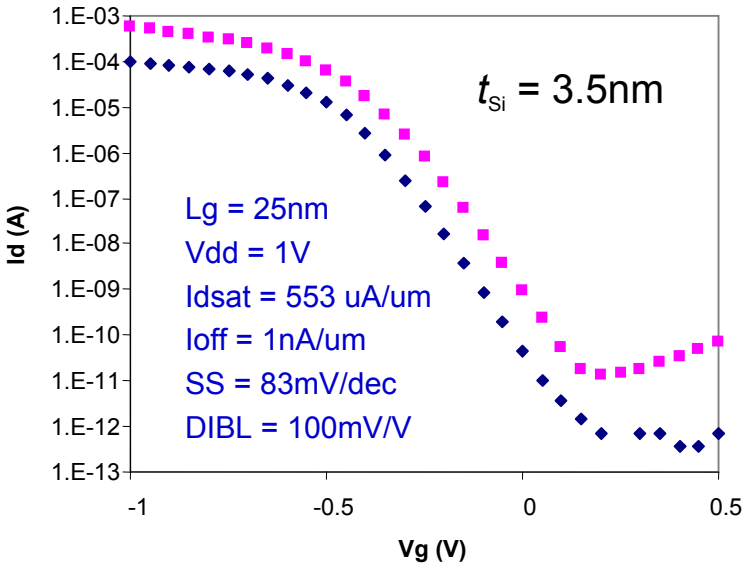
- SOI thickness (t_{Si}) scaling is required along with gate length (Lg) as technology is scaled.

- L_g/t_{Si} ratio is critical for scaling ETSOI while maintaining good electrostatics.

	22nm	16nm	11nm
Lg (nm)	**25**	**20**	**16**
t_{Si} (nm) (L_g/t_{Si} = 4)	**6.3**	**5**	**4**

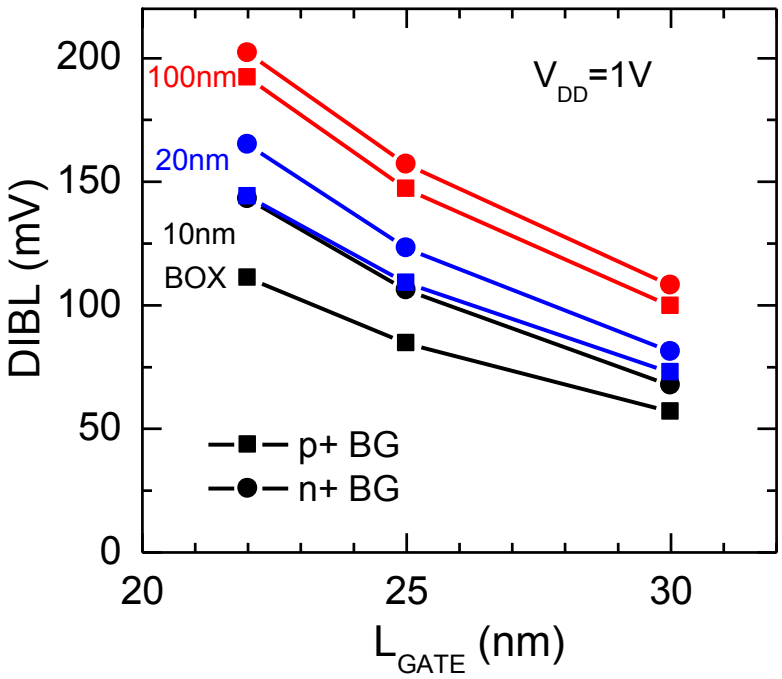
Thin SOI Scaling

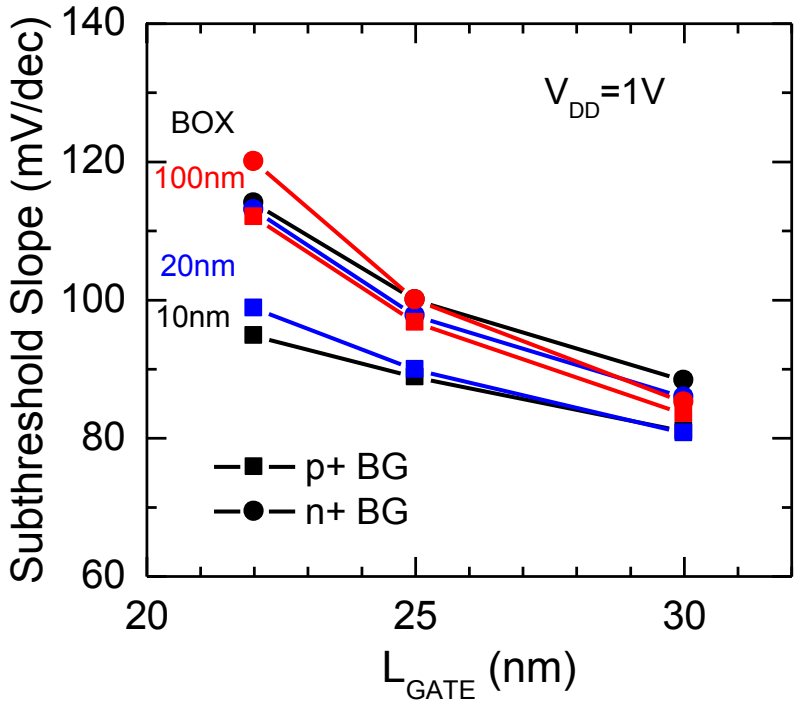




[Cheng 09-1]

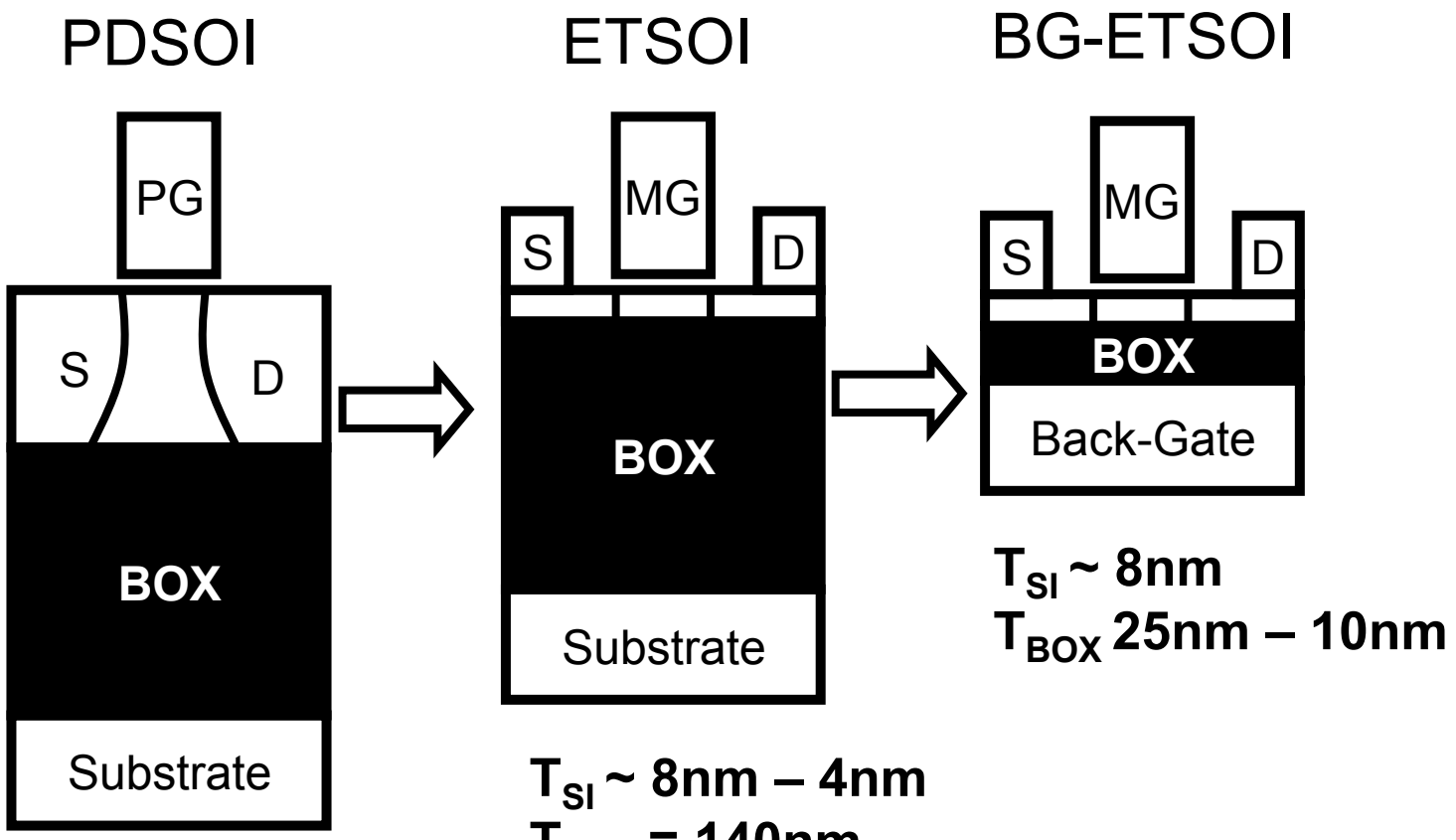
Thin BOX to Improve the SCE





- Thin BOX is a path to continue scaling

Other Scaling Path for PDSOI



T_{SI} ~ 60nm
T_{BOX} = 140nm

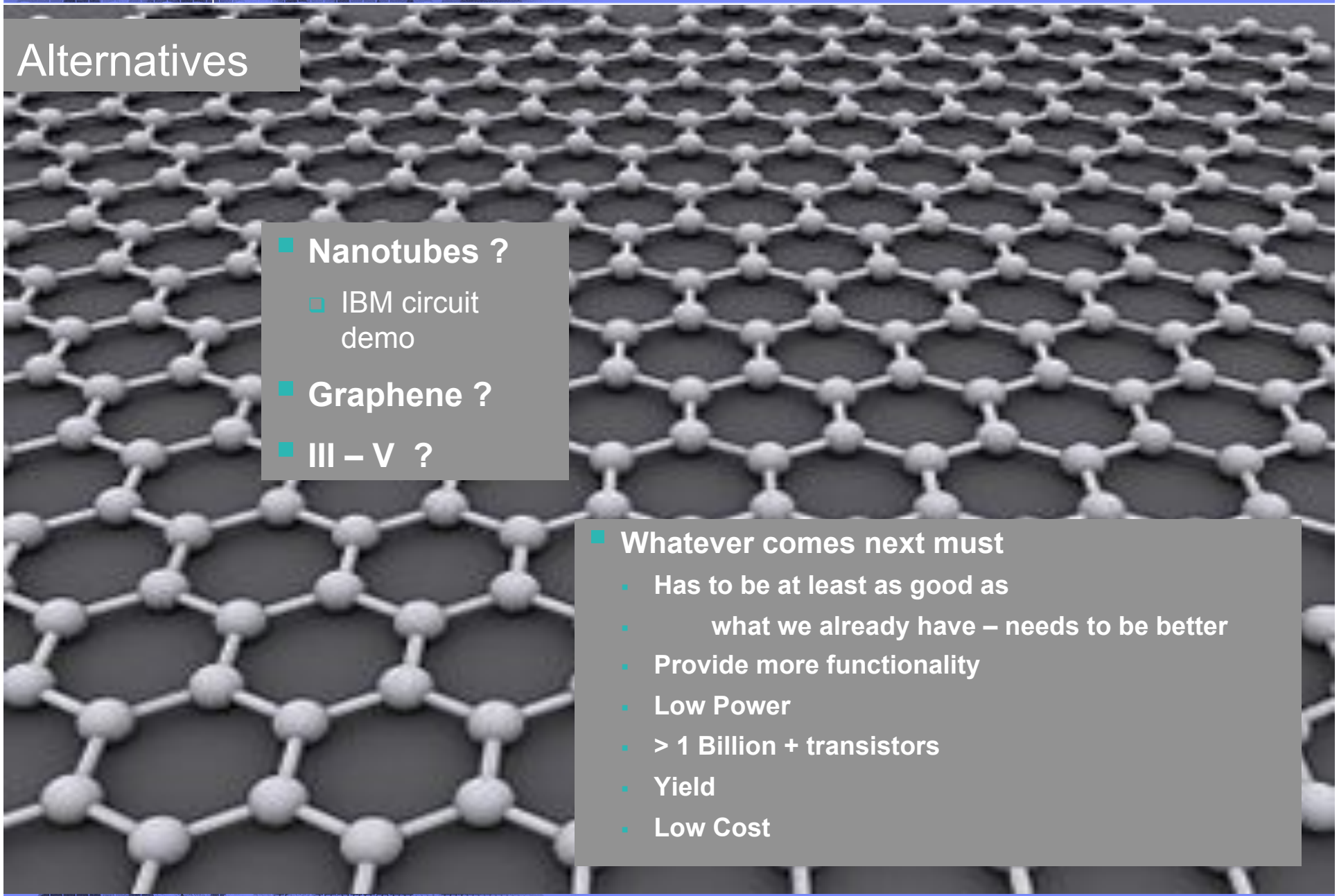
T_{SI} ~ 8nm – 4nm
T_{BOX} = 140nm

T_{SI} ~ 8nm
T_{BOX} 25nm – 10nm

Predictions

- Future is very bright for SOI
- SOI wafers will have extremely thin Si
- SOI wafers will be astonishingly flat
- SOI wafers will have very thin BOX
- SOI wafers may have alternate surface orientations
- SOI wafers may have alternate materials
- SOI wafers will be stacked to form 3d chips

Alternatives



- **Nanotubes ?**
  - IBM circuit demo
- **Graphene ?**
- **III – V ?**

- **Whatever comes next must**
  - **Has to be at least as good as**
  - **what we already have – needs to be better**
  - **Provide more functionality**
  - **Low Power**
  - **> 1 Billion + transistors**
  - **Yield**
  - **Low Cost**

Thank you for Listening !

Dr. Carl Das
EUROPRACTICE, IMEC, Belgium

EUROSOI RUMP SESSION

THE CONTRIBUTION OF SOI IN THE BRILLIANT FUTURE OF NANOELECTRONICS

CARL DAS

IMEC

SOI FROM THE VIEW OF SERVICES

Availability

Supportability & qualified IP

Affordability

AVAILABILITY

- Cfr. SOI mentioned 20 years ago
- When will SOI become widely available?
- What node ?
- What means availability ?
  - Technology is available in the fab ?
  - Do we need more than just a technology ?
  - Cfr. Pure play foundries in the early days
  - For which applications ?

SUPPORTABILITY & QUALIFIED IP

- Success of CMOS ?
  - Scalable
  - Although NRE cost and wafer cost increase every node, unit price decreases every node
  - For SoC in high volume, there has been a driver for the next node
  - SoC needs a large portfolio of SC libraries and IP
    - TTM
    - Cheaper than own design and risk free
- Is this the case for SOI ? And will IP vendors invest in IP in SOI ?

AFFORDABILITY

- Talking about the next node beyond CMOS ? 28nm, 16nm, ...
- Large SoC ?
- NRE cost will be high
  - Masks + IP + design
  - Number of customers will be smaller and smaller
- Unit price ?
- Will SOI be competitive to CMOS/3D for the large volume products?
- Or will SOI be a technology for a niche market or for a happy few ?

Dr. Olivier Faynot
CEA-LETI, Grenoble, France

2011

The contribution of SOI in the brilliant future of Nanoelectronics

O. Faynot

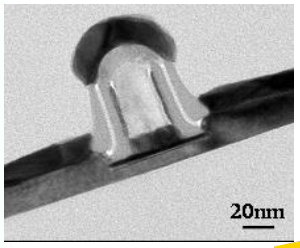
EurSOI

leti

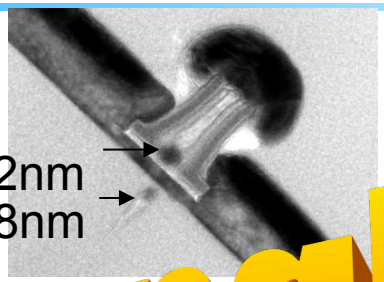
MINATEC

cea

Technological offers on SOI

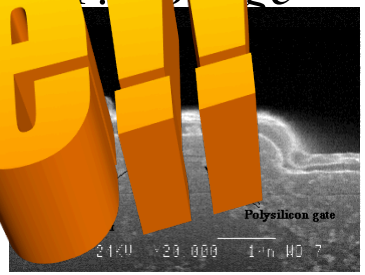


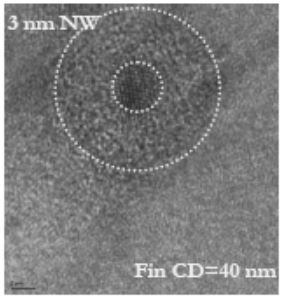
1 gate



1.5 gates... if self-aligned!!

LETI, VLSI 2006





SOI Jungle!!

4 gates

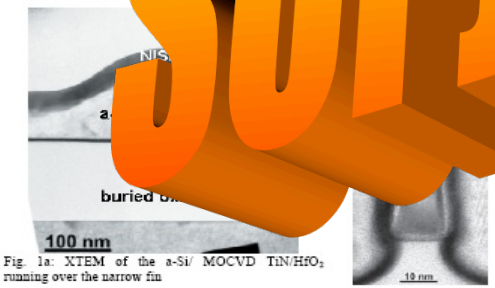
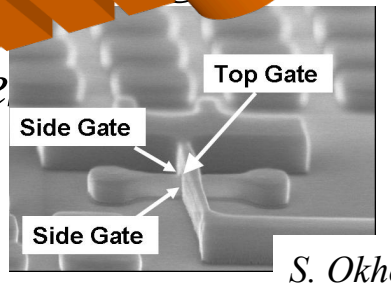


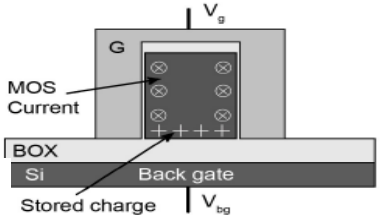
Fig. 1a: XTEM of the a-Si/ MOCVD TiN/HfO2 running over the narrow fin

IMEC, VLSI 2005



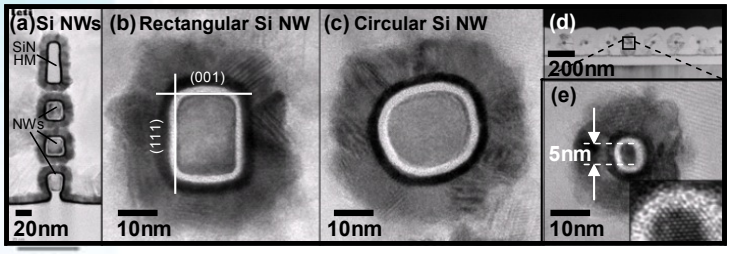
Intel, VLSI 2006

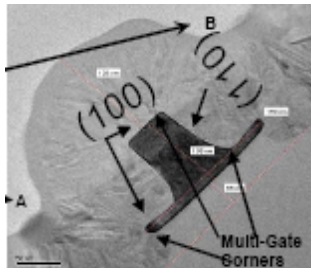
New Generation of Z-RAM



S. Okhonin et al, IEDM'07

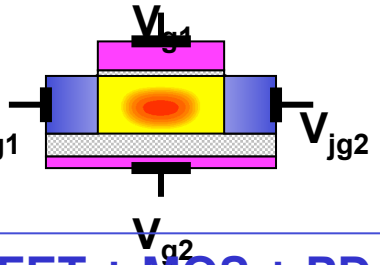
Cristoloveanu et al, '02





Freescale, IEDM 2005

5 gates? V_{jg1} V_{jg2}

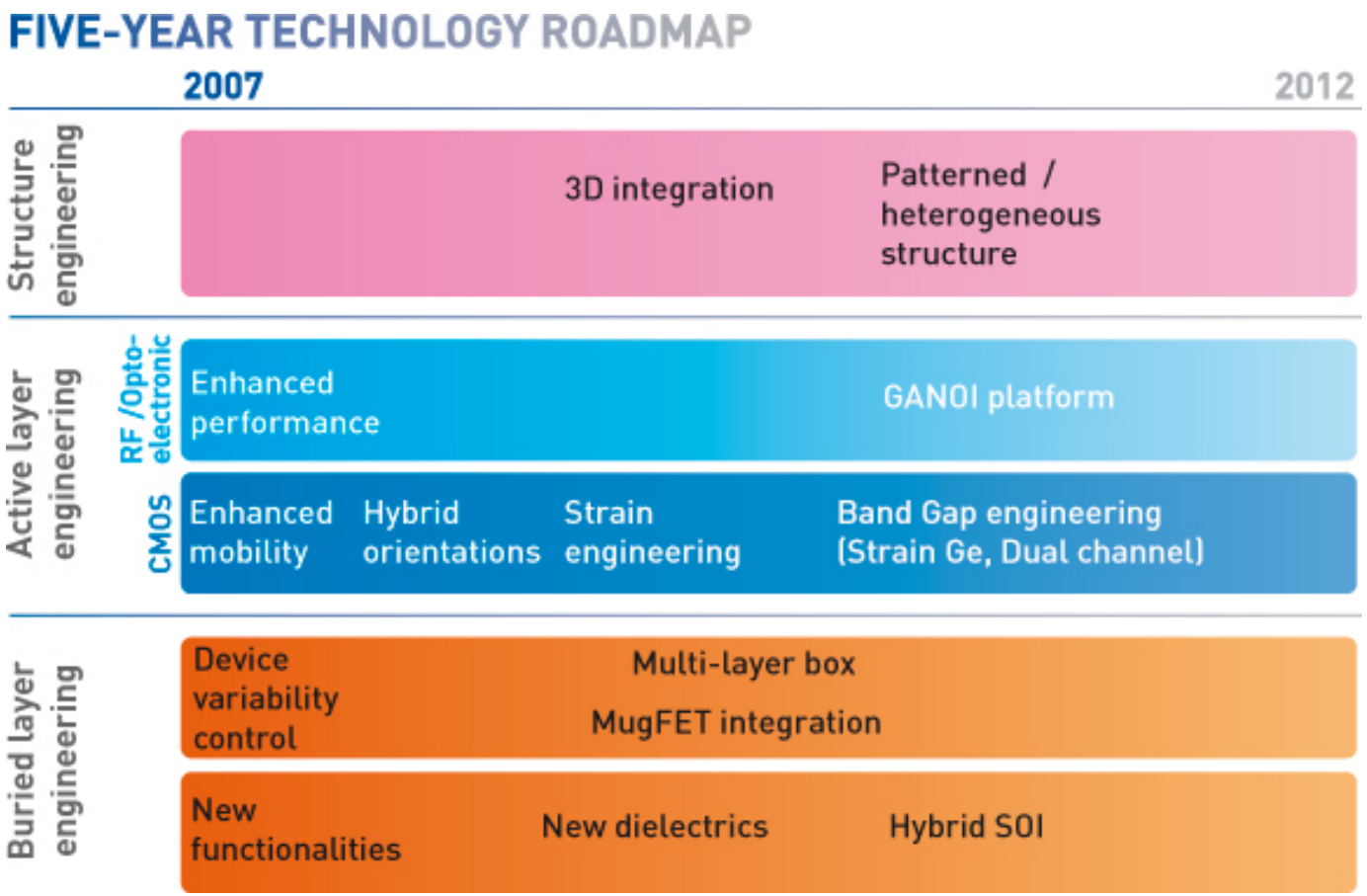


G4 = J-FET + MOS + PD-body

Offer on SOI architectures

- Mainly Research lab, but companies participate!!
- Make science (or at least noise!!)
- Publication target: have the highest number of publications for a given period…

Even wider today and tomorrow!



Source: www.SOITEC.com

Much smaller spectrum in terms of applications…

- More Moore:
  - Global offer on SOI… only High Performance and gaming offers
  - If FinFET arrives… it will be on Bulk? See TSMC…
  - Low Power still on Bulk

	90's	00's	10's	20's
Tbox	400nm	145nm	15-25nm	0?

- More than Moore:
  - MEMs on SOI in a reality
  - Power devices on SOI is a reality
  - Photonics on SOI is starting
  - Nothing yet on SOI Memories

If the rump session title is a question…

- Yes SOI will contribute at the technological level
- Not so sure at the application level!...

  Unless designers and technological teams are working closer to enable the design infrastructure!!

Dr. Noboyuki Sugii
LEAP, Tokyo, Japan

The contribution of SOI in the brilliant future of Nanoelectronics

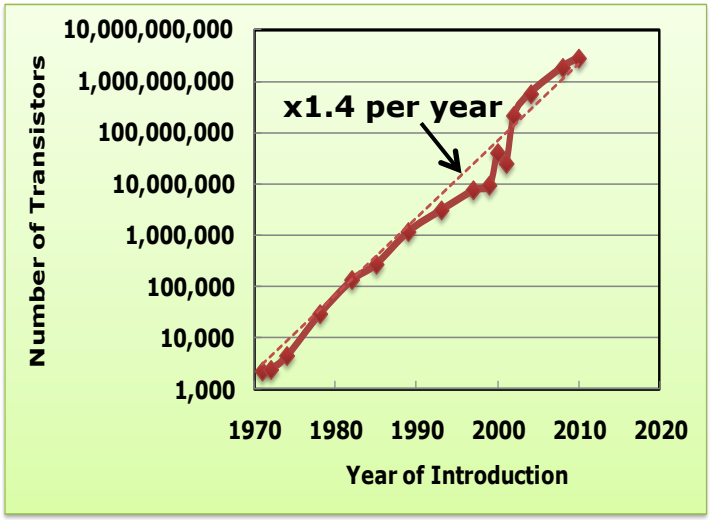
Low-power Electronics Association & Project (LEAP)

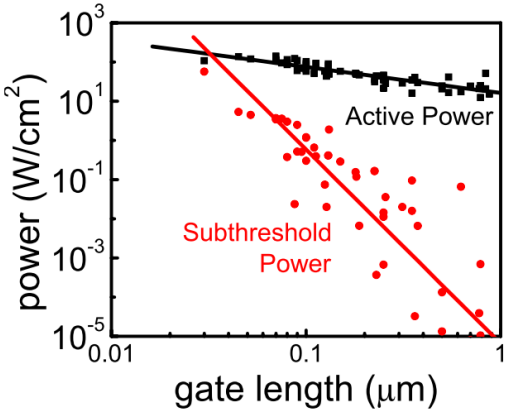
Nobuyuki Sugii

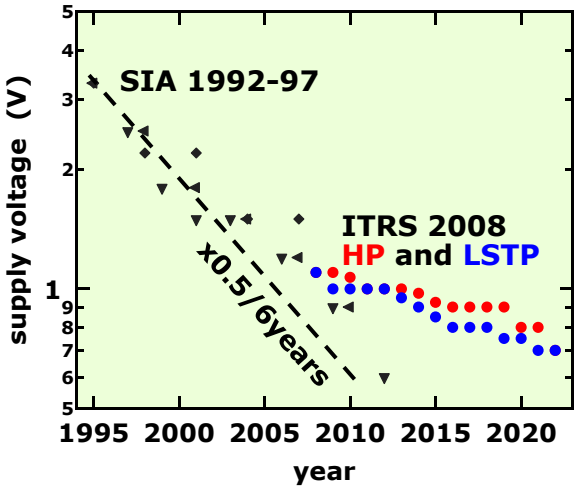
http://tia-nano.jp/English/index.html http://www.leap.or.jp

What is More Moore?

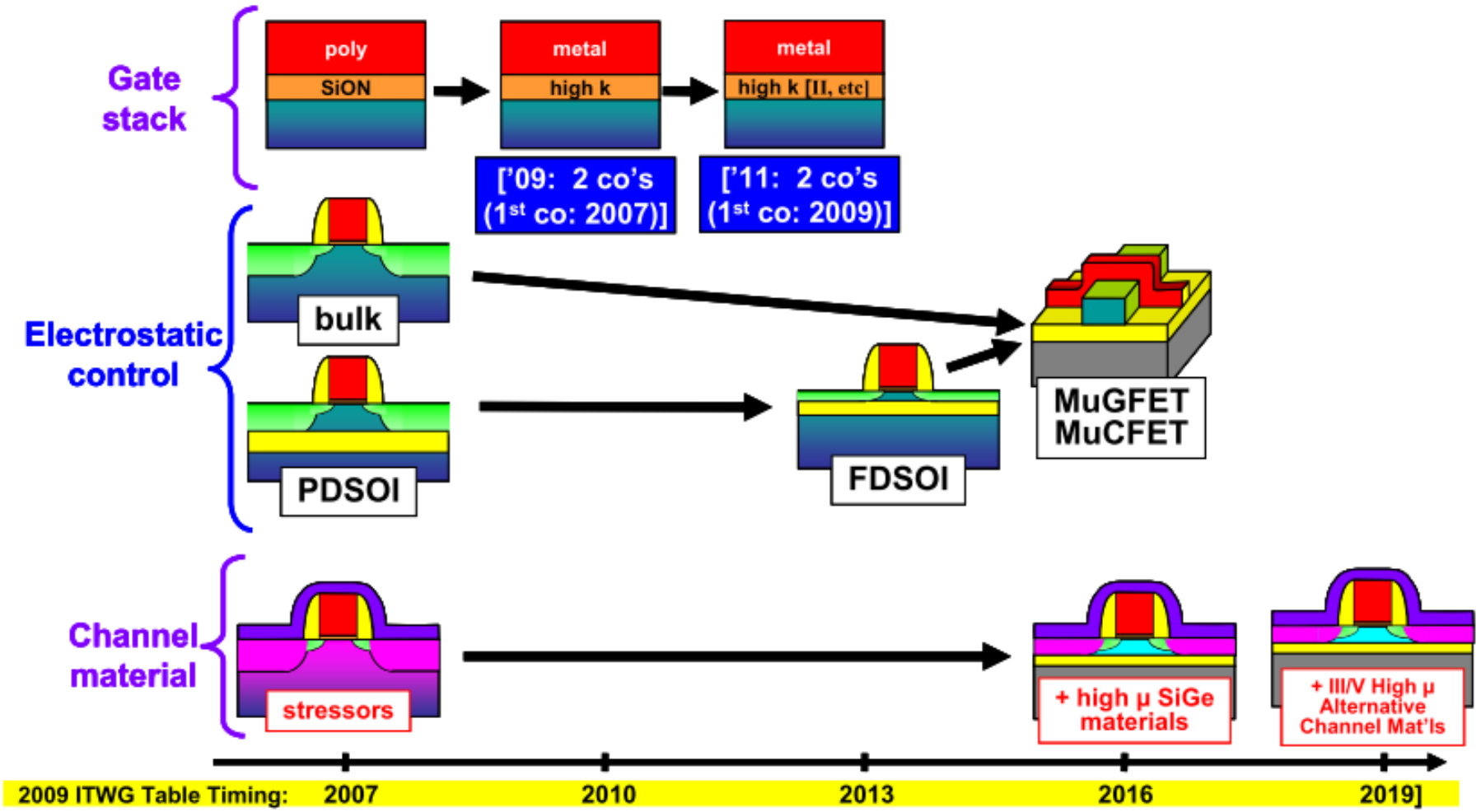
Item	Validity	Category
# of transistors?	Still valid	Original definition
Feature size?		Derived definition
Speed?		
Active power?	Partly valid	
Leakage power?		
Supply voltage?	Not valid	Requirement







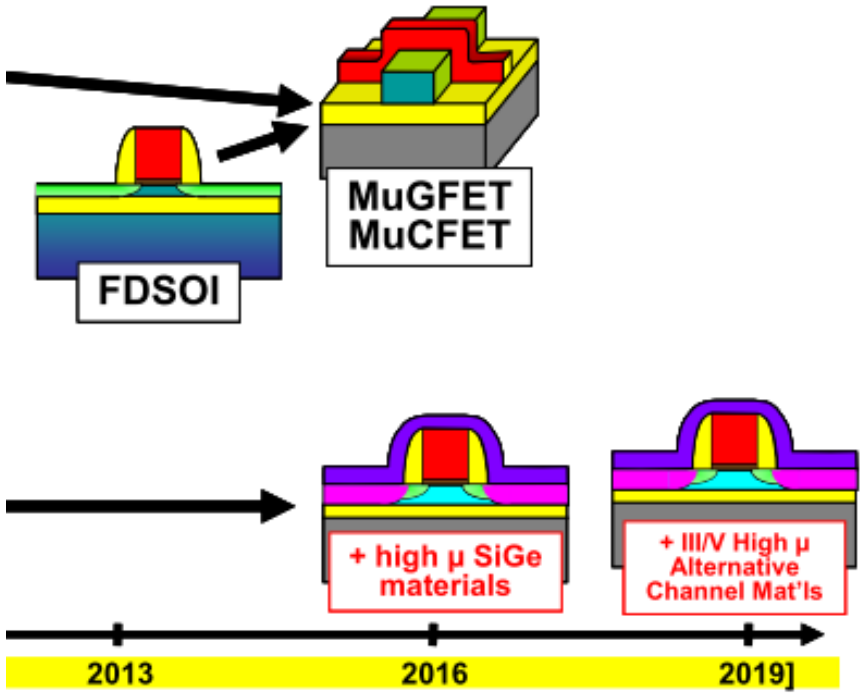
Tr. Options for More Moore



ITRS 2009 Executive summary

All the LE-Trs. are SOI

- **Semiconductor-on-Insulator Trs.**



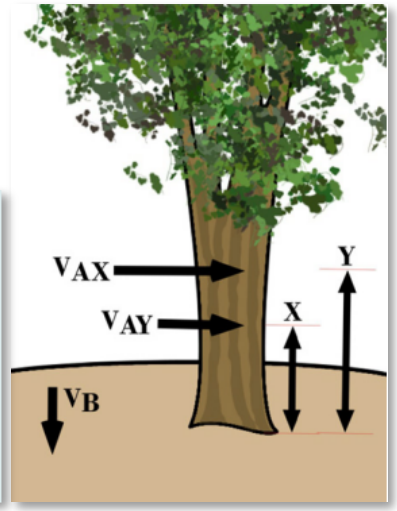
In terms of getting more power efficiency, that is, reducing both active and leakage power, inserting the insulating layer is mandatory.
And new semiconductor materials for channel are awaited.

More voltage scaling

- **Supersteep subthreshold tr.**
  - **Mostly SOI-type structure**
- **Independent DG action**
  - **Adaptive control to maximize power efficiency**
- **ULV (ULP) applications**
  - **Trs. used at the maximum efficiency conditions, e.g. subthreshold logic**
  - **With energy harvesting (More Than Moore)**

ULP applications:
Sensor nodes
Implanted medical
Healthcare, etc.

Even trees can generate electrical power.
ΔV=few mV ~ few hundred mV

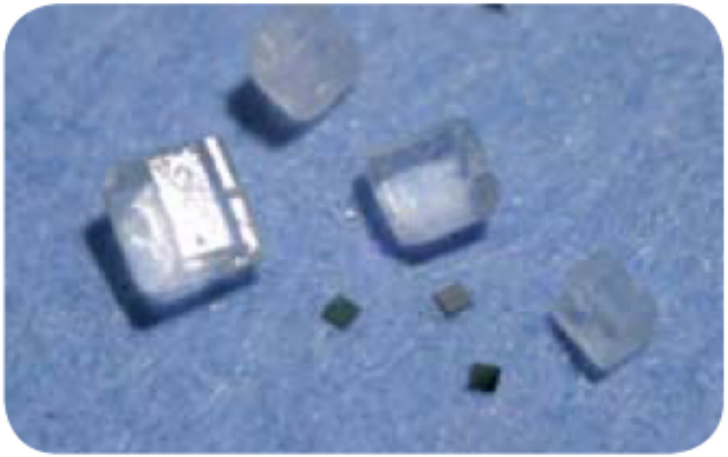


C. Himes et al., IEEE Trans Nanotechnology, vol. 9 (1), pp. 2, Jan. 2010.

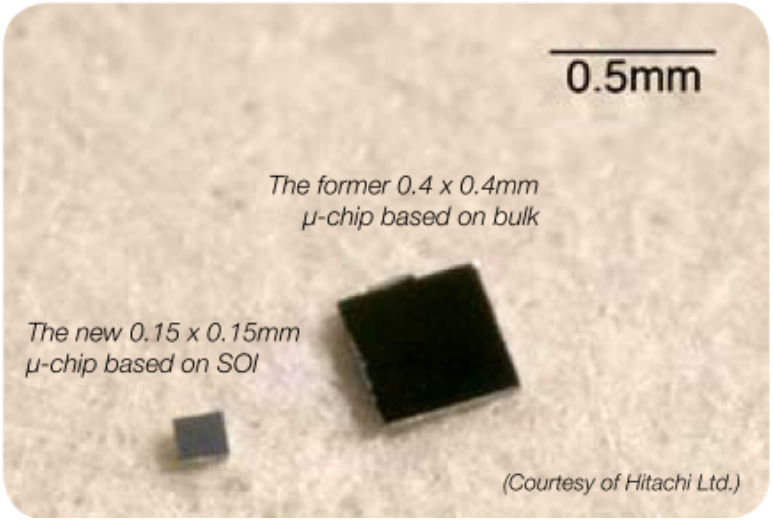
Cost Cost Cost Cost Cost Cost Cost Cost Cost

- **Affordable or not?**

  Low power=Low cost



Thanks to SOI, the newest generation of Hitachi's μ is the world's smallest RFID chip – far smaller than even these grains of salt. (Courtesy: Hitachi)



Hitachi's mu chip:
SOI and even EB direct writing are used for such tiny chips.
(ASN, No. 6, 2006)

Find applications affordable for LP-SOI.