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PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
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1.- Introduction

One of the most promising technology replacement for bulk silicon to continue scaling beyond 32/28nm node is planar fully-depleted (FD) SOI technology [Skotnicki, TED 2008] [Faynot, IEDM 2010]. For low-voltage low-power applications, FD SOI MOSFETs provides excellent characteristics such as reduced short-channel effects, improved subthreshold swing controlled by the thickness of the ultra-thin body (UTB). Consequently, the UTB can be left undoped without compromising short-channel effects. This significantly mitigates threshold voltage (Vt) variability due to random dopant fluctuations (RDF).

These advantages allow for reducing the supply voltage while meeting SRAM robustness constraints and logic timing constraints, thereby significantly saving power consumption. Moreover, FD SOI also offers the traditional advantages of partially depleted SOI: low parasitic capacitances, which further increases power savings, and a simple CMOS process, which makes it economically viable.

In order for FD SOI to be adopted by design houses and foundries, it is critical that circuit designers benchmark FD SOI vs. conventional bulk silicon technology on their own circuit topologies. Moreover, to fit in CMOS scaling roadmap, this has to be done at next technology nodes. Therefore, we developed pre-silicon compact MOSFET models in both FD SOI and bulk technologies in 22/20nm low-power flavour. These modes are made available on-line to enable predictive SPICE simulations of FD SOI vs. bulk for all circuit designers.

This report describes the models that were developed. The modelling methodology is presented in Section 2. A verification of the models is performed vs. foundry models at 45nm node in Section 3. The results at 22nm node are given in Section 4 and the limitations are discussed in Section 5.

2.- Pre-silicon modelling methodology

Pre-silicon compact modelling of MOSFET in bulk silicon technology was proposed in [Zhao, TED 2006] (PTM models). The developed model cards for BSIM4 compact model are based on extrapolation of trends from published experimental data. These pre-silicon models were refined in [Bol, TVLSI 2009][Bol, ISLPED 2009] to improve MOSFET characteristics important for low-voltage low-power design. The refined methodology depicted in Fig. 1 is selected for model generation. We start from PTM models to get a set of basic parameters for BSIM4 model cards for the target devices (gate length, oxide thickness, Vt). Pre-silicon estimation of subthreshold swing, DIBL effect, Vt variability, gate leakage, parasitic capacitances is done based on analytical/empirical studies from the literature. The key parameters in the model cards are tuned to fit the values of the predicted MOSFET characteristics.

This generic methodology is versatile and efficient as it allows for generating a wide variety of compact models from high-performance to low-power CMOS flavours while tuning a minimum set of model parameters.

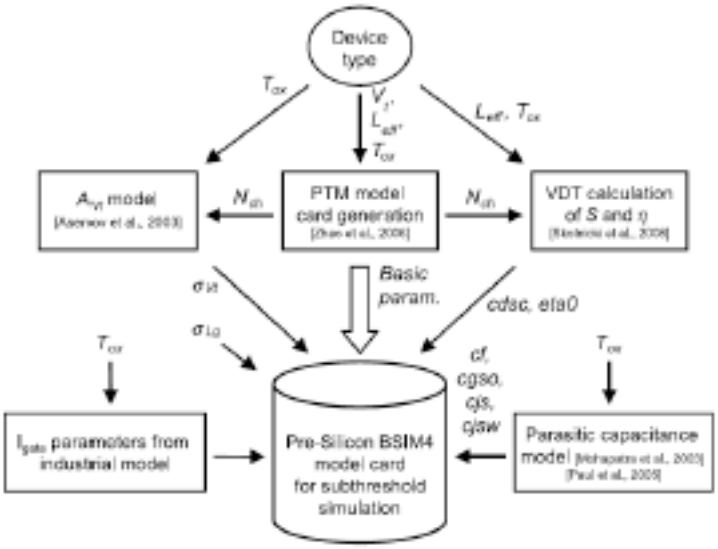

Fig. 1: Pre-Silicon modelling methodology [Bol, TVLSI 2009] [Bol, ISLPED 2009] [Bol, TODAES 2010]

A key target for technology benchmarking at simulation level is to achieve a fair comparison free from model disturbances. For this purpose, we model FD SOI MOSFETs with the same model card generation methodology as bulk MOSFETs based on BSIM4 compact model. Although it is basically intended for bulk MOSFETs, BSIM4 is able to emulate FD SOI characteristics by proper tuning of the parameters. This approach was successfully used in [Bol, SOIC 2008] and [Bol, TODAES 2010].

3.- Sanity check of the methodology @45nm LP

In order to validate the pre-silicon modelling methodology, we performed a sanity check at 45nm node. We generated the model cards to emulate low-power MOSFETs from a 45nm technology based on foundry inputs (gate length, oxide thickness, V_t) and compared the results foundry models. Fig. 2 shows an excellent agreement for statistical distribution (Monte-Carlo simulation with variability) of both Ion and $I_{off.}$ The only mismatch is on the lower bound of the Ioff distribution, which is higher for the foundry models. This is due to gate leakage in foundry models because these 45nm MOSFETs have a standard-κ/poly-Si gate stack whereas in the generated models the gate stack is high-κ/metal gate.

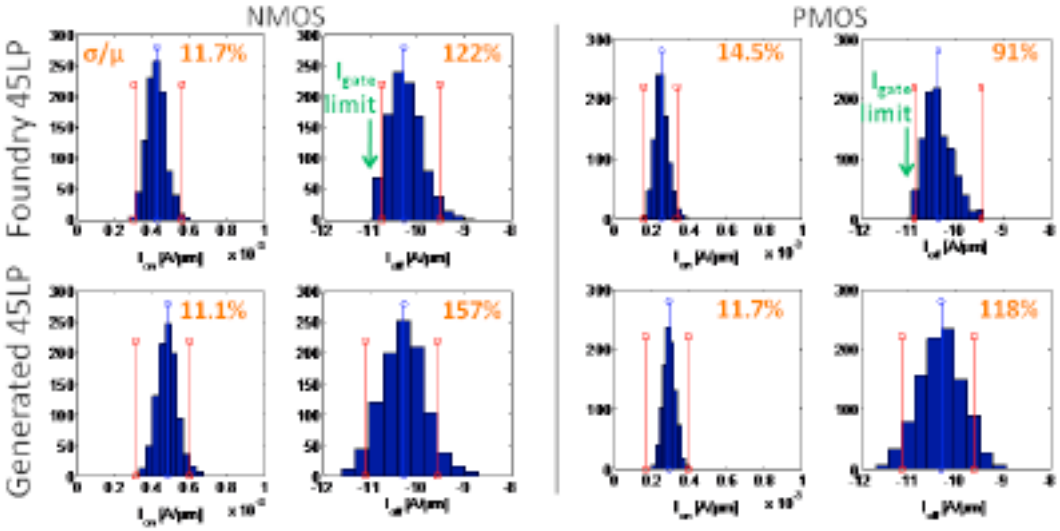

Fig. 2: Sanity check results

4.- Delivered models @22/20nm LSTP

The models for both bulk and FD SOI technologies have been generated at 22/20nm node for low-standby power (LSTP) CMOS flavour, according to ITRS specifications [ITRS, 2009] for V_{dd}, gate length, oxide thickness and V_t. Bulk and FD SOI models share these values and the BSIM4 model with most of the model card parameters, which allows a fair comparison. Models feature is high-κ/metal gate stack for both bulk and FD SOI at 22/20nm node.

Fig. 3 shows the data sources for main MOSFET characteristics. Notice that V_t tuning is performed with a common I_{off} target for bulk and FD SOI, taking into account the differences in subthreshold swing, mobility, DIBL effect, V_t roll-off.

Parameter	Bulk	FD SOI
V_{dd}, EOT, L_g	ITRS /PTM (identical)	Identical
R_{sd}, N_{sh}	ITRS/PTM (identical)	Identical
C_{fringe}	ITRS	ITRS
C_{ov}	PTM	Identical
C_j	[Bol, TVLSI'10]	[Bol, SOIC'08]
Body effect (for device stack)	PTM	Disabled [Bol, SOIC'08]
VTH0	ITRS (tuned to match I_{off})	ITRS (tuned to match I_{off})
Mobility	PTM	[Cheng,SVLSI'09]
Subthreshold swing, DIBL	< literature	[Cheng, SVLSI'09]
A_{Vt}	[Arnaud, IEDM'09]	[Cheng, SVLSI'09]
Global σ for CD	ITRS	Identical
Vt roll-off (→ σ_{Vt} < global σ_{CD})	[Diaz, IEDM'08]	[Khakifirooz, VLSITSA'10]
Temperature effect	μ(T) < [Bol,ESSCIRC'10]	Vt(T) < [Sakurai, Springer'06]

Fig. 3: Data sources of the considered values for main MOSFET characteristics

Fig. 4 shows the results in terms of $I_{d,sat}$, $I_{d,lin}$ and I_{off} statistical distributions for NMOS and PMOS in bulk and FD SOI. FD SOI improves $I_{d,sat}$ by 40% with a significant reduction of the spread.

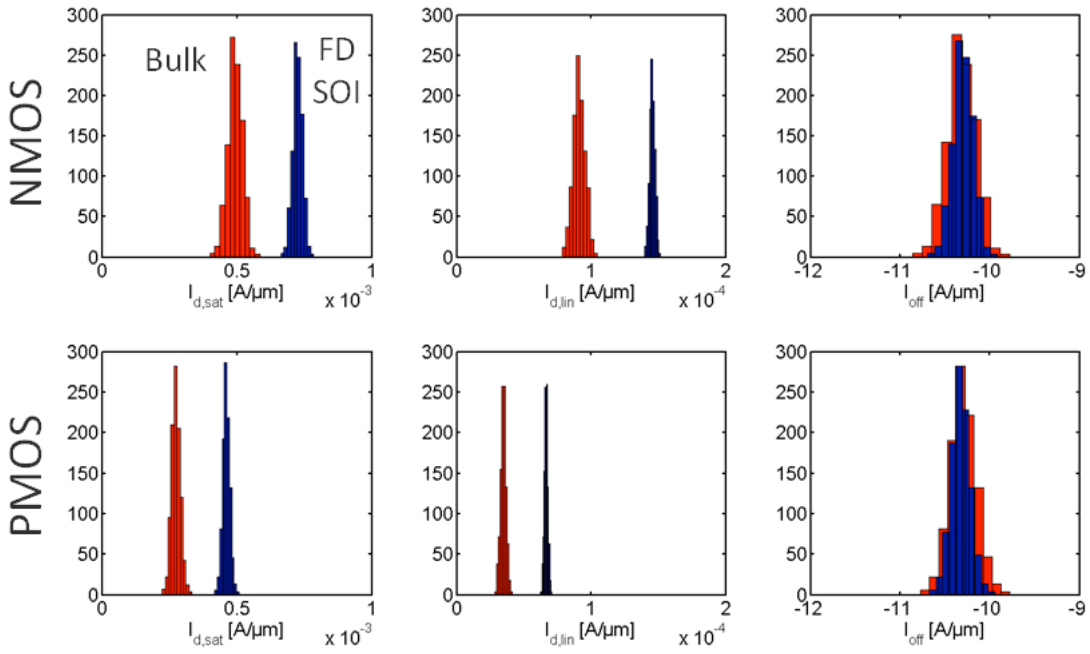

Fig. 4: Model results – current level with mismatch

Global process corners have also been generated. Results are given in Fig. 5, confirming the potential of FD SOI.

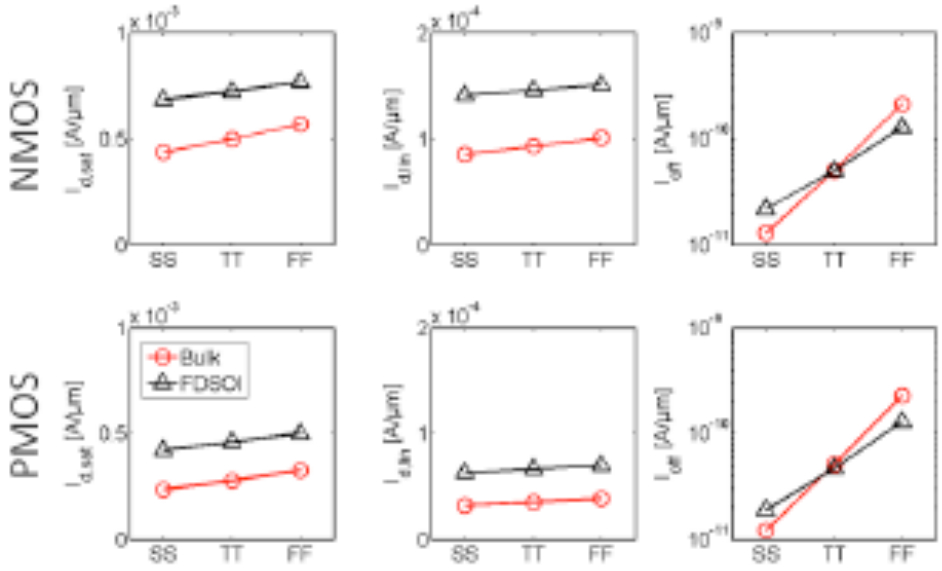

Fig. 5: Model results – current level with process corners

5.- Conclusions: model access and limitations.

The results need to be published prior to providing an on-line access to bulk and FDSOI models for both low-standby-power (LSTP) and low-operating-power (LOP) CMOS flavors at 22nm node. Tentative publication is ESSDERC 2011.

However, in the meantime 45nm models from [Bol, SOIC 2008][Bol, TODAES 2010] are available on-line at http://www.dice.ucl.ac.be/~bol. These models are more intended for ultra-low voltage operation (0.3-0.5V) but also give interesting insight at nominal voltage (1V).

The main limitations of the FD SOI models are temperature dependence of the subthreshold swing and intrinsic gate capacitance in subthreshold regime. Indeed, these two aspects can hardly be modified as they are based on built-in BSIM4 equations valid for bulk MOSFETs. Therefore, no temperature sweep can be performed on the generated FD SOI models. Rather, an independent model card should be generated with modification of the subthreshold swing at this temperature. Intrinsic gate capacitance in subthreshold regime is lower in FD SOI due to BOX isolation and the generated FD SOI models are thus pessimistic with regards to this capacitance contribution as it uses the same values as in bulk.

6.- References.

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[Zhao, TED 2006] W. Zhao and Y. Cao, “New generation of predictive technology model for sub-45nm early design exploration”, in IEEE Trans. Electron. Devices, vol. 53, (11), pp. 2816-2823.