INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

Grant Agreement nº 216373

D4.6 Final "Who is who" Guide

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Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

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Section 1. Deliverable description.

The “Who is Who” guide is intended to be a compendium of the different research groups, industrial groups and design groups whose main activities lie in the field of SOI: materials, devices, circuits and electronic end-user applications. Each group will be identified by its profile: contact information and their expertise and experience in the field. Our goal is that everybody working in SOI ambit should be identified so that other partners know where to address inquiries.

We persuade the following objectives:

1. To increase knowledge and expertise about SOI technology in Europe by enhancing interaction and synergy between academic groups and industries.

2. To compile, filter and provide structured information about SOI in Europe.

3. To foster the exchange of knowledge between research groups working in: materials, devices, circuits and electronic end-user applications.

4. To promote interaction between existing SOI projects at national and European level, and facilitate the coordination of their work.

The present document is a paper copy of the web-based guide which is available at http://www.eurosoi.org/who_is_who.asp, where the reader could find on-line all the information and different search tools help to organize the listed institutions according to different criteria.

Section 2. "Who_is_who" guide

2.1. EUROSOI+ Members

	Organization	Short name	Country
1.-	Comissariat a l'Energie Atomique	CEA	France
2.-	Chalmers University of Technology	CHALMERS	Sweden
3.-	Interuniversitair Micro-Elektronica Centrum vzw	IMEC	Belgium
4.-	Institut Polytechnique de Grenoble	Grenoble-INP	France
5.-	University College Cork, National University of Ireland Cork	TYNDALL	Ireland
6.-	Université catholique de Louvain	UCL	Belgium
7.-	Universidad de Granada	UGR	Spain

	Wafer Processing	SOI Materials	Device Fabrica.	Structural Charact.	Electrical Character.	Optical Character.
UGR						
IMEP						
UCL						
IMEC						
CHALMERS						
CEA-LETI						
TYNDALL						

	Process Simul.	SOI Reliab.	Circuit Design: High-T, Low-Pow	Circuit Design: RF	Automotive Applications	Organization SOI training events
UGR						
IMEP						
UCL						
IMEC						
CHALMERS						
CEA-LETI						
TYNDALL						

2.2. Non-members

	Organization	Short name	Country
1.-	Gesellschaft für angewandte Mikro- und Optoelektronik mbH	AMO	Germany
2.-	CISSOID S.A.	CISSOID	Belgique
3.-	Centre National de la Recherche Scientifique	CNRS-UM2	France
4.-	Consejo Superior de Investigaciones Cientificas	CSIC	Spain
5.-	Ditocom	DITOCOM	France
6.-	Swiss Federal Institute of Technology Lausanne	EPFL	Switzerland
7.-	Institut für Mikroelektronik und Mechatronik-Systeme GmbH	IMMS	Germany
8.-	Institut Supérieur d'Electronique de Paris	ISEP	France
9.-	Institute of Semiconductor Physics, National Academy of Sciences of Ukraine	ISP	Ukraine
10.-	University of Liverpool	LIVUNI	United Kingdom
11.-	Politecnico di Torino	POLITO	Italy
12.-	The Queens University of Belfast	QUB	United Kingdom
13.-	SOITEC Silicon On Insulator Technologies	SOITEC	France
14.-	Institute for Microelectronics / University of Technology of Vienna	TUW - IME	Austria
15.-	Universitat Autonoma Barcelona	UAB	Spain
16.-	Universita` degli Studi di Udine	UNIUD	Italy
17.-	Universitat Rovira I Virgili	URV	Spain
18.-	Universidad de Salamanca	USAL	Spain
19.-	Uppsala University	UU	Sweden
20.-	University of Twente	UT	The Netherlands
21.-	Technical Research Center of Finland	VTT	Finland
22.-	Politechnika Warszawska (Warsaw University of Technology)	WUT	Poland
23.-	X-FAB Semiconductor Foundries AG	XFAB	Germany
24.-	ARCES, Alma Mater Studiorum, Università di Bologna	ARCES	Italy
25.-	The University of Glasgow	GLASGOW	United Kingdom
26.-	Institut fuer Mikroelektronik Stuttgart	IMS-CHIPS	Germany
27.-	Innovative Silicon S.A.	ISI	Switzerland
28.-	Kungl Tekniska Högskolan	KTH	Sweden
29.-	University of Southampton	SOTON	United Kingdom
30.-	SILTRONIC AG	SILTRONIC	Germany
31.-	SOISIC SA – Silicon On Insulator and Integrated Circuits	SOISIC	France
32.-	STMicrolectronics Digital Design	ST	France
33.-	STMicrolectronics Central R&D	ST	France

34.-	STMicroelectronics-RF/Analog design	ST	France
35.-	Tracit Technologies SA	TRACIT	France

EUROSOI

MEMBERS

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Laboratoire d'Electronique de Technologie de l'Information**
Organization short name:	CEA – LETI
Internet homepage:	**www-leti.cea.fr**

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Experience and expertise fields

LETI is involved since more than 20 years in SOI technologies. LETI has a large experience in the field of Soi material (SIMOX, SMART CUT), in the field of SOI transistor process (Partially, Fully Depleted and Multi-gate SOI), as well as in the field of device modeling and circuit design.

Facilities and Equipment

- 100, 200 and 300mm clean room facilities, with physical characterization labs.
- Electrical characterization equipements for parametric test, hand probing test and circuit tests.
- RF caracterization and modeling is also an important activity in the laboratory.

Three last international research projects

ADAMANT
NESTOR
SATURN
EUROSOI

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Chalmers Tekniska Högskola AB**
Organization short name:	CHALMERS
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Experience and expertise fields

Manufacture of SOI and other advanced materials by wafer bonding. Electrical device and materials characterisation. RF device modelling. MEMS structures in SOI. Nanoscaled Si devices on SOI.

Facilities and Equipment

The facilities of MC2 include 1240 m^2 state-of-the-art cleanroom offering processing platforms for a variety of materials and technologies. The equipment include 10 nm e-beam lithography as well as processing capabilities for up to 150 mm silicon wafers. In addition to the cleanroom facility a wide range of equipment and tools for electrical characterisation from dc to several hundred Ghz are available in our measurement laboratories. A wide range of physical characterisation equipment is also available at Chalmers primarily outside the Department of Microtechnology and Nanoscience.

Three last international research projects

- EU: SINANO
- EU: SOICMOS (CMOS SOI for low power logic and RF wireless)
- EU: SESIBON
- EUROSOI

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Interuniversiair Mikro-Electronica Centrum**
Organization short name:	IMEC
Internet homepage:	**www.imec.be**

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Experience and expertise fields

IMEC has a long standing experience in design, processing and testing of deep submicron SOI devices. Study of device physics, reliability, LF noise, radiation effects, and low temperature performance. Processing on 200 mm wafers. Present efforts are focussing on FinFETS for the 50 nm technology mode. Also activities on strained Si on SOI and GeOI.

Facilities and Equipment

Fully equipped 200 mm processing line, and 300 mm in start-up.
Extensive analytical and structural characterization facilities.
Equipment for electrical device characterization, including low frequency noise.

Three last international research projects

Presently involved in NANOCMOS and SINANO.
NESTOR, ARTEMIS, VAMOS, EUROSOI

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Institute Polytechnique de Grenoble**
Organization short name:	IMEP-INPG
Internet homepage:	**http://www.imep.enserg.fr/**

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Experience and expertise fields

IMEP has 30 years experience in SOI and SOS technologies, including material and device characterization, modelling and simulations. Many conferences, summer schools and other SOI-related events have been organized by IMEP.

Facilities and Equipment

Advanced equipments for electrical characterization (parametric test, hand probing test, noise and low-temperature measurements, RF characterization, magneto-transport, photoluminescence, etc). Simulations tools are also available.

Three last international research projects

SINANO
NESTOR
NANOCMOS
EUROSOI

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**National University of Ireland, University College Cork, Tyndall National Institute**
Organization short name:	TNI
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Other Senior Researchers

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3. Dr Vladimir Lavayen, vladimir.lavayen@tyndall.ie

Experience and expertise fields

Expertise in SOI 2-dimensional photonic crystal waveguides (design, fabrication and characterisation) and nanoimprint lithography. Fabrication and characterisation of optics-inspired SOI-organic structures and non-linear magnetic photonic crystals. Dr Lavayen is an expert in functional nanotubes and is developing methods to integrate non-carbon nanotubes on silicon platforms. Prof Sotomayor Torres expertise is in electron-phonon interaction, laser spectroscopy and optical transitions in low dimensional structures.

Facilities and Equipment

Access to a full 100 nm Si fabrication line, electron beam pattern generator, focused ion beam and associated clean-room facilities. As part of the Tyndall National Institute access to a whole range of fabrication, design, characterisation and testing equipment is available.

Three last international research projects

1) EU IST 1999-13415 (CHANIL), 2000-2002.
2) EU Growth programme, GRD1-2000-25592 (MONALISA), 2001-2003.
3) EU IST 510162, Photonic Hybrid Architectures based on two- and three-dimensional silicon photonic crystals, (PHAT) 2004-2006

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Université catholique de Louvain**
Organization short name:	UCL
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Experience and expertise fields

Overall study of SOI technologies, devices and circuits, for low-voltage low-power, radiation-hardened, microwave, high-temperature and quantum applications. Device characterization, modelling and subsequent analog, RF and digital circuit design in many SOI processes down to sub-100nm generations. Fabrication of Microsystems fully co-integrating sensors or MEMS with their associated CMOS electronics, as well as of quantum nanoscale devices.

Facilities and Equipment

Complete pilot fabrication line of about 400 m^2, for the rapid prototyping and validation of new fabrication steps and of new integrated devices or microsystems, on silicon/SOI substrates (3-inch).
Electrical measurement set-ups over a large range of frequencies (from DC up to 110 GHz) and temperatures (from few mK up to 400°C) on wafer-scale (semi-automatic prober) as well as packaged circuits levels.

Semiconductor simulation tools (ISE, Avanti and Silvaco) in the Microelectronics Laboratory. Electro-magnetic simulations in the Microwaves lab.

Three last international research projects

SINANO – Silicon based nano-devices – Network of excellence, FP6
ATHIS – Advanced Techniques for High-temperature System-on-chip – Growth, FP5
T206 – Low-power / RF SOI circuits – MEDEA+

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Universidad de Granada**
Organization short name:	UGR
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Experience and expertise fields

UGR has 20 years experience in simulation on electron devices and in particular SOI technology. Modelling of semiconductor devices with emphasis on Full band Monte Carlo transport techniques for free and quantized electron gases.
In addition UGR features state-of-the-art electrical characterization facilities.

Facilities and Equipment

In house developed device simulators:
1) Self-consistent multisuband-emsemble Monte Carlo transport simulator for electron and holes (3d in k-space, 2d in r-space, bulk and SOI MOSFET) in different materials Si, Ge, strained-Si, III-V
2) general purpose 1-D and 2-D Schroedinger Poisson solver in the effective mass approximation for multi-dielectric gate stacks featuring both electron and hole quantization and tunnelling gate current calculation.
3) general purpose self-consistent Monte Carlo transport code for quantized electron gas (2d in k-space, 2d in r-space, bulk and SOI MOSFET).
4) 100m^2 state-of-the-art electrical characterization facilities including 2x- 300mm semiautomatic probe-stations, semiconductor analyzers with attoampere resolution, arbitrary function generation, pseudo-MOS characterization setup, up-to 110MHz impedance analyzer...

Three last international research projects

SINANO
EXTRA

NON-MEMBERS

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**CISSOID S.A.**
Organization short name:	CISSOID
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Experience and expertise fields

CISSOID is a Fabless company focusing on SOI and offering:
- IC design services for high-temperature and low-power applications
- High-temperature standard products (above 200°C)
- Low-power and RF IP's

To maintain its leadership in SOI analog circuit design, CISSOID is strongly investing in R&D through European research projects. CISSOID is a spin-off company from UCL.

Facilities and Equipment

CISSOID is a design center and a fabless company focusing on IC Design. Other activities (IC fabrication, packaging and test) are subcontracted. The tools/equipments used by CISSOID are:

- IC Design tools necessary to provide GDS2 files to the foundry subcontractor: Circuit simulation (ELDO, …), Layout (DRC, LVS, …) on PC workstations
- Electrical measurements equipments and proprietary set-ups for analogue and high-temperature characterization of IC prototypes.
- For RF and On-wafer measurements, CISSOID is cooperating with UCL.

Three last international research projects

ATHIS – Advanced Techniques for High-temperature System-on-chip – Growth, FP5
T206 – Low-power / RF SOI circuits – MEDEA+
4G-Radio – A Silicon Application platform for radio communications – MEDEA+ A107

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Centro Nacional de Microelectrónica (Consejo Superior de Investigaciones Científicas)**
Organization short name:	CSIC - CNM
Internet homepage:	**www.cnm.es**

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Experience and expertise fields

CNM has a large experience on Bulk power semiconductor devices, including LDMOS transistors in SOI and SOS substrates. Four fields are covered on SOI: thermal management and new solutions to reduce self-heating effects, high-voltage power LDMOS, very low voltage protection devices (TVS) and advanced power LDMOS structures for RF applications.

Facilities and Equipment

CNM holds a flexible Clean Room with standard CMOS technology (2.5 µm) and several other technologies addressed to sensors, microsystems and power devices. Nanofabrication equipments are also available. Fabricated sensors, ICs and power devices can be packaged and electrically tested at CNM. Simulation tools available are ANSYS, Silvaco, ISE-TCAD, Cadence, Flowtherm and specific software for analogue and digital design.

Three last international research projects

Advanced Techniques for High Temperature System-on-Chip (ATHIS) GRD1-2001-40466 – Growth Programme (UE)
Power and Thermal Management of Wide Bandgap Semiconductors AO/ITT A04349 - European Space Agency (ESA –UE)
Establishing Silicon Carbide Applications in Power Electronics in Europe (ESCAPEE) GRD2-2000-30399 – Growth Programme (UE)

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**DITOCOM**
Organization short name:	DITOCOM
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Other Senior Researchers

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Experience and expertise fields

DITOCOM is a fabless company focusing on :
* system architecture for silicon integration.
* silicon design services for wireless.
* low-power applications.
* radiofrequency.

Main application areas are:
* Digital television (DVB-S/C/T/H).
* WiFi (IEEE 802.11a/b/g).
* UWB.
* WiMax.

Facilities and Equipment

PCs
Workstations
Lab equipped with test and measurement equipment.

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Swiss Federal Institute of Technology Lausanne Institute of Microelectronics and Microsystems**
Organization short name:	EPFL
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Other Senior Researchers

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Experience and expertise fields

- SOI-based process fabrication: SOI silicon nanowires, Hybrid CMOS/single electron transistors, Resonating MEMS-like SOI structure, Optoelectronics devices.
- TCAD process simulation and modeling of emerging nanoelectronics devices.
- SOI technology & development of a Hall effect sensor.
- Radio Frequency integrated circuits on SOI substrates.

Facilities and Equipment

- 4" and 6" CMOS compatible clean room facilities including photolithography, FIB processing, CVD and oxidation, etching (http://cmi.epfl.ch).
- Devices characterisation tools.
- Tools for analog/digital circuits design, simulation and testing.

Three last international research projects

SINANO
OPTOSIMOX
NANOTIMER

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Institiut für Mikroelektronik und Mechatronik Systeme gGmbH**
Organization short name:	IMMS gGmbH
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Experience and expertise fields

Modelling of circuit elements of a partially depleted SOI technology. Analogue and digital circuit design of high temperature SOI circuits. Realised and measured circuits 10Bit ADC, DAC, Bandgap reference, voltage regulators, comparators, OpAmps (Analogue Library). HT-camshaft sensor, HT pressure sensor interface, SOI EEPROM circuit and cell design, SRAM.

Facilities and Equipment

- Wafer prober with bridge, pulse measurement units, ICCAP for device measurements and modelling,
- digital tester HP82000, thermo stream (T=-70..225°C), digital data analyser, spectrum analyser, network thermo chuck (T=-40..225°C), HP4155, low leakage switch matrix, LCR measurement analyser
- RF measurements equipment up to 50 GHz, high frequency noise measurements, on wafer characterisation (8 inch wafer)
- Low frequency noise measurement equipment, on wafer characterisation (8 inch wafer)

Three last international research projects

TERMIS - High temperature/ High-Voltage Mixed-Signal SOI ASICs for Aerospace Applications – ESPRIT: 29'598 (European commission) -
ATHIS - Advanced Techniques for High Temperature System-On-Chip - GRD1-2001-40707 (European commission)

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Institut Superieur d'Electronique de Paris**
Organization short name:	ISEP
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Other Senior Researchers

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Experience and expertise fields

Amara Amara obtained his HDR (Confirmation of Leading Research Capabilities) in 1999 from Evry university, a Ph.D. in computer science in 1989 and a DEA (MSc) in 1984 in microelectronics and computer science both from Paris VI university.
Andrei Vladimirescu received the M.S. and Ph.D. degrees in electrical engineering and computer sciences from the University of California, Berkeley, in 1980 and 1982, respectively.

5. Fields of Expertise

SOI Integrated Circuits. Modeling and Simulation. Low-voltage, low-power design Ultra-low voltage operation. Analog, Mixed-signal and RF design and simulation

Facilities and Equipment

Simulation and Design Lab equipped with
- 20 Sun Workstations (Ultra-10)
- Leading EDA IC design software
- ST 0.13um SOI Design Kits and Standard Cell Library

Three last international research projects

T206 Medea+ on SOI
TEMPUS
Sanara – Medea+ (Galileo)

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Lashkaryov Institute of Semiconductor Physics, National Academy of Sciences of Ukraine**
Organization short name:	ISP
Internet homepage:	**www.isp.kiev.ua**

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Other Senior Researchers

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Dr. I.Tyagulskii, cryo@lab15.kiev.ua

Experience and expertise fields

Main experience is in electrical characterization methods and theory of SOI structures and MOSFETs operation at extreme conditions, such as: cryogenic and high temperatures (from 4.2 to 700K); high-field electron injection in dielectric layers; ionizing radiation; thermal-bias effect. Main technical direction is the development of laser zone melting recrystallization technique for SOI wafers fabrication with special buried dielectrics.

Facilities and Equipment

Current thermally activated spectroscopy and I-V in wide temperature range (from 4.2 to 673K); Capacitance and conductance DLTS (T_{op} – 80 to 573K); High-frequency capacitance relaxation technique (80-673K); Combined equipment for high-field FN and low-field UV electron injections operated in constant current and constant voltage regimes together with C-V or I-V measurements in temperature range from 300 to 600K; C-V at frequency from 20 Hz to 10^6 Hz and temperature from 80 to 373K;
RTA and RF plasma treatment equipments.

Three last international research projects

NATO Collaborative Linkage Project SST.CLG 975925 "Development of SOI technology for microelectronic devices working under harsh conditions (extension)" (1999-2001); STCU project 2332 "Technology of silicon-on-insulator and silicon-carbide-on- insulator structures for high-temperature microelectronic devices" (European Financial Supporting) (2001-2003); Network of Excelence of 6th Framework Programme "Silicon-based nanodevices" (2004-2006).

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**University of Liverpool**
Organization short name:	LIVUNI
Internet homepage:	**http://www.liv.ac.uk/eee/research/sse/sse.htm**

Contact person					
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Other Senior Researchers

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Experience and expertise fields

Electrical, materials and optical characterisation including: scanning ellipsometry, AES, FTIR, TEM, SEM, charge pumping, photo I-V, I-V, C-V, SHE, CHE
Device physics, design and trouble-shooting
Small circuits design: analogue and digital

Facilities and Equipment

Measurements Laboratory equipped for above purposes
Small clean room for preparing capacitors etc: wet benches, lithography, metal dep etc
Low temp. plasma anodisation (oxidation) – uses rf plasma – oxide growth not dep
Cadence
Spectro-ellipsometer
Range: near IR (up to 1700 nm) and UV region (185-240 nm)
Very fast acquisition time: 700 wavelengths in less than 1 second!
Variable Angle (VASE) system. WVASE32TM software used.
100um 'micro' spot size
Internal Photo-emission system
UV 250nm/5eV (IR 900nm/1.4eV)
AFM with nanolithography capability

Three last international research projects

SIGMOS in Framework 5
SINANO in Framework 6
UK NorthWest hi-k consortium
Collaboration between Liverpool and Manchester Universities and IMEC

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Centre National de la Recherche Scientifique (AD13), 3 rue Michel Ange, 75794 Paris cedex 16.**
Organization short name:	CNRS - UM2/GES/JRU5650
Internet homepage:	

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Other Senior Researchers

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Antoine TIBERJ, antoine.tiberj@ges.univ-montp2.fr)

Experience and expertise fields

The group at UM2 has more than six years experience in the characterization of SOI materials, including the effect of processing steps on the SOL (Silicon Over Layer) morphology, the residual stress in the SOL, buried oxide and handle wafer and, finally, the electrical properties. The effect of 3C-SiC deposition on SOI has also been considered.

Facilities and Equipment

Numerous optical and electrical characterization techniques are available at G.E.S.

- Double X-ray Diffraction (DDX).
- Two different set-up to perform electrical (Hall effect and resistivity) measurements in the temperature range: 4 K – 300 K (with high hydrostatic pressure and/or high magnetic field) and 300K – 1000 K.
- Micro-Infrared and Micro-Raman set-up
- LTPL (Low Temperature Photo-Luminescence) set-up.

Three last international research projects

• « SICOIN » (European Brite-Euram Contract,1997-2000, BRPR-CT96-0261) : Pressure Sensor based on 3C-SiCon Si or SOI.
• « HERO » (EURISMUS,1999-2003, HERO.n°EM.57) :Hall sensor based on SOI.

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**The Queen's University of Belfast**
Organization short name:	QUB
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Experience and expertise fields

QUB has 40 years experience in silicon device technology and simulation.
Experienced in producing novel SOI structures including the incorporation of tungsten silicide layers for minimising series resistance and increasing cross talk suppression.
Optimisation of SOI structures for RF ICs, MMICs and MEMS applications.
Modelling of semiconductor devices and circuits.

Facilities and Equipment

Complete silicon fabrication facility for 100-150 mm wafers.
Silicon wafer bonding with precision grinding and polishing.
Epitaxy for Si and SiGe, BESOI, SmartCut for SOI
e-beam lithography, double sided alignment, g-line stepper, thick PR
ICP deep trench etching.
CVD of tungsten, tungsten silicide, cobalt and copper.
Atomic layer deposition of HfO_2 and WN.
Silvaco simulation tools and Tanner layout CAD and mask making capability.
Electrical measurement systems for I-V and C-V characterisation.
High frequency measurements up to 110GHz on heated chuck.

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**S.O.I.TEC Silicon On Insulator Technologies**
Organization short name:	SOITEC
Internet homepage:	**www.soitec.com**

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Experience and expertise fields

Commercial spin-off of LETI, founded in March 1992 to produce very high-quality silicon-on-insulator (SOI) substrates. UNIBOND SOI wafers, introduced in July 1995, are manufactured using a patented technology called Smart Cut™. Process based on implantation technique and wafer bonding. Uses standard manufacturing equipment. 480 employees today. Annual turnover in the 80-100 MEuros range for the last fiscal years. SOITEC technology has been licensed to Shin Etsu Handotai and more recently to Siltronic for the manufacturing of SOI wafers.

Facilities and Equipment

Manufacturing / headquarters facility has been created in 1998 in Bernin, France, near Grenoble. The initial fab capacity has been increased (Bernin 2+R&D line) to a present level of more than 1,000,000 wafers start per year (equivalent eight-inch start wafers) and with an extension allowing 300mm capability. All equipments for Smart Cut SOI.
See www.soitec.com

Three last international research projects

MEDEA+ T206 : *CMOS RF*

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**TU Wien – Institut fuer Mikroelektronik**
Organization short name:	TUW-IME
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Experience and expertise fields

Semiconductor device and process modeling, development of TCAD tools (MINIMOS, MINIMOS-NT, PROMIS, SAP, SIMON, VMC) and a TCAD framework (SIESTA), classical transport (drift-diffusion, energy transport, six-moments of the Boltzmann equation, full-band Monte Carlo simulation) and quantum transport (Wigner equation, tunnelling models, carbon nanotube simulation).

Facilities and Equipment

The heart of the Institute´s computing infrastructure is an IBM server cluster block.
The cluster consists of four IBM p655 server nodes based on the 64 Bit Power 4+ Processor architecture. The cluster provides 192 GB total amount of RAM and 2 TB total disk space. The server nodes and storage system are linked by a Gigabit Ethernet. In addtion, shared computing is performed the Institute´s network. Each personal workstation is integrated in a Linux cluster and can be controlled remotely for performing compilation and simulation tasks.

Three last international research projects

IST-NANOTCAD
IST-MAGIC_FEAT
IST-MULSIC

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Universitat Autònoma de Barcelona**
Organization short name:	UAB
Internet homepage:	**www.uab.es**

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Experience and expertise fields

(i) Simulation, modelling and reliability of sub-100 nm MOSFETs: conventional MOSFETs, multiple-gate MOSFETs, silicon nanowire transistors.

(ii) Analysis of the dielectric breakdown of gate insulator in MOS devices under circuit operation conditions and its effect in the performance of devices and circuits.

Facilities and Equipment

(i) ISE-TCAD simulator
(ii) Electron devices electrical characterization system.
(iii) Conductive Atomic Force Microscope.

Three last international research projects

"Nanostructure fabrication by controlled deposition of atoms (NANOFAB)".
TMR Project ERBFMRX CT97-0129.

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Universita` degli Studi di Udine**
Organization short name:	UNIUD
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Experience and expertise fields

Modelling of semiconductor devices with emphasis on Full band structure calculations and Full band Monte Carlo transport.
Techniques for free and quantized electron gases.
Dc, ac, rf (20 GHz), time domain and pulsed characterization of semiconductor devices with emphasis on carrier transport, hot carrier effects, ultra-low currents.
Spectrally resolved characterization of Electro-luminescence with single photon counting techniques.

Facilities and Equipment

Commercial (ISE) and in house developed device simulators including:
1) general purpose self-consistent Monte Carlo transport code for free electron gas (3d in k-space, 2d in rspace, bulk and SOI MOSFET) in Si and SiO2 featuring quantum corrections for charge displacement from interfaces, substrate current and gate current and anode hole injection calculation, photon emission calculation.
2) general purpose Schroedinger Poisson solver in the effective mass approximation for multi-dielectric gate stacks featuring both electron and hole quantization and tunnelling gate current calculation.
3) general purpose self-consistent Monte Carlo transport code for quantized electron gas (2d in kspace, 2d in r-space, bulk and SOI MOSFET).
4) Complete dc, ac and rf (20GHz) and time domain characterization of semiconductor devices, on wafer (8") in the -65 – 200 degree C temperature range.
77K characterization of packaged devices.

Three last international research projects

UE - ULIS working Group on ULtimate Integration of Silicon.
UE - NESTOR project on 25nm Double Gate SOI Transistors (IST-2001-37114).
UE - SINANO Network of Excellence on Silicon Nanotechnology.

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Politecnico di Torino**
Organization short name:	Polito
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Experience and expertise fields

Design of digital Application Specific Integrated Circuits (ASIC) in CMOS Bulk and SOI; Low-power SOI SRAM design; SOI DTMOS and other body-biasing schemes; High-speed SOI domino logic; Modelling of SOI behaviour in digital circuits (Partially and Fully Depleted); Performance trend predictions for future SOI and Bulk CMOS technologies.

Facilities and Equipment

SUN Solaris and PC Workstations fully equipped for ASIC design with up-to-date EDA tools (front-end to back-end: Mentor, Synopsys, Hspice, Eldo, Cadende) and design-kits of CMOS Bulk and SOI technologies;
High-end Xilinx FPGA boards for prototyping;
Testing machine for packaged chips;
High-speed digital oscilloscopes;

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Universitat Rovira i Virgili**
Organization short name:	URV
Internet homepage:	**http://www.urv.es**

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Other Senior Researchers

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Prof. Roger Cabré, rcabre@etse.urv.es

Experience and expertise fields

Our main research activities are the simulation, characterisation and modelling of advanced semiconductor devices, in particular nano-crystalline Si and organic Thin-Film Transistors and thin-film SOI MOSFETs. The group is currently working in the development of compact models for nanoscale SOI MOS devices, such as Double Gate and Surrounding Gate MOSFETs.

Facilities and Equipment

Characterisation

Prober Karl Süss PM5. Impedance Analyzer HP4192A (C-f)
Capacimeter HP4280A (C-V, C-t). Electrometer Keithley 619
Temperature controller (20 ^{o}C - 200 ^{o}C). Parametric analyzer HP4145B (I-V)
ARC SpectraPro-150

Modelling & Simulation

Synopsis package. NANOMOS simulator
AIM-Spice source code for device model development

Three last international research projects

PROJECT: "Characterisation and Modelling of SiC Thin Film Transistors" (ACI2002-34), 2003-2004 (Bilateral Research Action with CINVESTAV, Mexico City)
PROJECT: "Silicon Nanodevices" (SINANO), Network of Excellence, 2004-2006
PROJECT: "EUROSOI", Coordination Action (Thematic Network), 2004-2005

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**University of Salamanca**
Organization short name:	USAL
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Other Senior Researchers

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Experience and expertise fields

The Silicon Electronics Group at USAL has a 8 year experience in the field of modeling and simulation of semiconductor materials and electronic devices, mainly using Monte Carlo techniques. In particular, Silicon, SiGe alloys and strained Si, one-port (Schottky, p-n Si and Si/Ge heterostructure diodes) and two-port (BJT and HBTs, MOSFETs and SOIs) electronic devices have been the subject of investigation. The group is mainly specialized in the analysis of noise in semiconductor devices, including the modelling of experimental submicron SOI transistors.

Facilities and Equipment

In the USAL we have all the hardware and software ingredients needed for the development of simulation tools of high-frequency noise in real devices:

- A 30-way cluster with PIV CPUs at 2.4 GHz,
- Two 2-way workstations with Alpha processors at 833 MHz

In-house Monte Carlo code for materials, 1D, and 2D Silicon bipolar and FET simulation.

Three last international research projects

METAMOS (Ref. 016677) Metallic Source / Drain Architecture for Advanced MOS Technology: European Project

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**UPPSALA UNIVERSITET**
Organization short name:	UU
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Other Senior Researchers

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Experience and expertise fields

- Development and manufacturing of devices on SOI and bulk materials
- Deposition and etching of thin film materials for microelectronics
- Piezoelectric devices on various advanced substrates
- Silicon RF devices
- Device modelling and simulation

Facilities and Equipment

The 2000 m^2 clean-room at The Ångström Laboratory in UU has a full process capability for device manufacturing. The laboratory is fully compatible with 3" and 4", and for many process modules also for 6". The Ångström Laboratory has also the most advanced and complete material analysis laboratory in northern Europe, with several state-of-the-art equipments. We are also in possession of a well-equipped electrical measurement laboratory, including software for high-frequency modeling and parameter extraction.

Three last international research projects

EU: SINANO
EU: TARGET
EU: MEDCOM

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**University of Twente**
Organization short name:	UT
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Other Senior Researchers:

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Experience and expertise fields

Our Semiconductor Components laboratory has an old tradition of performing research on technology development, reliability and device modelling of silicon-integrated components and circuits, particularly CMOS circuits. We have a strong link with the integrated circuit design laboratory of our faculty in which design research is done for RF CMOS circuits.

Facilities and Equipment

The group is co-owner of the versatile MESA+ Clean room, see http://www.mesaplus.utwente.nl/facilities/cleanroom.doc/, which enables manufacturing of MOS and bipolar devices as well as MEMS and integrated optics, to name a few. The group further exploits the MESA Test Center, http://icejive.ewi.utwente.nl/mtc/, for electrical characterization of test structures, devices and circuits.

Last international research projects

The research group last participated in the EC-funded SAFEGAS project, 2000-2003; see http://www.nmrc.ie/projects/safegas/ .
Prof. Schmitz (as a Philips Research employee) last participated in the EC-funded project ARTEMIS 2002-2004; see http://www.imec.be/artemis/

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Technical Research Centre of Finland**
Organization short name:	VTT
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Other Senior Researchers

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Experience and expertise fields

- Thick SOI materials by direct bonding for MEMS applications.
- Thin SOI materials by hydrogen implantation and cold cut.
- Transport measurement in thin SOI.
- Velocity modulation transistors.
- SOI based MEMS and SOI based integrated optical waveguides.

Facilities and Equipment

- 1800 m^2 clean room (class 10-1000).
- 0.6 µm polySi gate CMOS, 0.8 µm Mo gate CMOS with all associated equipment.
- Backend processing equipment for wafer bumping, dicing and assembly.
- Equipment for direct wafer bonding, backgrinding and chemical-mechanical planarization.
- Equipment for physical characterization: SEM/EDX, RBS, AFM, SAM.
- Wafer probing up to 110 GHz.
- Low-temperature transport measurements down to 300 mK and upto 11 Tesla.
- Mentor Graphics / Cadence design software.
- Spice, APLAC simulation tools.

Three last international research projects

EU-IST projects:
NEAR, EXTRA, PHAT

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Politechnika Warszawska (Warsaw University of Technology)**
Organization short name:	WUT
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Lidia Łukasiak, lukasiak@imio.pw.edu.pl
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Experience and expertise fields

Processing: Ultrathin oxide layers fabrication by thermal oxidation, plasma oxidation and PECVD methods. Ultrathin oxynitride and nitride (PECVD) layers fabrication. Low thermal budget technology of test structures fabrication (<400ºC).
Modeling: Simulation of the bulk MOS, SOI and Double Gate SOI structures, including quantum-mechanical effecs: Electrostatics. Scattering mechanisms and mobility of carriers (RTA approach). Drain current. Tunnel currents. Capacitances. Simulation of I-V characteristics of the silicon resonant tunneling devices.
Characterization: Analysis of C-V curves: tox, Nsub, UFB, Qeff, Dit, etc.. Analysis of MOSFET I-V curves: UT, gm, Rsd, Leff, meff, etc.. Analysis of MOSCAP I-V curves: UBR, tbd, Qbd. Analysis of charge pumping current: UT, UFB,Dit_av, Dit(E).

Facilities and Equipment

Processing: Class 1000/100 clean-room equipped with equipment allowing basic MOS devices fabrication; Effective CD > 1um; 2" wafers for the whole process flow; 4" wafers for plasma processing (plasma oxidation, PECVD and RIE).
Characterization: HF and LF CV measurement equipment, I-V measurement equipment, charge pumping measurement equipment (2- and 3-level).
Simulation: Unique software developed by the research team.

Three last international research projects

SiNANO - Silicon-based Nanodevices – NoE of 6 FP.

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**X-FAB Semiconductor Foundries**
Organization short name:	X-FAB
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Other Senior Researchers

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Experience and expertise fields

- High Voltage CMOS/SOI and BICMOS technologies including Flash and EEPROM
- High temperature(250°C), high voltage electronics (100V) on SOI
- MEMS processes for pressure and inertial sensors, for infrared sensors and BioMEMS
- Primitive device layout and characterisation

Facilities and Equipment

Facilities:
X-FAB AG, Erfurt, Germany
X-FAB UK, Plymouth, England
X-FAB Texas, Lubbock, USA
Equipment:
3 fab's for wafers up to 8 inch wafers and 0.35µm structure size.
Wafer level characterisation equipment for temperatures up to 300°C on wafer level.

Three last international research projects

TERMIS - high temperature / high voltage mixed signal SOI.
ATHIS - advanced techniques for high temperature on chip.
MANGHO – SOI wafer based angular rate sensors.

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**ARCES, Alma Mater Studiorum, Università di Bologna**
Organization short name:	ARCES
Internet homepage:	**www.arces.unibo.it**

Contact person			
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Other Senior Researchers

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Massimo Rudan, mrudan@deis.unibo.it
Susanna Reggiani, sreggiani@deis.unibo.it
Claudio Fiegna, cfiegna@arces.unibo.it

Experience and expertise fields

Physics-based numerical simulation of advanced SOI MOSFETS and nanowire-channel Multi-Gate MOSFETs. Monte Carlo, Schrödinger-Poisson. Application of numerical simulation to the analysis of CMOS-SOI scaling.
Experience: Extraction of device parameters (mobility, multiplication factors, etc..) up to very high operating temperatures; Investigation of transport modeling in emerging or alternative nanoelectronic devices such as nanotubes and nanowire-channel MOSFETs. Efficient solution of the Boltzmann Transport equation using the spherical harmonic expansion method applied to nanoscale MOSFETs; Mobility modelling in ultra thin silicon layers.

Facilities and Equipment

10 PC-Linux for numerical simulation. PC-Linux cluster for high-performance calculation. Characterization of devices and circuits from DC to RF and characterization of MEMS. Equipment: Probe Station Cascade SUMMIT 11751 8; E5071B Agilent Technologies Network Analyzer; Semiconductor parameter analyzer HP 4156C with option 41501B; Optical profilometer Wyko NT 1100.
Software: ISE simulation Tools, Crystal98 simulation tool.

Three last international research projects

SINANO Network of Excellence IST 6th FP
IST-2001-38931 EU Project "High-Tree"
IST FP6 EU Project "MAESTRO"

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Name of the organisation	
Organization Legal name:	**The University of Glasgow**
Organization short name:	GLASGOW
Internet homepage:	**http://www.elec.gla.ac.uk/groups/dev_mod/**

Contact person				
Name:	*Asenov*		*Title:*	*Prof.*
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Other Senior Researchers

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Dr. A. Martinez, A.Martinez@elec.gla.ac.uk
Mr. A. Brown, A.Brown@elec.gla.ac.uk

Experience and expertise fields

Solid state and semiconductor physics. Solid state device physics. Quantum transport. Simulation based device design and analysis. Solid state device modelling and simulations. Drift diffusion, Monte Carlo and quantum simulation techniques. Compact model parameter extraction and statistical circuit simulation. Numerical methods and algorithms. Parallel algorithms. Simulation of intrinsic parameter fluctuations in nano-CMOS devices.

Facilities and Equipment

6. Hardware

- 40 processors IBM p640
- 32 processors SMP SGI Origin 300
- 30 processors SMP Sun Enterprise
- Suit of 25 Unix workstations
- 124 processors UNIX cluster (in procurement)

7. Software

In house 2D/3D Monte Carlo. Simulator for Si, Ssi, Ge and III-V devices.
In house 3D 'atomistic' drift-diffusion simulator with density gradient quantum corrections featuring random discrete dopants, interface roughness and LER
In house 2D/3D NEGF simulator (in development).
Full TCAD simulation suite from Synopsis

Full TCAD simulation suite from ISE.

Three last international research projects

IBM Shared University Research Grant "Intrinsic Fluctuations in Decanano Silicon Devices: Impact on Scaling, Device Architecture, and Circuit Performance"
SEMATECH "Advanced Gate Stack External Research"
EC SINANO NoE

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Institut fuer Mikroelektronik Stuttgart**
Organization short name:	IMS-Chips
Internet homepage:	**www.ims-chips.de**

Contact person					
Name:	*Appel*			*Title:*	*Dr.*
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Other Senior Researchers

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Dr. Jörg Butschke, butschke@ims-chips.de
Dr. Florian Letzkus, Letzkus@ims-chips.de

Experience and expertise fields

Wafer bonding, membrane etching, deep trench etching, epitaxy on porous silicon, buried silicide, stress engineering in SOI-film

Facilities and Equipment:

Suess Bond Aligner, STS Trench Etcher, KOH wet etching, e-beam direct writer, CMOS equipment

Three last international research projects

Hiperlogic (EC), Ion Projection Lithography (MEDEA), ISOSURF (BMBF), ILIAS (BMBF)

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Innovative Silicon**
Organization short name:	ISi
Internet homepage:	**http://www.innovativesilicon.com/**

Contact person			
Name:	*Fazan*	*Title:*	*CTO*
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Other Senior Researchers:

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Gregory Popoff, gpopoff@innovativesilicon.com
Mikhail Nagoga, mnagoga@innovativesilicon.com
Cedric Bassin, cbassin@innovativesilicon.com

Experience and expertise fields

Innovative Silicon, which was formed in 2002, is developing a novel, ultra-dense, semiconductor memory technology that was invented by its founders - Prof. Pierre Fazan and Dr. Serguei Okhonin in collaboration with the electronics laboratory of the Swiss Federal Institute of Technology of Lausanne (EPFL). Innovative Silicon is headquartered in the "Parc Scientifique" of EPFL in Lausanne, Switzerland.

Facilities and Equipment

All tools for circuit design, device and circuit testing.

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Kungl Tekniska Högskolan**
Organization short name:	KTH
Internet homepage:	**www.kth.se, www.ict.kth.se**

Contact person					
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Other Senior Researchers

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Prof Carl-Mikael Zetterling, bellman@imit.kth.se
Assoc. Prof Per-Erik Hellström, pere@imit.kth.se
Assoc. Prof Martin Domeij, martind@imit.kth.se
Research Assoc. Dr Gunnar Malm, malm@imit.kth.se
Assoc. Prof Nils Nordell, nordell@imit.kth.se

Experience and expertise fields

- Complete process line for 100 mm SOI MOSFETs
- Electrical device and materials characterisation
- Device simulation and modelling
- MEMS structures in SOI
- Nanoscaled Si/SiGe devices on SOI

Facilities and Equipment

The cleanroom facility at KTH is named the Electrum Laboratory (ELAB)and has a 1300 sqm cleanroom area. A decananometer silicon process line is serving the research projects. ELAB has a 100 mm wafer capability with some equipment having 200 mm wafer size. Among these an ASM2000 Si/SiGe epitaxy and Reactive etching can be mentioned. ELAB is equipped with both I-line and G-line stepper lithography and newly installed imprint lithography. In addition a MEMS fabrication line on bulk Si or SOI is available. ELAB also offers a III-V epitaxy for InP and GaAs based semiconductors, possible to integrate with novel silicon devices.

Three last international research projects

IST-5th framework SIGMOS
IST 6th framework SINANO
IST 6th Cadres

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**University of Southampton**
Organization short name:	SOTON
Internet homepage:	**http://www.soton.ac.uk**

Contact person				
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Other Senior Researchers

Dr. Kees de Groot, chdg@ecs.soton.ac.uk
Dr. Darren Bagnall, dmb@ecs.soton.ac.uk

Experience and expertise fields

Technology for the fabrication of SiGe HBTs on Silicon-On-Insulator substrates (SiGe HBTs on SOI). Expertise includes technology, device physics and epitaxy techniques compatible with SiGe HBTs on SOI.

Facilities and Equipment

Fully equipped clean room, and device characterisation facilities.

Three last international research projects

Framework 6 SINANO project
Framework 5 SIGMOS project
Consultancy for Sarnoff Corp. New Jersey

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**Siltronic AG**
Organization short name:	Siltronic
Internet homepage:	**www.siltronic.com**

Contact person					
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Postal Address	*Johannes-Hess-Strasse 24, 84489 Burghausen, Germany*				

Other Senior Researchers

Dr. Atsuki Matsumura
Dr. Peter Storck

Experience and expertise fields

Siltronic is a global leader in the market for ultra-pure silicon wafers and the partner of numerous leading chip manufacturers. Siltronic develops and manufactures wafers with diameters of up to 300 mm at production sites in Europe, Asia, Japan and the United States. Silicon wafers form the heart of modern micro -and nanoelectronics- for computers, mobile telephones, Internet, DVD players, flat-panel displays, navigation systems, airbags, computer tomography machines, aircraft control systems and many other applications.

Facilities and Equipment

SIMOX, strained Silicon

Three last international research projects

German funded BMBF "TeSiN" project
MEDEA+ "Silonis.

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**SOISIC SA – Silicon On Insulator and Integrated Circuits**
Organization short name:	SOISIC
Internet homepage:	**www.soisic.com**

Contact person					
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Other Senior Researchers

Remy POTTIER Business Development Manager, remy.pottier@soisic.com

Experience and expertise fields

SOISIC is positioned as provider of hard IP cores for the design and manufacturing of integrated circuits on SOI/CMOS technologies. SOISIC offer includes standard and I/O cells libraries, ROM and RAM compilers, ASIC design and RF design. SOISIC benefits from more than 15 years of R&D in the SOI field. SOISIC design teams are experienced in both digital and analog/RF design.

Facilities and Equipment

SOISIC has two design Center one in Grenoble, one in Paris.

Three last international research projects

MEDEA+ T206
MEDEA+ WITNESS

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**STMicrolectronics**
Organization short name:	ST
Internet homepage:	**www.st.com**

Contact person					
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Sebastien Heandler, sebastien.heandler@st.com
Gilles Gouget, gilles.gouget@st.com

Experience and expertise fields

Digital SOI design for low-power applications:

- Standard Cells & IOs Libraries
- Memories
- ESD protections
- SOI modelling

Facilities and Equipment

STMicroelectronics - Central R&D

Three last international research projects

- European Projects: Aldebaran, SATURN, MEDEA T206

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**STMicroelectronics Central R&D**
Organization short name:	ST
Internet homepage:	**www.st.com**

Contact person			
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Other Senior Researchers

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Gianesello Frederic, frederic.gianesello@st.com

Experience and expertise fields

RF/analog design and device modeling in SOI partially depleted technologies.

Facilities and Equipment

Availability of PD SOI process for the 0.13um , 90nm and 65nm technology nodes.

Three last international research projects

MEDEA+

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**STMicroelectronics**
Organization short name:	ST
Internet homepage:	**www.st.com**

Contact person					
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Gilles Gouget, Gilles.gouget@st.com
Patrick Scheer, Patrick.scheer@st.com
Philippe Flatresse, Philippe.flatresse@st.com
Carlo Tinella, Carlo.tinella@st.com
Olivier Richard, Olivier-cro.richard@st.com

Experience and expertise fields

At ST level:
PD and FD SOI process modules and assembly, active and passive devices DC, AC, RF characterisation and modelling, circuits design for Low Power/Low Voltage SoC (digital, mixed and RF)
Personnal: CMOS (bulk, SOS, SOI) and BICMOS circuits design, test
process-devices characterisation-modeling
RF projects management (cmos, bicmos, soi)

Facilities and Equipment

All facilities and equipments for R&D and production for process generations till 32nm

Three last international research projects

IST SATURN SOI Advanced Technology for Ultra Rapid Networks (2000-2003)
MEDEA T204 Advanced Si Ge BICMOS Technologies for RF applications (2001-2002)
MEDEA+ T206 CMOS SOI for low Power logic and RF Wireless (2002-2005)

EUROSOI "Who is Who" Guide

Name of the organisation	
Organization Legal name:	**TRACIT TECHNOLOGIES SA,**
Organization short name:	
Internet homepage:	**www.tracit-tech.com**

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Other Senior Researchers

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Dr Michael FIEVRE, michael.fievre@tracit-tech.com
Dr Gwenaelle RUMEN, gwenaelle.rumen@tracit-tech.com

Experience and expertise fields

Tracit Technologies is a spin-off from the CEA-LETI, specialized in thin film transfer by molecular adhesion and mechanical and/or chemical thinning.
TRACIT Technologies is specialized in BSOI wafers, customized BSOI wafers and D-BSOI^{TM} wafers, and in the field of transfer of thin circuits onto different supports .

Facilities and Equipment

Clean-rooms with all the equipments to process BSOI wafers, to perform Direct Wafer Bonding (cleaning – annealing), chemical mechanical polishing, mechanical & chemical thinning.

Three last international research projects

- PICMOS (European Project 6th PCRD)

Section 3. SOI technology in the world

In the following table, in order to conclude the contents of this document, a list of companies and institutions that have been involved in one way or another with SOI technologies R&D or production activities is given. This list is formed with few of the most important ones; however we do not pretend to give an exhaustive list. The web URL is also given for each company. Search engines can be found within these pages for internal contents where SOI activities and products can be located.

Company or Institution	Web information
Agilent	www.agilent.com
AMD	www.amd.com
AmSem	www.americansemi.com
Analog Devices	www.analog.com
Atmel	www.atmel.com
Applied Materials	http://www.appliedmaterials.com/
ARM	http://www.arm.com/
Berkeley	http://www.berkeley.edu/
Cadence Design Systems.	www.cadence.com
Canon	www.canon.com
Ericsson	www.ericsson.com
First Sensor Tech.	www.first-sensor.com
Freescale	www.freescale.com
Fuji	www.fujifilm.com
Global Foundries	http://www.globalfoundries.com/
Hitachi	www.hitachi.co.jp
Honeywell	www.ssec.honeywell.com
IBIS Technology Corp.	www.ibis.com
IBM	www.ibm.con
IEMN	www.iemn.univ-lille1.fr
Infineon AG	www.infineon.com
Infotech	http://www.infotech-enterprises.com/
Innovative Silicon Inc.	http://www.innovativesilicon.com/
Intel	www.intel.com
ISE Integrated Systems Engineering	www.ise.ch
Kanazawa Inst Tech	http://www.kanazawa-it.ac.jp/ekit/
KLA Tencor	http://www.kla-tencor.com/
Kulite	www.kulite.com
LAM Research	http://www.lamrc.com/
Lockheed	www.lockheedmartin.com
MAGMA	http://www.magma-da.com/
Melco	www.melco.com
MEMC	http://www.memc.com/

Mentor	www.mentor.com
Mitsubishi	www.mitsubishi.com
Motorota	www.motorola.com
Nec	www.nec.com
Nokia	www.nokia.com
NTT	www.ntt.com
NVIDIA	http://www.nvidia.com/
OKI	www.oki.com
Okmetic	www.okmetic.com
Peregrine	www.peregrine-semi.com
Philips	www.philips.com
Prof. J.Fossum's Group University of Florida, Gainesville, Florida, USA	www.ece.ufl.edu/facultystaff/fossum.html
Renesas	http://www.renesas.com/
Ritsumeikan	http://www.ritsumei.ac.jp
Samsung	www.samsung.com
Seiko	www.seiko.co.jp
Semico	http://www.semico.com/
Sharp	www.sharp.com
ShinEtsu	http://www.sehe.com/
SiGen corporation	www.sigen.com
Silvaco	www.silvaco.com
SIMGUI	www.simgui.com.cn
Stanford	http://www.stanford.edu/
Sony	www.sony.com
ST	http://www.st.com/
Sumco	www.sumcosi.com
Synopsys, Inc.	www.synopsys.com
Toshiba	www.toshiba.com
UMC	http://www.umc.com/
UMICORE	www.umicore.com
Varian Sem. Equip.	http://www.vsea.com/
Zarlink Semiconductor	http://www.zarlink.com/