INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

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D5.4: First version of the user manual and reference manual of the Research-dedicated Design Kit (RDK)

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Project coordinator organisation: University of Granada, Spain Rev.1

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Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

To be able to address new circuit design opportunities and new applications on SOI, it is essential to have access to a Design Kit and its associated documentation and user's manual. Through other founded projects, LETI is now elaborating a research dedicated design kit for its FDSOI technology. This Research Process Design kit (PDK) is now available (for its first version). Design rules (based on 65nm Back-end process), typical SPICE model parameters, Design rules Control (DRC) and Layout Versus Schematic (LVS) files have been developed and incorporated into this RDK.

The goal of the task 5.2 is to elaborate the user, reference manuals, and documentation necessary to promote, explain, and spread the use of the RDK to European companies. All these informations have been included in a single document called "FDSOI PDK Reference manual ". The first version has been elaborated on April 22nd 2009 and is available since Month 18. This availability have been announced and reported during the 2009 April 24th review meeting (see some presented slides in Annex 1). Annex 2 contains the provided documentation.

This documentation contains the following informations:

- The configuration guide that helps for the installation of the PDK
- The architecture of the PDK
- The FDSOI technology package explaining the various contents of the PDK: design rules, transistor p-cells, SPICE model, parasitic extraction, DRC and LVS files, dummies generation
- The PDK tree explaining where the various files are located

With such documentation, EUROSOI+ partners are able to design FDSOI circuits with the provided LETI FDSOI technology.

Annex 1: Few presented Slides by CEA-LETI during the April 24th 2009 review meeting.

PDK structure overview

- **PDK architecture:**

```
<Install_Path>
    |-----bin/        (Binary directory)
    |-----cad/        (PDK infrastructure directory)
    |-----cdsuser/    (User setup directory)
    |-----doc/        (Document directory)
    `-----tech/       (Technology specific directory)
```

- **FTP external diffusion:**
  - Installation procedure,
  - Release notes,
  - **FDSOI PDK LETI Reference Manual**

- **CAD environment:**
  - Solaris 2.8
  - Linux RHEL4.0

Summary for the design kit

Already available Design Kits:

- FDSOI_45n_2M v3.2 (available since april 08)
  - Already delivered to CEA/DAM and Edimburgh University
- FDSOI_45n_2M v4.0 (=v3.2 with parasitics: Mid 08)
  - Available for circuit designers

Next steps:

- FDSOI45n_4M with 4 levels of Metals. Target: Mid 09
- Change BSIM SPICE model into PSP SOI model: Mid 09

Summary for the FDSOI platform

- Design Kit already available for designers
- Technology already available at LETI, with co-processing at ST
  - improved yield
  - raise the issue of access: no problem for R&D institutions, but no transferability to industrial third partners of results or infos on process (NDA required)
- MPW (Multi Project Wafers) for EUROSOI+ members access:
  - Cost per mm^2 under evaluation
  - Entry points:
    - Meeting with EUROPRACTICE in Sept 08 to discuss possible introduction into their offer (discussion ongoing)
    - Suggestion by ST to use CMP (TIMA in Grenoble) which already offer MPW access to their Bulk and SOI technologies (existing infrastructure to handle PI issues, no decision yet)
- In phase with what already scheduled in EUROSOI+ program

Annex 1: First version of the FDSOI PDK Reference manual elaborated on April 22nd 2009

FDSOI PDK LETI Reference Manual

Table of contents

1 Introduction

The purpose of this document is to give the end user an installation guide for the FDSOI Process Design Kit (PDK). It explains the PDK architecture and points out specific details of the FDSOI LETI information.

Section (2) “Configuration guide” contains installation instructions for the PDK administrator and user setup instructions. It describes how to setup the PDK in the customer design environment and basic checks that are necessary to work consistently with the PDK.

Section (3) “PDK architecture” gives an overview about the architecture of the PDK, reference libraries and the supported analog design flow.

Section (4) “FDSOI technology package information” gives detailed information about FDSOI technology; technology library, devices, Pcells , Eldo simulation models, and physical verification with Calibre.

Here is a list of recommended Cadence tools to be used with the PDK:

- ✓ Cadence : 5.10.41.500.4.72,
- ✓ Adms : 2006.2b (eldo v6.8_3.1),
- ✓ Calibre : 2006.4_35.37

Following platforms/operating systems are supported:

- ✓ Solaris 2.8
- ✓ Linux Red Hat Enterprise 4.0

2 Configuration guide

2.1) PDK installation instructions

For the first installation of the KIT, create a directory:
ex: mkdir <your path>/DKIT_FDSOI

Copy into this directory the next files:
- DK_LETI_FDSOI_<version>.tar.gz,
- pdk_leti_install,
- readme.

Change directory : cd /<your path>/DKIT_FDSOI

Change permission: chmod 555 ./pdk_leti_install

Execute the script: ./pdk_leti_install DK_LETI_FDSOI_<version>.tar.gz

After unpacking the PDK, following PDK base directory structure is visible. (See section (3) for more details about the complete PDK directory structure).
The PDK base structure:

```
<Install_Path>
        |-----bin/        (Binary directory)
        |-----cad/        (PDK infrastructure directory)
        |-----cdsuser/    (User setup template directory)
        |-----doc /       (Document directory)
        `-----tech/       (Technology directory)
```

2.2) PDK user setup

To setup the user UNIX environment some UNIX variables have to be set and some files have to be installed in the user directory. PDK “cdsuser” directory contains template files illustrating required setup:

Required UNIX variables:

- ✓ PDK_ROOT points to the installation directory of the PDK
- ✓ CDSDIR points to installation directory of Cadence Design Framework
- ✓ MGC_AMS_HOME points to installation directory of ADMS (Eldo)
- ✓ MGC_HOME points to the installation directory of Calibre
- ✓ PATH points to the bin directory
- ✓ CDS_Netlisting_Mode sets to Analog.

cdsuser directory structure:

```
<PDK_ROOT>
        `-----cdsuser/
                |-----.artist_states
                |-----.cdsinit
                |-----.simrc
                |-----cds.lib
                |-----cdsuser_file.tar
                `-----simulation
```

- ✓ User .artist_states directory, which will contain states of Analog Design Environment
- ✓ User .cdsinit file, which is just a call to $PDK_ROOT/cad/.cdsinit
- ✓ User cds.lib file includes just inclusions of $PDK_ROOT/tech/tools/dfII/tech.lib and analogLib for Eldo. The files define available libraries in the Library Manager
- ✓ User simulation directory, which will contain results simulations with Eldo
- ✓ cdsuser_file.tar tar file contains all files above:

At project startup, the user can execute the script *pdk_leti_install_user* ($PDK_ROOT/bin) which installs all these files.

$PDK_ROOT/cdsuser/cds.lib:

-- Library techno
SOFTINCLUDE $PDK_ROOT/tech/tools/dfII/tech.lib

-- AnalogLib for Eldo
SOFTINCLUDE $MGC_AMS_HOME/etc/cds/cds.lib

Content of the tech.lib file:

DEFINE DK_fdsoi45Lib $PDK_ROOT/tech/tools/dfII/cdb/DK_fdsoi45Lib

This file defines technology dependent library. This library are part of the PDK installation. Library is located in the $PDK_ROOT/tech/tools/dfII/cdb directory.

DK_fdsoi45Lib library contains the technology data (Devices, Pcell, Contacts)

Content of the cds.lib file of Eldo:

```
DEFINE  analogLib       $MGC_AMS_HOME/data/cdslib/510/analogLib
DEFINE  mgcLib          $MGC_AMS_HOME/data/cdslib/510/mgcLib
DEFINE  basic           $MGC_AMS_HOME/data/cdslib/510/basic
DEFINE  aamix           $MGC_AMS_HOME/examples/artist_link/cdslib/CDB/aamix
DEFINE  aatest          $MGC_AMS_HOME/examples/artist_link/cdslib/CDB/aatest
DEFINE  CommLib         $MGC_AMS_HOME/data/cdslib/CommLib
DEFINE  CommLibQS       $MGC_AMS_HOME/data/cdslib/CommLibQS
DEFINE  CommLibRF       $MGC_AMS_HOME/data/cdslib/CommLibRF
```

$PDK_ROOT/cad/.cdsinit:

This is the initialization file of the Cadence software. The environment is initialized in the following order:

- ✓ Load Artist Link Skill customisation located under $MGC_AMS_HOME/etc/cds/.cdsinit
- ✓ Load .cdsenv file located under $PDK_ROOT/cad
- ✓ Load of DFII Display Resource File (DRF) display.drf file located under $PDK_ROOT/tech/tools/dfII folder
- ✓ Set the default simulator in Analog Design Environment to EldoD and insert the Model Library file
- ✓ Variables declaration for Calibre DRC/LVS:

PDK_CALIBRE_LVS_DECK =$PDK_ROOT/tech/tools/calibre/fdsoi45.calibrelvs
PDK_CALIBRE_DRC_DECK =$PDK_ROOT/tech/tools/calibre/fdsoi45.calibredrc
PDK_CALIBRE_DUM_DECK =$PDK_ROOT/tech/tools/calibre/fdsoi45.calibredum
MGC_CALIBRE_LVS_RUNSET_FILE =$PDK_ROOT/tech/tools/calibre/fdsoi45.runsetlvs
MGC_CALIBRE_DRC_RUNSET_FILE =$PDK_ROOT/tech/tools/calibre/fdsoi45.runsetdrc
MGC_CALIBRE_DRC_RUNSET_LIST=$PDK_ROOT/tech/tools/calibre/fdsoi45.runsetfile
MGC_CALIBRE_DUM_SWITCH_FILE=$PDK_ROOT/tech/tools/calibre/calibreI_dum_switchdef

- ✓ Load Skill customization for Virtuoso Layout Environment:

BindKeys : $PDK_ROOT/tech/il/fdsoiBK.il
GuardRing : $PDK_ROOT/tech/il/fdsoiGR.il

3 The PDK architecture

3.1) PDK directory structure overview

The Process Design Kit (PDK) is standalone without any assumptions on the target design environment.

```
<Install_Path>
        |-----bin/        (Binary directory)
        |-----cad/        (PDK infrastructure directory)
        |-----cdsuser/    (User setup directory)
        |-----doc/        (Document directory)
        `-----tech/       (Technology specific directory)
```

The design kit is accessible with UNIX environment variable “PDK_ROOT” pointing to the PDK installation directory.

cdsuser directory contains the user setup template files. At project startup, the user must execute the script *pdk_leti_install_user* ($PDK_ROOT/bin) which installs all initialisation files.

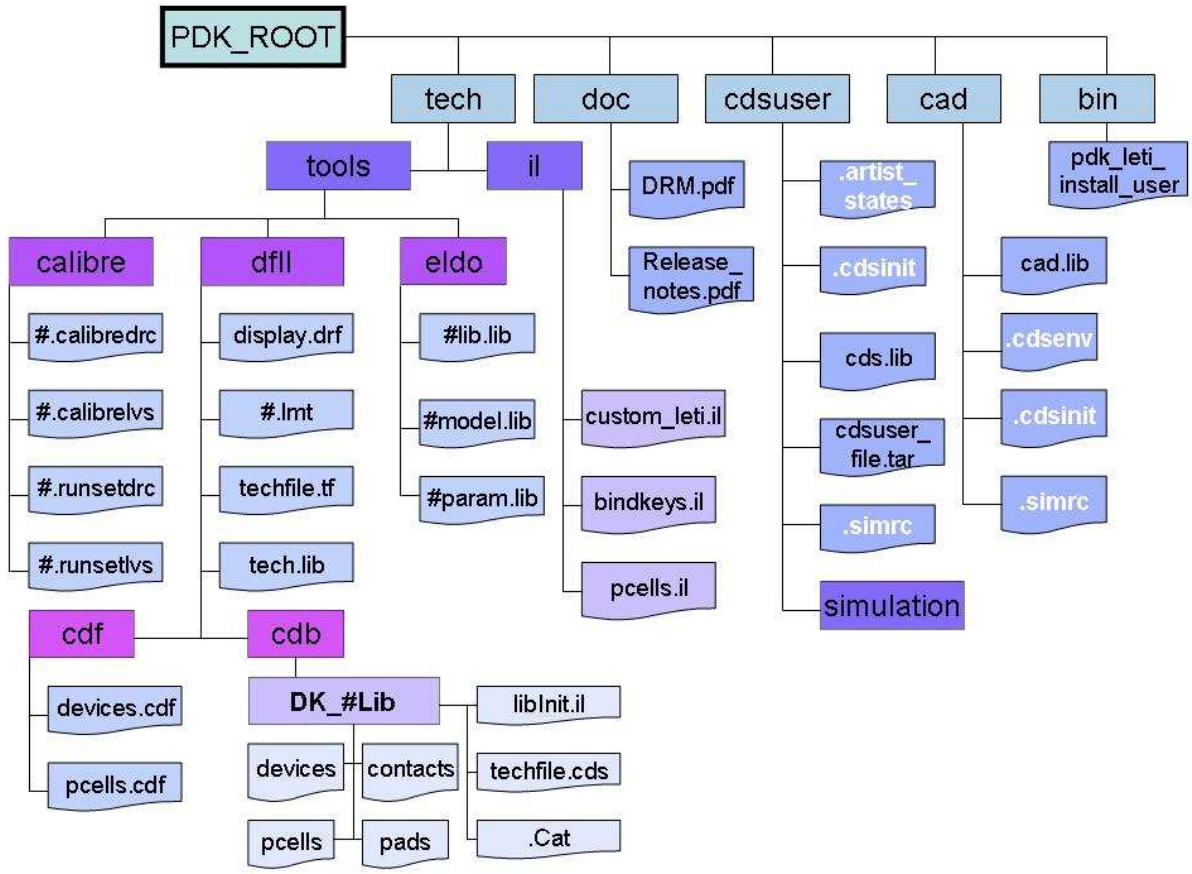
cad directory contains process technology independent data. Installed routines and data are only tool dependent and can be used for more than one technology.

tech directory contains process technology dependent data. It contains DFII libraries, tool specific data (Calibre files, Eldo models, etc), and technology specific SKILL routines.

doc directory contains documents of pdk: Design Rules Manual and Releases Notes.

3.2) Detailed directory structure

The entire PDK directory structure looks like the following:



3.3) Reference library

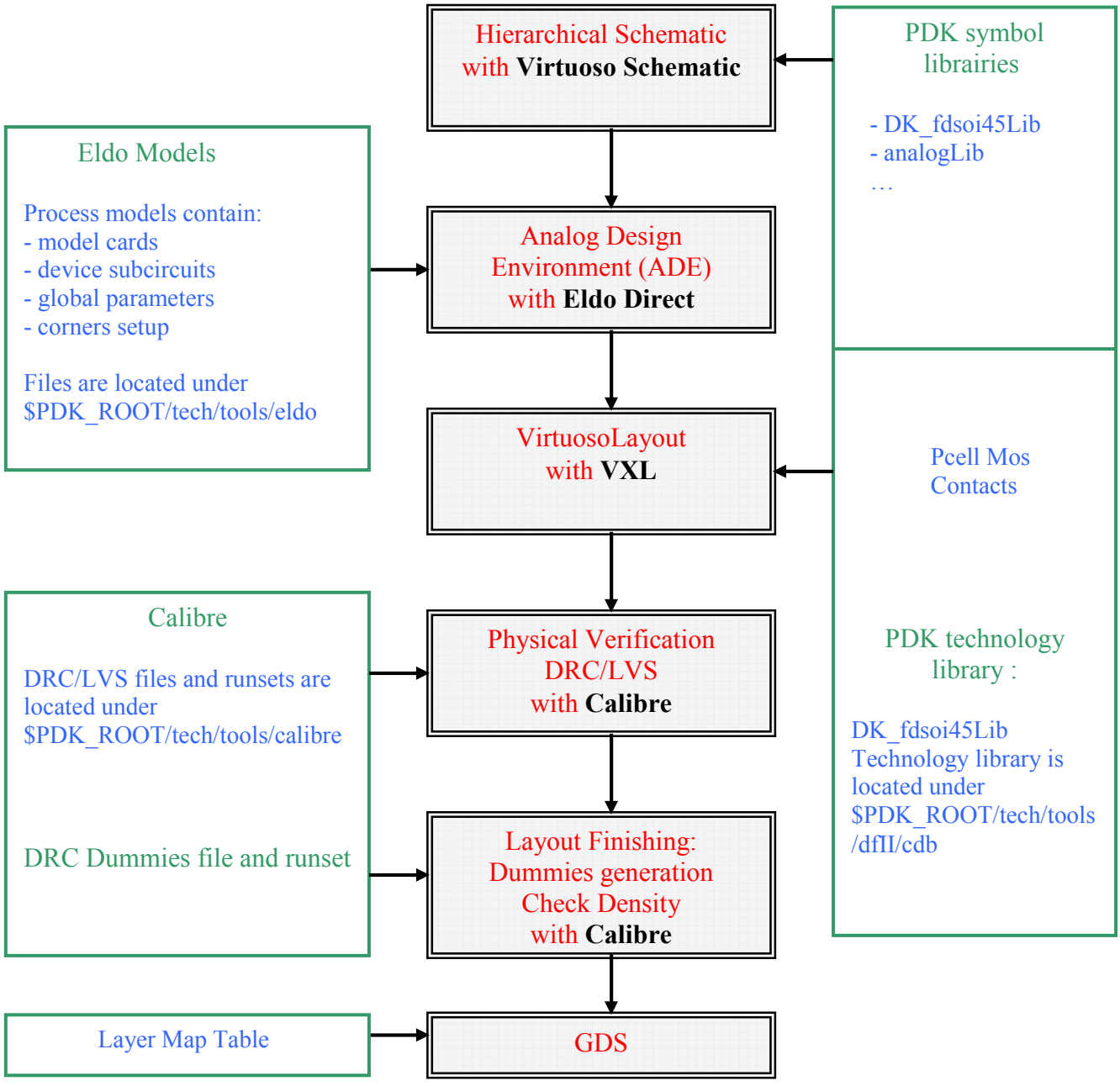
The PDK reference library *DK_fdsoi45Lib* contains the technology data:

- Devices symbol : nmosfd & pmosfd
- Pcell MOS :
  + pc_std_mos (standard pcell for multifinger mosfet)
  + pc_chnl_mos (standard pcell for multichannel mosfet)
  + pc_dnp_mos (Gated Diode pcell)
  + pc_body_mos (Body Contacted pcell)
  + pc_scribe_22pads (Scribe packaging pcell)
- Contacts

3.4) Analog design flow

The PDK is supposed to the standard Cadence analog design flow based on a unified integration within DFII. Such an analog flow contains the following tools:

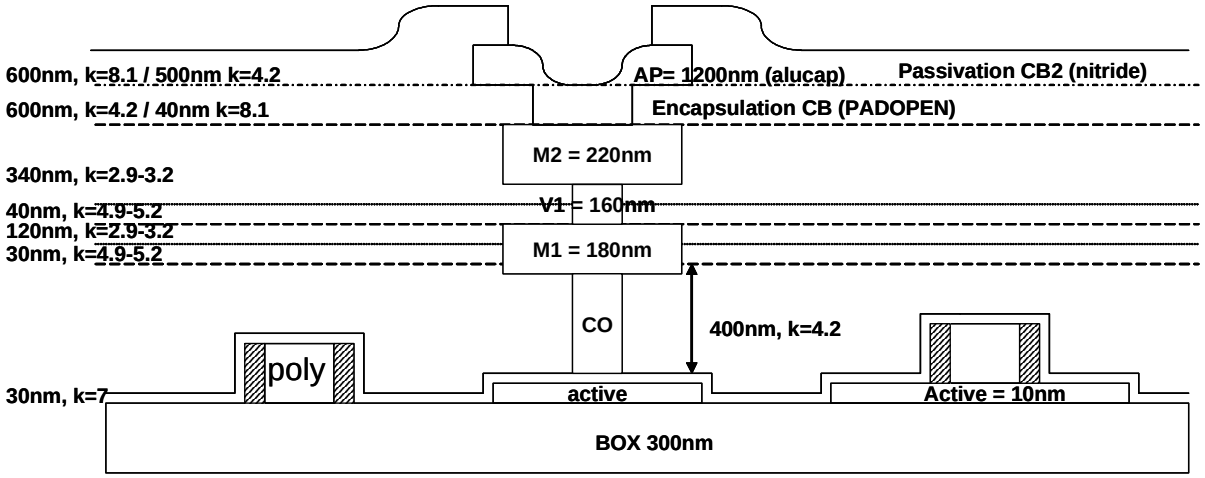
- Design Framework (5.1.41)
- Calibre (2006.4)
- Adms/Eldo (2006.2b)



4 FDSOI45 technology package information

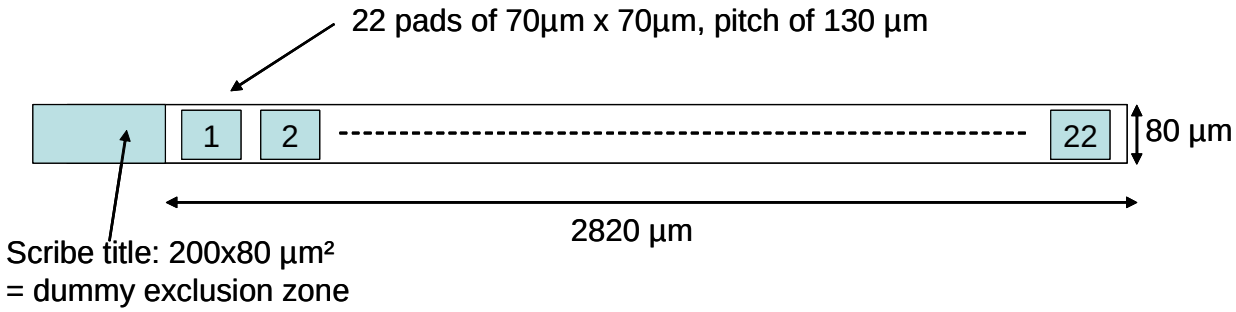
4.1) General definitions

FDSOI45 technology allows a design using 2 metal layers.
There are 2 Devices nmosfd & pmosfd. The "Back End" description is detailed below (for more information see "Design Rules Manual" under $PDK_ROOT/doc directory):



Back End description

The default pad structure is a metal1/metal2 stack, the layers of metal are connected together by via1.



Scribe 22 pads description

If required, pads can be designed also at the active or poly level, with the same pattern as the metal1 one. When this option is activated, a choice between active and poly levels is made for each pad of the 22 pads structure.
In that case, the designed device is connected to the pad at the lowest level (active or poly) and the connection is stacked to the metal1 level (no contact matrix in the pad).

List of layers

Level	Layer #
ACTIVE	02
VTN	60
VTP	43
GO2	06
POLY1	13
POLY2	42
DSN	16
DSP	17
CONTACT	19
METAL1	23
VIA1	25
METAL2	27
PADOPEN	40
ALUCAP	41
NITRIDE	31

LSW

Purpose:

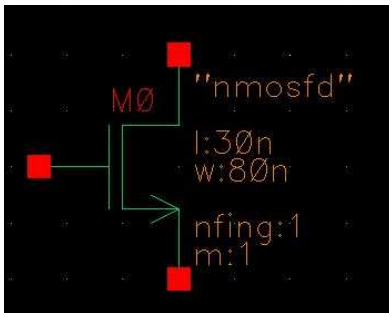
- dg : drawing
- pn : pin (for Calibre LVS)
- de : dummy exclude (exclude zone for ACTIVE/POLY and/or METAL)
- te : tile (dummy generation) → non visible by default in the LSW

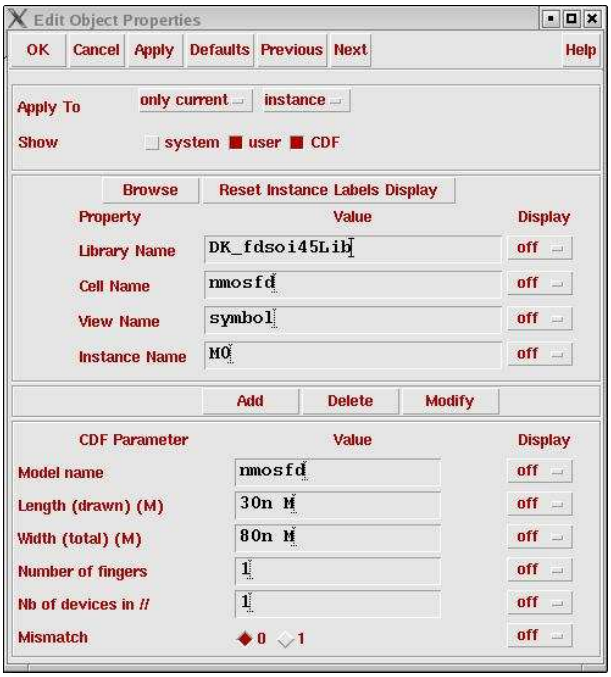
Note: Layer MARKER is used to define zone where no DRC will be execute.

4.2) FDSOI device models

There are 2 devices in the FDSOI45 technology. Each component is an associated model for Eldo simulator and a layout parameterised cell (Pcell Standard).

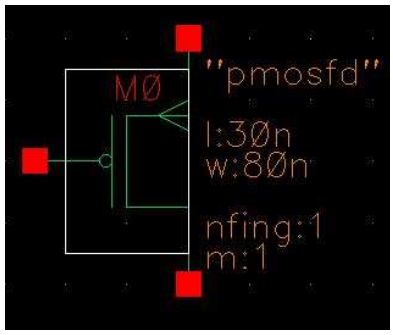
4.2.1) NMOSFD transistor

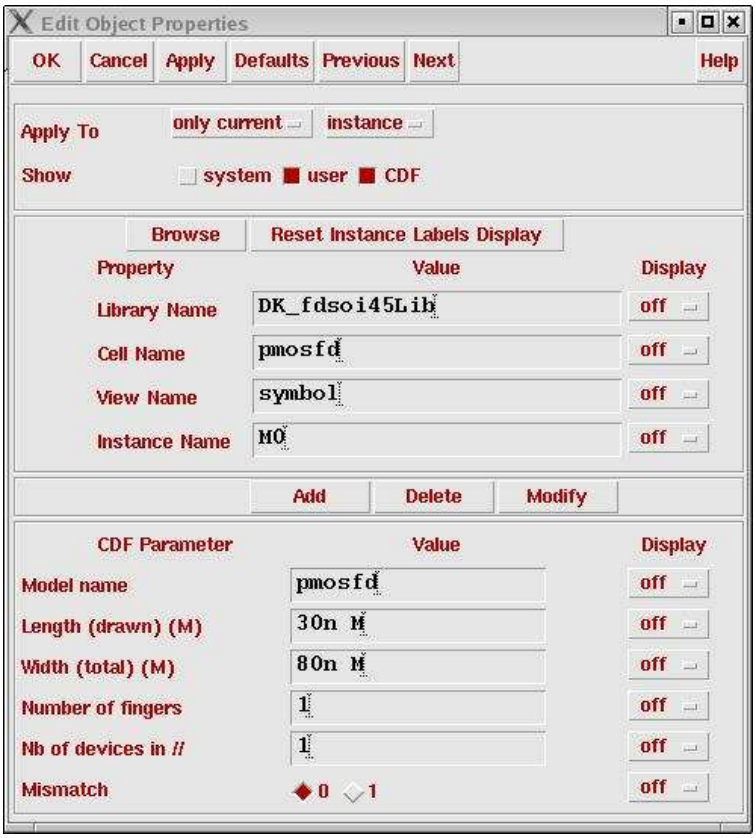




CDF parameter	Description	Default
Model name	Device model	nmosfd
Length (drawn) (M)	Length of the transistor (l)	30n
Width (total) (M)	Width of the transistor (w) This value corresponds to Weffective x Number of fingers	80n
Number of fingers	Number of fingers (nfing)	1
Nb of devices in //	Number of devices nmosfd in parallel (m)	1
Mismatch	Flag for mismatch simulation	0

4.2.2) PMOSFD transistor





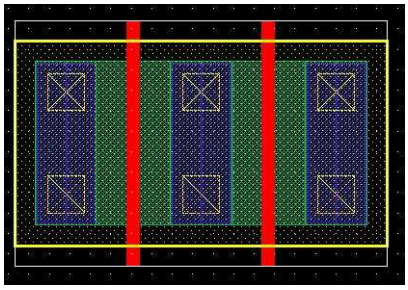
CDF parameter	Description	Default
Model name	Device model	pmosfd
Length (drawn) (M)	Length of the transistor (l)	30n
Width (total) (M)	Width of the transistor (w) This value corresponds to Weffective x Number of fingers	80n
Number of fingers	Number of fingers (nfing)	1
Nb of devices in //	Number of devices pmosfd in parallel (m)	1
Mismatch		0

4.3) FDSOI Pcell mos

All Pcells are accessibles through the Pcells category into the reference library DK_fdsoi45Lib.

4.3.1) Standard Pcell

The standard pcell “pc_std_mos” corresponds to standard multifinger mosfet. Only one pcell is used for the two devices (nmosfd & pmosfd).

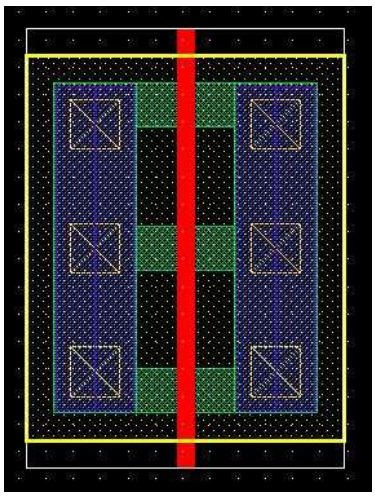


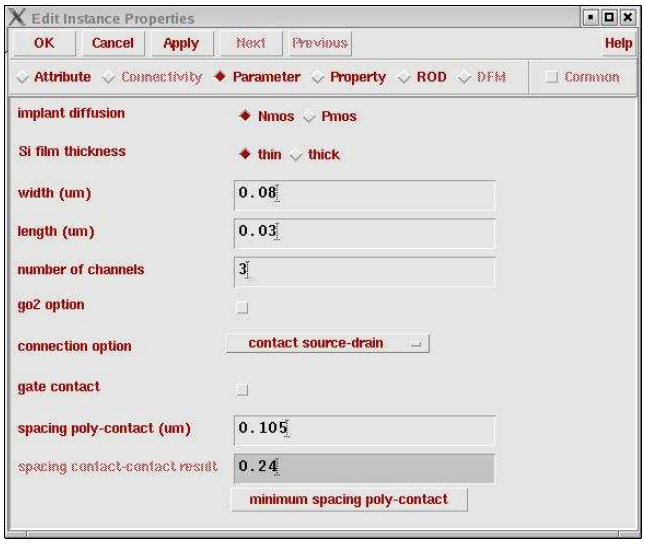
CDF parameter	Description	Default
implant diffusion	Choice of the diffusion type **Choices "Nmos" / "Pmos"** *Info: Nmos => DSN / Pmos => DSP*	Nmos
Si film thickness	Choice of the Si film thickness **choices "thin" / "thick"** *Info: thin <=> VTN / thick <=> VTP* *Choice of implant diffusion, generate the standard Si film thickness as default* *=> standard Nmos, "Nmos" and "thin"* *=> standard Pmos, "Pmos" and "thick"* *Important : For test structure, change the Si film thickness after the implant diffusion*	thin
width (um)	Width total of the transistor's active area minValue 0.08 minValue2 0.40 with go2	0.8µm
length (um)	Length of the transistor's poly area minValue 0.03 minValue2 0.15 with go2	0.03µm
number of fingers	Number of fingers **choices “int >0”**	1

	Info: the width value correspond to the W unit drawn multiplied by the number of fingers. Iif numbers of channels AND numbers of fingers are >1, they get the default value	
go2 option	Creation of the GO2 layer or not **choices "true if the option is on"** *Info: the minimum DRM value change with the GO2 layer*	nil
connection option	choice of contacts connection for source and drain "contact source-drain" => simple contacts for both "contact source only" => simple contacts for source only "contact drain only" => simple contacts for drain only "no contact source-drain" => no contact "double contact source-drain" => double contacts for both	
gate contact	Creation of a poly/metal1 path to connect the gate **choices "true if the option is on"** *Info: for several fingers, the gated are linked*	nil
spacing poly-contact (um)	Distance between the poly gate and the contact of source/drain area minValue 0.105 if U-shaped MOS / 0.055 otherwise (float) minValue2 0.110 with go2	0.105µm
spacing contact-contact result (um)	Not a parameter, it is an information Distance between the contact of source area and the contact of drain area value length + 2* spacing poly-contact	0.24µm
minimum spacing poly-contact	Not a parameter, it is a button to reset the spacing poly-contact value depending on your options	

4.3.2) Test structure Pcell

The pcell "pc_chnl_mos" is a multichannel mosfet. No device corresponds to this Pcell, because it's not LVS extracted..



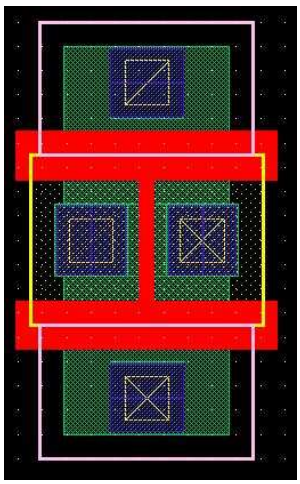


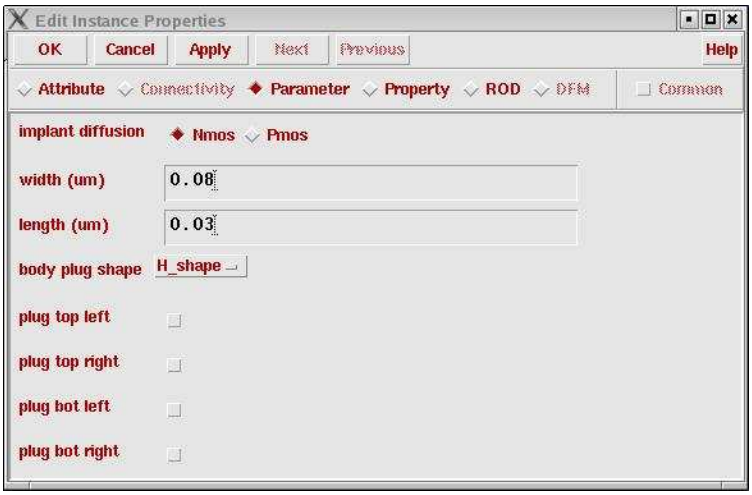
CDF parameter	Description	Default
implant diffusion	Choice of the diffusion type **choices "Nmos" / "Pmos"** *Info: Nmos => DSN / Pmos => DSP*	Nmos
Si film thickness	Choice of the Si film thickness **choices "thin" / "thick"** *Info: thin <=> VTN / thick <=> VTP* *Choice of implant diffusion, generate the standard Si film thickness as default* *=> standard Nmos, "Nmos" and "thin"* *=> standard Pmos, "Pmos" and "thick"* *Important : For test structure, change the Si film thickness after the implant diffusion*	thin
width (um)	Width total of the transistor's active area minValue 0.08 (float) minValue2 0.40 with go2	0.08µm
length (um)	Length of the transistor's poly area minValue 0.03 (float) minValue2 0.15 with go2	0.03µm
number of channels	Number of channels **choices "int >0"** *Info : the width value correspond to the W unit drawn for each channel*	1
go2 option	Creation of the GO2 layer or not **choices "true if the option is on"** *Info: the minimum DRM value change with the GO2 layer*	nil
connection option	Choice of contacts connection for source and drain "contact source-drain" => simple contacts for both "contact source only" => simple contacts for source "contact drain only" => simple contacts for drain "no contact source-drain" => no contact "double contact source-drain" => double contacts for both	
gate contact	Creation of a poly/metal1 path to connect the gate **choices "true if the option is on"** *Info: for several fingers, the gated are linked*	nil
spacing poly-contact (um)	Distance between the poly gate and the contact of source/drain area minValue 0.105 if U-shaped MOS / 0.055 otherwise (float) minValue2 0.110 with go2	0.105µm
spacing contact-contact result (um)	Not a parameter, it is an information Distance between the contact of source area and the contact of drain area value length + 2* spacing poly-contact	0.24µm

minimum spacing poly-contact	Not a parameter, it is a button to reset the spacing poly-contact value depending on your options	

4.3.3) Body contacted MOSFET Pcell

Pcell “pc_body_mos” is used for the Body contacted MOSFET. No device corresponds to this Pcell.

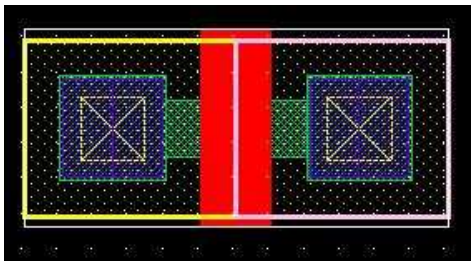


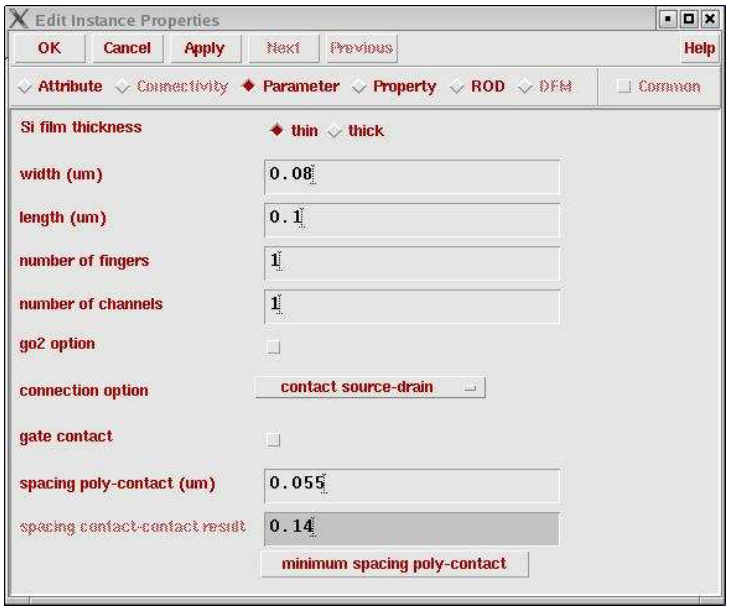


CDF parameter	Description	Default
implant diffusion	Choice of the diffusion type **choices "Nmos" / "Pmos"** *Info: Nmos => DSN / Pmos => DSP*	Nmos
width (um)	Width total of the transistor's active area minValue 0.08 (float) minValue2 0.40 with go2	0.08µm
length (um)	Length of the transistor's poly area minValue 0.03 (float) minValue2 0.15 with go2	0.03µm
body plug shape	Adaptation of the poly gate shape **choices "H_shape" / "T_shape"**	H_shape
plug top left	Creation of a poly/metal1 plug to connect the top gate on left **choices “true if the option is on”** *Iinfo: if T_shape => top connections are not available*	nil
plug top rigth	Creation of a poly/metal1 plug to connect the top gate on rigth **choices “true if the option is on”** *Iinfo if T_shape => top connections are not available*	nil
plug bottom left	Creation of a poly/metal1 plug to connect the bottom gate on left **choices “true if the option is on”**	nil
plug bottom rigth	Creation of a poly/metal1 plug to connect the bottom gate on rigth **choices “true if the option is on”**	nil

4.3.4) Gated diodes Pcell

Pcell “pc_dnp_mos” is used for the Gated diode. No device corresponds to this Pcell.



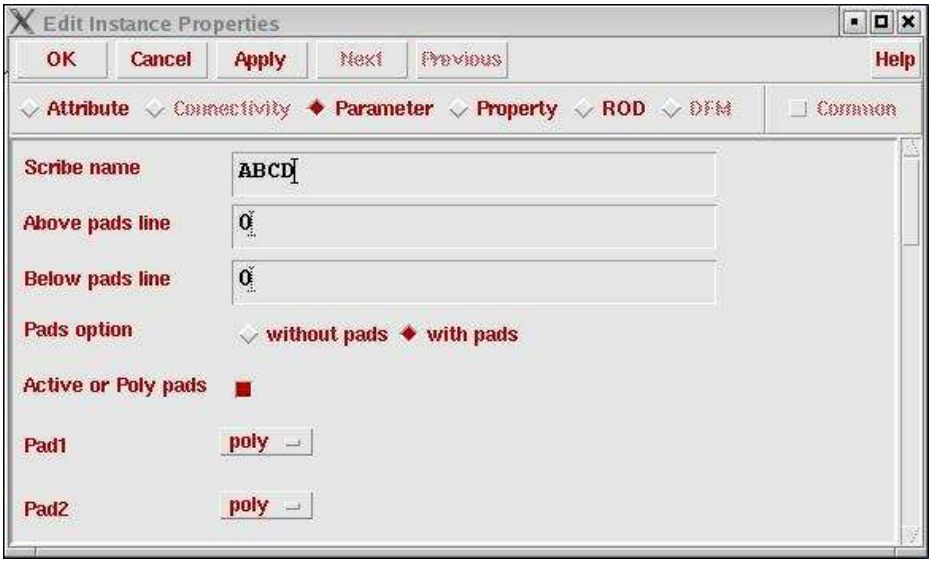


CDF parameter	Description	Default
Si film thickness	Choice of the Si film thickness **choices "thin" / "thick"** *Info: thin <=> VTN / thick <=> VTP*	thin
width (um)	Width total of the transistor's active area minValue 0.08 (float) minValue2 0.40 with go2	0.08µm
length (um)	Length of the transistor's poly area minValue 0.03 (float) minValue2 0.15 with go2	0.03µm
number of fingers	Number of fingers **choices “int >0”** *Info: the width value correspond to the W unit drawn multiplied by the number of fingers. If numbers of channels AND numbers of fingers are >1, they get the default value*	1
number of channels	Number of channels **choices “int >0”** *Info: the width value correspond to the W unit drawn for each channel. If numbers of channels AND numbers of fingers are >1, they get the default value*	1
go2 option	Creation of the GO2 layer or not **choices “true if the option is on”** *Info: the minimum DRM value change with the GO2 layer*	nil

connection option	Choice of contacts connection for source and drain "contact source-drain" => simple contacts for both "contact source only" => simple contacts for source "contact drain only" => simple contacts for drain "no contact source-drain" => no contact "double contact source-drain" => double contacts for both	
gate contact	Creation of a poly/metal1 path to connect the gate **choices** **"true if the option is on"** *Info: for several fingers, the gated are linked*	nil
spacing poly-contact (um)	Distance between the poly gate and the contact of source/drain area minValue 0.105 if U-shaped MOS / 0.055 otherwise (float) minValue2 0.110 with go2	0.055µm
spacing contact-contact result (um)	Not a parameter, it is an information Distance between the contact of source area and the contact of drain area value length + 2* spacing poly-contact	0.14µm
minimum spacing poly-contact	Not a parameter, it is a button to reset the spacing poly-contact value depending on your options	

4.3.5) Scribe 22 pads Pcell

Pcell "pc_scribe_22pads is the Scribe 22 pads. No device corresponds to this Pcell.

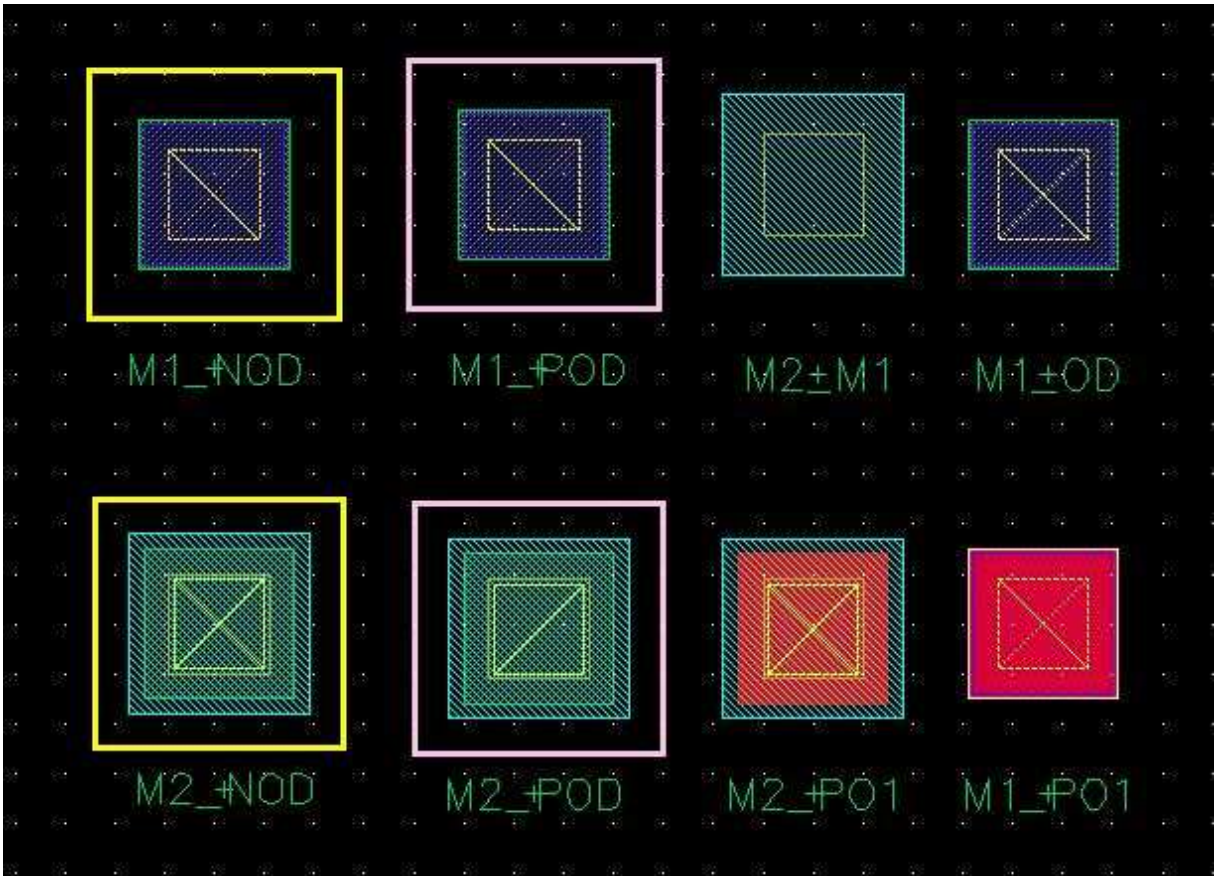


CDF parameter	Description	Default
Scribe name	Creation of the name of the scribe *info* *4 characters max*	ABCD
Above pads line	Above extension of the drawing area defValue 0 (integer>0) *info* *unit : 1 pitch = 80 um*	0
Below pads line	Below extension of the drawing area defValue 0 (integer>0) *info* *unit : 1 pitch = 80 um*	0
Pads option	Choice of pads or not **choices** **"with pads" / "without pads"**	with pads
Active or Poly pads	Selection of specific pads for test **choices** **“true if the option is on”** *info* *only possible if "with pads" is on*	t
Pad#	Add active or poly layer under the pad, to specify for each pad **choices** **"active" / "poly"** *info* *only possible if "choice -active- or –poly- under the pad" is on*	poly

4.4) FDSOI Contacts

All contacts described below are accessible across the Contact category into the reference library DK_fdsoi45Lib.

Name	Description
M1_NOD	Connect Metal1 to Active by Contact with DSN
M1_POD	Connect Metal1 to Active by Contact with DSP
M1_OD	Connect Metal1 to Active by Contact
M2_M1	Connect Metal2 to Metal1 by Via1
M2_NOD	Connect Metal2 to Active via VIA1/Metal1/Contact with DSN
M2_POD	Connect Metal2 to Active via VIA1/Metal1/Contact with DSP
M1_PO1	Connect Metal1 to Poly1 by Contact
M2_PO1	Connect Metal2 to Poly1 via VIA1/Metal1/Contact



4.5) Eldo module

This section gives an overview about the different Eldo corner model files for devices.
Eldo model files are located in directory:

$PDK_ROOT/tech/tools/eldo

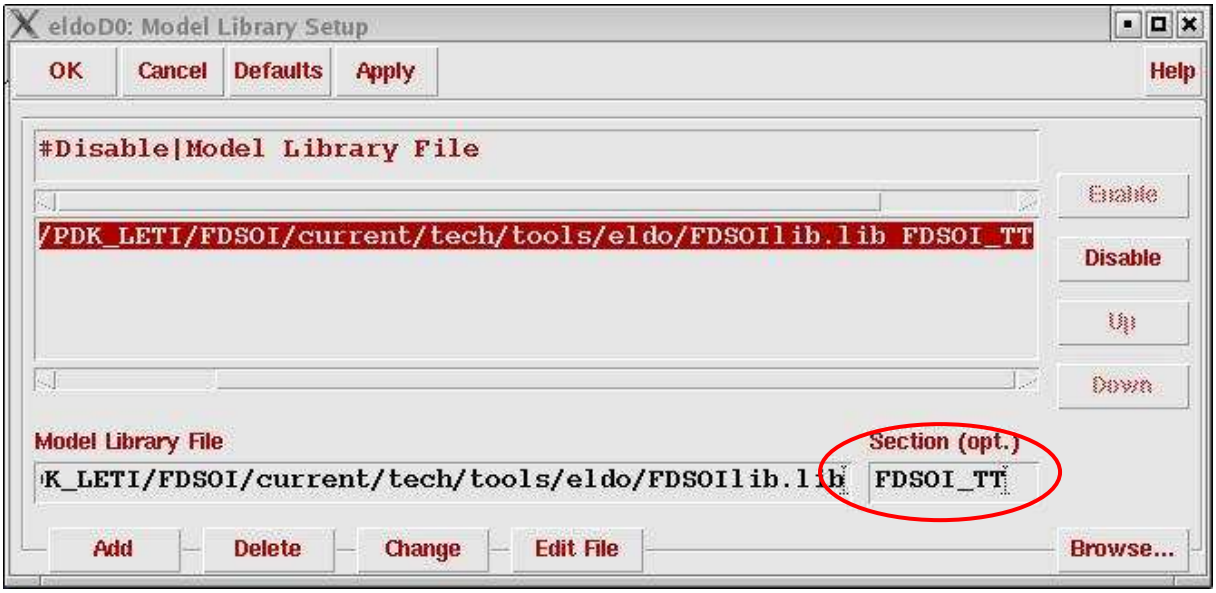
The version of Eldo simulator is 6.8_3.1 (Adms 2006.2b). Model parameters and corners are described below:

Model parameters	**Description**
Length	drawn channel length (units: meter)
Width	total channel width (units: meter)
Number of fingers	for multifinger device using common diffusion regions - the finger width is Width/Number of fingers
Nb of devices in //	total width is M*Width
Mismatch	flag for mismatch simulation (0=no mismatch)

Corners definition	**Description**
FDSOI_TT	*typical case for NMOS and PMOS (default)*
FDSOI_FF	fast case for NMOS and PMOS
FDSOI_SS	slow case for NMOS and PMOS
FDSOI_FFA	fast case for NMOS and PMOS for analog
FDSOI_SSA	slow case for NMOS and PMOS for analog

FDSOI_FS	fast case for NMOS and slow case for PMOS
FDSOI_SF	slow case for NMOS and fast case for PMOS
FDSOI_FSA	fast case for NMOS and slow case for PMOS for analog
FDSOI_SFA	slow case for NMOS and fast case for PMOS for analog
FDSOI_stat	for MC simulation

You can change your corner definition in the field Section (cf below) after having selected Setup→ Model Librairies… in the Analog Design Environment window.



4.6) Calibre module

Calibre v2006.4 is used here as the main physical verification to perform design rule checks (DRC) and to run layout-versus-schematic (LVS) on layout. The Calibre Interactive Graphical User Interface (GUI) is a front-end interface that eases the task of performing interactive verification. The PDK load the Calibre Skill Interface into Virtuoso/VirtuosoXL to start GUI directly from layout window.

The Calibre Skill Interface adds a Calibre menu item automatically to layout windows during start-up of Virtuoso/Virtuoso XL :

The following commands are available in the Calibre menu:

- Run DRC: Starts Calibre Interactive DRC.
- Run LVS: Starts Calibre Interactive LVS. This is not supported in this PDK.

The next section will give information about how to set Calibre Interface GUI for various physical verification tasks.

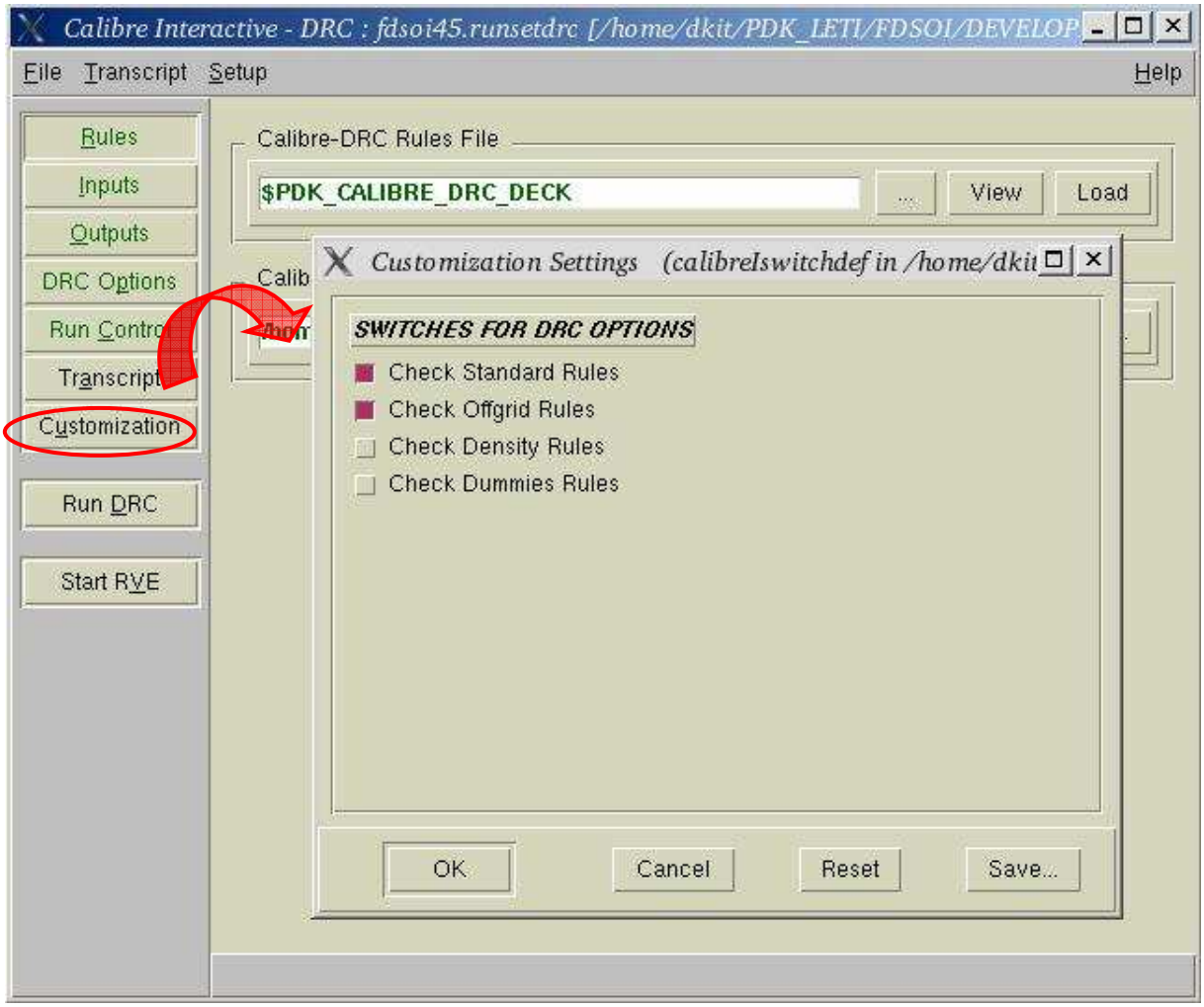
4.6.1) Calibre DRC

The Calibre DRC file is located under $PDK_ROOT/tech/tools/calibre directory.
In the Calibre Interactive interface, this file is loaded with the $PDK_CALIBRE_DRC_DECK variable.

A runset is automatically loaded with the $MGC_CALIBRE_DRC_RUNSET_FILE variable.

In the “Customization” button, you can select checks like this:

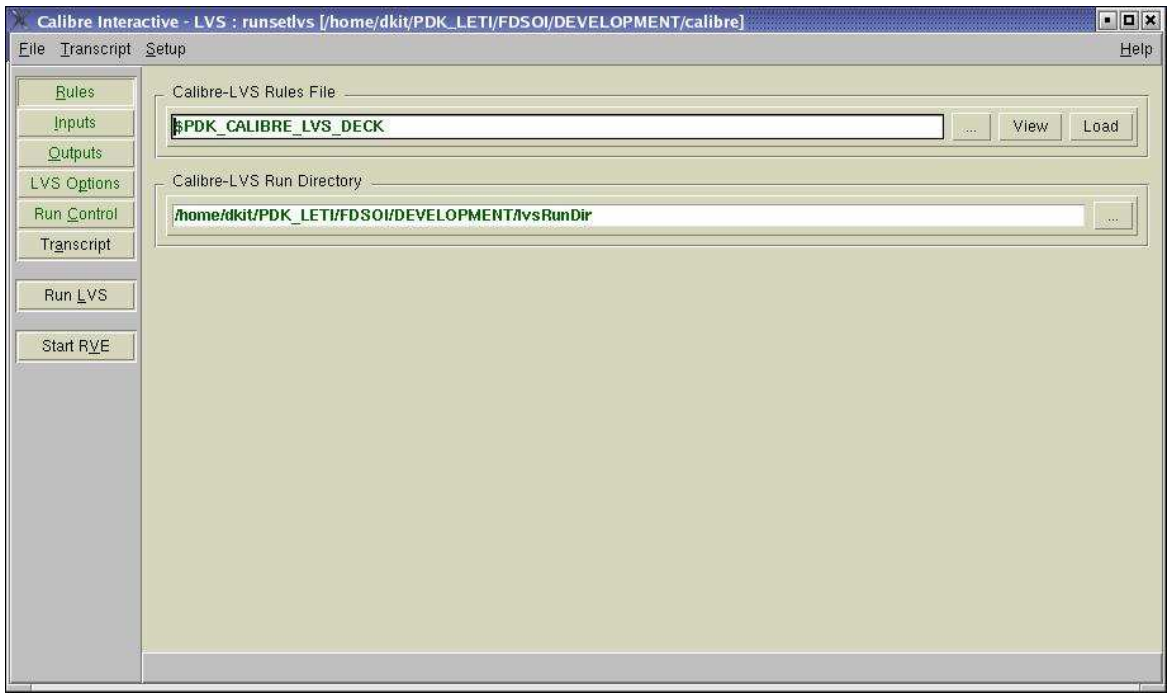
Group	Description	Default
Check Standard Rules	Select all rules except Offgrid, Density and Dummies rules	t
Check Offgrid Rules	Select all Offgrid rules	t
Check Density Rules	Select all Density rules	nil
Check Dummies Rules	Select all Dummies rules	nil



4.6.2) Calibre LVS

The Calibre LVS file is located under $PDK_ROOT/tech/tools/calibre directory.
In the Calibre Interactive interface, this file is loaded with the $PDK_CALIBRE_LVS_DECK variable.

A runset is automatically loaded with the $MGC_CALIBRE_LVS_RUNSET_FILE variable.

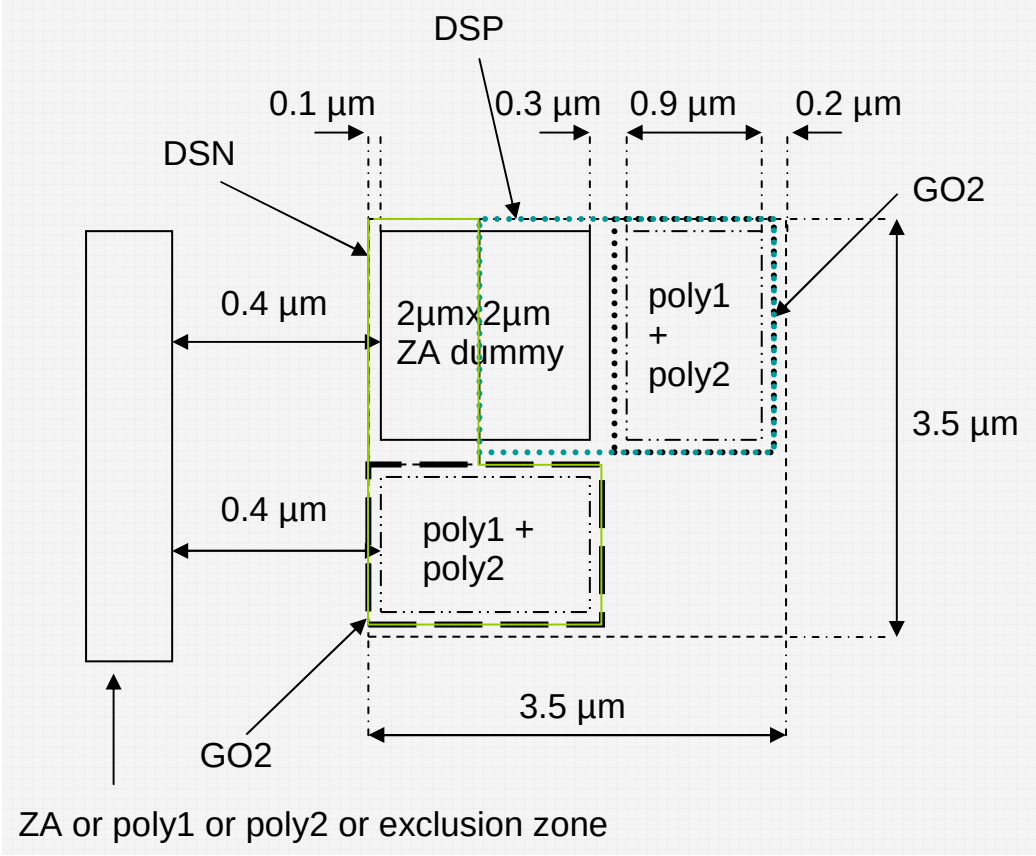


4.6.3) Calibre Dummies generation

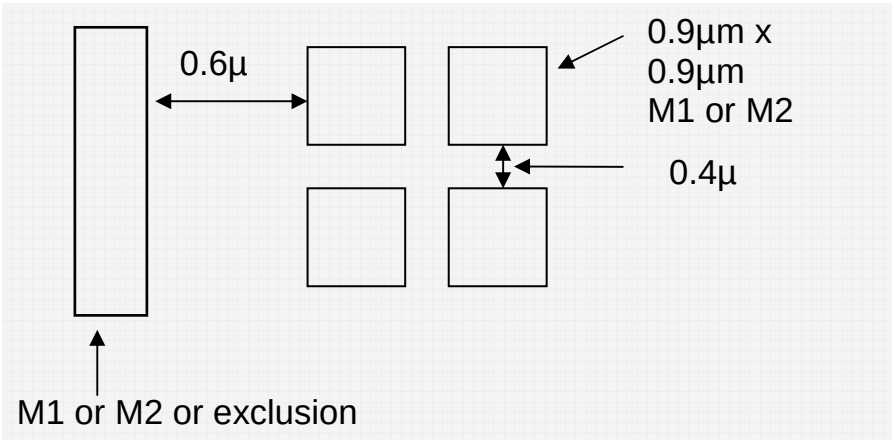
There are two passes to generate dummies in low density regions.

4.6.3.1) First pass

For ZA,PO, DSN/DSP & GO2 insert square dummies in low density regions like this:

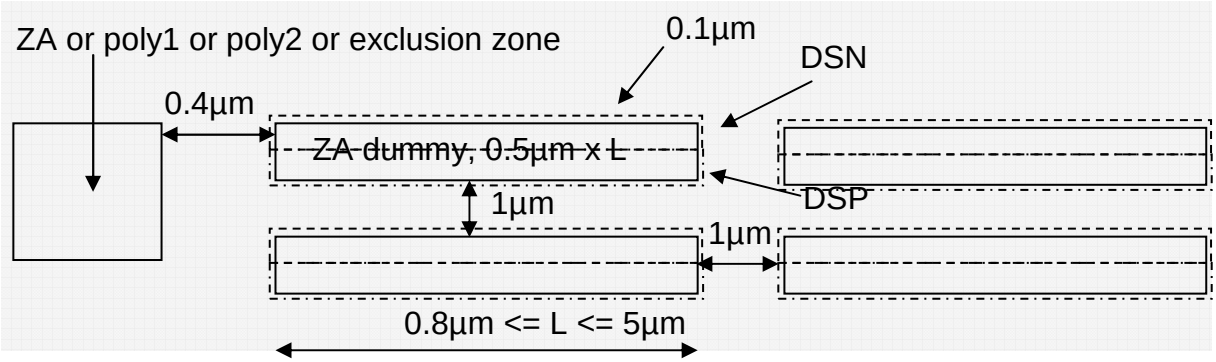


For Metal1 & Metal2 insert square dummies in low density regions like this:

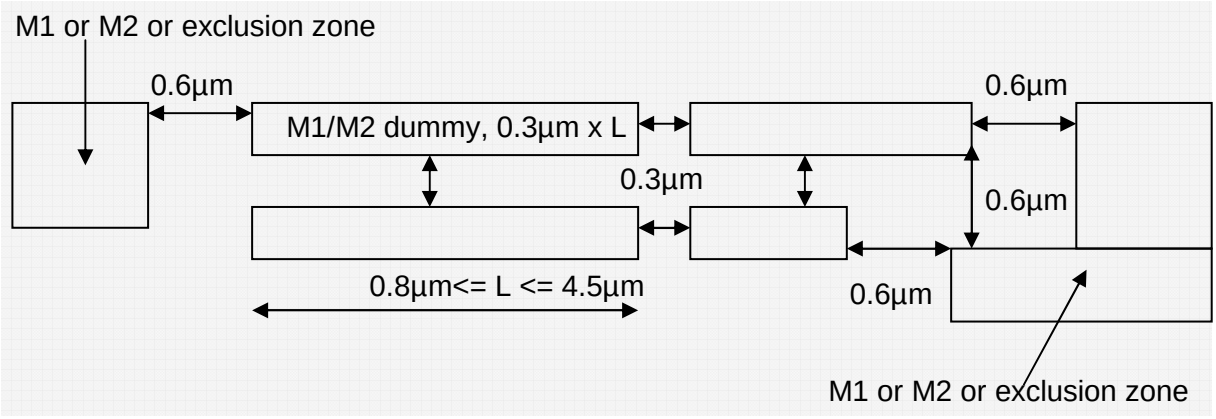


4.6.3.2) Second pass

For ZA, DSN & DSP insert rectangular dummy stripes in horizontal and vertical direction in low density regions like this:



For Metal1 & Metal2 insert rectangular dummy stripes in horizontal and vertical direction in low density regions like this:

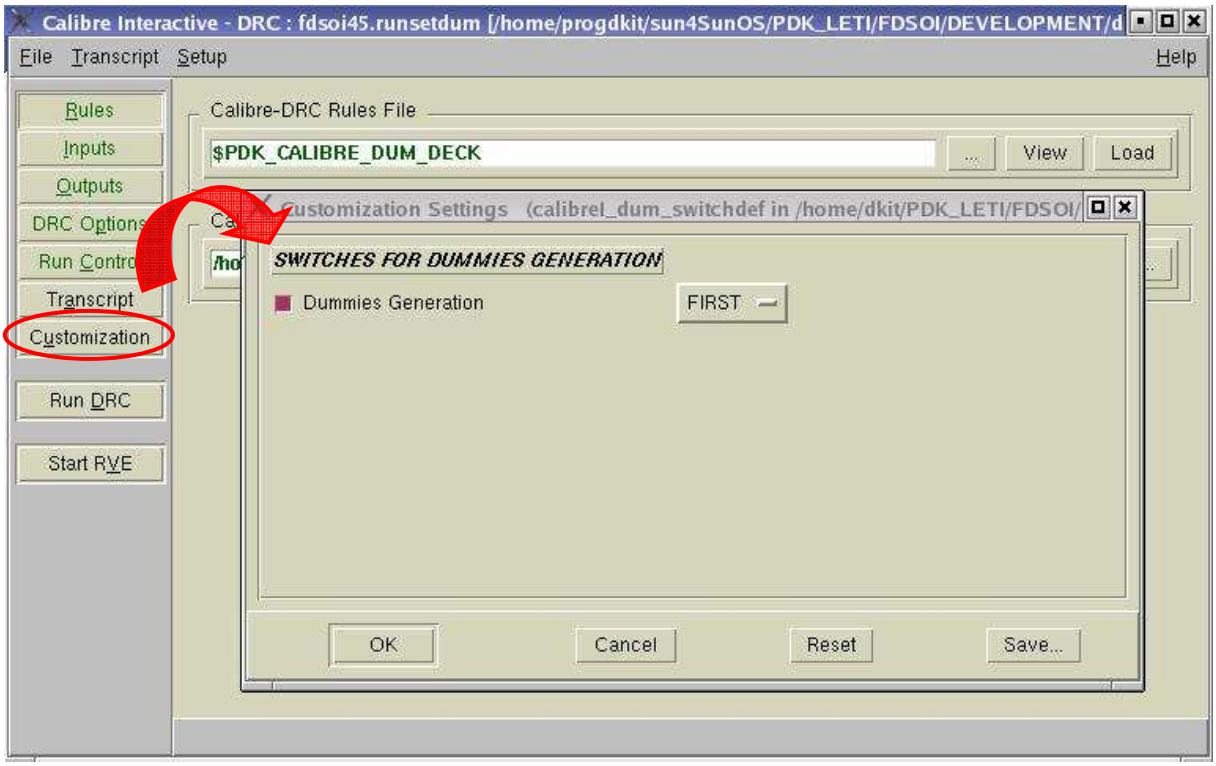


The Calibre Dummies file is located under $PDK_ROOT/tech/tools/calibre directory.
To generate dummies, launch “Run DRC” and this file will be loaded into the Calibre Interactive DRC interface across the $PDK_CALIBRE_DUM_DECK variable.

To load the correct runset file, select “fdsoi45.runsetdum” in the list when you launch “Load Runset…” in the “File” menu.
This list of runset file is automatically loaded with the $MGC_CALIBRE_DRC_RUNSET_LIST variable.

In the “Customization” button, you can choose the type of Dummies generation:

- FIRST : first pass of dummies generation
- SECOND : second pass of dummies generation



Important: after the first dummies generation, check the density and dummies rules (See 4.6.1 Calibre DRC section). If the check is not valid, launch the second dummies generation.

5 PDK tree

```
$PDK_ROOT
|-- bin/
|   `-- pdk_leti_install_user
|-- cad/
|   |-- .cdsenv
|   |-- .cdsinit
|   |-- .simrc
|   `-- cad.lib
|-- cdsuser/
|   |-- .artist_states/
|   |-- .cdsinit
|   |-- .simrc
|   |-- cds.lib
|   |-- cdsuser_file.tar
|   `-- simulation/
|-- doc/
|   |-- DRM_FDSOI_193nm.pdf
|   `-- release_notes_v2.2.pdf
`-- tech/
    |-- il/
    |   |-- LTlabpol.il
    |   |-- custom_leti.il
    |   |-- fdsoiBK.il
    |   |-- fdsoiGR.il
    |   |-- fdsoiRT.il
    |   |-- pc_body_mos.il
    |   |-- pc_chnl_mos.il
    |   |-- pc_dnp_mos.il
    |   |-- pc_scribe_22pads.il
    |   `-- pc_std_mos.il
    `-- tools/
        |-- calibre/
        |   |-- calibreI_dum_switchdef
        |   |-- fdsoi45.calibredrc
        |   |-- fdsoi45.calibredum
        |   |-- fdsoi45.calibrelvs
        |   |-- fdsoi45.runsetdrc
        |   |-- fdsoi45.runsetdum
        |   |-- fdsoi45.runsetfile
        |   `-- fdsoi45.runsetlvs
        |-- dfII/
        |   |-- cdb/
        |   |   `-- DK_fdsoi45Lib/
        |   |       |-- Contact.Cat
        |   |       |-- DK_fdsoi45Lib.TopCat
        |   |       |-- Devices.Cat
        |   |       |-- M1_NOD/
        |   |       |   `-- symbolic/
        |   |       |       |-- layout.cdb
        |   |       |       |-- master.tag
        |   |       |       `-- pc.db
        |   |       |-- M1_OD/
        |   |       |   `-- symbolic/
        |   |       |       |-- layout.cdb
        |   |       |       |-- master.tag
        |   |       |       `-- pc.db
        |   |       |-- M1_PO1/
        |   |       |   `-- symbolic/
```

```
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- M1_POD/
|   |       |   `-- symbolic/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- M2_M1/
|   |       |   `-- symbolic/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- M2_NOD/
|   |       |   `-- symbolic/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- M2_OD/
|   |       |   `-- symbolic/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- M2_PO1/
|   |       |   `-- symbolic/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- M2_POD/
|   |       |   `-- symbolic/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PAD_D_ELEM1_ACT/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PAD_D_ELEM1_ACT_RING/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PAD_D_ELEM1_ACT_UNIT/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PAD_D_ELEM1_M1/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PAD_D_ELEM1_M1_UNIT/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PAD_D_ELEM1_M2/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
```

```
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PAD_D_ELEM1_M2_UNIT/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PAD_D_ELEM1_POLY1/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PAD_D_ELEM1_POLY1_RING/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PAD_D_ELEM1_POLY1_UNIT/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PAD_D_ELEM1_RING/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PAD_D_ELEM1_VIA1/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PAD_D_ELEM1_VIA1CONT/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- Pad.Cat
|   |       |-- PadActV1/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PadPolyV1/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- PadV1/
|   |       |   `-- layout/
|   |       |       |-- layout.cdb
|   |       |       |-- master.tag
|   |       |       `-- pc.db
|   |       |-- Pad_Act.Cat
|   |       |-- Pad_Met.Cat
|   |       |-- Pad_Poly.Cat
|   |       |-- Pcells.Cat
|   |       |-- bindkeys/
|   |       |   `-- manual/
|   |       |       |-- master.tag
|   |       |       `-- text.txt
```

```
|   |       |-- cdsinfo.tag
|   |       |-- libInit.il
|   |       |-- nmosfd/
|   |       |   |-- auCdl/
|   |       |   |   |-- master.tag
|   |       |   |   |-- pc.db
|   |       |   |   `-- symbol.cdb
|   |       |   |-- eldoD/
|   |       |   |   |-- master.tag
|   |       |   |   |-- pc.db
|   |       |   |   `-- symbol.cdb
|   |       |   |-- prop.xx
|   |       |   `-- symbol/
|   |       |       |-- master.tag
|   |       |       |-- pc.db
|   |       |       |-- prop.xx
|   |       |       `-- symbol.cdb
|   |       |-- pc_body_mos/
|   |       |   |-- layout/
|   |       |   |   |-- layout.cdb
|   |       |   |   |-- master.tag
|   |       |   |   `-- pc.db
|   |       |   |-- manual/
|   |       |   |-- prop.xx
|   |       |   `-- text.txt
|   |       |-- pc_chnl_mos/
|   |       |   |-- layout/
|   |       |   |   |-- layout.cdb
|   |       |   |   |-- master.tag
|   |       |   |   `-- pc.db
|   |       |   |-- manual/
|   |       |   |   |-- master.tag
|   |       |   |   `-- text.txt
|   |       |   `-- prop.xx
|   |       |-- pc_dnp_mos/
|   |       |   |-- layout/
|   |       |   |   |-- layout.cdb
|   |       |   |   |-- master.tag
|   |       |   |   `-- pc.db
|   |       |   |-- manual/
|   |       |   |   |-- master.tag
|   |       |   |   `-- text.txt
|   |       |   `-- prop.xx
|   |       |-- pc_scribe_22pads/
|   |       |   |-- layout/
|   |       |   |   |-- layout.cdb
|   |       |   |   |-- master.tag
|   |       |   |   `-- pc.db
|   |       |   |-- manual/
|   |       |   |   |-- master.tag
|   |       |   |   `-- text.txt
|   |       |   `-- prop.xx
|   |       |-- pc_std_mos/
|   |       |   |-- layout/
|   |       |   |   |-- layout.cdb
|   |       |   |   |-- master.tag
|   |       |   |   `-- pc.db
|   |       |   |-- manual/
|   |       |   |   |-- master.tag
|   |       |   |   `-- text.txt
|   |       |   `-- prop.xx
```

```
|   |       |-- pmosfd/
|   |       |   |-- auCdl/
|   |       |   |   |-- master.tag
|   |       |   |   |-- pc.db
|   |       |   |   `-- symbol.cdb
|   |       |   |-- eldoD/
|   |       |   |   |-- master.tag
|   |       |   |   |-- pc.db
|   |       |   |   `-- symbol.cdb
|   |       |   |-- prop.xx
|   |       |   `-- symbol/
|   |       |       |-- master.tag
|   |       |       |-- pc.db
|   |       |       |-- prop.xx
|   |       |       `-- symbol.cdb
|   |       |-- prop.xx
|   |       |-- techfile.cd%
|   |       `-- techfile.cds
|   |-- cdf/
|   |   |-- nmosfd.cdf
|   |   |-- pc_body_mos.cdf
|   |   |-- pc_chnl_mos.cdf
|   |   |-- pc_dnp_mos.cdf
|   |   |-- pc_scribe_22pads.cdf
|   |   |-- pc_std_mos.cdf
|   |   `-- pmosfd.cdf
|   |-- display.drf
|   |-- fdsoi45.lmt
|   |-- tech.lib
|   `-- techfile.tf
`-- eldo/
    |-- FDSOIlib.lib -> FDSOIlibV1p3.lib
    |-- FDSOIlibV1p3.lib
    |-- FDSOImodelV1p3.lib
    `-- FDSOIparamV1p3.lib
```

ANNEXES

$PDK_ROOT/cad/.cdsinit :

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;
; Company : CEA/LETI
; Author  : Gérald Cibrario
; Date    : 06/02/2008
;
; Location: <PDK_ROOT>/cad/.cdsinit
; Version : 1.1
;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

println("------------------------------------------")
println("            PDK LETI                ")
println("                              ")
println("          Techno : FDSOI              ")
println("                              ")
println("------------------------------------------")

;Artist Link initialisation
let((t_amsPath t_file)
        t_amsPath = getShellEnvVar("MGC_AMS_HOME")
        when(t_amsPath
                t_file = strcat(t_amsPath "/etc/cds/.cdsinit")
                when(isFile(t_file) load(t_file))
        )
)

;Load .cdsenv file
envLoadFile(strcat( env(PDK_ROOT) "/cad/.cdsenv"))

;Load display.drf file
drLoadDrf(strcat(getShellEnvVar("PDK_ROOT") "/tech/tools/dfII/display.drf"))

;eldoD simulator default into Analog Artist
envSetVal("asimenv.startup" "simulator" 'string "eldoD")

;Model Library Setup for eldoD
envSetVal("eldoD.envOpts" "modelFiles" 'string strcat( env(PDK_ROOT)
"/tech/tools/eldo/FDSOIlib.lib;FDSOI_TT"))

;when File->Exit in the CIW the "Save Display Information" doesn't appear
procedure(CCSsuppressDispForm()
hiRegTimer("hiFormCancel(techSaveDrmForm)" 10)
)
regExitBefore('CCSsuppressDispForm)

;Variables declaration for DRC and LVS file + runset + dummies
pdk_calibre_lvs_file      = strcat("PDK_CALIBRE_LVS_DECK=" getShellEnvVar("PDK_ROOT") "/"
"tech/tools/calibre/fdsoi45.calibrelvs")
pdk_calibre_drc_file      = strcat("PDK_CALIBRE_DRC_DECK=" getShellEnvVar("PDK_ROOT") "/"
"tech/tools/calibre/fdsoi45.calibredrc")
pdk_calibre_dum_file      = strcat("PDK_CALIBRE_DUM_DECK=" getShellEnvVar("PDK_ROOT") "/"
"tech/tools/calibre/fdsoi45.calibredum")
```

```
pdk_calibre_runset_lvs_file = strcat("MGC_CALIBRE_LVS_RUNSET_FILE="
getShellEnvVar("PDK_ROOT") "/" "tech/tools/calibre/fdsoi45.runsetlvs")
pdk_calibre_runset_drc_file = strcat("MGC_CALIBRE_DRC_RUNSET_FILE="
getShellEnvVar("PDK_ROOT") "/" "tech/tools/calibre/fdsoi45.runsetdrc")
pdk_calibre_runset_drc_list = strcat("MGC_CALIBRE_DRC_RUNSET_LIST="
getShellEnvVar("PDK_ROOT") "/" "tech/tools/calibre/fdsoi45.runsetfile")

pdk_calibre_switch_dum_file = strcat("MGC_CALIBRE_DUM_SWITCH_FILE="
getShellEnvVar("PDK_ROOT") "/" "tech/tools/calibre/calibreI_dum_switchdef")
pdk_calibre_switch_drc_file = strcat("MGC_CALIBRE_DRC_SWITCH_FILE="
getShellEnvVar("PDK_ROOT") "/" "tech/tools/calibre/calibreIswitchdef")

setShellEnvVar(pdk_calibre_lvs_file)
setShellEnvVar(pdk_calibre_drc_file)
setShellEnvVar(pdk_calibre_dum_file)
setShellEnvVar(pdk_calibre_runset_lvs_file)
setShellEnvVar(pdk_calibre_runset_drc_file)
setShellEnvVar(pdk_calibre_runset_drc_list)
setShellEnvVar(pdk_calibre_switch_dum_file)
setShellEnvVar(pdk_calibre_switch_drc_file)

load(strcat( env(PDK_ROOT) "/tech/il/fdsoiBK.il"))
load(strcat( env(PDK_ROOT) "/tech/il/fdsoiGR.il"))
```

$PDK_ROOT/tech/tools/dfII/fdsoi45.lmt :

# Cadence Name	Layer Purpose	GDSII Number	layer DataType
ACTIVE	drawing	02	0
ACTIVE	tile	02	1
POLY1	drawing	13	0
POLY1	tile	13	1
POLY2	drawing	42	0
POLY2	tile	42	1
GO2	drawing	06	0
GO2	tile	06	1
VTN	drawing	60	0
VTP	drawing	43	0
DSN	drawing	16	0
DSN	tile	16	1
DSP	drawing	17	0
DSP	tile	17	1
CONTACT	drawing	19	0
METAL1	drawing	23	0
METAL1	pin	23	83
METAL1	tile	23	1
VIA1	drawing	25	0
METAL2	drawing	27	0
METAL2	pin	27	83
METAL2	tile	27	1
PADOPEN	drawing	40	0
ALUCAP	drawing	41	0
NITRIDE	drawing	31	0
NITRIDE	pin	31	83
ACTPOLY	duexclude	80	0
METAL	duexclude	81	0
MARKER	drawing	82	0
instance	drawing	236	0
prBoundary	drawing	235	0
text	drawing	230	0

$PDK_ROOT/tech/tools/calibre/fdsoi45.runsetdrc:

```
*drcRulesFile: $PDK_CALIBRE_DRC_DECK
*drcRunDir: ../VERIF/DRC
*drcLayoutPaths: %l.calibre.gds
*drcLayoutPrimary: %l
*drcLayoutGetFromViewer: 1
*drcResultsFile: %l.drc.results
*drcSummaryFile: %l.drc.summary
*drcViewSummary: 0
*cmnTemplate_LP: ../../VERIF/GDS/%l.calibre.gds
*cmnShowOptions: 1
*cmnUseCustomFile: 1
*cmnCustomFileName: $MGC_CALIBRE_DRC_SWITCH_FILE
*cmnNumTurbo:
*cmnNumTurboLitho:
```

$PDK_ROOT/tech/tools/calibre/fdsoi45.runsetdum:

```
*drcRulesFile: $PDK_CALIBRE_DUM_DECK
*drcRunDir: ../VERIF/DUM
*drcLayoutPaths: %l.calibre.gds
*drcLayoutPrimary: %l
*drcLayoutGetFromViewer: 1
*drcResultsFile: %l.dum.gds
*drcResultsFormat: GDSII
*drcDRCMaxResultsAll: 1
*drcDRCMaxVertexCount: 200
*drcSummaryFile: %l.dum.summary
*drcTemplate_RD: %l.dum.gds
*drcTemplate_SF: %l.dum.summary
*cmnWarnLayoutOverwrite: 0
*cmnShowOptions: 1
*cmnUseCustomFile: 1
*cmnCustomFileName: $MGC_CALIBRE_DUM_SWITCH_FILE
*cmnNumTurbo:
*cmnNumTurboLitho:
*cmnSlaveHosts: {use {}} {hostName {}} {cpuCount {}} {a32a64 {}} {rsh {}} {maxMem {}} {workingDir
{}} {layerDir {}} {mgcLibPath {}} {launchName {}}
```

$PDK_ROOT/tech/tools/calibre/fdsoi45.runsetlvs:

```
*lvsRulesFile: $PDK_CALIBRE_LVS_DECK
*lvsRunDir: ../VERIF/LVS
*lvsLayoutPaths: %l.calibre.gds
*lvsLayoutPrimary: %l
*lvsLayoutGetFromViewer: 1
*lvsSourcePath: %l.src.net
*lvsSourcePrimary: %l
*lvsSourceGetFromViewer: 1
*lvsReportFile: %l.lvs.report
*lvsMaskDBFile: %l.maskdb
*lvsSpiceFile: %l.sp
*lvsAutoMatch: 1
*lvsReportOptions: A B C D
*lvsAbortOnSoftchk: 1
```

*lvsPowerNames: VDD vdd "vdd!" "vdd;" VDDS vdds "vdds!" "vdds;"
*lvsGroundNames: GND gnd "gnd!" "gnd;" GNDS gnds "gnds!" "gnds;"
*lvsRecognizeGates: NONE
*lvsERCDatabase: %l.erc.results
*lvsERCSummaryFile: %l.erc.summary
*lvsIsolateShorts: 1
*lvsTemplate_IS: 1
*cmnWarnLayoutOverwrite: 0
*cmnWarnSourceOverwrite: 0
*cmnVConnectNames: "vdd;" "gnd;" VDD GND vdd gnd "vdd!" "gnd!" "vdds;" "gnds;" VDDS GNDS vdds gnds "vdds!" "gnds!"
*cmnShowOptions: 1
*cmnRemoteClusterQueueCmd: bsub -q <queue_name> %C
*cmnSlaveHosts: {use {}} {hostName {}} {cpuCount {}} {a32a64 {}} {rsh {}} {maxMem {}} {workingDir {}} {layerDir {}} {mgcLibPath {}} {launchName {}}