INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

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D5.6: Report on EUROPRACTICE meeting, Granada, January 18, 2011

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Dissemination Level		
PU	Public	X
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1.- Introduction.

Up to now, a lot of research activities have been pursued in Europe around SOI: at the substrate level, at the device level and at the circuit level. Since few years, advanced SOI technologies have been developed in research labs in order to address the downscaling required for 32 nm nodes and below. Today such researches are mainly dedicated to technology development. Among the various ones, we can mention the LETI Fully Depleted SOI technology (developed with high-k and metal gate) that has now enough maturity to be evaluated at circuit level. So, it becomes obvious that a research-dedicated platform has to be developed in order to address the circuit design aspects, focussing on the advantage of such technology for Low Power applications. Access to such platform is a long-time wish of European researchers. One of the main goals of EUROSOI+ is to coordinate the formation of such research-dedicated platform which will provide, through the integration at some point in EUROPRACTICE or other technology brokers such as CMP (http://cmp.imag.fr) or MOSIS (http://www.mosis.org), prototyping and MPW in SOI open to European research groups and Fabless Semiconductor companies using LETI SOI process.

To make this platform a reality, different activities has been coordinated along the last years:

a) Coordination of a scientific board (with EUROSOI+ members) that has identified the topics that need to be addressed to construct this platform.
b) Already processed CEA-LETI Fully Depleted SOI devices with high-K and metal gate have been provided by LETI to the EUROSOI+ partners with interest, expertise and proper resources to characterize these devices.
c) Organization of meetings and workshops focussed on FDSOI technology.
d) Distribution to EUROSOI+ partners of a Research dedicated Design Kit based on LETI FDSOI technology.
e) Intensive promotion at the European level of the FDSOI technology.
f) Evaluate, through meetings with EUROPRACTICE organization, the possibility to integrate this technology in the existing EUROPRACTICE structure, making this technology ready and available to the EUROSOI+ members, for small circuit prototyping.

Using this platform, EUROSOI members will have access to a flexible research platform for small volume prototyping (through Multi-project wafer development (MPW)), with a support of cell libraries and research design kits (elaborated for the most popular CAD tools). Such platform should enable the optimization of the circuit design for Low Power applications, taking full advantage of the SOI structure, combined with high K, Metal gate and the Fully Depleted structure.

This task is of utmost importance for universities, research centres and fabless companies to develop and demonstrate high design expertise in the EU. This is also a way to foster new ideas for innovative products, start-ups. The Ultra-Low-Power application field is certainly of huge interest for EU industrial

domains such as biomedical applications, RF applications, etc. Another known weakness in EU is the lack of system level design when compared to cells/building blocks design.

Along these last years we have had several contacts with people in charge of EUROPRACTICE and CMP and they have shown interest in the integration of the SOI technology whenever there are potential customers and CEA-LETI offers its own technology.

Our first idea was to collaborate with EUROPRACTICE, since they have developed several successful projects funded by the EU Commission, but without excluding any other IC service who might be interested.

Once LETI technology was mature enough, the design kit was finished and calibrated, LETI decided to open the FDSOI technology and design flow via an R&D oriented MPW offer which will provide users with first hand experience and results on advanced FDSOI. In October 2010, CEA-LETI announced during the FDSOI Workshop at Tokyo University the launch of an Exploratory MPW (Multi Project Wafers) initiative based on FDSOI (Fully Depleted SOI) 20nm process, opening the access of its 300mm infrastructure to the design community. This first exploratory service has been launched through CMP for several logistic reasons. However, there is full predisposition to go on with our intention to provide a similar service to EUROPRACTICE. With this aim, EUROSOI members met Prof. Carl DAS, EUROPRACTICE co-ordinator, in Granada on January, 18th, 2011.

2.- Minutes of the meeting held with EUROPRACTICE in Granada, January 18th, 2011

Attendees:

Prof. Carl Das, EUROPRACTICE, IMEC, Leuven, Belgium
Prof. Sorin Cristoloveanu, IMEP, Grenoble
Prof. Cor Claeys, IMEC, Leuven
Prof. Denis Flandre, UCL, Louvain la Neuve
Dr. Carlo Reita, CEA-LETI, CEA, Grenoble
Dr. Olivier Faynot, CEA-LETI, Grenoble
Prof. Andrés Godoy, UGR, Granada
Prof. Francisco Gámiz, UGR, Granada (Co-ordinator)

Agenda:

1.- Welcome (Francisco Gamiz)
2.- LETI FDSOI technology status (Carlo Reita).
3.- EUROPRACTICE (Carl Das).
4.- Discussion.
5.- Questions and suggestions.

1.- Prof. Gamiz welcome the attendees to this meeting, and briefly reported the goals of EUROSOI network related to this issue and the steps already taken in this regard. Prof. Gamiz reminded the previous contact (meetings) and phone calls kept with Dr. Carl Das in the past.

2.1.- Prof. Gamiz asked Dr.Carlo Reita, from CEA-LETI to summarize the status of the LETI FDSOI technology. Basically the figures of merit of the technology are:

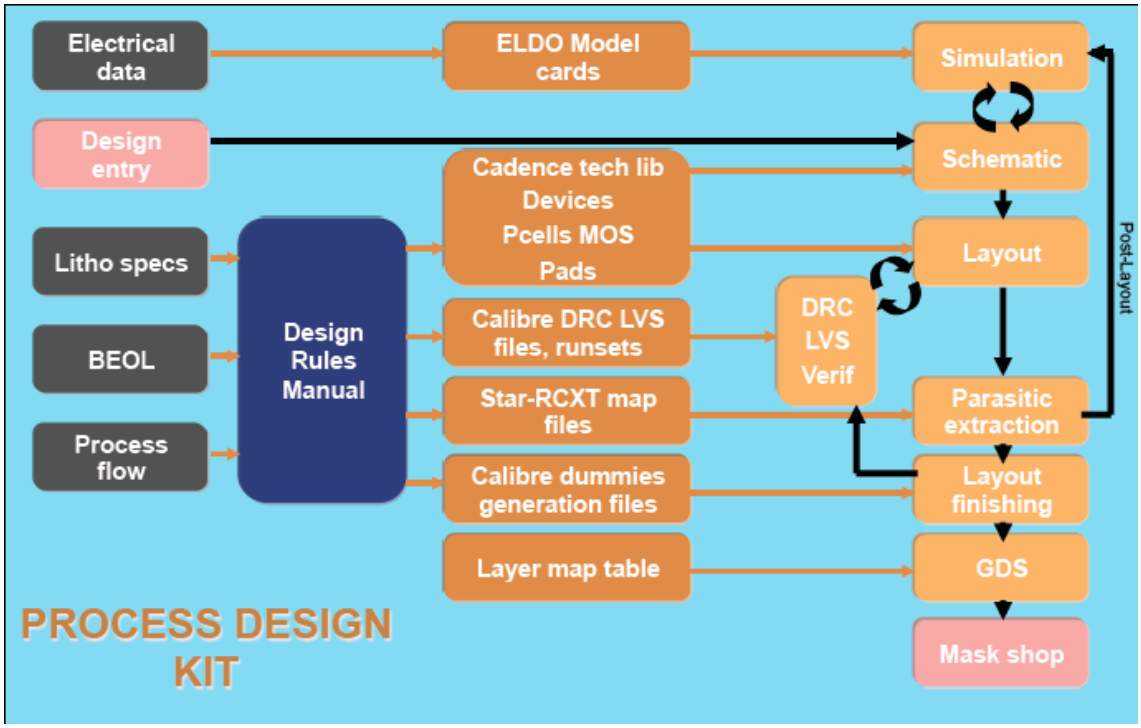
a) Process on 300mm (BEOL via partnership with STM Crolles)
b) CMOS devices
c) Optical lithography with available e-beam options
d) ***No channel doping, No Pocket implant***
e) Ultra-thin BOX material option
f) Threshold voltage variability on undoped channels fully meets 20nm LP specification and largely exceed similar figures of merit for bulk technology on the same nodes.
g) Fabricated devices show very competitive I_{ON}/I_{OFF} ratio even at V_{DD}=0.9V, compared to Low Power Bulk at V_{DD}>1V.
h) Fabricated SRAM cells show Static-Noise-Margin curves large enough to demonstrate cell functionality down to 0.7 V.

In summary, FDSOI technology presents important advantages of SoC:

i. **Excellent Electrostatic Control**
    a. Ability to use undoped Si-channel → low variability → SRAM functionnality at low V_{cc}
    b. Low DIBL → increased speed performance

ii. **Using UTBOX**
   a. Possibility of V_{th} control by Back-Bias (scalable)
   b. Increased scalability below 16nm
   c. Potential for Hybrid Bulk/FDSOI process for Power devices

2.2.- Once Dr. Reita introduced the technology, he also said that LETI has developed a Process Design Kit, summarized in the next figure. The manual of this PDK can be found in Deliverable D5.5



2.3.- Dr. Reita introduced the Multiproject Wafer initiative launched in October through CMP service. The offer consists of:

i. R&D oriented Design Kit made available via CMP service:
   a. 20nm node FEOL with 65nm back-end in a first phase
   b. 20nm node FEOL with 28nm back-end in a second phase.
   c. Evolution towards 16nm planned
ii. Received designs implemented in one LETI run
iii. IP rules adapted for R&D
iv. R&D oriented Design Kit made available with initial parameter set
   a. min Lg=25nm
   b. single Vt n- and p-MOSFETS with balanced Vth of ±0.4V
   c. back end rules 65nm
   d. 4 metal levels
   e. ~40 cells library
   f. place and route available

The proposed timetable for fhis exploratory MPW offer is the following:

- 10Q4 end – Distribution of DK via CMP
- 11Q3 (sept) – GDS to be delivered to CMP
- 11Q4 beg. – Tape-out and run start
- 12Q1 end – Silicon delivery

2.4. Dr.Reita also exposed the reasons why this MPW initiative was launched through CMP service, and that can be summarized as follows:

a. One is the geographical positioning: as CMP is based in Grenoble and French speaking this facilitates the exchanges between the teams for the establishment of a successful offer which is a premiere for LETI and, to our knowledge, is also the first offer from a Research Institute of an MPW possibility and on such an advanced technology. Getting rid of delays and communication obstacles should profit the entire community. Moreover CMP is also an academic consortium, albeit French, and is not limited by the need of submitting project proposals at regular intervals like Europractice.

b. A second reason is that CMP is already a provider of the ST technology and this simplifies a number of IP issues we already outlined in the discussion in the EUROSOI+ consortium.

c. A third one is the fact that CMP understood the specificity of the offer from a non-foundry and made proposals and valuable contribution to the establishment of the necessary tools.

The first two were the main reasons for the choice, while the third was an important facilitator for a speedy introduction.

Dr. Reita expressed our expectation that the two organisations (EUROPRACTICE and CMP) can work together to open this offer to the academic community in the largest possible manner.

3.- Dr. Das recognized that the data presented by Dr.Reita were spectacular, however at the same time he expressed his doubts whether in the short term, there would be enough designs or requests that justify the fact that two IC services simultaneously offer the FDsOI technology. Dr. Das also said that there are several questions to be answered before SOI becomes the mainstream technology:

a. Will SOI be competitive to CMOS/3D for the large volume products or will SOI be a technology for a niche market?.
b. SoC needs a large portfolio of standard cell libraries and IP. They are available for bulk technology but not for SOI. This is an important drawback.

According to Dr. Das, when these questions are answered, perhaps, a wider SOI offer would have sense. In this regard, Dr. Das encourage us to continue our activity in the future.

4.1.- Dr. Faynot (CEA-LETI) agreed with Dr.Das that this technology is expensive, it is not fully validated, and designers might prefer to use a more tested bulk technology for their designs. But, he also mentioned that the benefits that this technology could have are very important, and that we will never know it if we do not give the chance to use it. Our intention is just to provide the chance of accessing to this technology if someone wants to use it. And also he remarked that LETI it is not a foundry.

4.2.- Dr. Das agreed with this idea, but for the time being, EUROPRACTICE will not be involved in this initiative. There is not enough time, and, according to his point of view, SOI technology it is not mature enough, the portfolio of standard cells libraries and IP it is not wide enough for the moment to guarantee a successful integration in EUROPRACTICE. More work on design, IP development, and validation is needed. It will be necessary to keep in touch in the near future to consider the inclusion of a SOI line in EUROPRACTICE. Dr. Das wished us good luck.

5.- Prof. Gamiz adjourned the meeting by thanking the attendees for their participation and collaboration.

3 .- Conclusions, recommendations and future actions.

One of the goals of EUROSOI+ is the launch of a dedicated platform that provides prototyping and MPW in SOI open to European research groups and Fabless Semiconductor companies using LETI SOI process. In this regard, the following milestones have been achieved:

- FDSOI technology is mature, available and reproducible.
- Process design Kit is available and preliminarily validated through bilateral collaborations between LETI and other partners such as UCL, STMicroelectronics, EPFL, Berkeley.
- CEA-LETI and CMP announced in October 2010, the launch of an exploratory MPW initiative using FDSOI technology

At the end of EUROSOI+ project, this goal has been achieved, although not through EUROPRACTICE, that was our first pretension, but through CMP IC service. The decision of launching a first exploratory MPW initiative through CMP instead of EUROPRACTICE was motivated by different reasons, being the main one that CEA-LETI is not a foundry, and that the BEOL will be made via partnership with STM Crolles.

According to EUROPRACTICE, the portfolio of SC libraries and IP on SOI technology is too short, the FDSOI technology is still too expensive and risky, and therefore, it is not expected a big demand of FDSOI designs, and therefore it is not necessary to involve a second IC service, as EUROPRACTICE.

The recommendation of EUROPRACTICE is keeping on working to get an extensive library of IP blocks.

EUROSOI could act as a broker to allow the exchange between partners of the building blocks fabricated/designed by the partners within EUROSOI+. Right to re-use for research could be allowed as a return for EUROSOI+ support. With this respect, EUROSOI+ would aim at becoming the “MIT of EU for SOI”, in the sense that MIT operates an advanced SOI process for other US partners and has the capability to develop SoC designs by gathering design library components.