INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

Grant Agreement nº 216373

D3.6 Summary report related to all the executed training activities within EUROSOI+ in the first reporting period (M1-M14)

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Project coordinator: Prof. Francisco Gámiz, UGR
Project coordinator organisation: University of Granada, Spain Rev.1

Project co-funded by the European Commission within the Seventh Framework Programme (FP7)		
Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

Table of contents

1. Introduction

One of the main objectives pursued by the network is the organization of a wide range of training activities. In this framework, different short-courses have been and will be organized addressing the following topics: SOI materials – SOI device physics – SOI Circuits – SOI for niche applications.

These one-day-courses are thought to be held at the same time as the programmed workshops: Cork 2008, Chalmers 2009, Grenoble 2010 and Granada 2011. Relevant speakers are invited and the participation of members of the SOI industrial community is encouraged. After each event, the opinion, comments and suggestions of the participants is collected through written inquiries. This feedback will be used by the MB to design following events.

2. Short Courses

• Short Course on SOI from Modeling to design. Tyndall, Ireland January 23rd 2008.

- **The SOI MOSFET: from Single Gate to Multigate** (Prof. Jean-Pierre Colinge, Tyndall)
- **Physics of the Multigate MOS System** (Prof. Bogdan Majkusiak, Warsaw University of Technology)
- **Mobility in Multigate MOSFETs** (Prof. Francisco Gamiz, University of Granada)
- **Multigate MOSFET Technology** (Dr. Malgorzata Jurczak, IMEC)
- **Radiation Effects in Advanced Single- and Multi-Gate SOI MOSFETs** (Dr. Véronique Ferlet-Cavrois, CEA)
- **Multigate MOSFET Circuit Design** (Dr. Gerhard Knoblinger, Infineon)

Available at http://www.eurosoi.org/tutorials.asp

• SOI for analog, digital and RF SOCs and Microsystems applications. IMEC Belgium; (15-16 May 2008)

Course Contents:

Silicon-on-Insulator (SOI) technology is no longer a lab curiosity for the future, but a mature industrial choice for present applications. Major semiconductor companies have already developed commercial successful SOI products and processes worldwide, in particular for the logic sector on one hand (i.e. the Cell microprocessor for gaming platforms) and for smart sensors or MEMS on the other hand.

This two-day course will offer a large perspective on the opportunities which SOI opens in the field of low-voltage, low-power CMOS systems-on-chip, with an emphasis on analog and microwave functions, besides the widely-demonstrated advantages of SOI for high-performance digital and memory applications.

The SOI assets will both theoretically and experimentally be investigated, from basic technology and device levels to original circuit studies, demonstrating properties and performances significantly superior to those obtained on bulk CMOS, in a large span of processes, from submicron CMOS for pure analog to advanced multiple-gate decananometer CMOS for systems-on-chip design.

Course modules:

<u>15 May 2008</u>

09.00h-10.30h: General Introduction, Prof. D. Flandre, UCL
As a necessary introduction to SOI CMOS technology, its general process, device and circuit properties will be briefly reviewed, emphasizing the different types of SOI substrates, CMOS processes and MOSFETs, their main electrical characteristics. the status of commercial and researchSOI CMOS developments, as well as giving an overview of SOI applications, from digital and memory, to niche applications such as rad-hard or high-temperature.

11.00h-12.30h: SOI MOSFET specific behaviours and performance assessment, Prof. D. Flandre, UCL
Substrate insulation is responsible for SOI-specific MOS behaviours, whether advantageous (such as reduced body effect or detrimental such as floating-body effects or self heating. These may have significant impacts on "hot" device issues such as gate leakage, short-channel effects, digital and analog properties… Basics and recent findings will be reviewed, notably in relation with dynamic and frequency-dependent phenomena and the benchmarking of analog performance.

14.00h-17.00h: Analog design and applications, Prof. D. Flandre, UCL

The design and experimental results of low-power thin-film SOI CMOS analog blocks will be comprehensively presented and compared to bulk Si.
- For amplifiers, the basis of the "gm/ID" design methodology will be introduced and extended to SOI CMOS. Building blocks synthesis (differential pair, current mirrors) as well as actual OTA examples will be described, targeting applications from micropower to very high-frequency, high-precision or high-temperature specifications and emphasizing SOI design tips and optimization opportunities.
- The advantages and specificities of SOI CMOS for the design of high-performance analog circuits (with regards to low power, high linearity…) will be addressed in continuous-time filters, switched-capacitor structures, VCO and PLL, bandgaps, voltage reference, charge-pump, rectifiers and RFID input stages for power management, transimpedance amplifiers and active pixel sensors for optoelectronics.
An original Ultra-low-power (ULP) design technique will also be presented.

16 May 2008

09.00h-10.30h: Bulk and surface micromachined SOI MEMS, Prof. J.P. Raskin, UCL
SOI substrates offer unique opportunities for implementing sensors and MEMS. Indeed, the buried oxide can be used as a structural layer for the formation of a suspended membrane oras a sacrificial layer in the case of surface micromachined MEMS or NEMS. Such structures can be further combined with electronics to co-integrate high-performance intelligent / smart micro-systems on a single SOI substrate. The present talk will report recent SOI developments of thin three-dimensional (3-D) released microsensors (temperature, flow, magnetic) and thin dielectric membranes (flow, gas, pressure), as well as micromachines implementing new experimental tools to probe mechanical responses at very small scales.

11.00h-12.30h: On-wafer wideband characterization of advanced MOS technologies, Prof. J-P. Raskin, UCL
Based on the extraction of a wideband equivalent small-signal circuit, various MOS technologies will be fairly compared and models with increased validity domain established. Microwave performance of thin-film partially-depleted and fully-depleted SOI MOSFETs will be assessed. The present limitations of silicon substrates to provide high quality integrated passive elements as well as to reduce the crosstalk and nonlinearity generation in mixed-mode IC's will be explained and technological solutions will be exposed.

13.30h-15.00h: SOI FinFET integration and digital applications, Dr. N. Collaert, IMEC
The multi-gate MOSFET is considered as one of the most promising device architectures for scaling CMOS beyond the 45nm technology node. Improved short channel effects and current drive capability can be expected from these devices. The most widely pursued integration scheme for making multi-gate devices is the FinFET. In this lecture, the benefits and challenges of this device architecture will be discussed. Some layout specific issues will be addressed

and finally, an overview of the performance of FinFET digital circuits will be presented.

15.30h-17.00h: The use of SOI FinFET devices in analog and RF circuits, Dr. P. Wambacq, IMEC
FinFET devices are promising for downscaling beyond 45 nm as they have less short-channel effects. Furthermore, the fins can be left undoped, which alleviates the variability problem of deeply downscaled CMOS. However, these devices show intrinsic speed limitations due to their high series resistance and larger fringing capacitance. This course first discusses the analog device performance of FinFET-on-SOI devices. Next, the performance of several analog circuits is considered. These circuits range from low-frequency opamps to RF oscillators and low-noise amplifiers.

• First FDSOI tutorial of the Thematic Network on SOI technology, devices and circuits. Grenoble, France, 17/11/2008 - 18/11/2008.

- **Variability Issues** (Prof. Asen Asenov, Glasgow University)
- **Fully-Depleted SOI for Nanometer Subthreshold Circuits** (D. Bol, D. Flandre, UCL)
- **Introduction of the First FDSOI Tutorial** (Olivier Faynot, CEA-LETI)
- **Compact Modeling of Undoped FDSOI MOSFET** (O. Rozeau, LETI)
- **EUROSOI+: European Platform for low-power applications on Silicon on Insulator Technology** (Prof. F. Gámiz, UGR)
- **FDSOI Devices: Physics and Characterization** (Prof. Sorin Cristoloveanu, IMEP)
- **FDSOI Circuit Design** (Alexandre Valentian)
- **FDSOI: Technology and Electrical Results** (F. Andrieu)

Available at http://www.eurosoi.org/tutorials.asp

• Short Course on SOI from Modeling to design. Chalmers January 19th 2009

- **Modelling of ultra thin body SOI nano-transistors** (Prof. Luca Selmi, University of Udine)

- **Strained channel materials for SOI transistors** (Prof. Siegfried Mantl, Forschungszenter, Jülich)

- **SOI technology: an opportunity for RF designers** (Jean-Pierre Raskin, Université Catholique de Louvain)

- **From MEMS to embedded NEMS** (Dr. Julien Arcamone, CEA-LETI, Grenoble)

- **Ultimately thin carbon on insulators: Graphene** (Dr. Max Lemme, Harvard University, Cambridge, Massachusetts)

- **SOI Circuits: Do you want Partially Depleted or Fully Depleted Devices?** (Prof. Jean-Pierre Colinge, Tyndall National Institute, Cork)

- **Digital SOI design in the nanometer era - from high-performance to ultra-low-power circuits** (David Bol, Université Catholique de Louvain)

Available at http://www.eurosoi.org/tutorials.asp

Short Course on Multi-Gate SOI MOSFETs

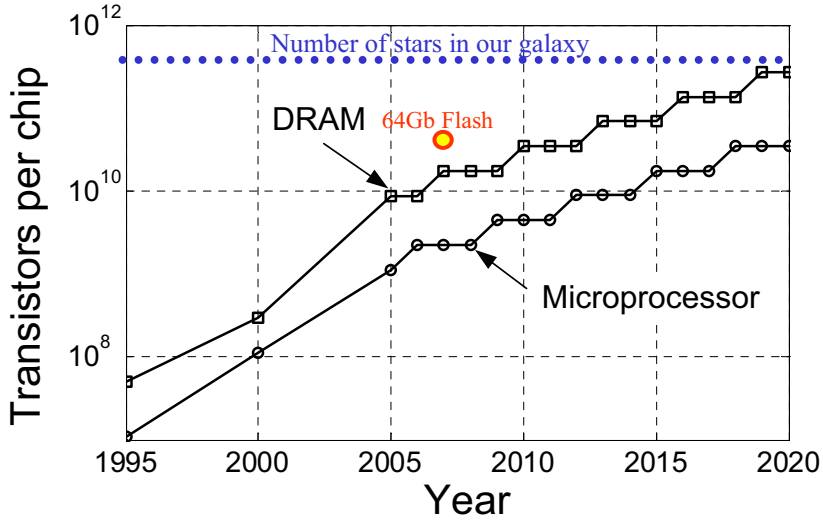
Wednesday, January 23, 2008

08:30	*REGISTRATION*	
09:15	**Welcome Address**	D. Lederer
09:30	**The SOI MOSFET: from Single Gate to Multi-Gate**	J.-P. Colinge
10:10	*COFFEE BREAK*	
10:30	**Multi-Gate MOSFET Technology**	M. Jurczak
11:20	**Physics of the Multi-Gate MOS System**	B. Majkusiak
12:10	*LUNCH*	
14:00	**Mobility in Multi-Gate MOSFETs**	F. Gámiz
14:50	**Radiation Effects in Advanced Single- and Multi-Gate SOI MOSFETs**	V. Ferlet-Cavrois
15:40	*COFFEE BREAK*	
16:00-16:50	**Multi-Gate MOSFET Circuit Design**	G. Knoblinger
19:00-21:00	*CONFERENCE WELCOME RECEPTION*	

The SOI MOSFET: from Single Gate to Multigate

Jean-Pierre Colinge
Silicon Research Group
Tyndall National Institute, Cork, Ireland

Moore's law



Multigate MOSFET technology

Malgorzata Jurczak
CMOS Device Research
IMEC
Belgium

Short Course EuroSOI Conference
Cork, Ireland, January 23, 2008

Outline

- Introduction
- FINFET process flow
- FinFET device design
  - Fin as transistor channel
  - VT engineering & gate stack
  - Series resistance & junction formation
- FINFET circuits
- Conclusions

Physics of the Multigate MOS System

Bogdan Majkusiak
Warsaw University of Technology
Institute of Micro- and Optoelectronics
Warsaw, Poland

Outline

Mobility in Multigate MOSFETs

Francisco Gamiz
Nanoelectronics Research Group
University of Granada, Granada, Spain

More Moore

The continuous scaling of CMOS requires significant innovations:

1.- Multi-gate devices. → **better scaling.**

2.- Enhacement of carrier mobility:
   a. Specific doping profiles
   b. Ligthly doped epitaxial layers
   c. Strained
   d. Crystall

Our goal:
Electron mobility in multigate devices

Radiation Effects in Advanced Single- and Multi-Gate SOI MOSFETs

V. Ferlet-Cavrois
CEA-DIF

EuroSOI Workshop 2008

"Multi-gate MOSFET Circuit Design"

G. Knoblinger

Infineon Technologies Austria AG
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9500 Villach, Austria
Gerhard.Knoblinger@infineon.com

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K. v. Arnim	IMEC / Infineon
M. Fulde	Techn. Univ. Munich / Infineon
J. Assenmacher	Infineon
L. Bertolissi	Infineon
J. Sedlmeir	Infineon
U. Baumann	IMMS Ilmenau

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EUROSOI 2009

Fifth Workshop of the Thematic Network on Silicon-On-Insulator

Technology, Devices and Circuits

TUTORIAL:
SOI FROM MODELLING TO DESIGN

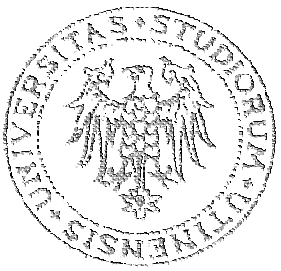
19 January 2009
Göteborg, Sweden

Tutorial program

Monday, January 19

8.30	**Registration**
9.00	**Welcome address and introduction** Francisco Gamiz, Universidad Granada, Spain
	Chair: Francisco Gamiz
9.15	**Modelling of ultra thin body SOI nano-transistors** Luca Selmi, University of Udine, Italy
10.00	**Strained channel materials for SOI transistors** Siegfried Mantl, Forschungszenter Jülich, Germany
10.45	**COFFEE BREAK**
11.00	**SOI technology: an opportunity for RF designers** Jean-Pierre Raskin, Université Catholique de Louvain, Belgium
11.45	**From MEMS to embedded NEMS** Julien Arcamone, CEA-LETI, Grenoble, France
12.30	**LUNCH**
	Chair: Cor Claeys
14.00	**Ultimately thin carbon on insulators : Graphene** Max Lemme, Harvard University, Cambridge, Massachusetts, U.S.A.
14.45	**SOI Circuits: Do you want Partially Depleted or Fully Depleted Devices?** Jean-Pierre Colinge, Tyndall National Institute, Cork, Ireland
15.30	**COFFEE BREAK**
15.45	**Digital SOI design in the nanometer era - from high-performance to ultra-low-power circuits** David Bol, Université Catholique de Louvain, Belgium
16.30	**Registration and Workshop welcome reception**

"Modeling of Ultra Thin Body SOI nano-transistors"



Luca Selmi

DIEGM - University of Udine, Italy – IU.NET

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F.Driussi, D.Esseni, P.Palestri, L.Lucci, M.De Michielis,
P.Toniutti, F.Conzatti
DIEGM, University of Udine

PULL-NANO integrated project
NANOSIL network
ITALIAN MIUR

JARA Jülich Aachen Research Alliance

JÜLICH FORSCHUNGSZENTRUM

Strained channel materials for SOI transistors

Siegfried Mantl

Institute of Bio- and Nanosystems (IBN1 – IT)

Research Centre Juelich

Outline

- Effect of strain on mobility
- Methods of applying stress:
  biaxial (global)
  uniaxial (local)
- Optimum crystal orientations of Si and Ge
- Ge on insulator (GOI)
- III/V semiconductors
- Why geometry matters:

  Nanowires

EUROSOI 2009

Fifth Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits

Chalmers University of Technology, Sweden, January 19-21, 2009

SOI technology: an opportunity for RF designers?

Prof. Jean-Pierre Raskin

Université catholique de Louvain
Microwave Laboratory
Place du Levant, 3, B-1348 Louvain-la-Neuve, Belgium
jean-pierre.raskin@uclouvain.be

Outline

- State-of-the-art of RF **CMOS performance**
- **Limiting factors** for active and passive devices in Silicon technologies
- **Diversity of SOI technologies** (PD, FD, strained SOI, SON, MuG)
- **High Resistivity SOI** substrates: a key substrate for RF applications
  - Transmission lines
  - Crosstalk in mixed-mode ICs
  - Optical RF switches
  - Non-linearities for high power Si ICs
- Conclusions

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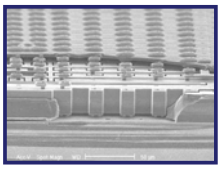
MINATEC
INSTITUT CARNOT CEA LETI

Outlook

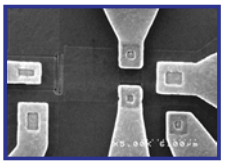
Introduction

- *MEMS: definition, interest, market, . . .*
- *Transition to NEMS*



Towards NEMS-CMOS monolithic integration

- *Detection techniques and electrical modeling of mechanical components*
- *Monolithic integration: benefits and implementation*



NEMS-CMOS co-integration technologies

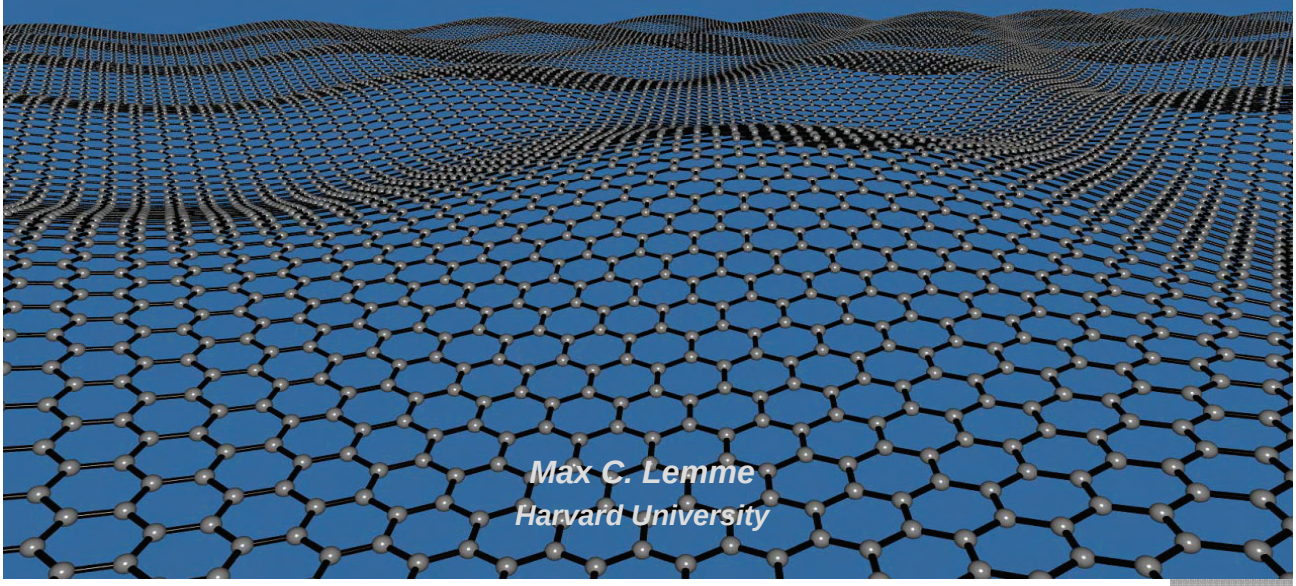
- *Main approaches*
- *Cost analysis*

Main realizations of NEMS devices

cea

Ultimately thin Carbon on Insulator: Graphene

EuroSOI 2009



Max C. Lemme
Harvard University

Acknowledgement:

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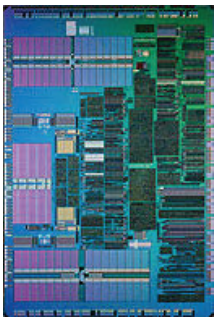
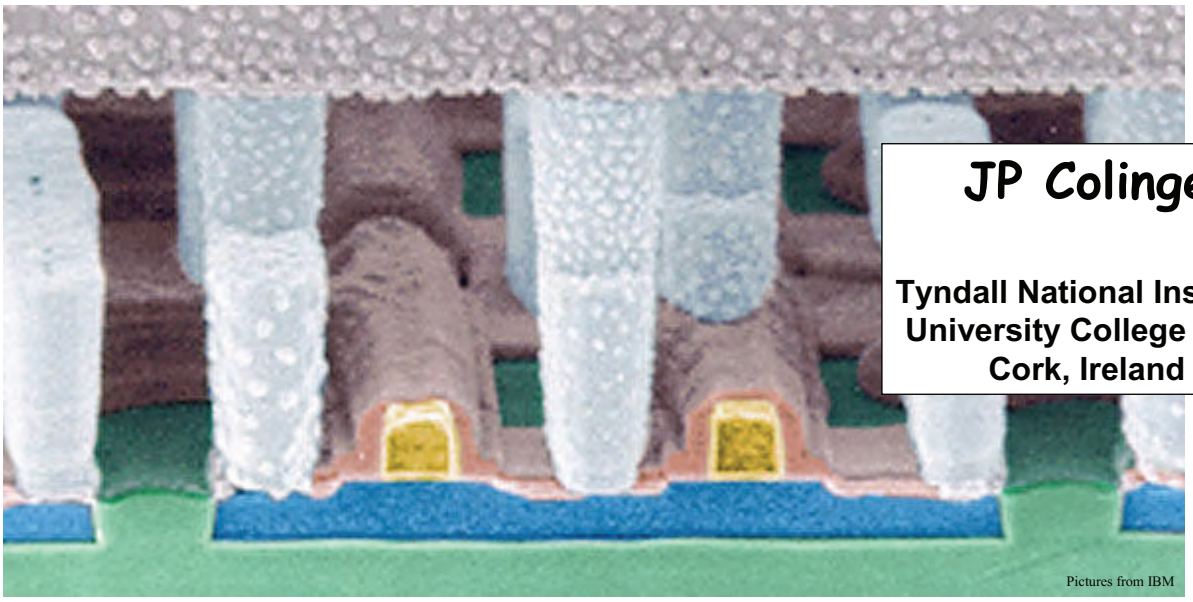
- **„ALEGRA“ project (German Federal Ministry of Education and Research (BMBF), www.alegra.info)**
- **„GRAND“ project (European Commission, www.grand-project.eu)**
- **Alexander von Humboldt Foundation for my Lynen Fellowship**
- **The EuroSOI organizers for inviting me to this conference!**

SOI Circuits:

Do you want Partially Depleted or Fully Depleted Devices?”





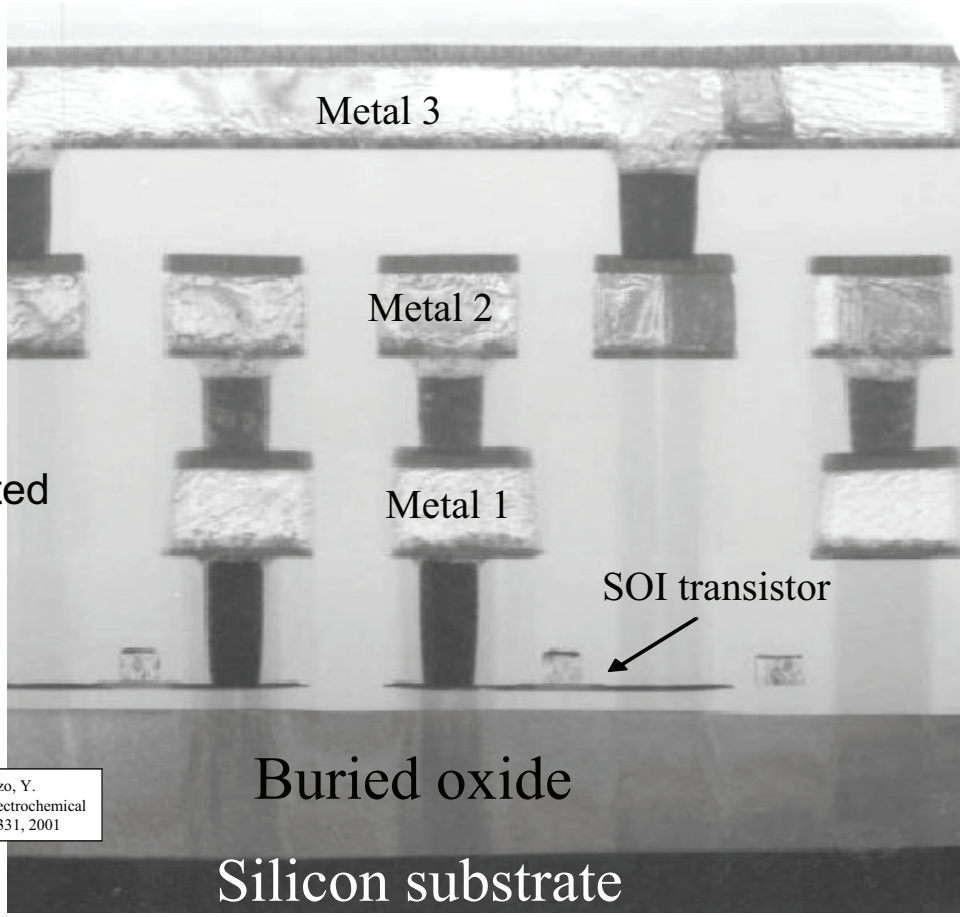
JP Colinge

Tyndall National Institute
University College Cork
Cork, Ireland

Pictures from IBM

OKI, 2001

Fully Depleted



M. Itoh, Y. Kawai, S. Ito, K. Yokomizo, Y. Katakura, Y. Fukuda, F. Ishikawa, Electrochemical Society Proceedings, Vol. 2001-3, p. 331, 2001

Digital SOI design in the nanometer era – From high-performance to ultra-low-power circuits

EuroSOI 2009 tutorial

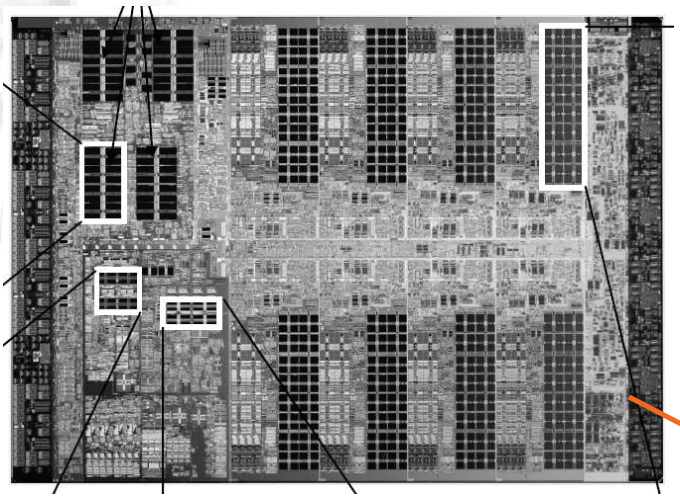
UCL Université catholique de Louvain

Microelectronics Laboratory

David Bol

January 19, 2009

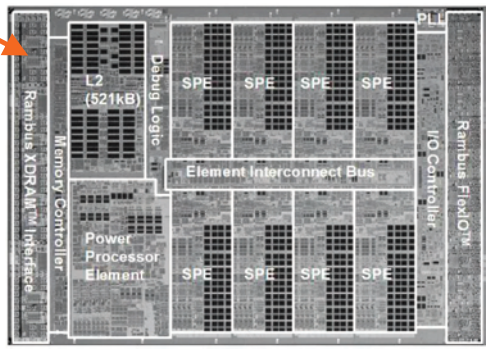
SOI for high-performance applications



IBM Cell Broadband Engine in 65nm SOI
[Pille, ISSCC'07]

Partially-depleted SOI technologies

IBM Cell Broadband Engine in 45nm SOI
[Takahashi, ISSCC'08]



Benefits of scaling:

- -34% area
- -100mV V_{dd}
- -40% power

@ iso-speed

General Introduction to SOI technology

- Historical & Designer Perspectives -

D. Flandre

Microelectronics Laboratory (DICE),
Research Center in Micro- and Nano-Scale Materials and Electronics Devices (CeRMiN),
Université catholique de Louvain (UCL)
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SOI MOSFET specific (analog) behaviours and performance assessment

1. Analog performance
2. Floating-body effects
3. Noise, 4. Mismatch

D. Flandre, UCL

UCL
Université
catholique
de Louvain

Analog design with Gm/Id methodology in bulk and SOI CMOS

D. Flandre

Mixed analog-digital functions - (Ultra) Low Power -

1. Optical transimpedance amplifier
2. Voltage-controlled ring oscillators, PLL
3. Filters (HD)
4. Switched Capacitor, ADC (switches)
5. Bandgap / voltage references (bipolar)
6. Ultra-low-power design technique