INFORMATION AND COMMUNICATION TECHNOLOGIES

COORDINATION AND SUPPORT ACTION

EUROSOI+

European Platform for Low-Power Applications on Silicon-On-Insulator Technology

Grant Agreement nº 216373

D5.8 Report on promotional activities for the use of EUROSOI design and prototyping platform during first reporting period

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Project coordinator: Prof. Francisco Gámiz, UGR
Project coordinator organisation: University of Granada, Spain Rev.1

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Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
RE	Restricted to a group specified by the consortium (including the Commission Services)	
CO	Confidential, only for members of the consortium (including the Commission Services)	

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1.- Introduction.

Technical promotion of SOI technologies is clearly one of the biggest goals of EUROSOI+. As the FDSOI platform is also a main achievement of this project, CEA-LETI and possibly other partners from EUROSOI+ will visit European IC and Fabless companies in order to promote the FDSOI technology and the work done in the frame of EUROSOI+. Such promotion will outline the potentialities of this technology, as well as the new circuit design opportunities and applications that will be raised during the meetings. Target companies are ARM, AMD, ST, Qimonda, Innovative Silicon, Nokia, etc... Two visits per year are programmed and budgeted (A total budget of 3600€ (600€ per visit) are allocated to cover travel costs and subsistence expenses of visitors). At the end of every year, a report explaining the activities developed during the visits, the companies visited and the outcomes of the visits will be delivered (D5.8, D5.9 and D5.10).

2.- Promotion of the FDSOI technology.

According to Task 5.1 LETI will provide already processed Fully Depleted SOI devices (fabricated on ultra-thin SOI films and coupled with high-K and metal gates) to EUROSOI partners.

FDSOI wafers with functional devices have been provided to the following EUROSOI+ partners:

- Jean-Pierre Raskin and Denis Flandre (UCL, Louvain La Neuve). Wafers with thick and thin Buried oxide have been provided for low and medium frequency measurement.

- Sorin Cristoloveanu (IMEP, Grenoble). Wafers with thick BOX have been provided for interface coupling characterization.

- Francisco Gamiz (UGR, Granada). Electrical measurements have been provided for mobility model calibration and comparison.

In addition, one important goal of EUROSOI+ is to boost the exchanges of information about the Fully Depleted SOI technology, based on the samples provided by LETI. To do so, we will organize three working group meetings (M5.2 and D5.1, D5.2 and D5.3). The first WG meeting should be organized in month 9 (M5.2) in Grenoble and the other two in parallel with the workshops held in Chalmers (month 13) and Grenoble (month 25). In addition, different experts from the rest of EUROSOI partners and from Industrial Advisory Board members will be invited to attend them. These workshops will be chaired by Dr.Olivier Faynot from CEA-LETI, who reported to the MB the details of the organization of this first workshop (M5.2, D5.1, m10). The ultimate goal of this first workshop is to organize a technical event with 7 or 8 presentations in order to see

1. What is available today with regard to LETI FDSOI technology?
2. What would be needed to go further?

As September is very crowed with Summer Schools (SINANO) and conferences (SISPAD, ESSDERC, etc.) and also the two first weeks of October (IEEE SOI Conference and ECS Symposium) Dr. Olivier proposed to hold the WG meeting in week 43, in particular, two days between 20th and 24th of October. The proposed format is to have a two day tutorial with technical sessions in the afternoon of the first day and the morning of the second day, thus facilitating the transportation of attendees. He also proposed to have:

- Three technical presentations (1 hour of duration) from LETI facing topics such as Technology, Device Physics, and Compact Modeling/Circuit design.
- Three technical presentations from people outside LETI:
  - Device characterization (IMEP)
  - Variability issues (Prof.Asenov, Glasgow University)
  - Applications (UCL, CISSOID, Japan or U.S.A.)
- A final panel discussion.

Finally, on November 17th-18th, Dr.Olivier Faynot from LETI organized in Grenoble a tutorial (free of charge for the EUROSOI members) focused on the training of European scientists on Fully Depleted SOI technology. Well recognized technologists, as well as international experts on devices and circuit design trained the attendees on SOI specific aspects, including: (1) Devices physics; (2) Technology description; (3) Modeling and circuit design; (4) Variability issues; (5) FDSOI platform development status.

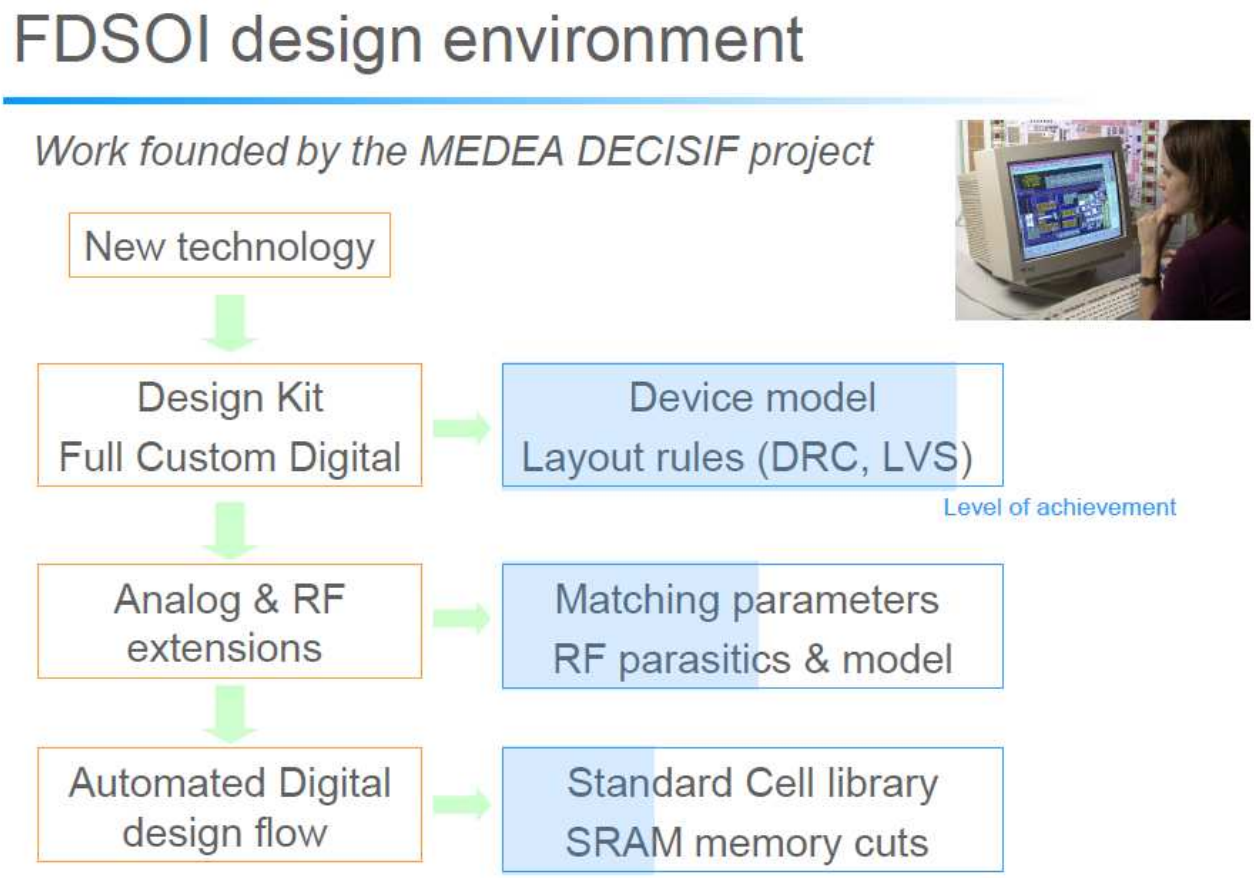
Monday, November 17th

2.00pm: EUROSOI + general introduction (30 mins)
F. Gámiz (UGR, Spain)
2.30pm: FDSOI tutorial introduction (15 mins)
O. Faynot (CEA-LETI, France)
3.00pm: FDSOI device physics (1hour)
S. Cristoloveanu (INPG, France)
4.00pm: BREAK
4.30pm: FDSOI technology description and
related electrical results (1,5 hour)
F. Andrieu (CEA-LETI, France)
6.00pm: Discussion around advantages and drawbacks of FDSOI
moderator: O.Faynot (CEA-LETI, France)

Tuesday, November 18th

8.30am: FDSOI modeling and circuit design (1 hour)
O. Rozeau / A. Valentian (CEA-LETI, France)
9.30am: Variability issues (1 hour)
A. Asenov (Univ. Glasgow, United Kingdom)
10.30am: BREAK
11.00am: Ultra-Low Power circuit design (1 hour)
D.Bol (UCL, Belgium)
12.00am: Tutorial conclusion and FDSOI platform status (30 mins)
O. Faynot (CEA-LETI, France)

The development of the research design kit is progressing in phase with what has been planned in the European project called DECISIF. The status of this development is shown in the following graph (level of achievement is colored in blue):



This design kit contains a digital part that includes device model, Design Rules Control file and Layout Versus Schematic file. These files are essential to model and control the layout generated by the designers. This part is completed at 85%. The design kit contains also an analog part that includes Matching parameters, RF parasitics and related model (completed at 50%). The design kit finally contains an automated digital Design flow that includes Standard cell library and SRAM memory cuts. This last part is completed at 30%.

With such level of achievement, the design kit can already be used to design some elementary circuits. It is scheduled to complete this design kit by mid-2009.

In addition to the design kit, a documentation manual is under construction.

The design kit and the associated user manual have already been provided to the University of Edimburgh (Scotland) and to the CEA-DAM (in Bruyeres Le Chatel, France).

Promotion of the FDSOI technology has been made by LETI during this period to the following companies:

- Presentation of the technology and results are regularly (every 3 months) made to SOITEC. Due to the location of both sites, no travel expenses are related to this promotion.

- Technology and electrical results have been also presented to ST Microelectronics in order to highlight the interest of such technology for Low Power applications. No travel expenses are related to this promotion.

- Promotion of FDSOI technology has also been done to AMD and ARM through a presentation at the SOI consortium meeting in November 2008. More detailed meetings will be planed for each company in 2009.

- We are now considered as one of the EUROPRACTICE projects (http://www.europractice.org/). We were invited to the EUROPRACTICE workshop organized in Warsaw in February, 2008, but finally it had to be cancelled. The new Workshop was held on September 4th, 2008 at IMEC (Belgium). The one day Workshop was a good opportunity to bring the various EUROPRACTICE projects together, to discuss what services are offered and identify where the gaps are, share best practice and encourage inter-project collaborations.